150mA Supercapacitor Charger

FEATURES

- **Low Noise Constant Frequency Charging of Two Series Supercapacitors**
- **Automatic Cell Balancing Prevents Capacitor Overvoltage During Charging**
- **Programmable Charge Current (Up to 150mA)**
- Selectable 2.4V or 2.65V Regulation per Cell (LTC3225)
- Selectable 2V or 2.25V Regulation per Cell (LTC3225-1)
- Automatic Recharge
- I_{VIN} = 20µA in Standby Mode
- I_{COUT} < 1µA When Input Supply is Removed
- No Inductors
- Tiny Application Circuit (2mm × 3mm DFN Package, All Components <1mm High)

APPLICATIONS

- Current Limited Applications with High Peak Power Loads (LED Flash, PCMCIA Tx Bursts, HDD Bursts, GPRS/GSM Transmitter)
- Backup Supplies

DESCRIPTION

The LTC®3225/LTC3225-1 are programmable supercapacitor chargers designed to charge two supercapacitors in series to a selectable fixed output voltage (4.8V/5.3V for the LTC3225 and 4V/4.5V for the LTC3225-1) from input supplies as low as 2.8V to 5.5V. Automatic cell balancing prevents overvoltage damage to either supercapacitor. No balancing resistors are required.

Low input noise, low quiescent current and low external parts count (one flying capacitor, one bypass capacitor at V_{IN} and one programming resistor) make the LTC3225/LTC3225-1 ideally suited for small battery-powered applications.

Charge current level is programmed with an external resistor. When the input supply is removed, the LTC3225/LTC3225-1 automatically enter a low current state, drawing less than 1µA from the supercapacitors.

The LTC3225/LTC3225-1 are available in a 10-lead 2mm × 3mm DFN package.

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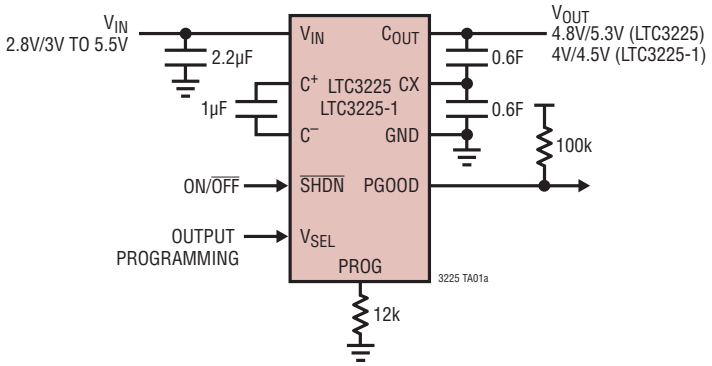
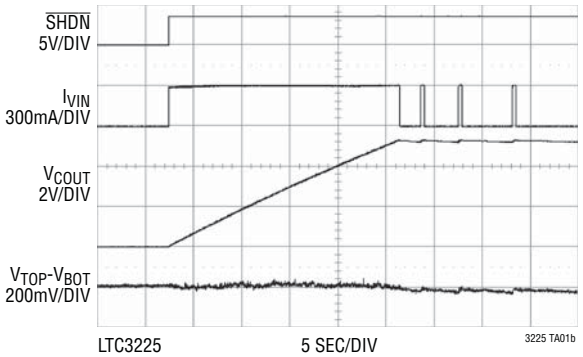
TYPICAL APPLICATION



Charging Profile with 30% Mismatch in Output Capacitance, C_{TOP} < C_{BOT}



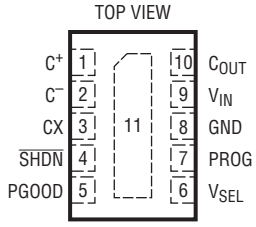
LTC3225
V_{SEL} = V_{IN}
R_{PROG} = 12k
C_{TOP} = 1.1F
C_{BOT} = 1.43F
C_{TOP} INITIAL VOLTAGE = 0V
C_{BOT} INITIAL VOLTAGE = 0V

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, C_{OUT} to GND ..... –0.3V to 6V
$\overline{SHDN}$, V_{SEL} ..... –0.3V to V_{IN} + 0.3V
C_{OUT} Short-Circuit Duration ..... Indefinite
I_{VIN} Continuous (Note 2) 350mA
I_{OUT} Continuous (Note 2) 175mA
Operating Temperature Range (Note 3) .... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 11) MUST BE SOLDERED TO LOW IMPEDANCE GND PLANE (PIN 8) ON PCB

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3225EDDB#TRMPBF	LTC3225EDDB#TRPBF	LCYR	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3225EDDB-1#TRMPBF	LTC3225EDDB-1#TRPBF	LFFS	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C

TRM = 500 pieces.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, C_{IN} = 2.2µF, C_{FLY} = 1µF, unless otherwise specified (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LTC3225							
$V_{IN-UVLO}$	Input Supply Undervoltage Lockout High-to-Low Threshold	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$	● ●	2.65 2.4	2.75 2.5	2.85 2.6	V V
$V_{IN-UVLO-HYS}$	Input Supply Undervoltage Lockout Hysteresis	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$			150 140		mV mV
V_{IN}	Input Voltage Range	$V_{SEL} = V_{IN}$ $V_{SEL} = 0V$	● ●	3 2.8		5.5 5.5	V V
V_{COUT}	Charge Termination Voltage Sleep Mode Threshold (Rising Edge)	$V_{SEL} = V_{IN}$ $V_{SEL} = 0V$	● ●	5.2 4.7	5.3 4.8	5.4 4.9	V V
$V_{COUT-HYS}$	Output Comparator Hysteresis				100		mV
$V_{TOP/BOT}$	Maximum Voltage Across Each of the Supercapacitors After Charging	$V_{SEL} = V_{IN}$ $V_{SEL} = 0V$	● ●			2.75 2.5	V V
LTC3225-1							
$V_{IN-UVLO}$	Input Supply Undervoltage Lockout High-to-Low Threshold	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$	● ●	2.25 2.0	2.35 2.1	2.45 2.2	V V
$V_{IN-UVLO-HYS}$	Input Supply Undervoltage Lockout Hysteresis	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$			150 140		mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, C_{IN} = 2.2µF, C_{FLY} = 1µF, unless otherwise specified (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$	● ●	2.8 2.8		5.5 5.5	V V
V_{COUT}	Charge Termination Voltage Sleep Mode Threshold (Rising Edge)	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$	● ●	4.4 3.9	4.5 4.0	4.6 4.1	V V
$V_{COUT-HYS}$	Output Comparator Hysteresis				100		mV
$V_{TOP/BOT}$	Maximum Voltage Across Each of the Supercapacitors After Charging	$V_{SEL} = V_{IN}$ $V_{SEL} = 0$	● ●			2.35 2.1	V V
LTC3225/LTC3225-1							
I_{Q-VIN}	No Load Operating Current at V_{IN}	I_{OUT} = 0mA	●		20	40	µA
$I_{SHDN-VIN}$	Shutdown Current	$\overline{SHDN}$ = 0V, V_{OUT} = 0V	●		0.1	1	µA
I_{COUT}	C_{OUT} Leakage Current	V_{OUT} = 5.6V, $\overline{SHDN}$ = 0V V_{OUT} = 5.6V, Charge Pump in Sleep Mode V_{OUT} = 5.6V, $\overline{SHDN}$ Connected to V_{IN} with Input Supply Removed	● ●		1 2	3 4 1	µA µA µA
I_{VIN}	Input Charge Current	V_{IN} = 3.6V, R_{PROG} = 12k, $C_{TOP} = C_{BOT}$			306		mA
		V_{IN} = 3.6V, R_{PROG} = 60k, $C_{TOP} = C_{BOT}$			55		mA
I_{OUT}	Output Charge Current	V_{IN} = 3.6V, R_{PROG} = 12k, $C_{TOP} = C_{BOT}$, V_{OUT} = 4.5V (LTC3225), V_{OUT} = 3.7V (LTC3225-1)		125	150	175	mA
		V_{IN} = 3.6V, R_{PROG} = 60k, $C_{TOP} = C_{BOT}$, V_{OUT} = 4.5V (LTC3225), V_{OUT} = 3.7V (LTC3225-1)			26		mA
V_{PGOOD}	PGOOD Low Output Voltage	I_{PGOOD} = –1.6mA	●			0.4	V
$I_{PGOOD-LEAK}$	PGOOD High Impedance Leakage Current	V_{PGOOD} = 5V	●			10	µA
V_{PG}	PGOOD Low-to-High Threshold	Relative to Output Voltage Threshold	●	92	94	96	%
V_{PG-HYS}	PGOOD Threshold Hysteresis	Relative to Output Voltage Threshold	●	0.25	1.2	2.5	%
R_{OL}	Effective Open-Loop Output Impedance (Note 4)	V_{IN} = 3.6V, V_{OUT} = 4.5V (LTC3225) V_{IN} = 3.6V, V_{OUT} = 3.7V (LTC3225-1)			8 9		Ω
f_{OSC}	CLK Frequency		●	0.6	0.9	1.5	MHz
V_{SEL}, $\overline{SHDN}$							
V_{IH}	Input High Voltage		●	1.3			V
V_{IL}	Input Low Voltage		●			0.4	V
I_{IH}	Input High Current		●	–1		1	µA
I_{IL}	Input Low Current		●	–1		1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Based on long-term current density limitations.

Note 3: The LTC3225/LTC3225-1 are tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3225/LTC3225-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

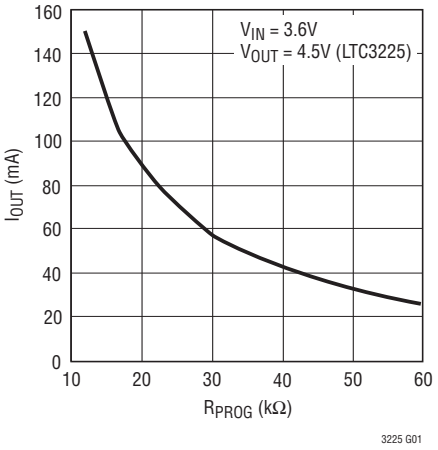
Note 4: Output not in regulation;

$R_{OL} \equiv (2 \bullet V_{IN} - V_{OUT})/I_{OUT}$

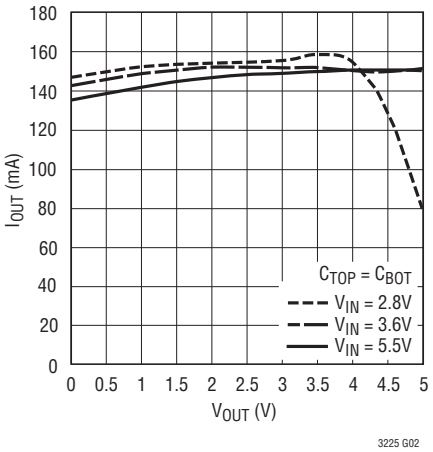
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, C_{FLY} = 1µF, C_{IN} = 2.2µF, C_{TOP} = C_{BOT}, unless otherwise specified)

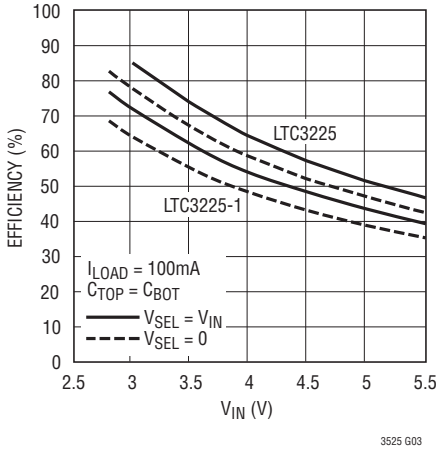
I_{OUT} vs R_{PROG}



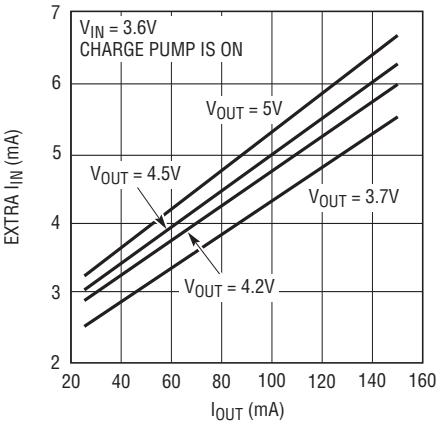
I_{OUT} vs V_{OUT} (R_{PROG} = 12k)



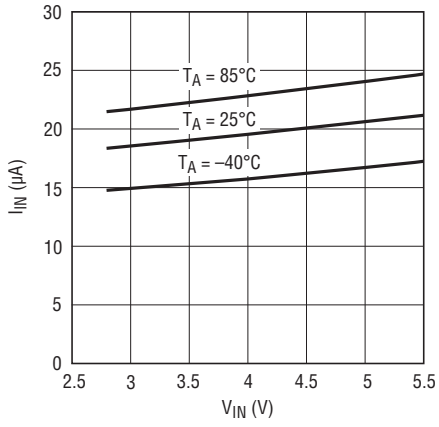
Efficiency vs V_{IN}



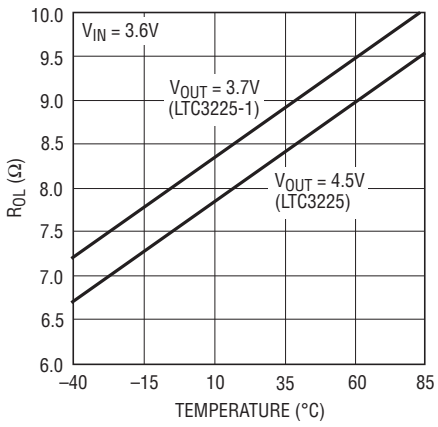
Extra Input Current vs Output Current (I_{VIN} – 2 • I_{OUT})



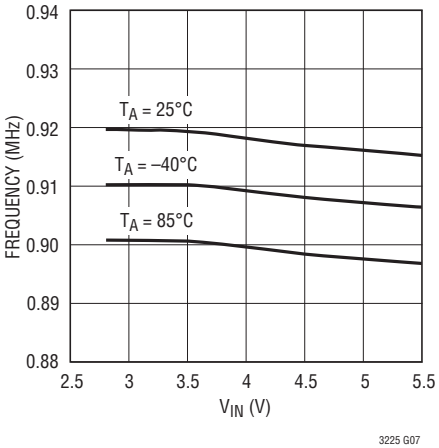
No-Load Input Current vs Supply Voltage



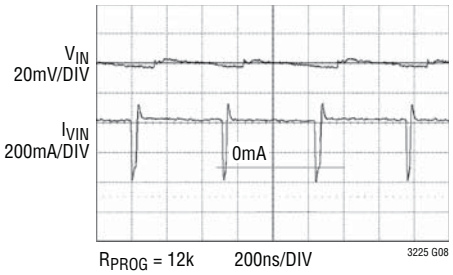
Charge Pump Open-Loop Output Resistance vs Temperature ($2V_{IN}$ – V_{COUT})/I_{OUT}



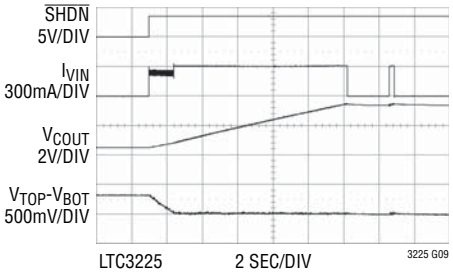
Oscillator Frequency vs Supply Voltage



Input Ripple and Input Current



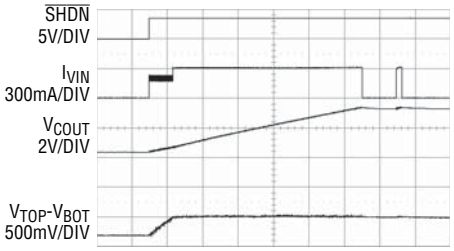
Charging Profile with Unequal Initial Output Capacitor Voltage (Initial V_{TOP} = 1.3V, V_{BOT} = 1V)



TYPICAL PERFORMANCE CHARACTERISTICS

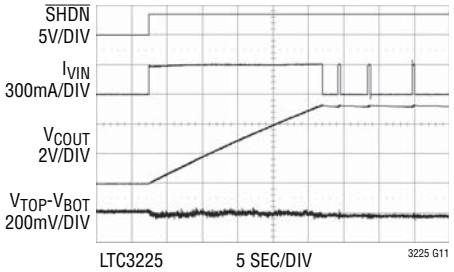
(T_A = 25°C, C_{FLY} = 1µF, C_{IN} = 2.2µF, C_{TOP} = C_{BOT}, unless otherwise specified)

Charging Profile with Unequal Initial Output Capacitor Voltage (Initial V_{TOP} = 1V, V_{BOT} = 1.3V)



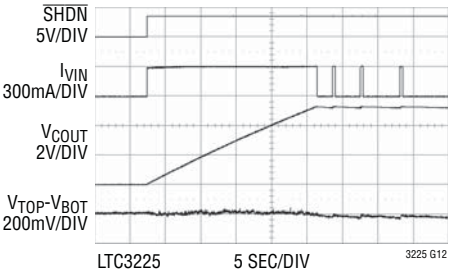
V_{SEL} = V_{IN}
R_{PROG} = 12k
C_{TOP} = C_{BOT} = 1.1F
C_{TOP} INITIAL VOLTAGE = 1V
C_{BOT} INITIAL VOLTAGE = 1.3V

Charging Profile with 30% Mismatch in Output Capacitance (C_{TOP} > C_{BOT})



V_{SEL} = V_{IN}
R_{PROG} = 12k
C_{TOP} = 1.43F
C_{BOT} = 1.1F
C_{TOP} INITIAL VOLTAGE = 0V
C_{BOT} INITIAL VOLTAGE = 0V

Charging Profile with 30% Mismatch in Output Capacitance (C_{TOP} < C_{BOT})



V_{SEL} = V_{IN}
R_{PROG} = 12k
C_{TOP} = 1.1F
C_{BOT} = 1.43F
C_{TOP} INITIAL VOLTAGE = 0V
C_{BOT} INITIAL VOLTAGE = 0V

PIN FUNCTIONS

C^+ (Pin 1): Flying Capacitor Positive Terminal. A 1µF X5R or X7R ceramic capacitor should be connected from C^+ to C^-.

C^- (Pin 2): Flying Capacitor Negative Terminal.

CX (Pin 3): Midpoint of Two Series Supercapacitors. This pin voltage is monitored and forced to track C_{OUT} (CX = C_{OUT}/2) during charging to achieve voltage balancing of the top and bottom supercapacitors.

$\overline{SHDN}$ (Pin 4): Active Low Shutdown Input. A low on $\overline{SHDN}$ puts the LTC3225/LTC3225-1 in low current shutdown mode. Do not float the $\overline{SHDN}$ pin.

PGOOD (Pin 5): Open-Drain Output Status Indicator. Upon start-up, this open-drain pin remains low until the output voltage, V_{OUT}, is within 6% (typical) of its final value. Once V_{OUT} is valid, PGOOD becomes Hi-Z. If V_{OUT} falls 7.2% (typical) below its correct regulation level, PGOOD is pulled low. PGOOD may be pulled up through an external resistor to an appropriate reference level. This pin is Hi-Z in shutdown mode.

V_{SEL} (Pin 6): Output Voltage Selection Input. A logic low at V_{SEL} sets the regulated C_{OUT} to 4.8V (LTC3225) or 4V (LTC3225-1); a logic high sets the regulated C_{OUT} to 5.3V (LTC3225) or 4.5V (LTC3225-1). Do not float the V_{SEL} pin.

PROG (Pin 7): Charge Current Programming Pin. A resistor connected between this pin and GND sets the charge current. (See Applications Information section).

GND (Pin 8, Exposed Pad Pin 11): Charge Pump Ground. These pins must be soldered directly to PCB ground. The exposed pad must be soldered to a low impedance PCB ground for rated thermal performance.

V_{IN} (Pin 9): Power Supply for the LTC3225/LTC3225-1. V_{IN} should be bypassed to GND with a low ESR ceramic capacitor of more than 2.2µF.

C_{OUT} (Pin 10): Charge Pump Output Pin. Connect C_{OUT} to the top plate of the top supercapacitor. C_{OUT} provides charge current to the supercapacitors and regulates the final voltage to 4.8V/5.3V (LTC3225) or 4V/4.5V (LTC3225-1).

SIMPLIFIED BLOCK DIAGRAM

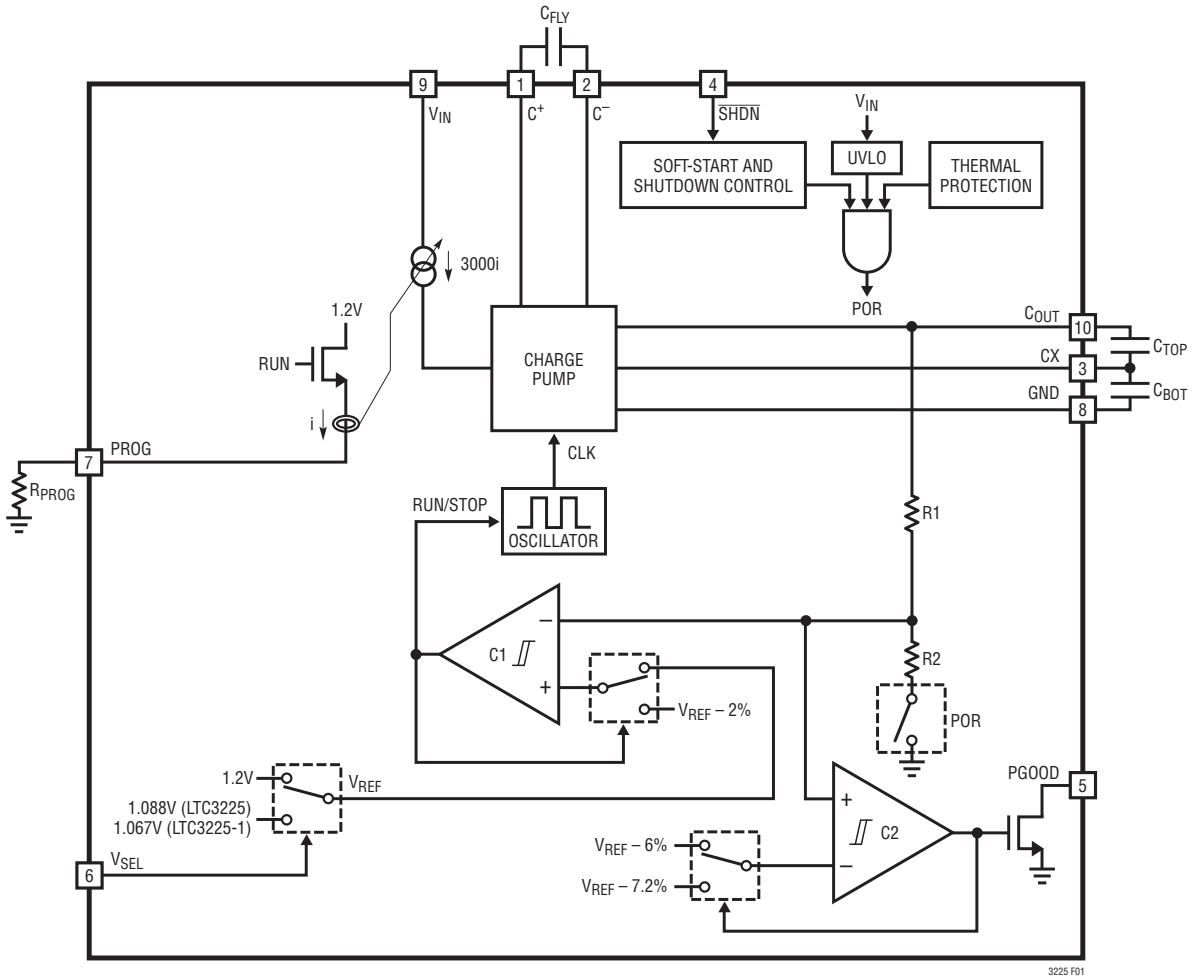


Figure 1

OPERATION

The LTC3225/LTC3225-1 are dual cell supercapacitor chargers. Their unique topology maintains a constant output voltage with programmable charge current. Their ability to maintain equal voltages on both cells while charging protects the supercapacitors from damage that is possible with other charging methods, without the use of external balancing resistors. The LTC3225/LTC3225-1 include an internal switched capacitor charge pump to boost V_{IN} to a regulated output voltage. A unique architecture maintains relatively constant input current for the lowest possible input noise. The basic charger circuit requires only three external components.

Normal Charge Cycle

Operation begins when the $\overline{SHDN}$ pin is pulled above 1.3V. The C_{OUT} pin voltage is sensed and compared with a preset voltage threshold using an internal resistor divider and a comparator. The preset voltage threshold is selectable with the V_{SEL} pin. If the voltage at the C_{OUT} pin is lower than the preset voltage threshold, the oscillator is enabled. The oscillator operates at a typical frequency of 0.9MHz. When the oscillator is enabled, the charge pump operates charging up C_{OUT}. Each time the charge pump starts up from shutdown, the input current drawn by the internal charge pump ramps up at approximately 20mA/µs until it reaches a level which is determined by R_{PROG}.

OPERATION

Once the output voltage is charged to the preset voltage threshold, the part shuts down the internal charge pump and enters into a low current state. In this state, the LTC3225/LTC3225-1 consume only about 20µA from the input supply. The current drawn from C_{OUT} is approximately 2µA.

Automatic Cell Balancing

Due to manufacturing tolerances, capacitance and leakage current can vary from supercapacitor to supercapacitor. Without the automatic cell balancing scheme used in the LTC3225/LTC3225-1, the voltages across the supercapacitors could differ from each other and potentially overvoltage a cell. This can affect the performance and lifetime of a supercapacitor.

The LTC3225/LTC3225-1 constantly monitor the voltage across both supercapacitors while charging. When the voltage across the supercapacitors is equal, both capacitors are charged with equal currents. If the voltage across one supercapacitor is lower than the other, the lower supercapacitor's charge current is increased and the higher supercapacitor's charge current is decreased. The greater the difference between the supercapacitor voltages, the greater the difference in charge current per capacitor. The charge currents can increase or decrease as much as 50% to balance the voltage across the supercapacitors. When the cell voltages are balanced, the supercapacitors are charged at a rate of approximately:

$$I_{COUT} = \frac{1}{2} \bullet I_{VIN}$$

If the leakage currents or capacitances of the two supercapacitors are mismatched enough that varying the charge current is not sufficient to balance their voltages, the LTC3225/LTC3225-1 stop charging the capacitor with the higher voltage until they are again balanced. This feature protects either capacitor from experiencing an overvoltage condition. Attempting to equalize the voltages using parallel resistors wastes power, discharges the supercapacitors, and takes time to equalize the voltages. A 30% capacitance mismatch leads to a 30% initial voltage difference after charging. It takes hours to equalize the voltages across 1F supercapacitors using 10k resistors.

Shutdown Mode

Asserting $\overline{SHDN}$ low causes the LTC3225/LTC3225-1 to enter shutdown mode. With the $\overline{SHDN}$ pin connected to V_{IN} and the input supply removed or grounded, less than 1µA is consumed from the output, allowing the supercapacitors to remain charged.

If the input supply is present at V_{IN} and the $\overline{SHDN}$ pin is grounded, the LTC3225/LTC3225-1 draw approximately 1µA of supply current. With the voltage at the C_{OUT} pin discharged to 0V, this current drops to less than 1µA. Since the $\overline{SHDN}$ pin is a high impedance CMOS input, it should never be allowed to float.

Output Voltage Programming

The LTC3225/LTC3225-1 have a V_{SEL} input pin that allows the user to set the output threshold voltage to either 4.8V or 5.3V for the LTC3225 and 4V or 4.5V for the LTC3225-1 by forcing a low or high at the V_{SEL} pin respectively.

Output Status Indicator (PGOOD)

During shutdown, the PGOOD pin is high impedance. When the charge cycle starts, an internal N-channel MOSFET pulls the PGOOD pin to ground. When the output voltage, V_{OUT}, is within 6% (typical) of its final value, the PGOOD pin becomes high impedance, but charge current continues to flow until V_{OUT} crosses the charge termination voltage. When V_{OUT} drops 7% below the charge termination voltage, the PGOOD pin again pulls low.

Current Limit/Thermal Protection

The LTC3225/LTC3225-1 have built-in current limit as well as overtemperature protection. If the PROG pin is shorted to ground, a protection circuit automatically shuts off the internal charge pump. At higher temperatures, or if the input voltage is high enough to cause excessive self-heating of the part, the thermal shutdown circuitry shuts down the charge pump once the junction temperature exceeds approximately 150°C. It will enable the charge pump once the junction temperature drops back to approximately 135°C. The LTC3225/LTC3225-1 are able to cycle in and out of thermal shutdown indefinitely without latch-up or damage until the overcurrent condition is removed.

APPLICATIONS INFORMATION

Programming Charge Current

The charge current is programmed with a single resistor connecting the PROG pin to ground. The program resistor and the input/output charge currents are calculated using the following equations:

$$I_{VIN} = \frac{3600V}{R_{PROG}}$$

$$I_{OUT} = \frac{I_{VIN}}{2} \text{ (with matched output capacitors)}$$

An R_{PROG} resistor value of 2k or less (i.e., short circuit) causes the LTC3225/LTC3225-1 to enter overcurrent shutdown mode. This mode prevents damage to the part by shutting down the internal charge pump.

Power Efficiency

The power efficiency (η) of the LTC3225/LTC3225-1 is similar to that of a linear regulator with an effective input voltage of twice the actual input voltage. In an ideal regulating voltage doubler the power efficiency is given by:

$$\eta_{2xIDEAL} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet 2I_{OUT}} = \frac{V_{OUT}}{2V_{IN}}$$

At moderate to high output power the switching losses and quiescent current of the LTC3225/LTC3225-1 are negligible and the above expression is valid. For example, with V_{IN} = 3.6V, I_{OUT} = 100mA and V_{OUT} regulated to 5.3V, the measured efficiency is 71.2% which is in close agreement with the theoretical 73.6% calculation.

Effective Open-Loop Output Resistance (R_{OL})

The effective open-loop output resistance (R_{OL}) of a charge pump is an important parameter that describes the strength of the charge pump. The value of this parameter depends on many factors including the oscillator frequency (f_{OSC}), value of the flying capacitor (C_{FLY}), the non-overlap time, the internal switch resistances (R_S) and the ESR of the external capacitors.

Charging Time Estimation

The estimated charging time with equal initial voltages across the two supercapacitors is given by the equation:

$$t_{CHRG} = \frac{C_{OUT} \bullet (V_{COUT} - V_{INI})}{I_{OUT}}$$

where C_{OUT} is the series output capacitance, V_{COUT} is the voltage threshold set by the V_{SEL} pin, V_{INI} is the initial voltage at the C_{OUT} pin and I_{OUT} is the output charge current given by:

$$I_{OUT} = \frac{1800V}{R_{PROG}}$$

When the charging process starts with unequal initial voltages across the supercapacitors, only the capacitor with the lower voltage level is charged; the other capacitor is not charged until the voltages equalize. This extends the charging time slightly. Under the worst-case condition, whereby one capacitor is fully depleted while the other remains fully charged due to significant leakage current mismatch, the charging time is about 1.5 times longer than normal.

Thermal Management

For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3225/LTC3225-1. If the junction temperature increases above approximately 150°C, the thermal shutdown circuitry automatically deactivates the output. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the GND pin (Pin 8) and the Exposed Pad (Pin 11) of the DFN package to a ground plane under the device on two layers of the PC board can reduce the thermal resistance of the package and PC board considerably.

APPLICATIONS INFORMATION

V_{IN} Capacitor Selection

The type and value of C_{IN} controls the amount of ripple present at the input pin (V_{IN}). To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) multilayer ceramic chip capacitors (MLCCs) be used for C_{IN}. Tantalum and aluminum capacitors are not recommended because of their high ESR.

The input current to the LTC3225/LTC3225-1 is relatively constant during both the input charging phase and the output charging phase but drops to zero during the clock non-overlap times. Since the non-overlap time is small (~40ns) these missing "notches" result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor, such as a tantalum, results in higher input noise. Therefore, ceramic capacitors are recommended for their exceptional ESR performance. Further input noise reduction can be achieved by powering the LTC3225/LTC3225-1 through a very small series inductor as shown in Figure 2.

A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

Flying Capacitor Selection

Warning: Polarized capacitors such as tantalum or aluminum should never be used for the flying capacitor since its voltage can reverse upon start-up of the LTC3225/LTC3225-1. Low ESR ceramic capacitors should always be used for the flying capacitor.

The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary to use at least 0.6µF of capacitance for the flying capacitor.

The effective capacitance of a ceramic capacitor varies with temperature and voltage in a manner primarily determined by its formulation. For example, a capacitor made of X5R or X7R material retains most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V type capacitor loses considerable capacitance over that range. X5R, Z5U and Y5V capacitors may also have a poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, over rated voltage and temperature conditions, a 4.7µF 10V Y5V ceramic capacitor in a 0805 case may not provide any more capacitance than a 1µF 10V X5R or X7R capacitor available in the same 0805 case. In fact, over bias and temperature range, the 1µF 10V X5R or X7R provides more capacitance than the 4.7µF 10V Y5V capacitor. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitance values are met over operating temperature and bias voltage.

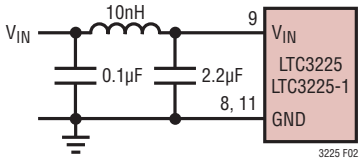


Figure 2. 10nH Inductor Used for Input Noise Reduction

APPLICATIONS INFORMATION

Table 1 contains a list of ceramic capacitor manufacturers and how to contact them.

Table 1. Capacitor Manufacturers

AVX	www.avx.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com
TDK	www.component.tdk.com

Layout Considerations

Due to the high switching frequency and high transient currents produced by the LTC3225/LTC3225-1, careful board layout is necessary for optimum performance. An unbroken ground plane and short connections to all the external capacitors improves performance and ensures proper regulation under all conditions.

The voltages on the flying capacitor pins C^+ and C^- have very fast rise and fall times. The high dV/dt values on these pins can cause energy to capacitively couple to adjacent printed circuit board traces. Magnetic fields can also be generated if the flying capacitors are far from the part (i.e. the loop area is large). To prevent capacitive energy transfer, a Faraday shield may be used. This is a grounded PC trace between the sensitive node and the LTC3225/LTC3225-1 pins. For a high quality AC ground it should be returned to a solid ground plane that extends all the way to the LTC3225/LTC3225-1.

Table 2. Supercapacitor Manufacturers

CAP-XX	www.cap-xx.com
NESS CAP	www.nesscap.com
Maxwell	www.maxwell.com
Bussmann	www.cooperbussmann.com
AVX	www.avx.com
Illinois Capacitor	www.illcap.com
Tecate Group	www.tecategroup.com

Charging a Single Supercapacitor

The LTC3225/LTC3225-1 can also be used to charge a single supercapacitor by connecting two series-connected matched ceramic capacitors with a minimum capacitance of 100µF in parallel with the supercapacitor as shown in Figure 3.

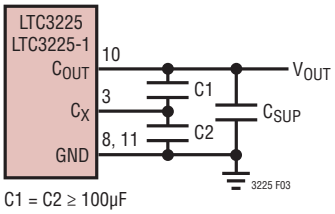
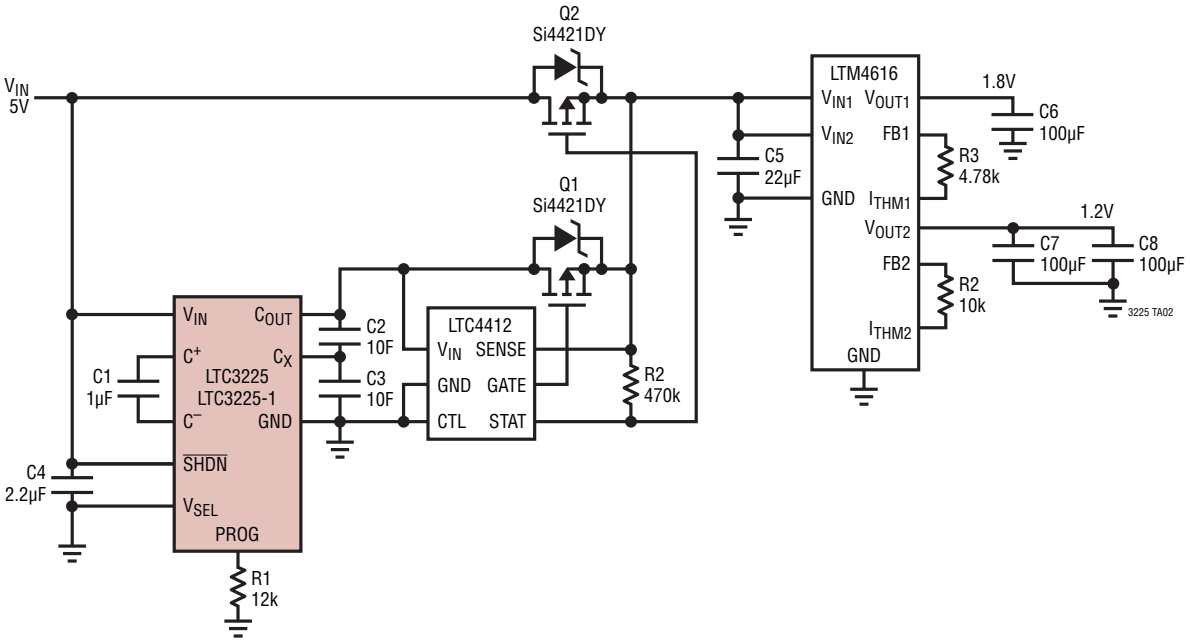


Figure 3. Charging a Single Supercapacitor

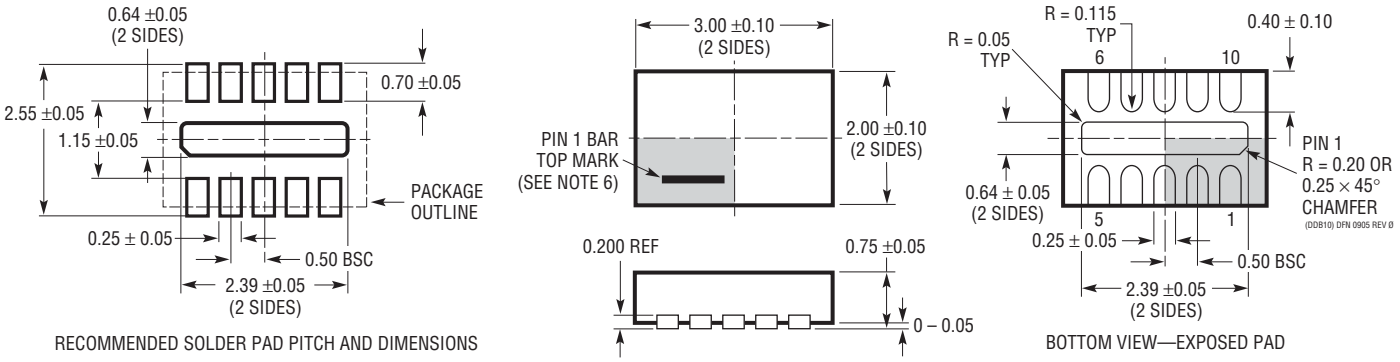
TYPICAL APPLICATION

5V Supercapacitor Back-Up Supply



PACKAGE DESCRIPTION

DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722 Rev Ø)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

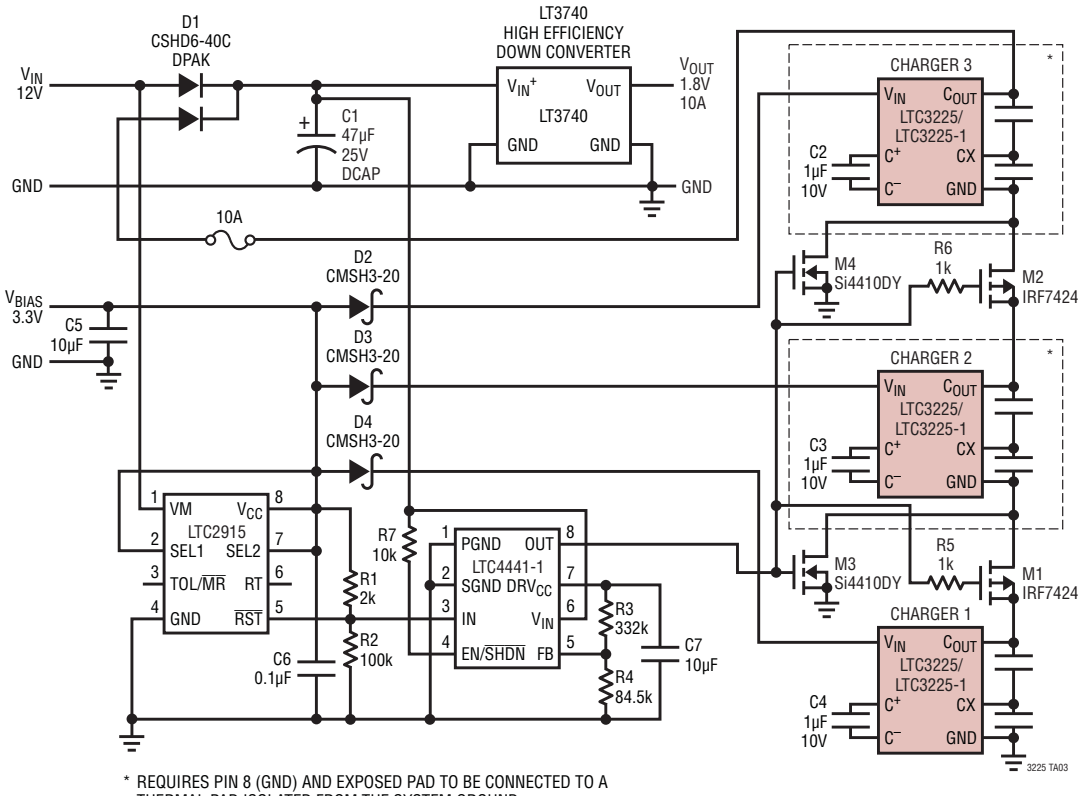
REV	DATE	DESCRIPTION	PAGE NUMBER
B	6/10	Updated Note 3 in Electrical Characteristics section.	2, 3
		Updates to Pins 8 and 11 in Pin Functions.	5
		Update to text in Layout Considerations section.	10
		Updated Typical Application and Related Parts.	14

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

12V Supercapacitor Back-Up Supply



* REQUIRES PIN 8 (GND) AND EXPOSED PAD TO BE CONNECTED TO A THERMAL PAD ISOLATED FROM THE SYSTEM GROUND.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1751-3.3/LTC1751-5	Micropower 5V/3.3V Doubler Charge Pumps	I_Q = 20µA, Up to 100mA Output, MS-8 Package
LTC3200	Constant Frequency Doubler Charge Pump	Low Noise, 5V Output or Adjustable
LTC3203/LTC3203B/ LTC3203B-1/LTC3203-1	500mA Low Noise High Efficiency Dual Mode Step-Up Charge Pumps	V_{IN}: 2.7V to 5.5V, 3mm × 3mm 10-Lead DFN Package
LTC3204/LTC3204B-3.3/ LTC3204-5	Low Noise Regulating Charge Pumps	Up to 150mA (LTC3204-5), Up to 50mA (LTC3204-3.3)
LTC3221/LTC3221-3.3/ LTC3221-5	Micropower Regulated Charge Pump	Up to 60mA Output
LTC3240-3.3/LTC3240-2.5	Step-Up/Step-Down Regulated Charge Pumps	Up to 150mA Output
LT®3420/LT3420-1	1.4A/1A Photoflash Capacitor Charger with Automatic Top-Off	Charges 220µF to 320V in 3.7 Seconds from 5V, V_{IN}: 2.2V to 16V, I_{SD} < 1µA, 10-Lead MS Package
LT3468/LT3468-1/ LT3468-2	1.4A/1A/0.7A, Photoflash Capacitor Charger	V_{IN}: 2.5V to 16V, Charge Time = 4.6 Seconds for the LT3468 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, ThinSOT™ Package
LTC3484-0/LTC3484-1/ LTC3484-2	1.4A/0.7A/1A, Photoflash Capacitor Charger	V_{IN}: 1.8V to 16V, Charge Time = 4.6 Seconds for the LT3484-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 2mm × 3mm 6-Lead DFN Package
LT3485-0/LT3485-1/ LT3485-2/LT3485-3	1.4A/0.7A/1A/2A Photoflash Capacitor Charger with Output Voltage Monitor and Integrated IGBT	V_{IN}: 1.8V to 10V, Charge Time = 3.7 Seconds for the LT3485-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 3mm × 3mm 10-Lead DFN Driver
LT3750	Capacitor Charger Controller	Charges Any Size Capacitor, 10-Lead MS Package
LT3751	Capacitor Controller with Regulation	Charges Any Size Capacitor, 4mm × 5mm QFN-20 Package

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