LTC3311

5V, 12.5A Synchronous Step-Down Silent Switcher in 3mm x 3mm LQFN

FEATURES

- **Pin Compatible with LTC3310/LTC3310S and LTC3311S**
- **Silent Switcher® Architecture:**
  - Ultralow EMI Emissions
- **High Efficiency—4.5mΩ NMOS and 16mΩ PMOS**
- **Wide Bandwidth, Fast Transient Response**
- Safely Tolerates Inductor Saturation in Overload
- V_{IN} Range: 2.25V to 5.5V
- V_{OUT} Range: 0.5V to V_{IN}
- V_{OUT} Accuracy: ±1% with Remote Sense
- Peak Current Mode Control
- Minimum On-Time: 35ns
- Programmable Frequency to 5MHz
- Precision 400mV Enable Threshold, 1μA in Shutdown
- Output Soft-Start with Voltage Tracking
- Power Good Output
- Die Temperature Monitor
- Configurable for Paralleling Power Stages in Forced Continuous Mode
- Thermally-Enhanced 3mm × 3mm LQFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive/Industrial/Communications
- Servers, Telecom Power Supplies
- Distributed DC Power Systems (POL)
- FPGA, ASIC, μP Core Supplies

DESCRIPTION

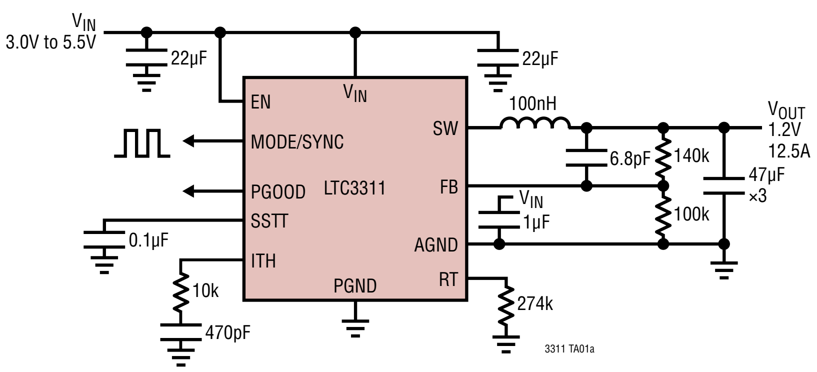
The LTC®3311 is a very small, low noise, monolithic step-down DC/DC converter capable of providing up to 12.5A of output current from a 2.25V to 5.5V input supply. The device employs Silent Switcher 1 architecture with internal hot loop bypass capacitors to achieve both low EMI and high efficiency at switching frequencies as high as 5MHz. For systems with higher power requirements, multi-phasing parallel converters is readily implemented.

The LTC3311 uses a constant frequency, peak current mode control architecture for fast transient response. A 500mV reference allows for low voltage outputs. 100% duty cycle operation delivers low drop out.

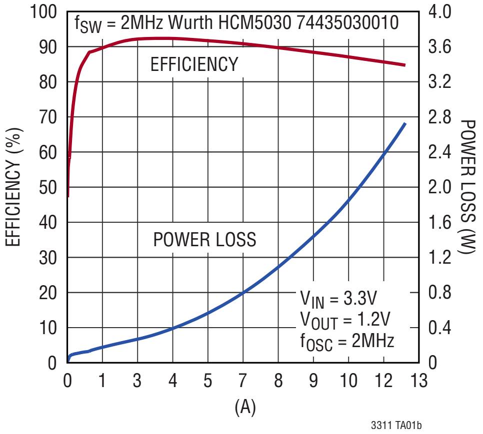
Other features include a power good signal when the output is in regulation, precision enable threshold, output overvoltage protection, thermal shutdown, a temperature monitor, clock synchronization, mode selection and output short circuit protection. The device is available in a compact 18-lead 3mm x 3mm LQFN package.

TYPICAL APPLICATION

1.2V 12.5A Step-Down Converter



Efficiency vs Load Current

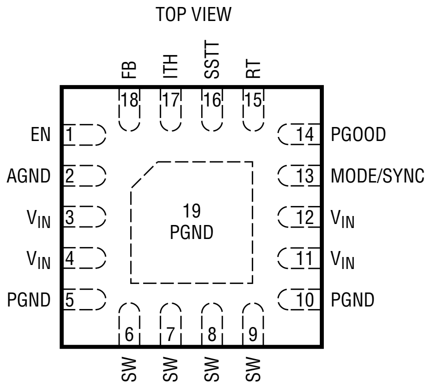


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}	–0.3V to 6V
EN, SSTT	–0.3V to Lesser of (V_{IN} + 0.3V) or 6V
MODE/SYNC	–0.3V to Lesser of (V_{IN} + 0.3V) or 6V
RT	–0.3V to Lesser of (V_{IN} + 0.3V) or 6V
FB	–0.3V to Lesser of (V_{IN} + 0.3V) or 6V
PGOOD	–0.3V to 6V
I_{PGOOD}	5mA
Operating Junction Temperature Range (Notes 2, 3)	
LTC3311J	–40°C to +150°C
LTC3311H	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Maximum Reflow (Package Body) Temperature	260°C

PIN CONFIGURATION



18-LEAD (3mm × 3mm) LQFN PACKAGE

θ_{JA} = 42°C/W, $\theta_{JCbottom}$ = 9°C/W, θ_{JCtop} = 62°C/W, θ_{JB} = 14°C/W
Ψ_{JT} = 1.25°C/W, θ VALUES DETERMINED PER JESD51-12
EXPOSED PAD (PIN 19) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE – TRAY/REEL	AUTOMOTIVE PRODUCTS**	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3311JV#PBF	LTC3311JV#WPBF	LHMN	18-Lead (3mm × 3mm) LQFN (Laminate Package with QFN Footprint)	–40°C to 150°C
LTC3311HV#PBF	LTC3311HV#WPBF			
LTC3311JV#TRPBF	LTC3311JV#WTRPBF			
LTC3311HV#TRPBF	LTC3311HV#WTRPBF			
LTC3311JV#TRMPBF	LTC3311JV#WTRMPBF			
LTC3311HV#TRMPBF	LTC3311HV#WTRMPBF			

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 3) V_{IN} = 3.3V, V_{EN} = V_{IN}, MODE/SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply						
Operating Supply Voltage (V_{IN})		●	2.25		5.5	V
V_{IN} Undervoltage Lockout	V_{IN} Rising	●	2.0	2.1	2.2	V
V_{IN} Undervoltage Lockout Hysteresis				150		mV
V_{IN} Quiescent Current	(Note 4)			1.3	2.0	mA
V_{IN} Quiescent Current in Shutdown	V_{EN} = 0.1V			1	2	µA
EN Threshold	V_{EN} Rising	●	0.375	0.4	0.425	V
EN Hysteresis				60		mV
EN Pin Leakage Current	V_{EN} = 0.4V				±20	nA
Voltage Regulation						
Regulated Feedback Voltage (V_{FB})		●	495	500	505	mV
Feedback Voltage Line Regulation	2.5V ≤ V_{IN} ≤ 5.0V			0.002	0.025	%/V
Feedback Pin Input Current	V_{FB} = 0.5V				±20	nA
Error Amp Transconductance				1		mS
Error Amp Sink/Source Current				±45		µA
Top Switch Current Limit	V_{OUT}/V_{IN} ≤ 0.2, Current Out of SW	●	15	18	21	A
Bottom Switch Current Limit ($I_{VALLEYMAX}$)	Current Out of SW	●	12	14	16	A
Top Switch ON-Resistance				16		mΩ
Bottom Switch ON-Resistance				4.5		mΩ
SW Leakage Current	V_{EN} = 0.1V			±100		nA
V_{ITH} to I_{Peak} Current Gain				26		A/V
Minimum On-Time		●		35	60	ns
Maximum Duty cycle		●	100			%
Power Good/Soft-Start/Temp Monitor						
PGOOD Rising Threshold	As a Percentage of the Regulated V_{OUT}	●	97	98	99	%
PGOOD Hysteresis		●	0.5	1	1.5	%
Overvoltage Rising Threshold	As a Percentage of the Regulated V_{OUT}	●	105	110	115	%
Overvoltage Hysteresis		●	1	2.5	3.5	%
PGOOD Leakage Current	V_{PGOOD} = 5.5V				20	nA
PGOOD Pull Down Resistance	V_{PGOOD} = 0.1V			12	20	Ω
PGOOD Delay				125		µs
PGOOD Input Threshold	Multi-Phase Mode, Rising	●	390	440	490	mV
PGOOD Input Hysteresis				130		mV
Soft-Start Charge Current	V_{SSTT} = 0.5V	●	7	10	13	µA
Temp Monitor Slope				4		mV/°C
Oscillator						
Switching Frequency Range	R_T Programmable	●	0.5		5	MHz
Switching Frequency	R_T = 274k	●	1.8	2	2.2	MHz
Synchronization Frequency Range	R_T = V_{IN}	●	0.5		2.25	MHz
Default Frequency	R_T = V_{IN}	●	1.8	2	2.2	MHz
SYNC Level High on MODE/SYNC		●	1.2			V
SYNC Level Low on MODE/SYNC		●			0.4	V
Minimum MODE/SYNC Pulse Width			40			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A = 25°C$. (Notes 2, 3) $V_{IN} = 3.3V$, $V_{EN} = V_{IN}$, MODE/SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
MODE/SYNC Input Resistance				200		kΩ
MODE/SYNC No Clock Detect Time				20		µs
MODE/SYNC Clock Out Rise/Fall Time	$C_{MODE/SYNC} = 50pF$			10		ns
MODE/SYNC Clock Low Output Voltage	$I_{MODE/SYNC} = 100µA$			0.2		V
MODE/SYNC Clock High Output Voltage	$I_{MODE/SYNC} = 100µA$			$V_{IN} – 0.2$		V
MODE/SYNC Clock Out Duty Cycle				50		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

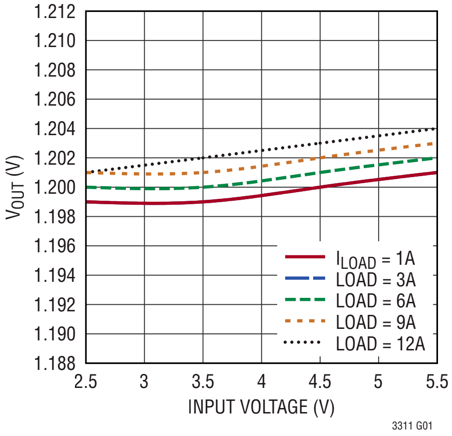
Note 2: The LTC3311J/ LTC3311H are guaranteed to meet performance specifications from –40°C to 150°C junction temperature.

Note 3: The LTC3311 includes overtemperature protection which protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

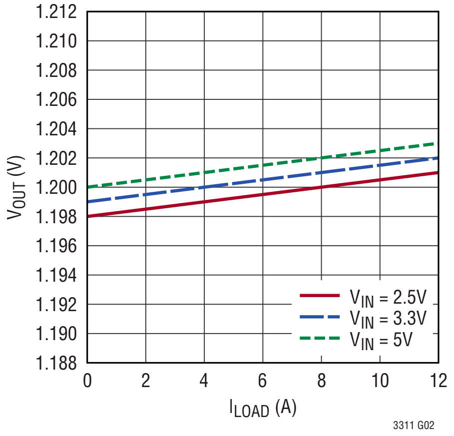
Note 4: Supply current specification does not include switching currents. Actual supply currents will be higher.

TYPICAL PERFORMANCE CHARACTERISTICS

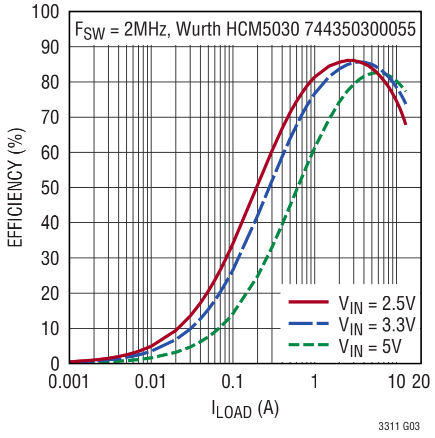
$V_{IN} = 3.3V$, $T_A = 25°C$, unless otherwise noted.



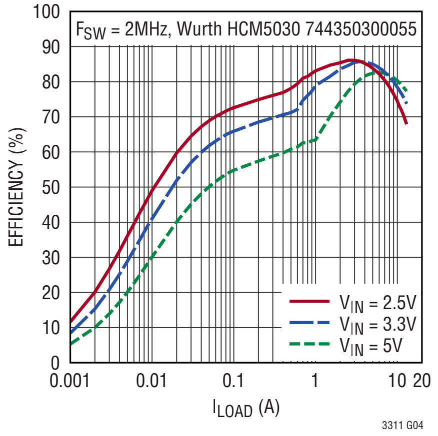
V_{OUT} Line Regulation
$V_{OUT} = 1.2V$



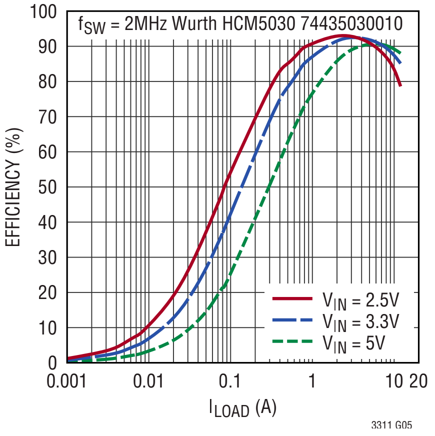
V_{OUT} Load Regulation
$V_{OUT} = 1.2V$



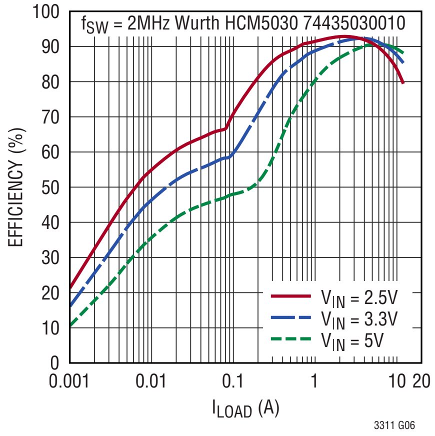
Efficiency, $V_{OUT} = 0.5V$
Forced Continuous Operation



Efficiency, $V_{OUT} = 0.5V$
Pulse Skip Mode Operation



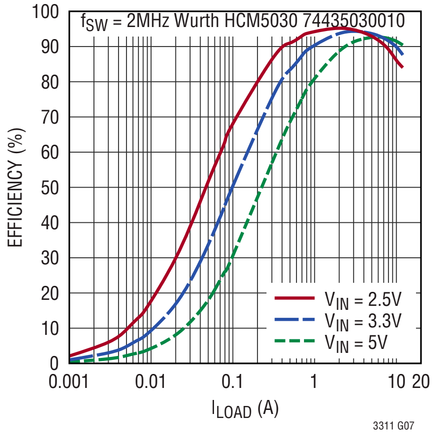
Efficiency, $V_{OUT} = 1.2V$
Forced Continuous Operation



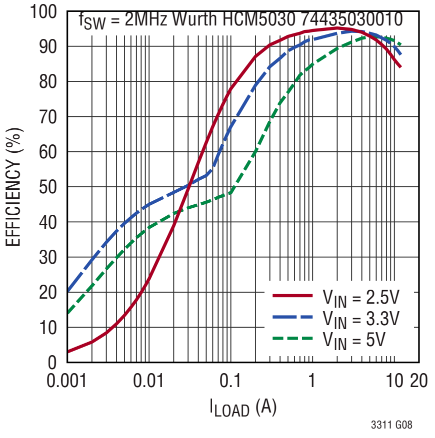
Efficiency, $V_{OUT} = 1.2V$
Pulse Skip Mode Operation

TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

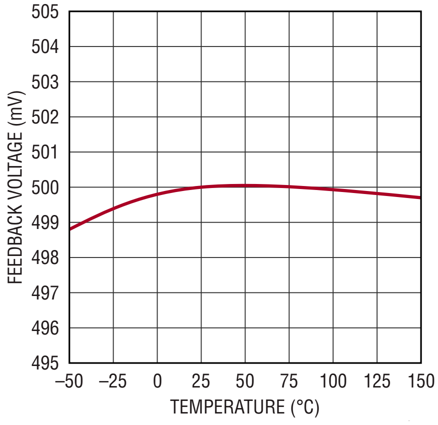
Efficiency, V_{OUT} = 1.8V Forced Continuous Operation



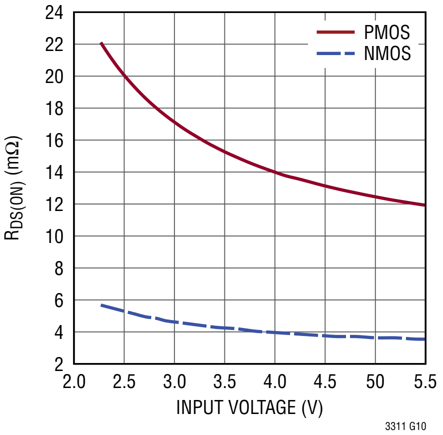
Efficiency, V_{OUT} = 1.8V Pulse Skip Mode Operation



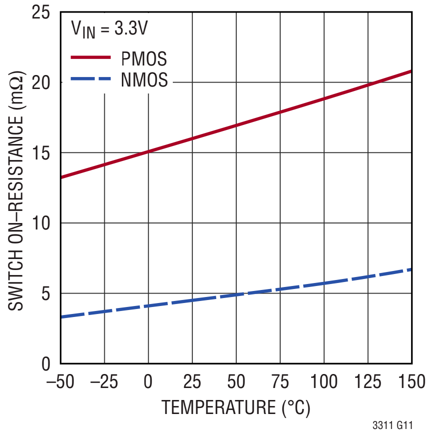
Feedback Reference Voltage



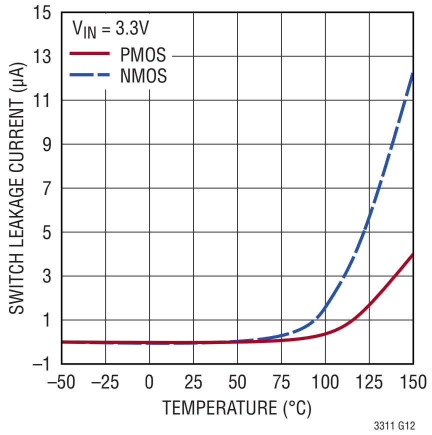
Switch On Resistance vs V_{IN}



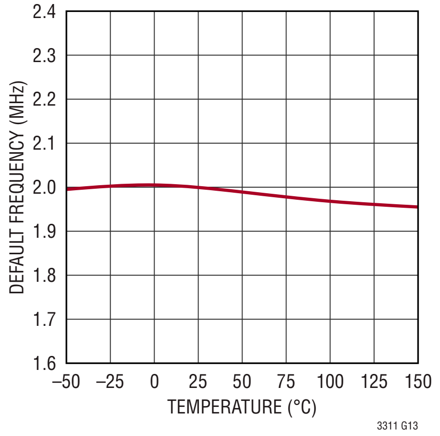
Switch On Resistance



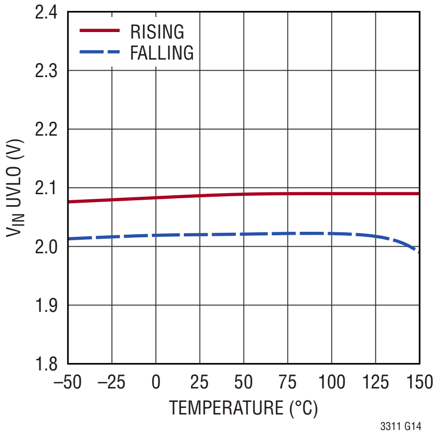
Switch Leakage



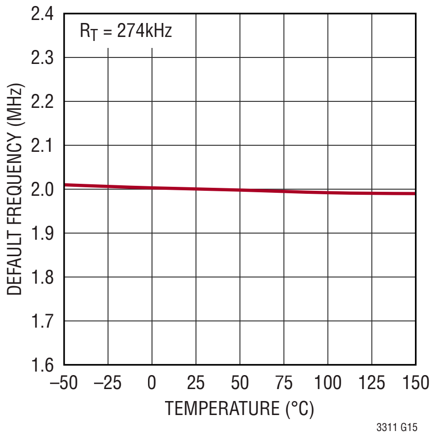
Default Switching Frequency



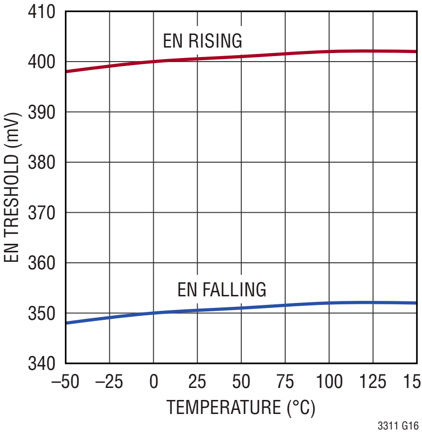
V_{IN} UVLO Threshold

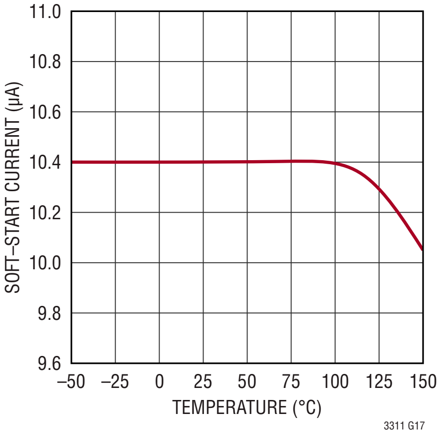


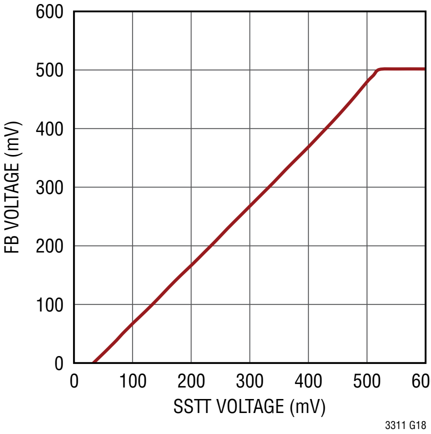
Switching Frequency

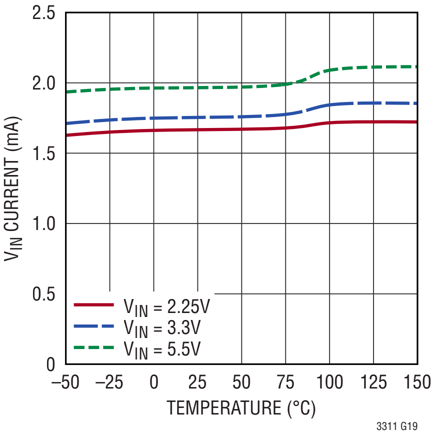


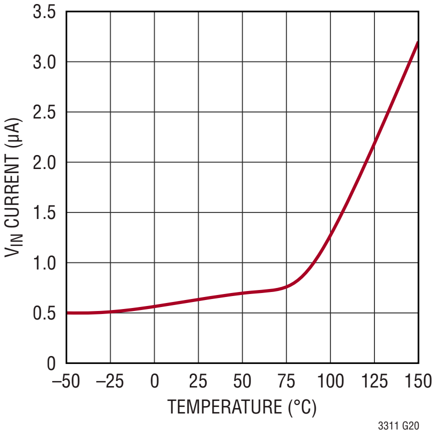
TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

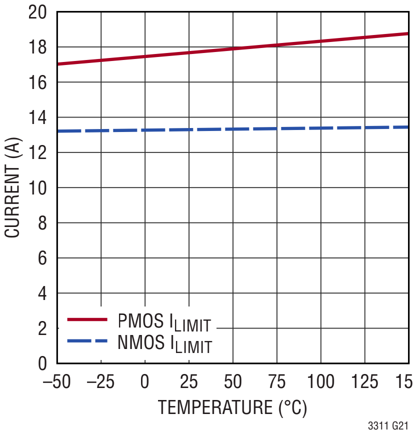

EN Pin Thresholds

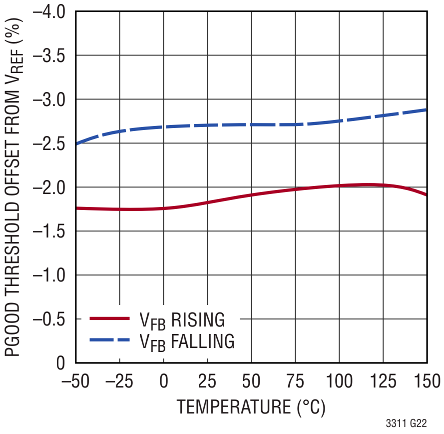

Soft-Start Current

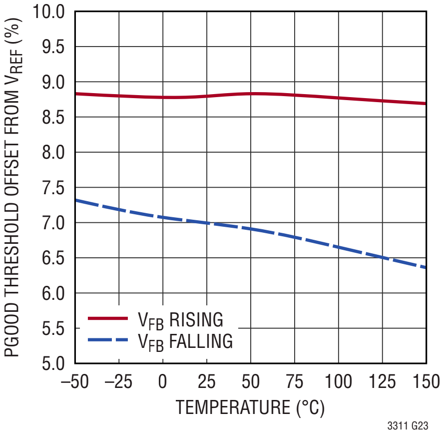

Soft-Start Tracking

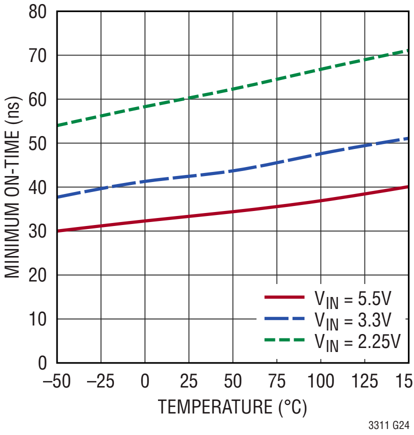

V_{IN} Quiescent Current


V_{IN} Shutdown Current


Switch Current Limit

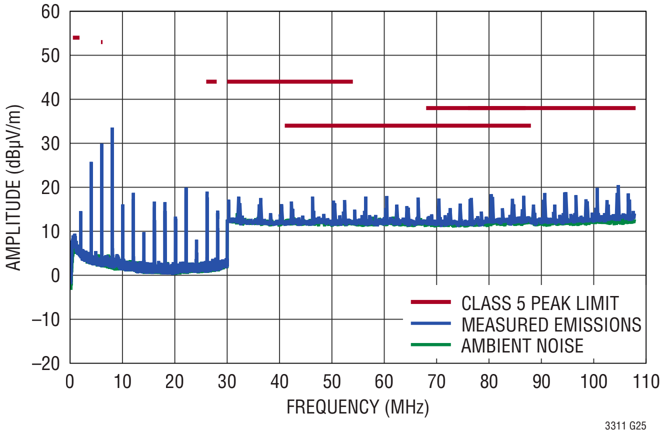

UV PGOOD Threshold


OV PGOOD Threshold


Minimum On-Time

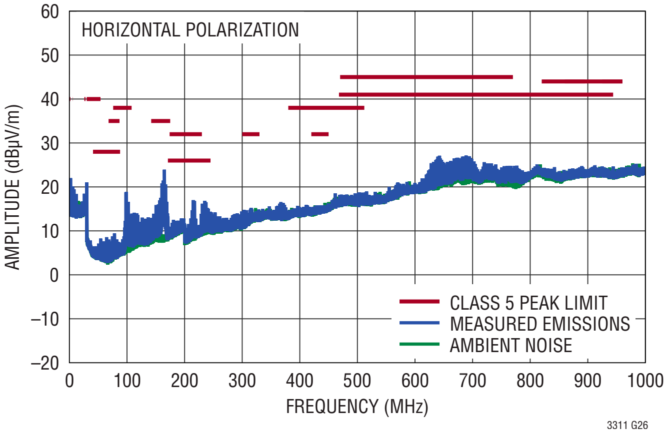
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

CISPR25 Conducted EMI Performance (CISPR25 Conducted Emission Test with Class 5 Peak Limits)



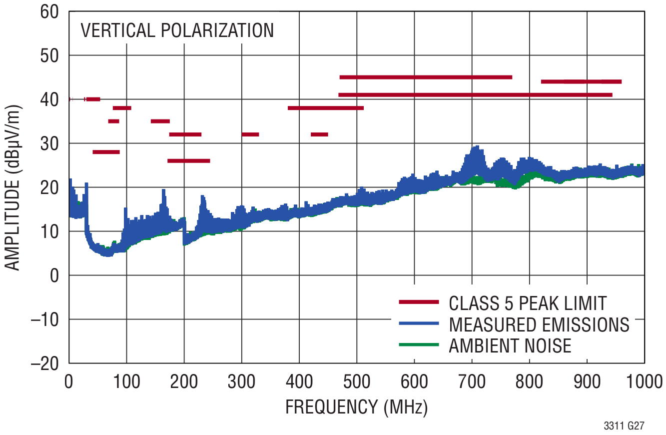
DC3056A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1.2V OUTPUT AT 10A, f_{SW} = 2MHz

Radiated EMI Performance (CISPR25 Radiated Emissions Test with Class 5 Peak Limits)



DC3056A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1.2V OUTPUT AT 10A, f_{SW} = 2MHz

Radiated EMI Performance (CISPR25 Radiated Emissions Test with Class 5 Peak Limits)



DC3056A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1.2V OUTPUT AT 10A, f_{SW} = 2MHz

PIN FUNCTIONS

EN (Pin 1): The EN pin has a precision enable threshold with hysteresis. An external resistor divider, from V_{IN} or from another supply, programs the threshold below which the LTC3311 will shut down. If the precision threshold is not used, directly connect the pin to V_{IN}. When the EN pin is low, the LTC3311 enters a low current shutdown mode where all internal circuitry is disabled.

AGND (Pin 2): The AGND pin is the output voltage remote ground sense. Connect the AGND pin directly to the negative terminal of the output capacitor at the load and to the feedback divider resistor.

V_{IN} (Pins 3, 4, 11, 12): The V_{IN} pins supply current to the internal circuitry and topside power switch. All of the V_{IN} pins must be connected together with short, wide traces and bypassed to PGND with low ESR capacitors located as close as possible to the pins.

PGND (Pins 5, 10, 19): The PGND pins are the return path of the internal bottom side power switch. Connect the PGND pins together and to the exposed pad. Connect the negative terminal of the input capacitors as close to the PGND pins as possible. The PGND node is the main thermal highway and should be connected to a large PCB ground plane with many large vias.

SW (Pins 6–9): The SW pins are the switching outputs of the internal power switches. Connect these pins together to the inductor with short, wide traces.

MODE/SYNC (Pin 13): The MODE/SYNC pin facilitates multiphase operation and synchronization to an external clock. Depending on the mode of operation, the MODE/SYNC pin either accepts an input clock pulse or outputs a clock pulse at its operating frequency. (see Multiphase Operation in Applications Information). The MODE/SYNC pin also programs the mode of operation: pulse skip or forced continuous.

PGOOD (Pin 14): The PGOOD pin is a power good pin and is the open drain output of an internal comparator. The PGOOD output is pulled low when V_{IN} is above 2.25V and the part is in shutdown. When connecting multiple phases in parallel, connect the PGOOD pins together.

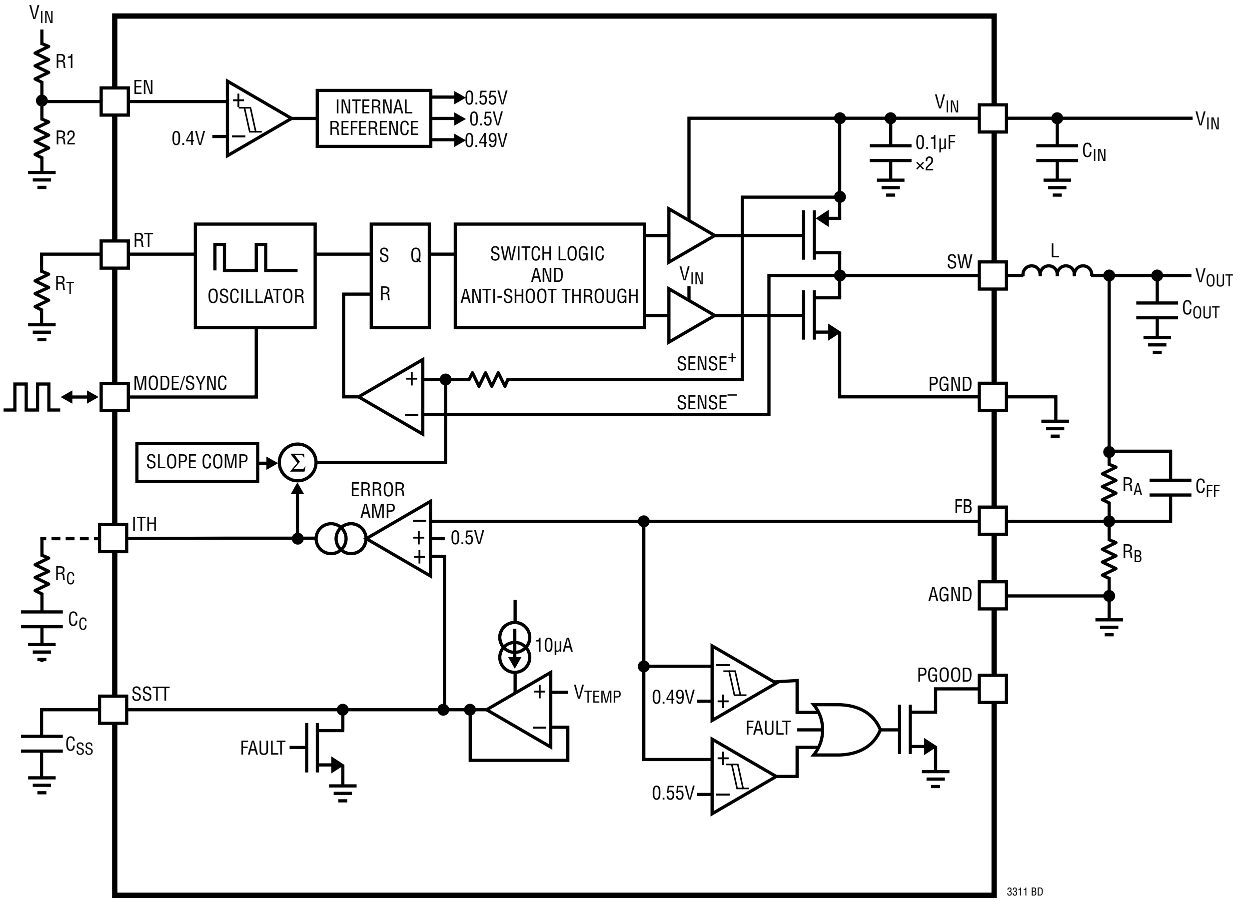
RT (Pin 15): The RT pin sets the oscillator frequency with an external resistor to AGND or sets the phasing for multiphase operation. (see Multiphase Operation in Applications Information).

SSTT (Pin 16): Soft-Start, Track, Temperature Monitor. An internal 10μA current into an external capacitor on the soft-start pin programs the output voltage ramp rate during start-up. During the soft-start cycle, the FB pin voltage will track the SSTT pin voltage. When the soft-start cycle is complete, the tracking function is disabled, the internal reference resumes control of the error amplifier and the SSTT pin servos to a voltage representative of junction temperature. For a clean recovery from an output short circuit condition, the SSTT pin is pulled down to approximately 140mV above the V_{FB} voltage and a new soft-start cycle is initiated. During shutdown and fault conditions, the SSTT pin is pulled to ground.

ITH (Pin 17): The ITH pin is the compensation node for the output voltage regulation control loop. Compensation components connected to this pin are referenced to AGND.

FB (Pin 18): The output voltage feedback pin is externally connected to the output voltage via a resistive divider and is internally connected to the inverting input of the error amplifier. The LTC3311 regulates the FB pin to 500mV. A phase lead capacitor connected between V_{FB} and V_{OUT} is used to optimize the transient response.

BLOCK DIAGRAM



OPERATION

Voltage Regulation

The LTC3311 is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the ITH node. The error amplifier servos the ITH node by comparing the voltage on the FB pin with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the ITH voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or, in pulse-skipping mode, inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The output voltage is resistively divided externally to create a feedback voltage for the regulator. In high current operation, a ground offset may be present between the LTC3311 local ground and ground at the load. To overcome this offset, AGND should have a Kelvin connection to the load ground, and the lowest potential node of the resistor divider should be connected to AGND. The internal error amplifier senses the difference between this feedback voltage and a 0.5V AGND referenced voltage. This scheme overcomes any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. The LTC3311 allows for remote output ground deviations as much as ±100mV with respect to local ground.

If the EN pin is low, the LTC3311 is shut down and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator will be enabled.

Synchronizing the Oscillator to an External Clock

The LTC3311's internal oscillator is synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the MODE/SYNC pin.

During synchronization, the top power switch turn-on is locked to the rising edge of the external frequency source. While synchronizing, the switcher operates in forced continuous mode. The slope compensation is automatically adapted to the external clock frequency.

After detecting an external clock on the first rising edge of the MODE/SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the signal on the MODE/SYNC pin. When the external clock is removed, the LTC3311 detects the absence of the external clock within approximately 20μs. During this time, the PLL will continue to provide clock cycles. Once the external clock removal has been detected, the oscillator gradually adjusts its operating frequency back to the default frequency.

Mode Selection

The MODE/SYNC pin either synchronizes the switching frequency to an external clock, is a clock output, or sets the PWM mode. The PWM modes of operation are either pulse skip or forced continuous. See Table 6 in the Applications Information section. In pulse skip mode, switching cycles are skipped at light loads to regulate the output voltage. During forced continuous mode, the top switch turns on every cycle and light load regulation is achieved by allowing negative inductor current.

Output Power Good

Comparators monitoring the FB pin voltage pull the PGOOD pin low if the output voltage varies from the nominal set point or if a fault condition is present. The comparator includes voltage hysteresis. A time delay to report PGOOD is used to filter short duration output voltage transients.

OPERATION

Soft-Start/Tracking/Temperature Monitor

The soft-start tracking function facilitates supply sequencing, limits V_{IN} inrush current and reduces start-up output overshoot. When soft-starting is completed, the SSTT pin parks itself at a voltage representative of the LTC3311 die junction temperature. The SSTT capacitor is reset during shutdown, V_{IN} UVLO and thermal shutdown. See Application section.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the DC voltage drop across the internal main P-channel MOSFET and the inductor.

In many designs when the input voltage approaches the output voltage, the amplitude of the output ripple voltage increases from its normally low value. To avoid any increase in output ripple voltage under these conditions, it is recommended to utilize a resistor divider on the EN input and limit the V_{IN} turn-on and turn-off thresholds to where the output ripple voltage is acceptable for the given application (typically 500mV above V_{OUT}).

Low Supply Operation

The LTC3311 is designed to operate down to an input supply voltage of 2.25V. An important thermal design consideration is that the $R_{DS(ON)}$ of the power switches increase at low V_{IN}. Calculate the worst case LTC3311 power dissipation and die junction temperature at the lowest input voltages.

Output Short-Circuit Protection and Recovery

The peak inductor current level, at which the current comparator shuts off the top power switch, is controlled by the voltage on the ITH pin. If the output current increases, the error amplifier raises the ITH pin voltage until the average inductor current matches the load current. The LTC3311 clamps the maximum ITH pin voltage, thereby limiting the peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle because the voltage across the inductor is low. To keep the inductor current in control, a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the bottom power switch is greater than the $I_{VALLEY(MAX)}$ the top power switch will be held off. Subsequent switching cycles will be skipped until the inductor current is reduced below $I_{VALLEY(MAX)}$.

Recovery from an output short circuit goes through a soft-start cycle. When V_{OUT} goes below regulation, as defined by the PGOOD threshold, the SSTT voltage is pulled to a voltage just above the FB voltage. Because the SSTT pin is pulled low, a soft-start cycle is initiated once the output short is removed.

APPLICATIONS INFORMATION

Refer to the Block Diagram for reference.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R_A = R_B\left(\frac{V_{OUT}}{500mV} - 1\right) \quad (1)$$

as shown in Figure 1:

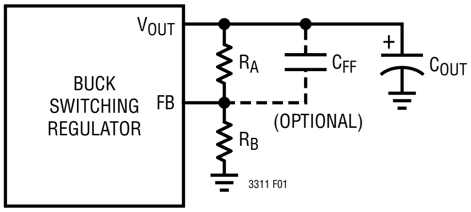


Figure 1. Feedback Resistor Network

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy. When optimizing the control loop for high bandwidth and optimal transient response add a phase-lead capacitor connected from V_{OUT} to FB.

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, transient response and input voltage range.

The advantage of high frequency operation is that smaller inductor and capacitor values may be used. Higher switching frequencies allow for higher control loop bandwidth and, therefore, faster transient response. The disadvantages of higher switching frequencies are lower efficiency, because of increased switching losses, and a smaller input voltage range, because of minimum switch on-time limitations.

Although the maximum programmable switching frequency is 5MHz, the minimum on-time of the LTC3311 imposes a minimum operating duty cycle. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated using Equation 2.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN(MAX)} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (2)$$

where $V_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops and $t_{ON(MIN)}$ is the minimum top switch on-time. Equation 2 shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

The LTC3311 is capable of a maximum duty cycle of 100%, therefore, the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, the inductor DCR and the load current.

Setting the Switching Frequency

The LTC3311 uses a constant frequency PWM architecture. There are three methods to set the switching frequency. The first method is with a resistor (R_T) tied from the RT pin to ground. The frequency can be programmed to switch from 500kHz to 5MHz. Table 1 shows the necessary R_T value for a desired switching frequency.

The R_T resistor required for a desired switching frequency is calculated using Equation 3.

$$R_T = 568 \bullet f_{SW}^{(-1.08)} \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.5	1210
1	549
2	274
2.2	243
3	178
4	130
5	100

APPLICATIONS INFORMATION

The second method to set the LTC3311 switching frequency is by synchronizing the internal PLL circuit to an external frequency applied to the MODE/SYNC pin. The synchronization frequency range is 0.5MHz to 2.25MHz.

The internal PLL starts up at the 2MHz default frequency. After detecting an external clock on the first rising edge of the MODE/SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the MODE/SYNC signal.

The LTC3311 detects when the external clock is removed and will gradually adjust its operating frequency to the 2MHz default frequency. The LTC3311 operates in forced continuous mode when synchronized to an external clock.

The third method of setting the LTC3311 switching frequency is to use the internal nominal 2MHz default clock. See Table 4 for pin configuration.

Inductor Selection and Maximum Output Current

Considerations in choosing an inductor are inductance, RMS current rating, saturation current rating, DCR and core loss.

A good first choice for the inductor value is given by Equation 4 and Equation 5.

$$L \approx \frac{V_{OUT}}{4A \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \text{for} \frac{V_{OUT}}{V_{IN(MAX)}} \le 0.5 \quad (4)$$

$$L \approx \frac{0.25 \bullet V_{IN(MAX)}}{4A \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (5)$$

where f_{SW} is the switching frequency in MHz, V_{IN} is the input voltage and L is the inductor value in µH.

To avoid overheating of the inductor, choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. Overload and short circuit conditions may need to be taken into consideration.

In addition, the saturation current (I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of the inductor ripple current (Equation 6).

$$I_{SAT} \ge I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (6)$$

where $I_{LOAD(MAX)}$ is the maximum output load current for a given application and ΔI_L is the inductor ripple current calculated using Equation 7.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (7)$$

where $V_{IN(MAX)}$ is the maximum application input voltage.

To keep the efficiency high, choose an inductor with the lowest series resistance (DCR). The core material should be intended for high frequency applications.

The LTC3311 limits the peak switch current in order to protect the switches and the system from overload faults. The inductor value must then be sufficiently large to supply the desired maximum output current, $I_{OUT(MAX)}$, which is a function of the switch current limit, I_{LIM}, and the ripple current (Equation 8).

$$I_{OUT(MAX)} = I_{LIM} - \Delta I_L \quad (8)$$

Therefore, the maximum output current that the LTC3311 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

Table 2. Inductor Manufacturers

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Toko	www.toko.com
Wurth Elektronik	www.we-online.com
Vishay	www.vishay.com
XFMRS	www.xfmrs.com

Input Capacitors

Bypass the input of the LTC3311 with at least two bulk storage ceramic capacitors close to the part, one on each side from V_{IN} to PGND. These capacitors should be 0603 or 0805 in size. See layout section for more detail. X7R or

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X5R capacitors are recommended for best performance across temperature and input voltage variations. Note that larger input capacitance is required when a lower switching frequency is used. For high frequency applications, adding two small capacitors close to the part is recommended. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LTC3311 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LTC3311's voltage rating. This situation is easily avoided (see Analog Devices Application Note 88).

Table 3. Ceramic Capacitor Manufacturers

VENDOR	URL
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
Samsung	www.samsungsem.com

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave, generated by the LTC3311, to produce the DC output. In this role it determines the output ripple, thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LTC3311's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

X5R or X7R type capacitors will provide low output ripple and good transient response. Transient performance is improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor saves space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications for suggested capacitor values.

Multiphase Operation

The LTC3311 is easily configurable for multiphase operation. See Table 4.

Connecting the RT pin, of the master phase, to a resistor to AGND programs the frequency and configures the MODE/SYNC pin to become clock output used to drive the MODE/SYNC pin of the slave phase(s).

Connecting the RT pin of the master phase to V_{IN} configures the MODE/SYNC pin to become an input capable of accepting an external clock. The switching frequency defaults to the nominal 2MHz internal frequency when the external clock is unavailable, such as during start-up.

Connecting the FB pin to V_{IN} configures a phase as a slave. The MODE/SYNC becomes an input and the voltage control loop is disabled. The slave phase current control loop is still active and the peak current is controlled via the shared ITH node. Careful consideration should be taken when routing the ITH node between phases. Routing the ITH and AGND nodes together is recommended to create a low inductance path. See the Multi-Phase Demo Board PCB layout as an example.

Connecting the PGOOD pins together and adding an external pull-up resistor allows the master phase to communicate with the slave phases on when start-up has been completed.

Table 4. LTC3311 Multiphase Configuration

Master/Slave	RT Pin	FB Pin	MODE/SYNC Pin	Switching Frequency (f_{SW})
Master	V_{IN}	V_{OUT} Divider	Clock Input	External Clock/2MHz Default
Master	Resistor to AGND	V_{OUT} Divider	Clock Output	RT programmed
Slave	V_{IN} Divider	V_{IN}	Clock Input	External Clock

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The phasing of a slave phase relative to the master phase is programmed with a resistor divider on the RT pin. Use of 1% resistors is recommended. See Table 5 for more information.

Table 5. LTC3311 Programming Slave Phase Angle

SYNC Phase Angle	R3 Ratio	R4 Ratio	R3 Example	R4 Example
0°	0Ω	NA	0Ω	NA
90°	3 • R	R	301k	100k
120°	7 • R	5 • R	243k	174k
180°	NA	0Ω	NA	0Ω
240°	5 • R	7 • R	174k	243k
270°	R	3 • R	100k	300k

When configured for master/slave operation, the slave phases operate in forced continuous modes.

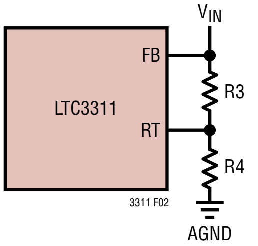


Figure 2. Phase Programming

MODE of Operation

For most configurations, the LTC3311 operates in forced continuous mode. While in forced continuous mode, regulation at low currents is achieved by allowing negative inductor current. Switching cycles are not skipped.

The LTC3311 operates in pulse skip mode when both R_T and MODE/SYNC pins are connected to V_{IN}. In this mode, the switching frequency is set with the nominal 2MHz internal clock. While in pulse skip mode negative current is disallowed and regulation at low currents is achieved by skipping switching cycles.

Table 6. LTC3311 Single Phase Configuration

RT Pin Connection	MODE/SYNC Pin Connection	MODE of Operation	Switching Frequency
VIN	Clock Input	Forced Continuous	External Clock
VIN	AGND	Forced Continuous	2MHz Default
VIN	VIN	Pulse Skip	2MHz Default
Resistor to AGND	Clock Output	Forced Continuous	RT Programmed

Synchronization

To synchronize the LTC3311 oscillator to an external frequency, configure the MODE/SYNC pin as an input by connecting the RT pin to V_{IN}. Drive the MODE/SYNC pin with a square wave in the frequency range of 500 kHz to 2.25MHz range, an amplitude greater than 1.2V and less than 0.4V with a pulse width greater than 40ns.

The LTC3311 phase locked loop (PLL) will synchronize the internal oscillator to the clock applied to the MODE/SYNC pin. At start up, before the LTC3311 recognizes the external clock applied to MODE/SYNC, the LTC3311 will switch at its default frequency of 2MHz. Once the externally applied clock is recognized, the switching frequency will gradually transition from the default frequency to the applied frequency. If the external clock is removed, the LTC3311 will slowly transition back to the default frequency.

The LTC3311 operates in forced continuous mode during synchronization. An internal 200kΩ resistor on MODE/SYNC pin to AGND allows the MODE/SYNC pin to be left floating.

Transient Response and Loop Compensation

When determining the compensation components, C_{FF}, R_C, and C_C, control loop stability and transient response are the two main considerations.

The LTC3311 has been designed to operate at a high bandwidth for fast transient response capability. Operating at a high loop bandwidth reduces the output capacitance required to meet transient response requirements.

Applying a load transient and monitoring the response of the system or using a network analyzer to measure the actual loop response are two ways to verify and optimize

APPLICATIONS INFORMATION

the control loop stability. LTpowerCAD® is a useful tool to help optimize the compensation components.

When using the load transient response method to stabilize the control loop, apply an output current pulse of 20% to 100% of full load current having a rise time of 1µs. This will produce a transient on the output voltage and ITH pin waveforms.

Switching regulators take multiple cycles to respond to a step in load current. When a load step occurs, V_{OUT} is immediately perturbed, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, monitor V_{OUT} for overshoot or ringing that would indicate a stability problem. The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R_C and the bandwidth of the loop increases with decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, adding a feed forward capacitor, C_{FF}, improves the high frequency response. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R_A to improve the phase margin. The compensation components of the typical application circuits are a good starting point for component values.

The output voltage settling behavior is related to the stability of the closed-loop system. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Analog Devices Application Note 76.

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of nominal, the LTC3311 top power switch will be turned off. If the output remains out of regulation for more than 100µs, the PGOOD pin will be pulled low.

An output overvoltage event should not happen under normal operating conditions.

Output Voltage Sensing

The LTC3311 AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. To achieve good load regulation, connect the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. A drop in the high current power ground return path will be compensated. All of the signal components, such as the FB resistor dividers and soft-start capacitor, should be referenced to the AGND node. The AGND node carries very little current and, therefore, can be a minimal size trace. See the example PCB Layout for more information.

Enable Threshold Programming

The LTC3311 has a precision threshold enable pin to enable or disable switching. When forced low, the LTC3311 enters a low current shutdown mode.

The rising threshold of the EN comparator is 400mV, with 60mV of hysteresis. Connect the EN pin to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to EN programs the LTC3311 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 9.

$$V_{IN(EN)} = \left(\frac{R1}{R2} + 1\right) \bullet 400\text{mV} \qquad (9)$$

where the LTC3311 will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

Alternatively, a resistor divider from an output of another regulator to the enable pin of the LTC3311 provides event-based power-up sequencing, enabling the LTC3311 when

APPLICATIONS INFORMATION

the output of the other regulator reaches a predetermined level.

Output Voltage Tracking and Soft-Start

The LTC3311 allows the user to program its output voltage ramp rate by means of the SSTT pin.

An internal 10µA pulls up the SSTT pin. Putting an external capacitor on SSTT enables soft-starting the output to prevent current surge on the input supply and output voltage overshoot. During the soft-start ramp, the output voltage will proportionally track the SSTT pin voltage. When the soft-start is complete, the pin will servo to a voltage proportional to the LTC3311 junction temperature. See Figure 3 showing the SSTT pin operating range.

The soft-start time is calculated using Equation 10.

$$t_{SS} = C_{SS} \bullet \frac{500mV}{10\mu A} \tag{10}$$

For output tracking applications, SSTT can be externally driven by another voltage source. From 0V to 0.5V, the SSTT voltage will override the internal 0.5V reference input to the error amplifier, thus regulating the FB pin voltage to that of SSTT pin. When SSTT is above 0.5V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage

An active pull-down circuit is connected to the SSTT pin to discharge the external soft-start capacitor in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low or thermal shutdown.

Temperature Monitor

Once the soft-start cycle has completed and the output power good flag thrown, the SSTT pin reports the die junction temperature. The LTC3311 regulates the SSTT pin to a voltage proportional to the junction temperature. While reporting the temperature, the SSTT voltage is not valid below 1V. The junction temperature is calculated with Equation 11.

$$T_J\ (^\circ C) = \frac{V_{SSTT}}{4mV} - 273 \tag{11}$$

The following procedure is used for a more accurate measurement of the junction temperature:

1. Measure the ambient temperature T_A.
2. Measure the SSTT voltage while in pulse skip mode with the V_{OUT} pulled up slightly higher than the regulated V_{OUT}.
3. Calculate the slope of the temperature sensing circuit with Equation 12.

$$\text{Slope}\ (mV/^\circ C) = \frac{V_{SSTT}}{T_A + 273} \tag{12}$$

4. Calculate the junction temperature with the new calibrated slope.

When the output voltage goes out of regulation and the power good pin is pulled low, the soft-start pin no longer reports the temperature.

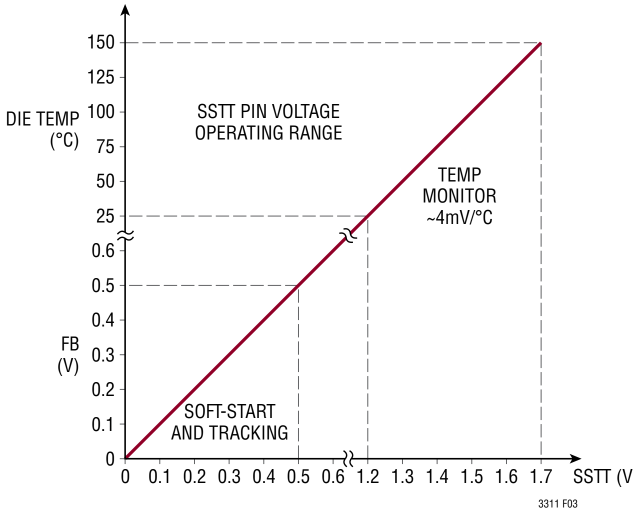


Figure 3. Soft-Start and Temperature Monitor Operation

Output Power Good

When the LTC3311's output voltage is within the –2/+10% window of the nominal regulation voltage the output is considered good and the open-drain PGOOD pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PGOOD pin low. To prevent glitching both the upper and lower thresholds, include 1% of hysteresis as well as a built in time delay, typically 100µs. The PGOOD

APPLICATIONS INFORMATION

pin is also actively pulled low during fault conditions: EN pin is low, V_{IN} is too low or in thermal shutdown.

For multiphase applications the PGOOD pin is used for communication between the master and slave phases. Connect the PGOOD pins together and pull-up to V_{IN} or V_{OUT} with an external resistor.

Output Short Circuit Protection and Recovery

The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the ITH pin. If the output current increases, the error amplifier raises the ITH pin voltage until the average inductor current matches the new load current. In normal operation, the LTC3311 clamps the maximum ITH pin voltage.

When the output is shorted to ground, the inductor current decays very slowly during the switch off time because of the low voltage across the inductor. To keep the current in control, a secondary limit is also imposed on the valley inductor current. If the inductor current measured through the bottom power switch increases beyond $I_{VALLEY(MAX)}$, the top power switch will be held off and switching cycles will be skipped until the inductor current is reduced.

Recovery from a short circuit can be abrupt and because the output is shorted and below regulation the regulator is requesting the maximum current to charge the output. When the short circuit condition is removed, the inductor current could cause an extreme voltage overshoot in the output. The LTC3311 addresses this potential issue by regulating the SSTT voltage just above the FB voltage anytime the output is out of regulation. Therefore, a recovery from an output short circuit goes through a soft-start cycle. The output ramp is controlled and the overshoot is minimized.

Low EMI PCB Layout

The LTC3311 is specifically designed to minimize EMI/EMC emissions and also to maximize efficiency when switching at high frequencies. For optimal performance, the LTC3311 requires the use of multiple V_{IN} bypass capacitors.

The LTC3311 does not have any internal bypass capacitors and hence requires three additional 0201 external capacitors (C_{IN5}, C_{IN6}, and C_{IN7}), as shown in Figure 4. Place these capacitors as close as possible to the IC.

To avoid noise coupling into FB, the resistor divider should be placed near the FB and AGND pins and physically close to the LTC3311. The remote output and ground traces should be routed together as a differential pair to the remote output. These traces should be terminated as close as physically possible to the remote output point that is to be accurately regulated through remote differential sensing.

See Figure 4 for a recommended PCB layout.

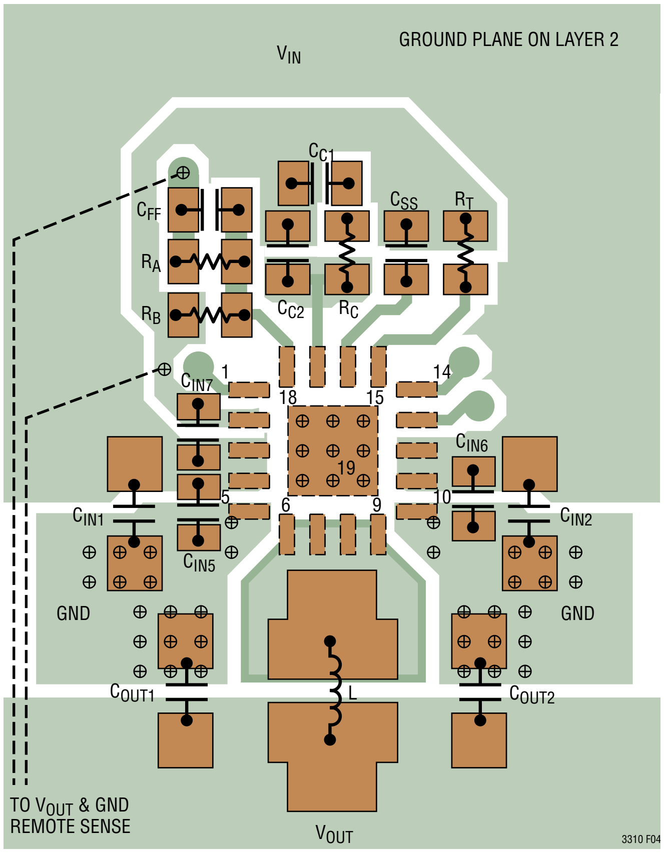


Figure 4. Recommended PCB Layout for the LTC3311

APPLICATIONS INFORMATION

Large, switched currents flow in the LTC3311 V_{IN}, SW and PGND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN} and PGND pins. Place the input capacitors, inductor and output capacitors on the same layer of the circuit board. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.

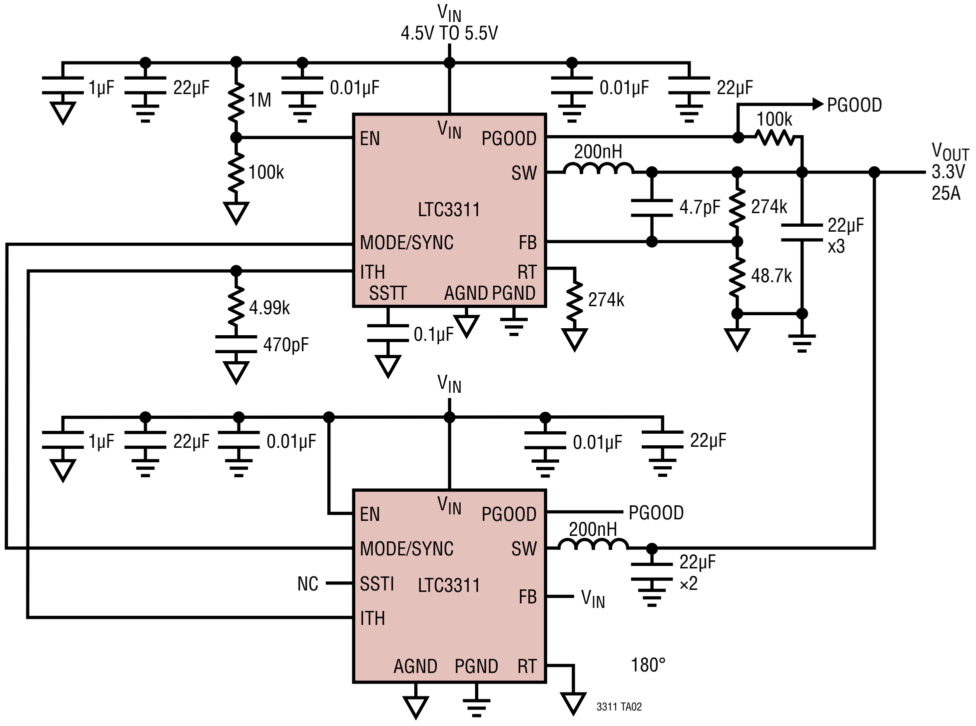
The SW node should be as short as possible. Finally, keep the FB and RT nodes small and away from the noisy SW node.

High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LTC3311. The PGND pins and the exposed pad on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with many thermal vias; these layers will spread heat dissipated by the LTC3311. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LTC3311 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is monitored with the SSTT pin.

TYPICAL APPLICATIONS

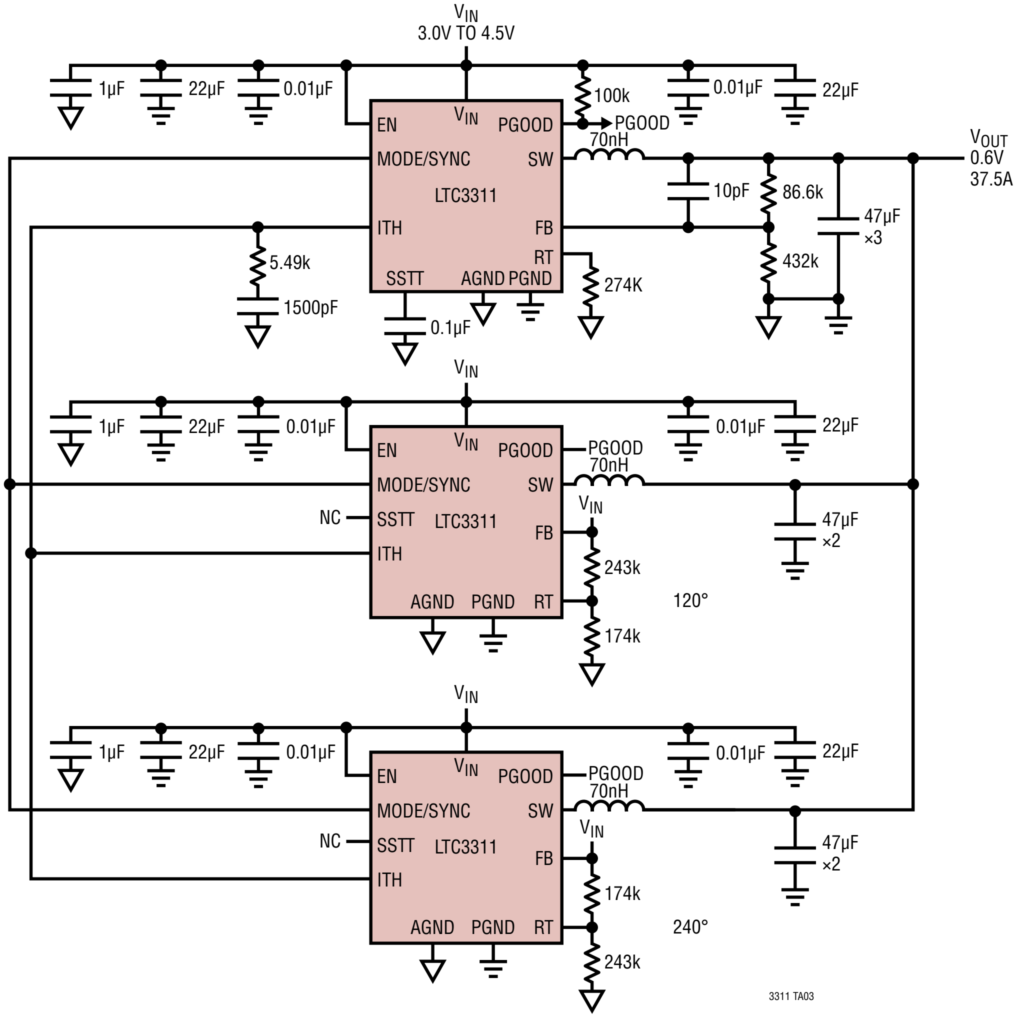
Dual Phase 5V to 3.3V, 25A, Forced Continuous Mode



L = COILCRAFT, XEL4030-201ME

TYPICAL APPLICATIONS

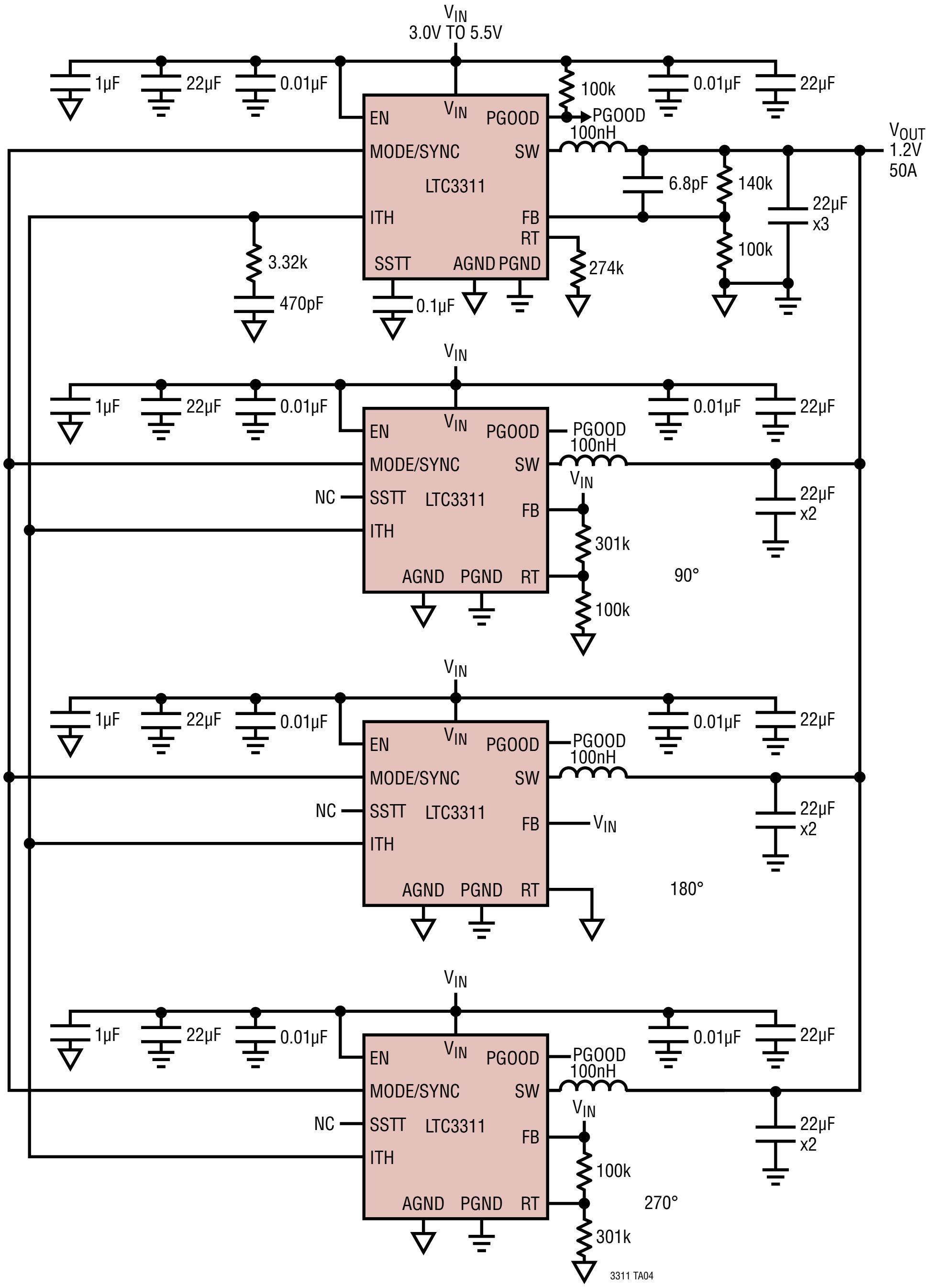
Three Phase, 0.6V, 37.5A, Forced Continuous Mode



L = COILCRAFT XEL3520-700MEB

TYPICAL APPLICATIONS

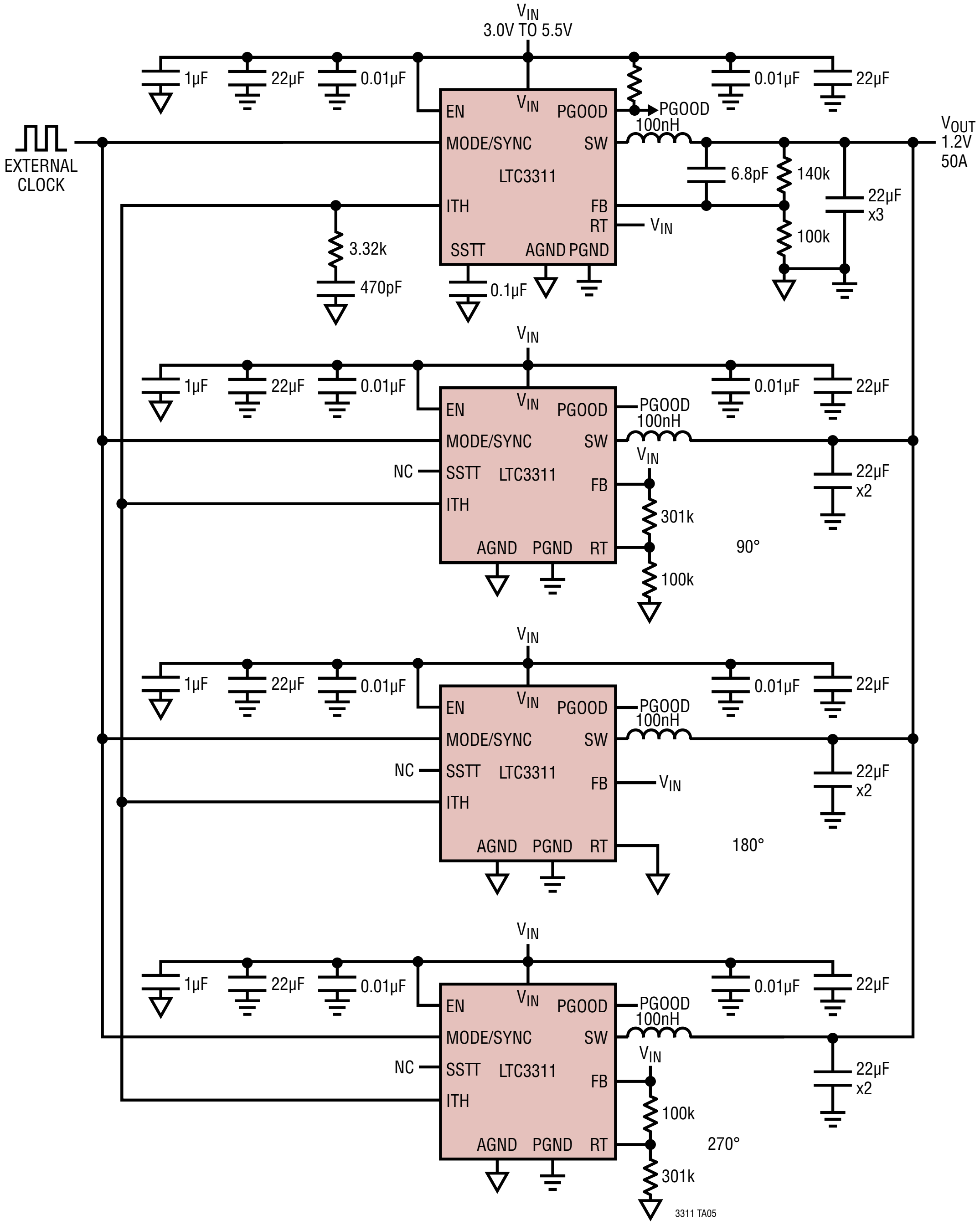
Four Phase, 2MHz, 1.2V, 50A, Forced Continuous Mode



L = COILCRAFT, XEL4030-101ME

TYPICAL APPLICATIONS

Four Phase, 2MHz, 1.2V, 50A Driven with External Clock, Forced Continuous Mode



L = COILCRAFT, XEL4030-101ME

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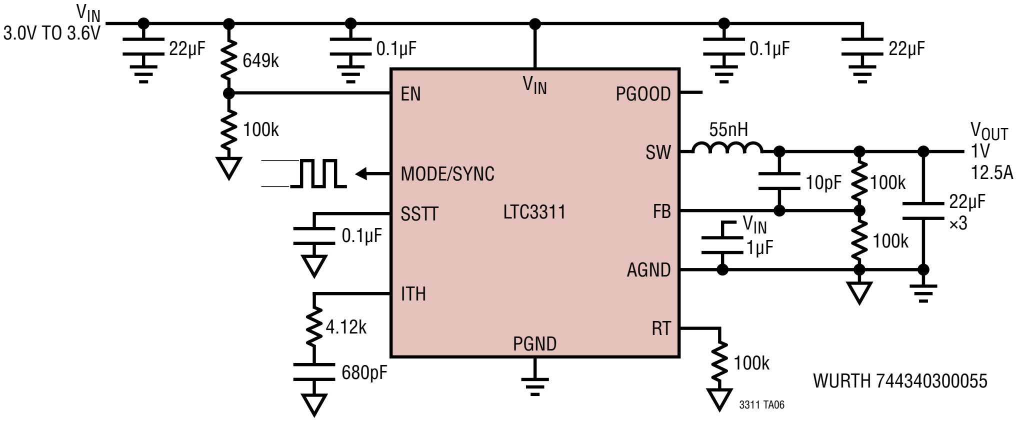
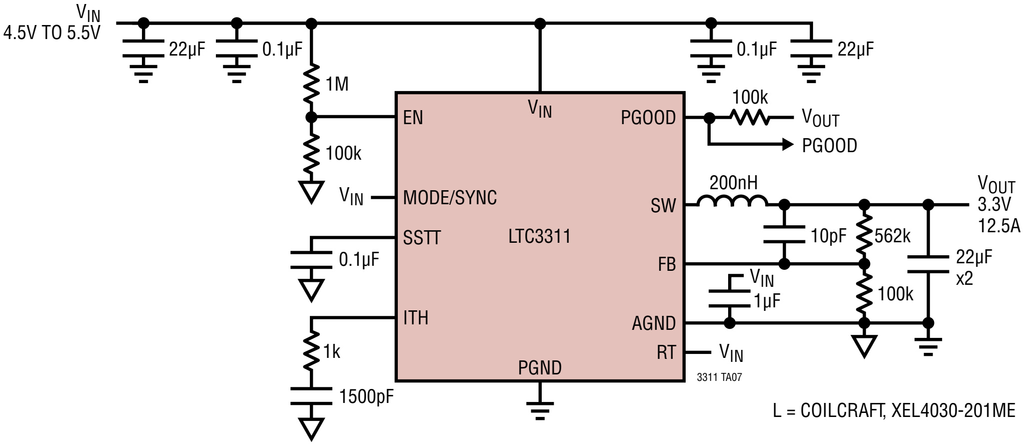
TYPICAL APPLICATIONS

5MHz, 1V, 12.5A, Forced Continuous Mode



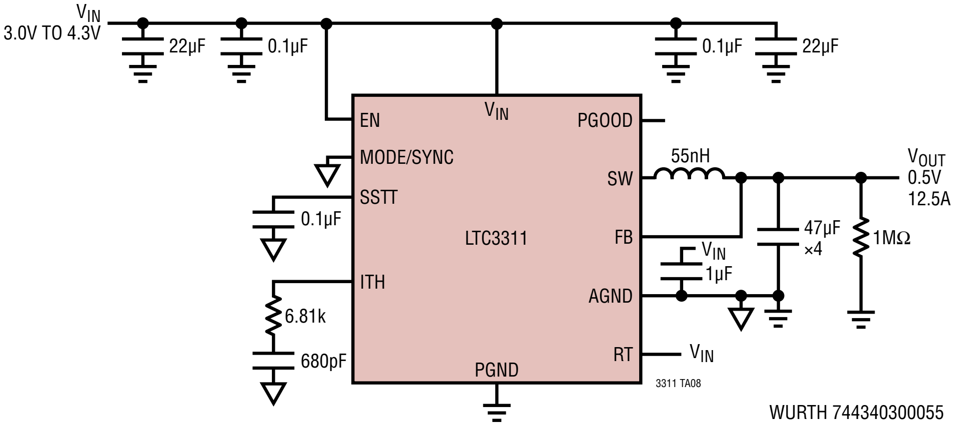
WURTH 744340300055

2MHz, 3.3V, 12.5A, Pulse Skip Mode



L = COILCRAFT, XEL4030-201ME

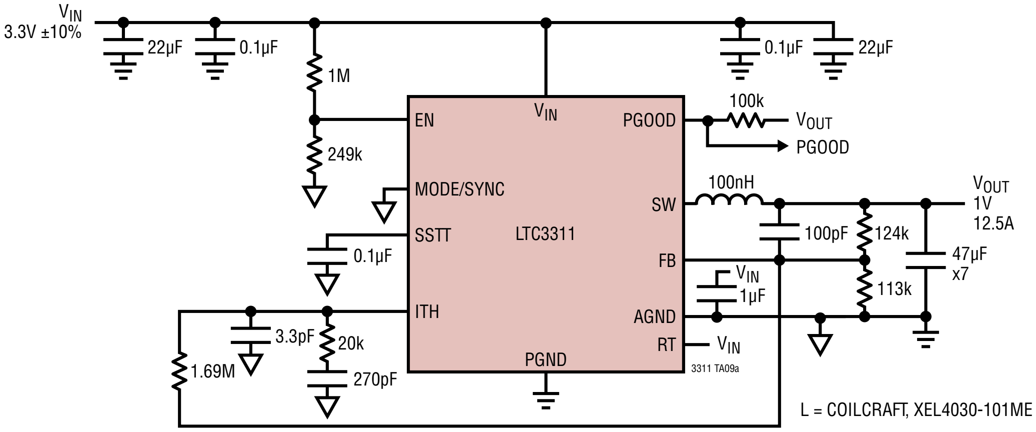
High Efficiency, 2MHz, 0.5V, 12.5A, Forced Continuous Mode, Low Part Count



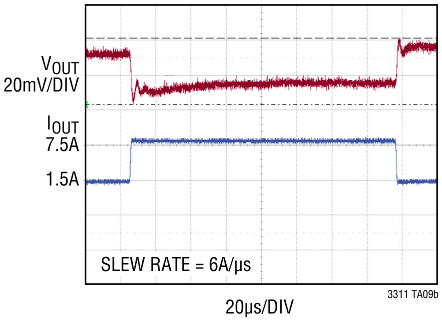
WURTH 744340300055

TYPICAL APPLICATIONS

2MHz, 1.0V, Forced Continuous
1.5A DC to 7.5A Step Load 6A/µs Transient, ±1.8% V_{OUT} Deviation

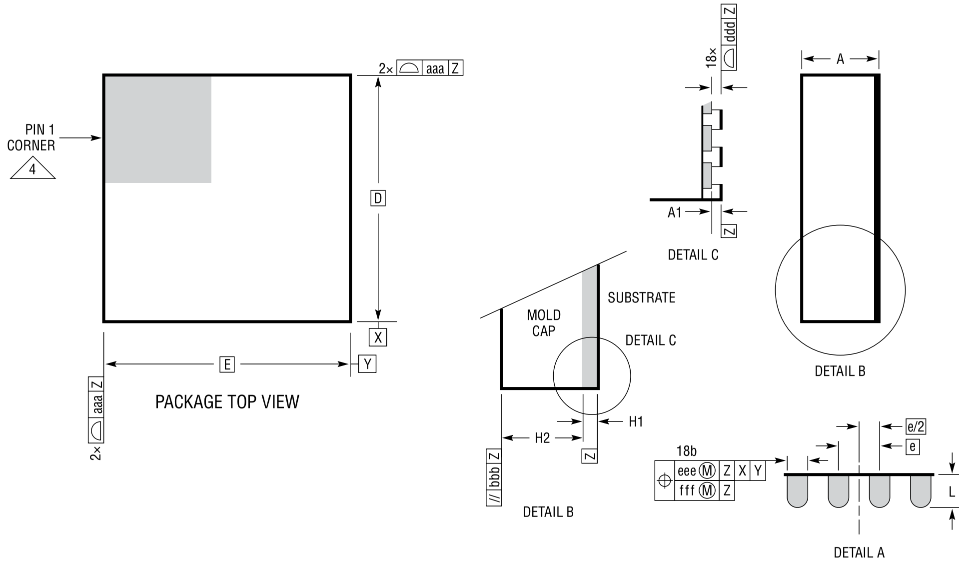


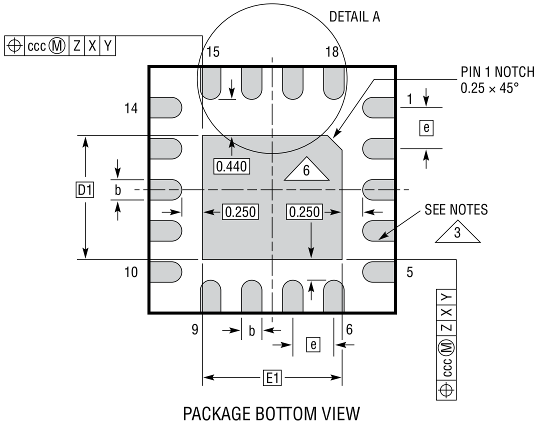
L = COILCRAFT, XEL4030-101ME



PACKAGE DESCRIPTION

LQFN Package
18-Lead (3mm × 3mm × 0.94mm)
(Reference LTC DWG # 05-08-1548 Rev C)

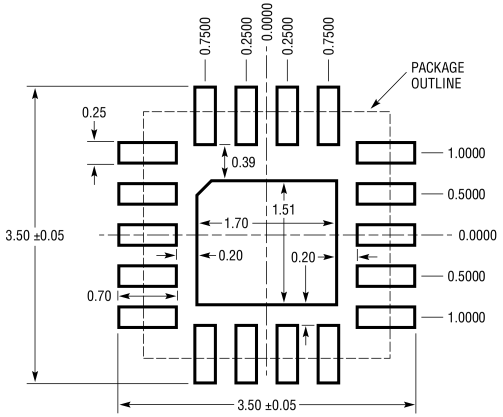




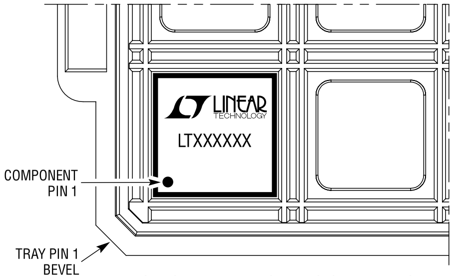
SYMBOL	MIN	NOM	MAX	NOTES
		DIMENSIONS		
A	0.85	0.94	1.03	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		3.00		
D1		1.51		
E1		1.70		
e		0.50		
H1		0.24 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.08	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINIALS AND HEAT FEATURES
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII



SUGGESTED PCB LAYOUT
TOP VIEW



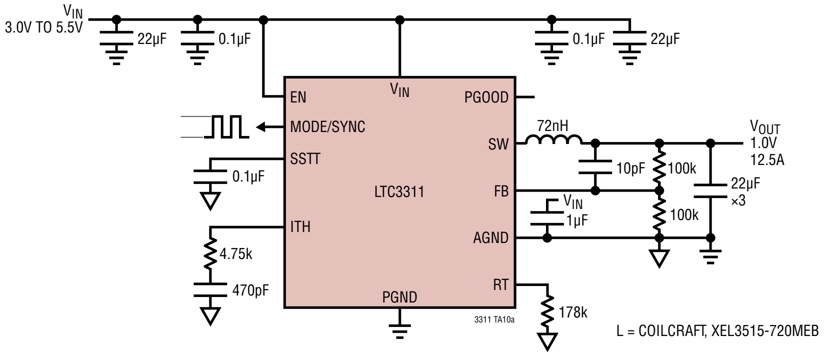
PACKAGE IN TRAY LOADING ORIENTATION

LQFN 18 1218 REV C

Rev. 0

TYPICAL APPLICATION

3MHz, 1.0V, 12.5A , Forced Continuous Mode



L = COILCRAFT, XEL3515-720MEB

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3311S	5V, 12.5A Synchronous Step-Down Silent Switcher 2 in 3mm × 3mm LQFN	Switching Frequencies Up to 5MHz. Silent Switcher Architecture 2 for Ultralow EMI Emissions. 2.25V to 5.5V Input Operating Range. 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy. PGOOD Indication, R_T Programming, SYNC Input. Configurable for Paralleling Power Stages. Pin Compatible with LTC3310/LTC3310S. 3mm × 3mm LQFN-18 Package.
LTC3310/ LTC3310S	5V, 10A Synchronous Step-Down Silent Switcher/Silent Switcher 2 in 3mm × 3mm LQFN	Switching Frequencies Up to 5MHz. Silent Switcher/Silent Switcher 2 Architecture for Ultralow EMI Emissions. 2.25V to 5.5V Input Operating Range. 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy. PGOOD Indication, R_T Programming, SYNC Input. Configurable for Paralleling Power Stages. 150°C Operation (LTC3310). Pin Compatible with LTC3311/LTC3311S. 3mm × 3mm LQFN-18 Package.
LTC3315A/ LTC3315B	Dual 5V, 2A Synchronous Step-Down DC/DCs in 2mm × 2mm LQFN	Dual Monolithic Synchronous Step-Down Voltage Regulators each Capable of Supplying 2A at Switching Frequencies up to 3MHz(A) and 10MHz(B). 2.25V to 5.5V Input Operating Range. 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy. PGOOD Indication, SYNC Input. 2mm × 2mm LQFN-12.
LTC3636/ LTC3636-1	Dual Channel 6A, 20V Monolithic Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V (LTC3636), 1.8V (LTC3636-1), I_Q = 1.3mA, I_{SD} < 13µA, 4mm × 5mm QFN-28
LTC3615/ LTC3615-1	Dual Channel 5.5V, 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	94% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 130µA, I_{SD} < 1µA, 4mm × 4mm QFN-24 Package
LTC3614/ LTC3616	5.5V, 4A/6A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Tracking and DDR	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LTC3612	5.5V, 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP-16E and 4mm × 4mm QFN-16 Packages
LTC7150S	20V, 20A Synchronous Step-Down Silent Switcher 2 Regulator	92% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} ≤ 40µA, Differential Remote Sense, 6mm × 5mm BGA
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2 Regulator	96% Efficiency, V_{IN}: 2.8V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 240µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LT8640S	42V, 6A Synchronous Step-Down Silent Switcher 2 with 2.5µA Quiescent Current	96% Efficiency, V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 1.0V, I_Q = 230µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LT8650S	Dual Channel 4A, 42V, Synchronous Step-Down Silent Switcher 2 with 6.2µA Quiescent Current	94.5% Efficiency, V_{IN}: 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 5mA, I_{SD} < 2µA, 4mm × 6mm LQFN-32
LTC7151S	20V, 15A Synchronous Step-Down Silent Switcher 2 Regulator	92.5% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.5V, I_Q = 2mA, I_{SD} < 20µA, 4mm × 5mm LQFN-28
LTC3307A/B, LTC3308A/B, LTC3309A/B	3A, 4A and 6A 5V Synchronous Step-Down Silent Switcher DC/DC in 2mm × 2mm LQFN-12	Monolithic Synchronous Step-Down DC/DC Capable of Supplying up to 6A at Switching Frequencies Up to 3MHz(A) and 10MHz(B). Silent Switcher Architecture for Ultralow EMI Emissions. 2.25V to 5.5V Input Operating Range. 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy. PGOOD Indication, RT Programming, SYNC Input. 2mm × 2mm LQFN-12