Primary Battery SOH Monitor with Precision Coulomb Counter

FEATURES

- **Battery Input Voltage Range: 1.8V to 5.5V**
- **100nA Quiescent Current**
- **8 Primary Battery Peak Input Current Limits: 5mA/10mA/15mA/20mA/25mA/50mA/75mA/100mA**
- **SOH Monitor for Primary Battery**
  - **Integrated Coulomb Counter (Q)**
  - **Additional Monitors for Battery Voltage (V), Battery Impedance (Z), and Temperature (T)**
- **Primary Battery Current (BAT_IN) or Load Current (BAT_OUT) is Counted**
- **Integrated ±10mA Supercapacitor Balancer**
- Programmable Coulomb Counter Prescaler for Wide Range of Battery Sizes
- Programmable Discharge Alarm Threshold with Interrupt Output
- I^2C Interface
- Tiny 12-Lead 2mm × 2mm LFCSP and 16-Ball 1.64mm × 1.64mm WLCSP Packages

APPLICATIONS

- Low Power Primary Battery Powered Systems (e.g., 1× $LiSOCl_2$, 2–3× Alkaline)
- Remote Industrial Sensors (e.g., Meters, Alarms)
- Asset Trackers
- Electronic Door Locks
- Keep-Alive Supplies/Battery Backup
- SmartMesh® Applications

DESCRIPTION

The LTC®3337 is a primary battery state of health (SOH) monitor with a built-in precision coulomb counter. It is designed to be placed in series with a primary battery with minimal associated series voltage drop. The patented *infinite dynamic range* coulomb counter tallies ALL accumulated battery discharge and stores it in an internal register accessible via an I^2C interface. A discharge alarm threshold based on this state of charge (SOC) is programmable. When it is reached, an interrupt is generated at the $\overline{IRQ}$ pin. Coulomb counter accuracy is constant down to no load.

The LTC3337 also integrates additional SOH monitoring which measures and reports via I^2C: battery voltage, battery impedance, and temperature.

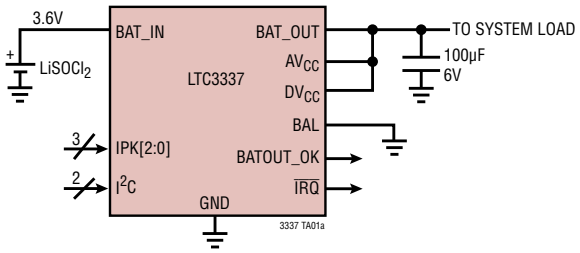
To accommodate a wide range of primary battery inputs, the peak input current limit is pin selectable from 5mA to 100mA.

Coulombs can be calculated for either the BAT_IN or BAT_OUT pin, determined by the AV_{CC} pin connection.

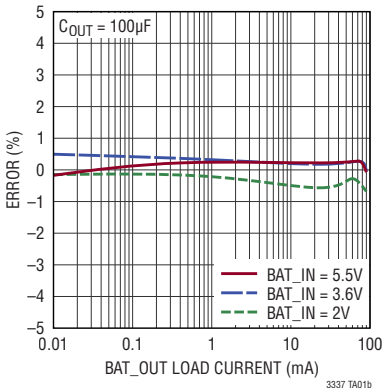
A BAL pin is provided for applications utilizing a stack of two supercapacitors (optional) at the output.

The LTC3337 is offered in both 12-lead 2mm × 2mm LFCSP and 16-ball 1.64mm × 1.64mm WLCSP packages.

TYPICAL APPLICATION



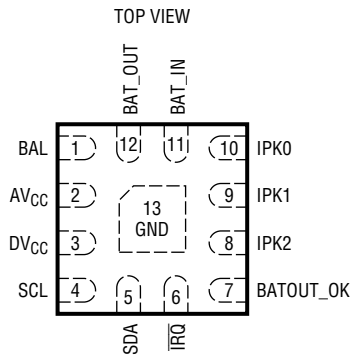
Total Coulomb Counter Error (100mA I_{PEAK} Setting)



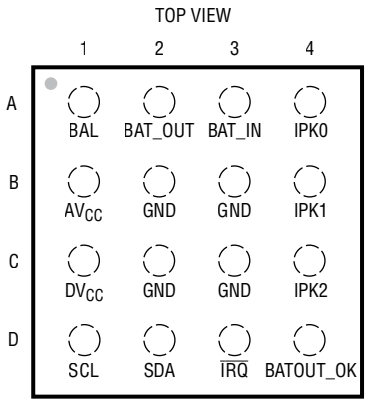
ABSOLUTE MAXIMUM RATINGS (Note 1)

BAT_IN, BAT_OUT, AV_{CC} Voltage ..... –0.3V to 6V
(BAT_OUT – BAT_IN) Differential Voltage 0.3V
DV_{CC}, SCL, SDA Voltage ..... –0.3V to 6V
IPK[2:0] Voltage ..... –0.3V to [Lesser of (BAT_IN + 0.3V) or 6V]
BAL Voltage ..... –0.3V to [Lesser of (BAT_OUT + 0.3V) or 6V]
$\overline{IRQ}$, BATOUT_OK Current ..... ±1mA
BAT_OUT Current 150mA
SDA Current 5mA
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to +125°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body) Temperature .. 260°C

PIN CONFIGURATION



LFCSP PACKAGE
12-LEAD (2mm × 2mm × 0.75mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 52.78°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



WLCSP PACKAGE
16-BALL (1.64mm × 1.64mm × 0.47mm)
T_{JMAX} = 125°C, θ_{JA} = 70.8°C/W
$\theta_{JC(TOP)}$ = 0.78°C/W (JDEC BOARD)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL (MINI)	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3337ERC#TRPBF	LTC3337ERC#TRMPBF	LHMM	12-Lead (2mm × 2mm × 0.75mm) LFCSP	–40°C to 125°C
LTC3337ACBZ-R7	N/A	3337	16-Ball (1.64mm × 1.64mm) WLCSP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2). BAT_IN = BAT_OUT = AV_{CC} = DV_{CC} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range (BAT_IN)	(Note 4)	●	1.8		5.5	V
AV_{CC} Voltage Range		●	1.8		5.5	V
Coulomb Counter						
Input Current into BAT_IN	BAT_IN – BAT_OUT = 50mV			0		nA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 100mA I_{PEAK} Setting	 ●	90 85	100 100	110 115	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 75mA I_{PEAK} Setting	 ●	67.5 65	75 75	82.5 85	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 50mA I_{PEAK} Setting	 ●	45 43	50 50	55 57	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 25mA I_{PEAK} Setting	 ●	22.5 21.5	25 25	27.5 28.5	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 20mA I_{PEAK} Setting	 ●	18 17	20 20	22 23	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 15mA I_{PEAK} Setting	 ●	13.5 13	15 15	16.5 17	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 10mA I_{PEAK} Setting	 ●	9 8.5	10 10	11 11.5	mA mA
	BAT_IN – BAT_OUT = 175mV (Current Source Turned On), 5mA I_{PEAK} Setting	 ●	4.5 4.2	5 5	5.5 5.8	mA mA
	Start-Up: BAT_OUT= 0V, 25mA/50mA/75mA/100mA I_{PEAK} Settings			25		mA
	Start-Up: BAT_OUT= 0V, 5mA/10mA/15mA/20mA I_{PEAK} Settings			5		mA
AV_{CC} Pin Input Quiescent Current	BAT_IN – BAT_OUT = 50mV			100	160	nA
q_{LSB} (for Prescaler Setting M = 0) (Notes 5, 6)	100mA I_{PEAK} Setting	●	14.17	14.91	15.66	mA • hr
	75mA I_{PEAK} Setting			11.18		mA • hr
	50mA I_{PEAK} Setting			7.457		mA • hr
	25mA I_{PEAK} Setting			3.728		mA • hr
	20mA I_{PEAK} Setting			2.983		mA • hr
	15mA I_{PEAK} Setting			2.237		mA • hr
	10mA I_{PEAK} Setting			1.491		mA • hr
	5mA I_{PEAK} Setting			745.7		µA • hr
Full-Scale Coulomb Count (Battery Capacity)	5mA I_{PEAK} Setting, M = 15 (Smallest Battery)			1.491		mA • hr
	100mA I_{PEAK} Setting, M = 0 (Largest Battery)	●	928.5	977.3	1026	A • hr
Total Coulomb Counter Error (Note 6)	(Note 7)	 ●	–3 –5		3 5	% %
Coulomb Counter Turn-On Threshold	(BAT_IN – BAT_OUT), BAT_OUT Rising			0.6		V
Coulomb Counter Turn-Off Threshold	(BAT_IN – BAT_OUT), BAT_OUT Falling			1.2		V
BATOUT_OK Threshold	(BAT_IN – BAT_OUT), BAT_OUT Rising	●	85	110	140	mV
BATOUT_OK Threshold	(BAT_IN – BAT_OUT), BAT_OUT Falling	●	375	400	425	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2). BAT_IN = BAT_OUT = AV_{CC} = DV_{CC} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PEAK} Turn-Off Threshold (V_{OUT_HIGH})	(BAT_IN – BAT_OUT), BAT_OUT Rising	●	85	110	140	mV
I_{PEAK} Turn-On Threshold (V_{OUT_LOW})	(BAT_IN – BAT_OUT), BAT_OUT Falling	●	140	160	230	mV
BAT_OUT Hysteresis	$V_{HYST} = V_{OUT\_LOW} – V_{OUT\_HIGH}$	●	40			mV
Voltage Monitor						
V_{LSB}				1.465		mV
Total Voltage Error		 ●	–1.0 –2.5		1.0 2.5	% %
Full-Scale Voltage (111111111111 Code)				6		V
Zero Voltage (000000000000 Code)				0		V
Temperature Monitor						
T_{LSB}				0.784		°C
Code for Room Temperature 25°C			–5LSBs	01010101	+5LSBs	
Full-Scale Temperature (11111111 Code)				159		°C
Zero-Scale Temperature (00000000 Code)				–41		°C
Hot Die Temperature Warning Threshold (Die Temperature that Causes $\overline{IRQ}$ = 0)	00000000 Code for Register Bits H[15:8] 11111111 Code for Register Bits H[15:8] (Default)			–41 159		°C °C
Cold Die Temperature Warning Threshold (Die Temperature that Causes $\overline{IRQ}$ = 0)	00000000 Code for Register Bits H[7:0] (Default) 11111111 Code for Register Bits H[7:0]			–41 159		°C °C
Supercapacitor Balancer						
V_{SCAP} (BAT_OUT Pin)	Supercapacitor Balancer Input Range	●	2.5		5.5	V
I_{SCAP} (BAT_OUT Pin)	Supercapacitor Balancer Quiescent Current, BAT_OUT = 5V, I_{BAL} = 0			62	150	nA
Supercapacitor Balancer Max Source Current	BAT_OUT = 5.0V, BAL = 2.4V		10			mA
Supercapacitor Balancer Max Sink Current	BAT_OUT = 5.0V, BAL = 2.6V				–10	mA
Supercapacitor Balance Point (V_{BAL})	Percentage of BAT_OUT Voltage	●	49	50	51	%
Digital Inputs and Outputs						
DV_{CC} Voltage Range		●	1.8		5.5	V
Digital Input High Voltage (V_{IH})	For Pins IPK[2:0] For Pins SDA, SCL	●	BAT_IN – 0.5 70			V %DV_{CC}
Digital Input Low Voltage (V_{IL})	For Pins IPK[2:0] For Pins SDA, SCL	●			0.5 30	V %DV_{CC}
Digital Input High Current (I_{IH})	For Pins IPK[2:0] For Pins SDA, SCL				10 10	nA nA
Digital Input Low Current (I_{IL})	For Pins IPK[2:0] For Pins SDA, SCL				10 10	nA nA
Digital Output High Voltage (V_{OH})	For Pins $\overline{IRQ}$, BATOUT_OK; 1µA Out of Pin		DV_{CC} – 0.5			V
Digital Output Low Voltage (V_{OL})	For Pins $\overline{IRQ}$, BATOUT_OK; 1µA into Pin For Pin SDA; 3mA into Pin				0.5 0.4	V V
I^2C Timing Characteristics (See Figure 1)						
I^2C Read Address I^2C Write Address				11001001 11001000		
Clock Operating Frequency	f_{SCL}				400	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2). BAT_IN = BAT_OUT = AV_{CC} = DV_{CC} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bus Free Time Between STOP/START	t_{BUF}		1.3			µs
Repeated START Set-Up Time	$t_{SU,STA}$		600			ns
Hold Time (Repeated) START Condition	$t_{HD,STA}$		600			ns
Set-Up Time for STOP Condition	$t_{SU,STO}$		600			ns
Data Set-Up Time (Input)	$t_{SU,DAT}$		100			ns
Data Hold Time (Input)	$t_{HD,DATI}$		0			µs
Data Hold Time (Output)	$t_{HD,DATO}$		0		0.9	µs
Clock/Data Fall Time	t_f		20		300	ns
Clock/Data Rise Time	t_r		20		300	ns
Clock LOW Period	t_{LOW}		1.3			µs
Clock HIGH Period	t_{HIGH}		0.6			µs
Spike Suppression Time	t_{SP}				50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3337 is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$.

Note 4: Coulomb counter and peak current limit accuracy are at their best for BAT_IN voltages above 2V. Voltage and Temperature Monitor accuracy are at their best down to 1.8V. See Extended Battery Range Below 2V in the Operation section.

Note 5: The equivalent charge of an LSB in the accumulated charge register depends on the I_{PEAK} setting and the internal prescaling factor M. See Choosing the Coulomb Counter Prescaler M section for more information. Note that:

1mA • hr = 3.6A • s = 3.6C.

Note 6: The specified accuracy of q_{LSB} in percent is better than that of the corresponding I_{PEAK} because the timebase used for calculating coulombs is internally adjusted to compensate for errors in the actual I_{PEAK} value. The Total Coulomb Counter Error specified includes any inaccuracy in q_{LSB}.

Note 7: This parameter is production tested only for the 100mA I_{PEAK} setting. For the other I_{PEAK} settings it is guaranteed by extension due to the internal design architecture and operation.

TIMING DIAGRAM

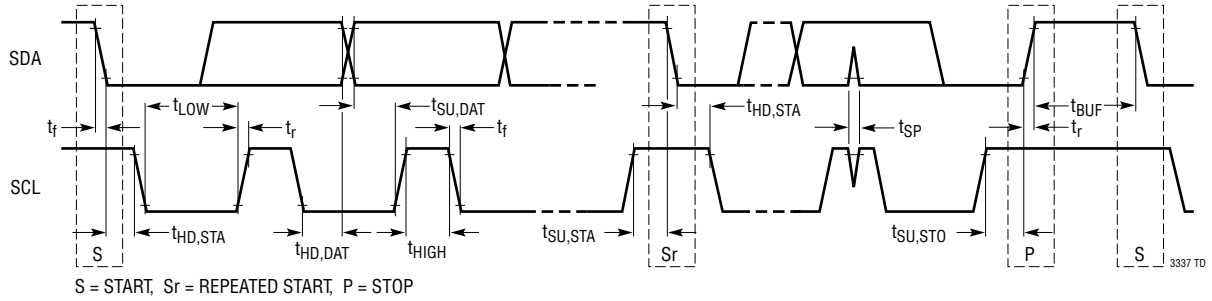
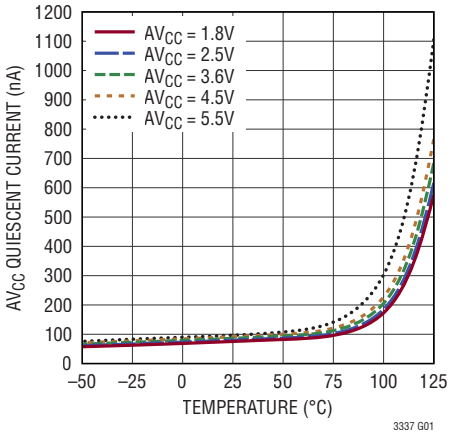


Figure 1. Definition of Timing on I^2C Bus

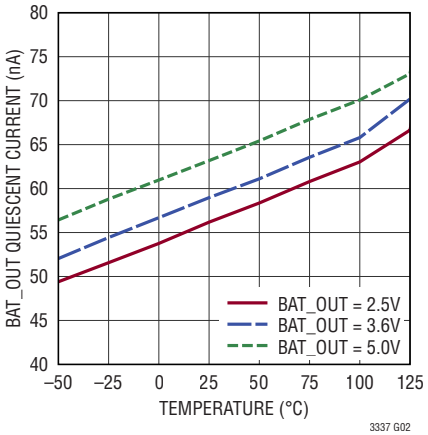
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, BAT_IN = BAT_OUT = AV_{CC} = DV_{CC} = 3.6V, 100mA I_{PEAK} unless otherwise noted.

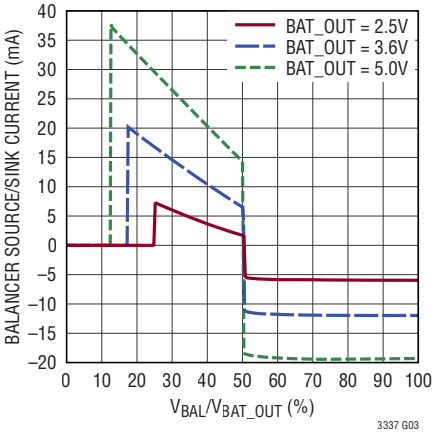
AV_{CC} Quiescent Current, Current Source is Off



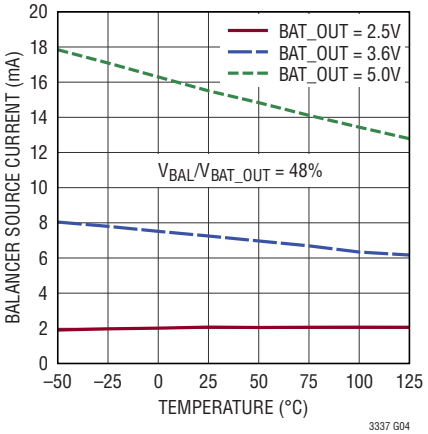
Supercapacitor Balancer Quiescent Current



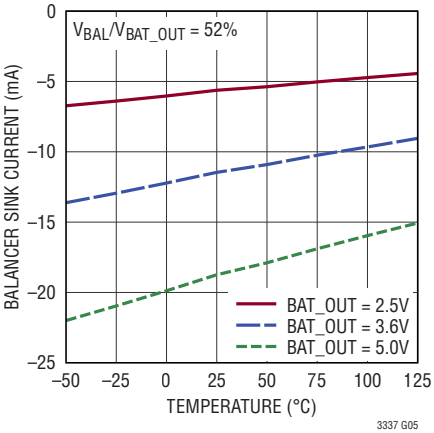
Supercapacitor Balancer Source/ Sink Current



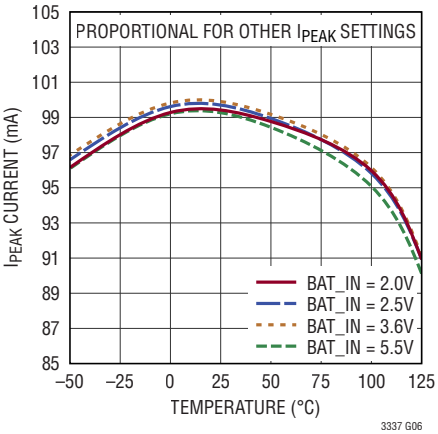
Supercapacitor Balancer Source Current



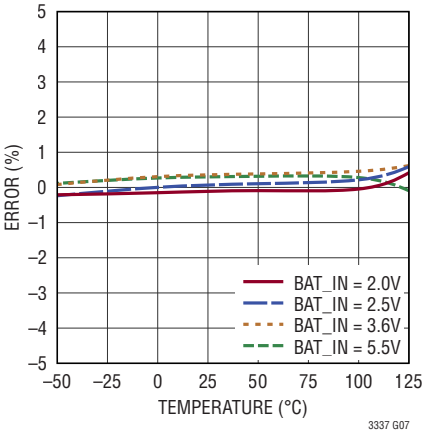
Supercapacitor Balancer Sink Current



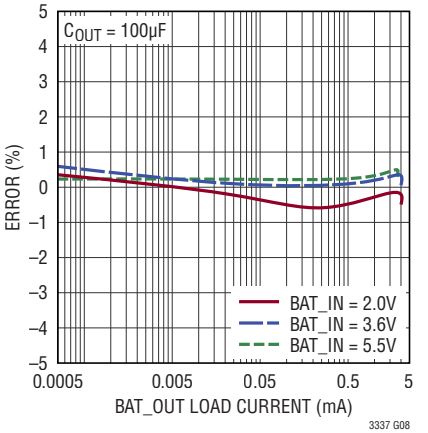
I_{PEAK} Current vs Temperature (100mA I_{PEAK} Setting)



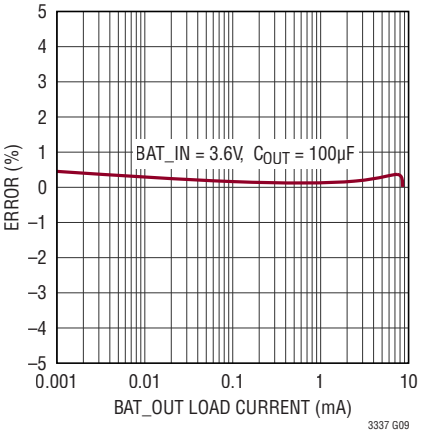
Coulomb Counter Error in Continuous Mode (100mA I_{PEAK} Setting)



Total Coulomb Counter Error (5mA I_{PEAK} Setting)



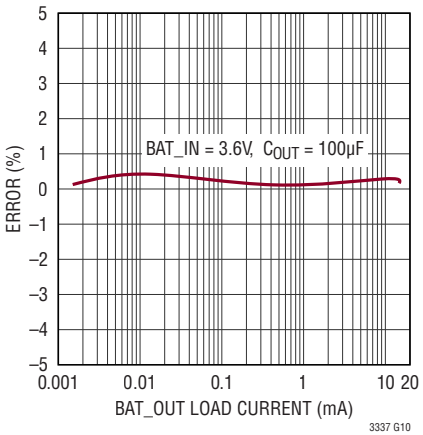
Total Coulomb Counter Error (10mA I_{PEAK} Setting)



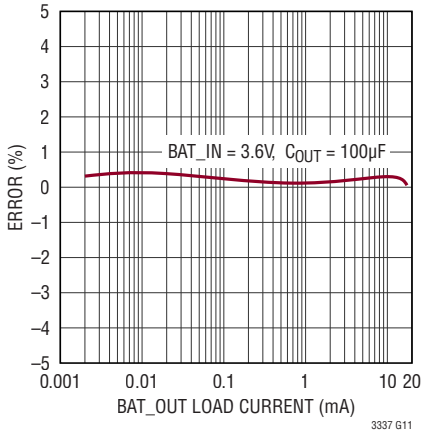
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, BAT_IN = BAT_OUT = AV_{CC} = DV_{CC} = 3.6V, 100mA I_{PEAK} unless otherwise noted.

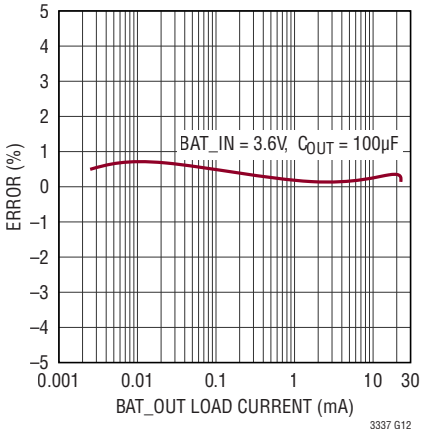
Total Coulomb Counter Error (15mA I_{PEAK} Setting)



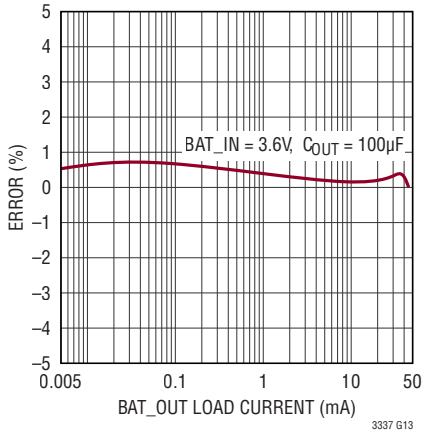
Total Coulomb Counter Error (20mA I_{PEAK} Setting)



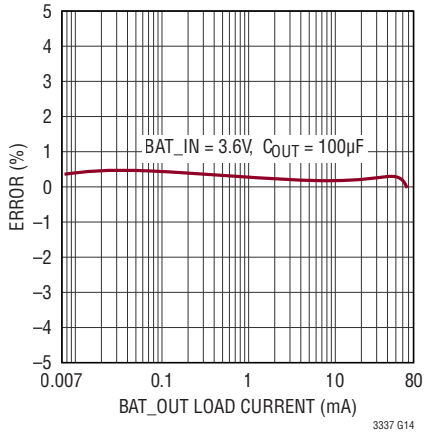
Total Coulomb Counter Error (25mA I_{PEAK} Setting)



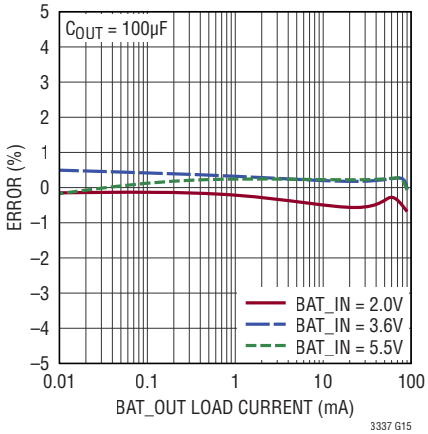
Total Coulomb Counter Error (50mA I_{PEAK} Setting)



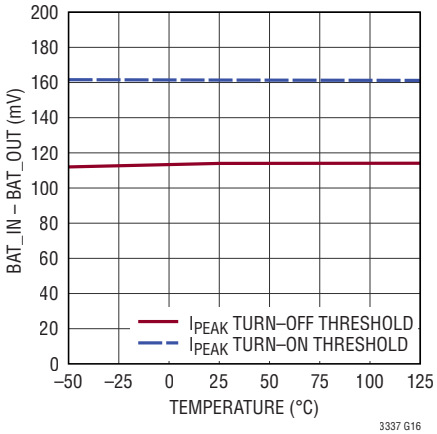
Total Coulomb Counter Error (75mA I_{PEAK} Setting)



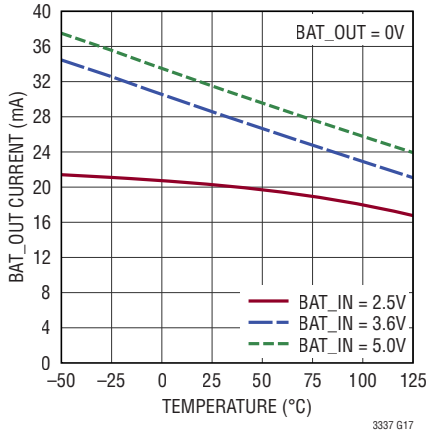
Total Coulomb Counter Error (100mA I_{PEAK} Setting)



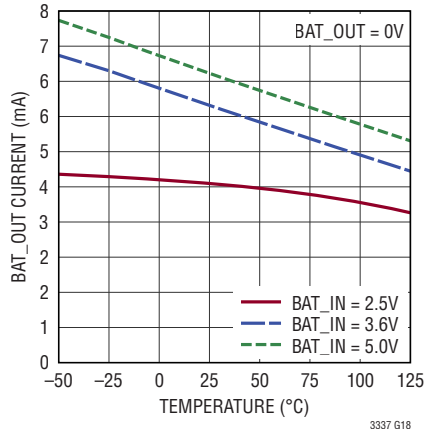
I_{PEAK} Turn–On/Off Thresholds



Start-Up Current Out of BAT_OUT Pin (I_{PK}[2] = 1 Settings)



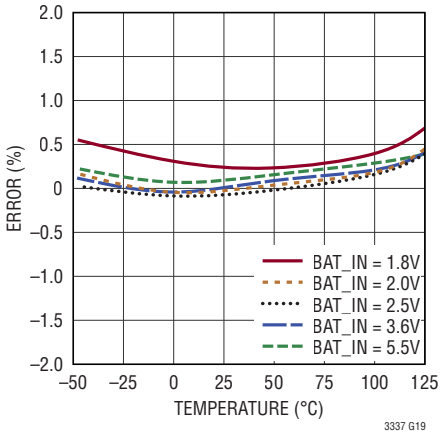
Start-Up Current Out of BAT_OUT Pin (I_{PK}[2] = 0 Settings)



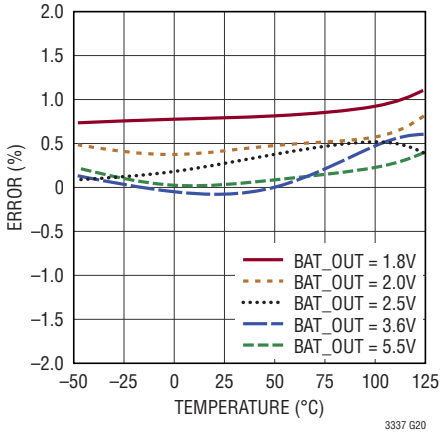
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, BAT_IN = BAT_OUT = AV_{CC} = DV_{CC} = 3.6V, 100mA I_{PEAK} unless otherwise noted.

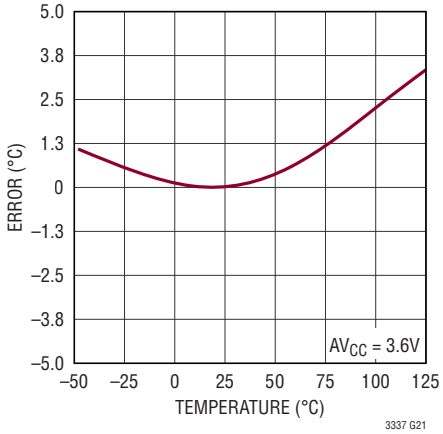
BAT_IN Voltage Error



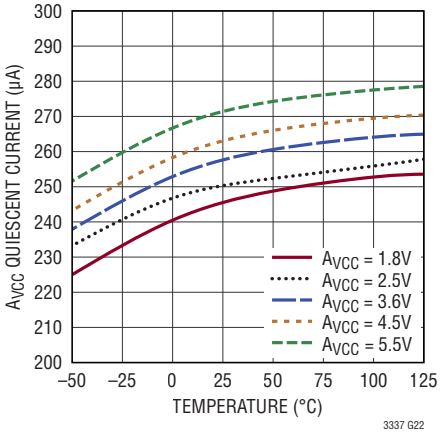
BAT_OUT Voltage Error



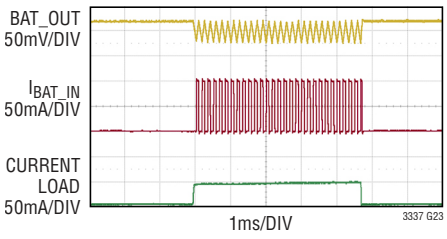
Temperature Sensor Error



AVCC Quiescent Current, Current Source is ON

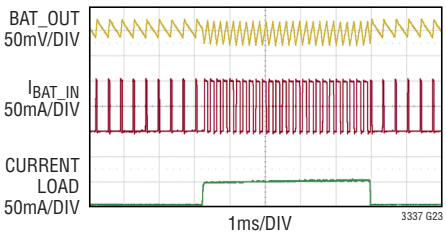


BAT_OUT Load Step Transient



C_{OUT} = 100µF
BAT_IN = 3.6V
LOAD STEP FROM 0mA TO 50mA

BAT_OUT Load Step Transient



C_{OUT} = 100µF
BAT_IN = 3.6V
LOAD STEP FROM 5mA TO 50mA

PIN FUNCTIONS (LFCSP/WLCSP)

BAL (Pin 1/Pin A1): Supercapacitor Balance Point. The common node of a stack of two supercapacitors (optional) connected to BAT_OUT. A source/sink balancing current of up to ±10mA is available. Tie BAL to GND to disable the balancer and its associated quiescent current.

AV_{CC} (Pin 2/Pin B1): Supply Rail for the Coulomb Counter and SOH Circuits. AV_{CC} is normally connected to BAT_OUT, but in some applications may connect to BAT_IN (see Applications Information section).

DV_{CC} (Pin 3/Pin C1): Supply Rail for the I^2C Serial Bus and for the $\overline{IRQ}$ and BATOUT_OK Outputs. DV_{CC} sets the reference level of the SDA and SCL pins for I^2C compliance.

The external I^2C pull-up resistors on SDA and SCL should connect to DV_{CC}. Depending on the application, DV_{CC} can be connected to AV_{CC} or to a separate external supply between 1.8V and 5.5V.

SCL (Pin 4/Pin D1): Serial Clock Input for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. Do not float.

SDA (Pin 5/Pin D2): Serial Data Input/Output for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. Do not float.

$\overline{IRQ}$ (Pin 6/Pin D3): Interrupt Output. Logic level output referenced to DV_{CC}. Active low. This pin is normally logic high but will transition low when either the coulomb counter alarm level or one of the temperature warning levels is reached.

BATOUT_OK (Pin 7/Pin D4): BATOUT_OK Comparator Output. Logic level output referenced to DV_{CC}. This pin is logic high when the BAT_OUT pin is high and in its normal operating range where the coulomb counter is operating properly.

IPK2 (Pin 8/Pin C4): Input Current Limit Select Bit (with IPK0 and IPK1). See IPK0. Do not float.

IPK1 (Pin 9/Pin B4): Input Current Limit Select Bit (with IPK0 and IPK2). See IPK0. Do not float.

IPK0 (Pin 10/Pin A4): Input Current Limit Select Bit (with IPK1 and IPK2). IPK0 should be tied to BAT_IN to select high or to GND to select low to program the desired I_{PEAK} (see Table 1 in the Operation section). Do not float.

BAT_IN (Pin 11/Pin A3): Battery Input Voltage. Connect the battery as close as possible to this pin.

BAT_OUT (Pin 12/Pin A2): Battery Output Voltage. Connect the load to this pin.

GND (Exposed Pad Pin 13/Pins B2, B3, C2, C3): Ground. The exposed pad (or center 4 WLCSP balls) must be soldered to the PCB.

BLOCK DIAGRAM

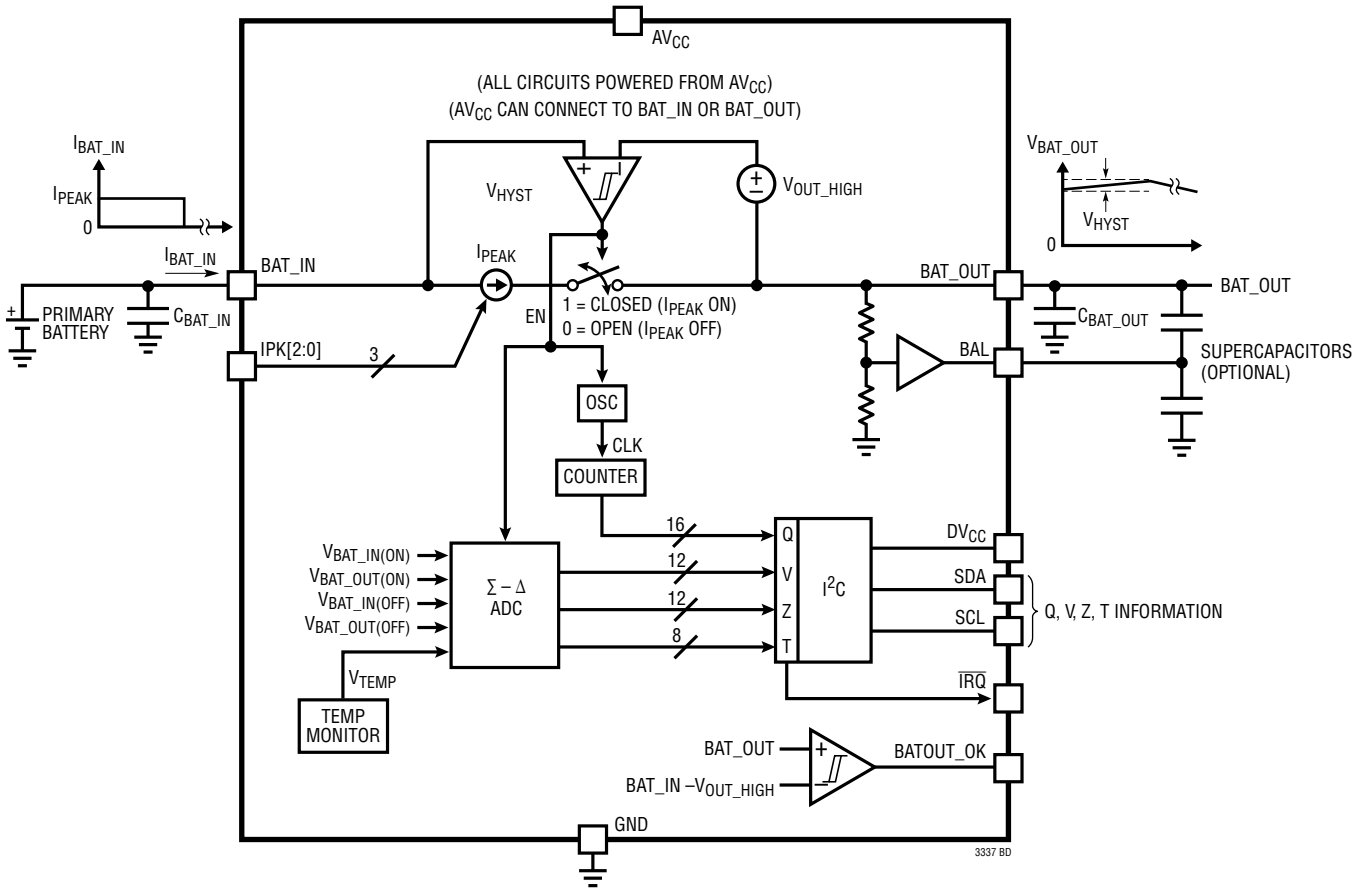


Figure 2. Block Diagram

OPERATION

Coulomb Counter (Q)

The LTC3337 integrates a precision coulomb counter which monitors the accumulated charge that is transferred from a primary battery connected to its BAT_IN pin to an output load connected to its BAT_OUT pin. I_{PEAK} is a low dropout current source between BAT_IN and BAT_OUT. The current source value can be set via the input current limit select pins IPK[2:0] (see Table 1).

Table 1. I_{PEAK} Selection

IPK2	IPK1	IPK0	I_{PEAK}
0	0	0	5mA
0	0	1	10mA
0	1	0	15mA
0	1	1	20mA
1	0	0	25mA
1	0	1	50mA
1	1	0	75mA
1	1	1	100mA

Referring to Figure 3, if BAT_OUT is less than BAT_IN – V_{OUT_LOW} (where V_{OUT_LOW} is nominally 160mV), the current source is turned on and charge is delivered from BAT_IN to BAT_OUT. After BAT_OUT charges up to BAT_IN – V_{OUT_HIGH} (where V_{OUT_HIGH} is nominally 110mV), the current source is turned off.

The capacitor connected between BAT_OUT and ground supports the load while the current source is off and should have a minimum value of 100µF for the 100mA I_{PEAK} setting. See Table 11 in the Applications Information section.

A hysteretic comparator senses both thresholds and controls the current source timing. The output of the comparator in one state represents the time (t_P) during which the battery is delivering a current equal to I_{PEAK}. This output enables an oscillator having a period T (500ns typical) which is used to increment a counter. The counter output bits represent a precise count of the battery coulombs. The last 2 bytes can be read via I^2C.

The amount of charge represented by the least significant bit (q_{LSB}) of the accumulated charge register is given in

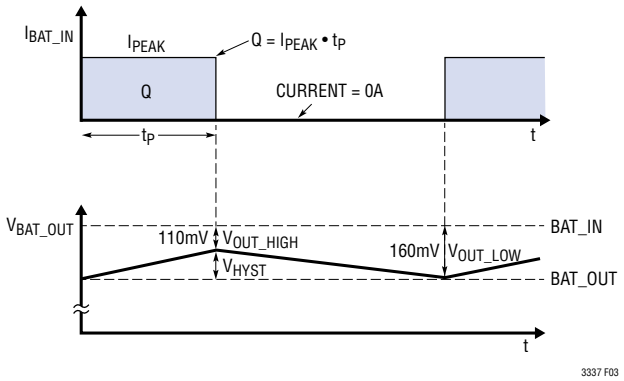


Figure 3. Coulomb Counter Operation

the Electrical Characteristics table for all 8 I_{PEAK} settings for the case of the default prescaler setting (M = 0). This default prescaler setting uses the full length of the internal counter. See Equation 1.

$$q_{LSB\ (M\ =\ 0)} = \frac{(2^{46} - 1) \bullet I_{PEAK} \bullet T}{65535} \quad (1)$$

Choosing the Coulomb Counter Prescaler M

To preserve adequate digital resolution for a wide range of battery capacities and I_{PEAK} current values, the LTC3337 includes a programmable prescaler. The user can set the prescaler value from 0 to 15 by writing bits A[3:0] (see Table 3). Note that the default value for the prescaler is 0.

To use the majority of the range of accumulated charge register B, the prescaler value (M) should be chosen for a given battery capacity Q_{BAT} based on Equation 2.

$$M = \log_2 \left(\frac{q_{LSB} \bullet 65535}{Q_{BAT}} \right) \quad (2)$$

where Q_{BAT} is the battery capacity and q_{LSB} is the typical value (for M = 0) from the Electrical Characteristics table for the selected I_{PEAK}. M must be an integer, so the result of Equation 2 must be rounded down to the nearest integer value. M has a maximum value of 15.

OPERATION

A smaller capacity battery will require a higher prescaler value M than a larger capacity battery for the same I_{PEAK}. Likewise, a lower I_{PEAK} will require a lower prescaler value M than a higher I_{PEAK} for the same capacity battery. The amount of charge represented by the least significant bit (q_{LSB_M}) of the accumulated charge register is given by Equation 3.

$$q_{LSB\_M} = \frac{q_{LSB}}{2^M} \quad (3)$$

where q_{LSB} is the typical (M = 0) value in the Electrical Characteristics table for the selected I_{PEAK}.

AV_{CC} Pin Connection

The AV_{CC} pin serves as the power supply for all internal LTC3337 circuits and can be connected to BAT_IN or to BAT_OUT. With AV_{CC} connected to BAT_OUT, the coulomb counter counts all coulombs coming out of the battery, including those associated with the LTC3337's own quiescent current, which effectively parallels the output load at BAT_OUT. When connecting AV_{CC} to BAT_IN, the LTC3337's own quiescent current represents an error on coulombs out of the battery. However, coulombs associated purely with the output load are now more accurately counted, and this may be beneficial in output power metering applications. In this second option a scaling factor of minus 1.6% needs to be applied to all coulomb counter measurements.

Battery Voltage (V) and Battery Impedance (Z) Monitors

The LTC3337 includes a 12-bit analog-to-digital converter (ADC), which is used to measure the battery voltage at the BAT_IN pin, the BAT_OUT pin voltage, and the LTC3337 die temperature.

The BAT_IN pin voltage is sampled when the coulomb counter is delivering a known I_{PEAK} pulse ($V_{BAT\_IN(ON)}$). The ADC converts this sampled value to a 12-bit value with an LSB = 1.465mV. The conversion time is typically 3.5ms. The BAT_IN voltage is then sampled a second time when the coulomb counter is delivering zero current, ($V_{BAT\_IN(OFF)}$). After a second conversion time, the last stored value is readable from register D (for $V_{BAT\_IN(ON)}$) and register E (for $V_{BAT\_IN(OFF)}$). See Table 2, Table 6, and Table 7.

The voltage measurement is performed only every 1024 on-cycles to minimize the AV_{CC} quiescent current.

Battery impedance can be calculated from the above two conversion values: $Z = (V_{BAT\_IN(OFF)} - V_{BAT\_IN(ON)})/I_{PEAK}$ based on the last stored values in registers D and E.

The BAT_OUT voltage is also sampled when the I_{PEAK} current source turns on ($V_{BAT\_OUT(ON)}$) and sampled a second time when the I_{PEAK} current source turns off ($V_{BAT\_OUT(OFF)}$). Again after two conversion times, the last stored values are readable from register F (for $V_{BAT\_OUT(ON)}$) and register G (for $V_{BAT\_OUT(OFF)}$). See Table 2, Table 8, and Table 9. Just like for the BAT_IN voltages these voltage measurements are performed only every 1024 on-cycles to minimize the AV_{CC} quiescent current.

Temperature Monitor (T)

The LTC3337 also measures its own die temperature and stores it in an 8-bit register. This temperature measurement is also taken only every 1024 on-cycles. The last stored value can be read from the 8MSBs in register C. See Table 2 and Table 5.

I^2C Interface

The 7-bit hard wired I^2C address of the LTC3337 is 1100100[R/$\overline{W}$]. The LTC3337 is a slave-only device meaning that the serial clock line (SCL) is only an input while the serial data line (SDA) is bidirectional.

Internal Registers

The LTC3337 has 8 internal sub-addressed I^2C registers, as shown in Table 2. Registers A and H are write-only registers, register B is read/write, and registers C, D, E, F, and G are read-only, as shown in Table 2 through Table 10.

OPERATION

Table 2. Register Map

SUB-ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	R/W	DEFAULT
01h	A	Prescaler Selection, Clear Interrupt, Coulomb Counter Shutdown, Gross Test and Coulomb Counter Alarm Threshold	W	FF00h
02h	B	Accumulated Charge, 16 Bits (Read), 8 Bits (Write)	R/W	0000h
03h	C	Status Register, Die Temperature	R	0000h
04h	D	BAT_IN Voltage when I_{PEAK} On	R	0000h
05h	E	BAT_IN Voltage when I_{PEAK} Off	R	0000h
06h	F	BAT_OUT Voltage when I_{PEAK} On	R	0000h
07h	G	BAT_OUT Voltage when I_{PEAK} Off	R	0000h
08h	H	Cold and Hot Die Temperature Alarms	W	00FFh

Table 3. Write Register A (Address 01h)

BIT	NAME	OPERATION	DEFAULT
A[3:0]	Prescaler Bits	Set Coulomb Counter Prescaling Factor M from 0 to 15	0000
A[4]	Clear_Int	Clear Interrupt (Alarm Reset)	0
A[5]	Counter Check	Counter Check Using $\overline{IRQ}$ Pin	0
A[6]	Coulomb Counter Shutdown	Extend Battery Range	0
A[7]	Set ADC Conversion when the Coulomb Counter is Turned Off	Start ADC Conversion of Battery Measurement and Temperature when A[6] = 1. This Bit Self-Resets when the ADC Measurements/Conversions are Finished	0
A[15:8]	Alarm Level	Coulomb Counter Alarm Level Threshold Calculated by the User Based on Battery Capacity and I_{PEAK} Current	FFh

Table 4. Read/Write Register B (Address 02h)

BIT	NAME	OPERATION	DEFAULT
B[15:0]	Accumulated Charge	Read Back 16MSBs of Counter Data, Only 8MSBs B[15:8] are Writable	0000h

Table 5. Read Register C (Address 03h)

BIT	NAME	OPERATION	DEFAULT
C[0]	Coulomb Counter Overflow	Coulomb Counter Operating Fault Due to an Improperly Chosen Prescaler Causing the Ripple Counter to Overflow	0
C[1]	Alarm Trip	Accumulator Register B Value Has Met or Exceeded the Alarm Threshold Set in Register A	0
C[2]	Alarm Minimum Die Temperature	The Die Temperature Has Reached the Min Die Temperature Set with Bits H[7:0]	0
C[3]	Alarm Maximum Die Temperature	The Die Temperature Has Reached the Max Die Temperature Set with Bits H[15:8]	0
C[4]	ADC Measurements Ready	Indicates when the ADC Measurements are Ready After a Read Request with Coulomb Counter Turned Off (Bit A[7] = 1 and Bit A[6] = 1) After this Bit is Read via I^2C, It Self-Resets	0
C[7:5]	Pin-Strapped IPK Pin	Read Back of IPK[2:0] Pins (Setting Latched at Start-Up)	000
C[15:8]	DIE_TEMP	Read Back 8MSBs of Die Temperature Measurement	00h

The die temperature DIE_TEMP can be calculated by using Equation 4.

$$DIE\_TEMP = T_{LSB} \bullet COUNT_C - 41°C \quad (4)$$

where T_{LSB} is the typical value in the Electrical Characteristics table and $COUNT_C$ is the 8MSBs of Register C.

Table 6. Read Register D (Address 04h)

BIT	NAME	OPERATION	DEFAULT
D[11:0]	$V_{BAT\_IN(ON)}$	Read Back BAT_IN Pin Voltage Measurement when I_{PEAK} Turns On	000000 000000
D[15:12]		Not Used	0000

The battery voltage $V_{BAT\_IN(ON)}$ can be obtained from the count in register D ($COUNT_D$) by using Equation 5.

$$V_{BAT\_IN(ON)} = V_{LSB} \bullet COUNT_D \quad (5)$$

where V_{LSB} is the typical value in the Electrical Characteristics table.

OPERATION

Table 7. Read Register E (Address 05h)

BIT	NAME	OPERATION	DEFAULT
E[11:0]	$V_{BAT\_IN(OFF)}$	Read Back BAT_IN Pin Voltage Measurement when I_{PEAK} Turns Off	000000 000000
E[15:12]		Not Used	0000

The battery voltage $V_{BAT\_IN(OFF)}$ can be obtained from the count in register E ($COUNT_E$) by using Equation 6.

$$V_{BAT\_IN(OFF)} = V_{LSB} \bullet COUNT_E \quad (6)$$

where V_{LSB} is the typical value in the Electrical Characteristics table.

Battery impedance can be calculated from the above two conversion values: $Z = (V_{BAT\_IN(OFF)} - V_{BAT\_IN(ON)})/I_{PEAK}$.

Table 8. Read Register F (Address 06h)

BIT	NAME	OPERATION	DEFAULT
F[11:0]	$V_{BAT\_OUT(ON)}$	Read Back BAT_OUT Pin Voltage Measurement when I_{PEAK} Turns On	000000 000000
F[15:12]		Not Used	0000

The BAT_OUT voltage $V_{BAT\_OUT(ON)}$ can be obtained from the count in register F ($COUNT_F$) by using Equation 7.

$$V_{BAT\_OUT(ON)} = V_{LSB} \bullet COUNT_F \quad (7)$$

where V_{LSB} is the typical value in the Electrical Characteristics table.

Table 9. Read Register G (Address 07h)

BIT	NAME	OPERATION	DEFAULT
G[11:0]	$V_{BAT\_OUT(OFF)}$	Read Back BAT_OUT Pin Voltage Measurement when I_{PEAK} Turns Off	000000 000000
G[15:12]		Not Used	0000

The BAT_OUT voltage $V_{BAT\_OUT(OFF)}$ can be obtained from the count in register G ($COUNT_G$) by using Equation 8.

$$V_{BAT\_OUT(OFF)} = V_{LSB} \bullet COUNT_G \quad (8)$$

where V_{LSB} is the typical value in the Electrical Characteristics table.

Table 10. Write Register H (Address 08h)

BIT	NAME	OPERATION	DEFAULT
H[7:0]	Cold Die Temperature Alarm Level	Minimum Temperature Threshold	00h
H[15:8]	Hot Die Temperature Alarm Level	Maximum Temperature Threshold	FFh

Counter Check Test

Setting bit A[5] = 1 allows the user to verify that the coulomb counter is operating correctly without having to wait for the accumulated charge register to increment from 0000h. In this mode the input clock of the ripple counter is output to the $\overline{IRQ}$ pin. The coulombs represented by each transition on the $\overline{IRQ}$ pin (time between two consecutive rising edges) is: $q_{LSB\_M}/2^{(24-M)}$, where q_{LSB} is given in the Electrical Characteristics table for each I_{PEAK} setting.

Alarms

Alarms cause the $\overline{IRQ}$ pin to be pulled low. The user can read register C to determine what caused the alarm. The alarm can then be cleared by writing a 1 to bit A[4]. The clear interrupt bit itself is self-clearing after action is taken on the $\overline{IRQ}$ pin.

If another alarm occurs while clearing a previous alarm, the $\overline{IRQ}$ pin will go high for 1µs (typical) before returning low again. At this time, the clear interrupt bit A[4] is also reset to zero.

There are 4 different fault/alarm conditions:

1. A coulomb counter overflow (C[0] is high) due to an improperly chosen prescaler (M) value causing the ripple counter to overflow. After the alarm is cleared the $\overline{IRQ}$ pin is released for 1µs and later pulled low again unless register C is overwritten with a lower value.
2. The preset alarm level is reached (C[1] is high) when the 8MSBs of the ripple counter are equal to or higher than the 8MSBs in register A (Coulomb Counter Alarm Threshold). The user should increase the alarm threshold in A[15:8] bits and write bit A[4] to 1 to

OPERATION

clear the alarm. The alarm threshold is only checked when the LSB of the accumulator register changes or when a write to register B or register A is done via I^2C. Therefore, if bit A[4] is set to 1 to clear an alarm interrupt without also changing the contents of register A and/or B, and this occurs during a long I_{PEAK} source off time, the $\overline{IRQ}$ pin is cleared and will not go back high again until the LSB bit of register B again changes. This could require several I_{PEAK} cycles.

3. The cold threshold of the die temperature alarm is reached (C[2] is high) due to the measured die temperature in C[15:8] being equal to or lower than the cold temperature threshold set in register H.
4. The hot threshold of the die temperature alarm is reached (C[3] is high) due to the measured die temperature in C[15:8] being equal to or higher than the hot temperature threshold set in register H.

Extended Battery Range Below 2V

When the coulomb counter is operating, the BAT_OUT voltage is lower than the BAT_IN voltage by a controlled amount (typically 110mV to 160mV). The coulomb counter works properly for BAT_IN voltages down to 2V and for BAT_OUT voltages down to 1.8V. The BAT_IN range can be somewhat extended down below 2.0V by setting bit A[6] = 1. This action disables the coulomb counter and the peak current limit I_{PEAK} and creates a low impedance connection between BAT_IN and BAT_OUT.

Because the current limit circuitry is disabled in this mode, care must be taken not to exceed the absolute maximum current rating of the BAT_OUT pin. Although this mode can be entered at any BAT_IN voltage, it is really only intended (and recommended) for “last gasp” end-of-life 2V and below operation.

The temperature monitor and the BAT_IN voltage monitor are still functional down to 1.8V on BAT_IN. These values can still be read on request by issuing a read command via I^2C.

Supercapacitor Balancer (Optional)

An integrated supercapacitor balancer with 62nA of quiescent current from the BAT_OUT pin is available to balance a stack of two supercapacitors at the BAT_OUT pin. The BAL pin is tied to the middle of the stack and can source or sink 10mA to regulate the BAL pin’s voltage to half that of the BAT_OUT pin’s voltage. To disable the balancer and its associated quiescent current, tie the BAL pin to ground.

Advantages of Supercapacitors

Supercapacitors are used in many power-management applications requiring many rapid charge/discharge cycles for short term power needs. Supercapacitors have many advantages. For instance, they maintain a long cycle lifetime and thanks to their low equivalent series resistance, supercapacitors provide high power density and high load currents to achieve almost instant charge in seconds.

One disadvantage of supercapacitors is their low energy density. Thus, they can not be used as a continuous power source. Also, the maximum voltage of a single cell is typically only 2.7V. If higher voltage is needed, a second cell must be connected in series.

APPLICATIONS INFORMATION

BAT_OUT Capacitor Selection

A minimum value of capacitance (C_{OUT}) is required between BAT_OUT and ground. This capacitor determines the I_{PEAK} pulse on and off durations. Its value should be selected based on the maximum current load at the BAT_OUT pin and the I_{PEAK} setting. For best coulomb counter accuracy, it is recommended to have 50µs minimum I_{PEAK} on/off durations (see Equation 9).

$$I_{PEAK\_ON}\ \text{time(min)} = \frac{C_{OUT} \bullet V_{HYST}}{I_{PEAK}} \qquad (9)$$

$$I_{PEAK\_OFF}\ \text{time(min)} = \frac{C_{OUT} \bullet V_{HYST}}{I_{LOAD(MAX)}}$$

where V_{HYST} is the voltage ripple value between V_{OUT_HIGH} and V_{OUT_LOW}. See Figure 3. The hysteresis is nominally set to 50mV.

For the 100mA I_{PEAK} setting and a maximum load current of 100mA, a 100µF C_{OUT} capacitor is recommended. See Table 11 for recommended C_{OUT} values for the other I_{PEAK} settings.

Table 11. Recommended Minimum C_{OUT} Values for Each I_{PEAK} Selection

IPK2	IPK1	IPK0	I_{PEAK}	RECOMMENDED C_{OUT}
0	0	0	5mA	4.7µF
0	0	1	10mA	10µF
0	1	0	15mA	15µF
0	1	1	20mA	22µF
1	0	0	25mA	33µF
1	0	1	50mA	47µF
1	1	0	75mA	82µF
1	1	1	100mA	100µF

The V_{OUT_HIGH} and V_{OUT_LOW} thresholds are DC levels. The actual AC values seen in application will be outside of these levels due to finite delay in the hysteretic comparator.

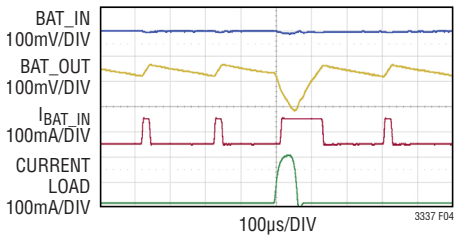
Battery ESR and Voltage Ripple

The ripple voltage between BAT_IN and BAT_OUT is also affected by the battery ESR value. For maximum coulomb counter accuracy, it is recommended to choose a battery such that ESR • I_{PEAK} is much smaller than the hysteresis. ESR • I_{PEAK} larger than the hysteresis generates very short I_{PEAK} pulses. If the duration is shorter than typically 3µs the ADC cannot correctly measure the BAT_IN and BAT_OUT voltages. An alternative is to increase the BAT_IN capacitor to a minimum of 10µF. The input capacitor helps in increasing the I_{PEAK} pulse duration. If the BAT_IN capacitor is too big the battery impedance measurement accuracy will suffer because it slows down BAT_IN voltage movement when I_{PEAK} turns on/off.

Maximum Load at BAT_OUT

The maximum continuous load at BAT_OUT cannot exceed I_{PEAK} or the output will lose regulation. The maximum instantaneous load, however, can exceed I_{PEAK} for short durations, provided that the overall average load does not. During the “bursts”, extra current is provided by the BAT_OUT capacitor and the BAT_OUT voltage discharges slightly. The length of the burst and the amount of acceptable BAT_OUT voltage droop will determine the required size of the BAT_OUT capacitor.

For low voltage (BAT_IN~2V) operation with bit A[6]=1, the maximum load is no longer limited by IPEAK, but rather by the absolute maximum rating of the BAT_OUT pin itself.



C_{OUT} = 100µF
BAT_IN = 3.6V
LOAD STEP FROM 10mA TO 200mA

Figure 4. BAT_OUT Load Step Transient with High Instantaneous Current

APPLICATIONS INFORMATION

I²C Interface

The LTC3337 communicates with a bus master using the standard I²C 2-wire serial interface. The Timing Diagram (Figure 1) shows the relationship of the signals on the bus.

The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors are required on these lines. The I²C control signals, SDA and SCL, are referenced internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the bus pull-up resistors.

DV_{CC} can be connected to AV_{CC} or to a separate external supply between 1.8V and 5.5V.

Bus Speed

The I²C port is designed to operate at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches.

START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high. The master may transmit either the slave write address or the slave read address. Once data is written to the LTC3337, the master may transmit a STOP condition which commands the LTC3337 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from low to high while SCL is high.

Byte Format

Each frame sent to or received from the LTC3337 must be eight bits long. The most significant bit (MSB) must be sent first. The eight bits are followed by an extra clock cycle for the acknowledge bit. The read or written data is always 2 bytes. The least significant byte is sent before the most significant byte.

Master and Slave Transmitters and Receivers

Devices connected to an I²C bus may be classified as either master or slave. A typical bus is composed of one or more master devices and several slave devices.

Some devices can act as either a master or a slave, but they may not change roles while a transaction is in progress.

The transmitter/receiver relationship is distinct from that of master and slave. The transmitter is responsible for control of the SDA line during the eight-bit data portion of each frame. The receiver is responsible for control of the SDA line during the ninth and final acknowledge clock cycle of each frame.

All transactions are initiated by the master with a START or repeat START condition. The master controls the active (falling) edge of each clock pulse on SCL, regardless of its status as transmitter or receiver. The slave device never brings SCL low.

The LTC3337 does not clock stretch and will never hold SCL low under any circumstance.

The master device begins each I²C transaction as the transmitter and the slave device begins each transaction as the receiver. For bus write operations, the master acts as the transmitter and the slave acts as receiver for the duration of the transaction. For bus read operations, the master and slave exchange transmit/receive roles following the address frame for the remainder of the transaction.

Acknowledge

The acknowledge signal (ACK) is used for handshaking between the transmitter and receiver. When the LTC3337 is written to, it acknowledges its write address as well as the subsequent data bytes as a slave receiver. When it is read from, the LTC3337 acknowledges its read address as a slave receiver. The LTC3337 then changes to a slave transmitter and the master receiver may optionally acknowledge receipt of the following data byte from the LTC3337.

APPLICATIONS INFORMATION

The acknowledge related clock pulse is always generated by the bus master. The transmitter (master or slave) releases the SDA line (high) during the acknowledge clock cycle.

The receiver (slave or master) pulls down the SDA line during the acknowledge clock pulse so that it is a stable low during the high period of this clock pulse.

When the LTC3337 is read from, it releases the SDA line after the eighth data bit so that the master may acknowledge receipt of the data. The I^2C specification calls for a not acknowledge (NACK) by the master receiver following the last data byte during a read transaction. Upon receipt of the NACK, the slave transmitter is instructed to release control of the bus. Because the LTC3337 transmits two bytes of data under all circumstances, a master acknowledging or not acknowledging the data sent by the LTC3337 has no consequence. The LTC3337 will release the bus after 2 bytes in either case.

Slave Address

The LTC3337 responds to a 7-bit address which has been factory programmed to 1100100[R/$\overline{W}$]. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC3337, and 1 when reading data from it. Considering the address an 8-bit word, then the write address is 0xC8, and the read address is 0xC9.

The LTC3337 will acknowledge both its read and write addresses.

Sub-Addressed Access

The LTC3337 has five read registers, two write registers and one read/write register. They are accessed by the I^2C port via a sub-addressed pointer system where each sub-address value points to one of the eight registers within the LTC3337. See Table 2 for sub-address information.

The sub-address pointer is always the first byte written immediately following the LTC3337 write address during bus write operations. The sub-address pointer value persists after the bus write operation and will determine which data byte is returned by the LTC3337 during any subsequent bus read operations. See Figure 5.

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
S: START CONDITION
P: STOP CONDITION
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)

											LSBYTE		MSBYTE		
S	ADDRESS	$\overline{W}$	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P	
	1100100	0	0	02h	0		1100100	1	0	80h	0	01h	1		

EXAMPLE: READ REGISTER B (SUB-ADDR 02h) → DATA READ: 0180h → 00000001 10000000

						LSBYTE		MSBYTE		
S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	DATA	A	P
	1100100	0	0	01h	0	F0h	0	01h	0	

EXAMPLE: WRITE REGISTER A (SUB-ADDR 01h) → DATA WRITTEN: 01F0h → 00000001 11110000

3337 F05

Figure 5. I^2C Reading and Writing Protocol

Bus Write Operation

The bus master initiates communication with the LTC3337 with a START condition and the LTC3337's write address.

If the address matches that of the LTC3337, the LTC3337 returns an acknowledge. The bus master should then deliver the sub-address. The sub-address value is transferred to a special pointer register within the LTC3337 upon the return of the sub-address acknowledge bit by the LTC3337.

If the master wishes to continue the write transaction, it may then deliver the 2 data bytes. The data bytes are transferred to an internal pending data register at the location of the sub-address pointer when the LTC3337 acknowledges both data bytes. The acknowledge bit is sent at the end of each byte. The LTC3337 is then ready to receive a new sub-address, optionally repeating the [SUB-ADDRESS] [DATA-byte1] [DATA-byte2] cycle indefinitely. The master may terminate communication with the LTC3337 with either a repeat START or a STOP condition. If a repeat START condition is initiated by the master, the LTC3337, or any other chip on the I^2C bus, can then be addressed.

The LTC3337 will remember, but not act on, the last input of valid data that it received at each sub-address location.

APPLICATIONS INFORMATION

This cycle can also continue indefinitely. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC3337 will immediately update all of its command registers with the most recent pending data that it had previously received.

Bus Read Operation

Only one sub-addressed data register is accessible during each bus read operation. The data returned by the LTC3337 is from the data register pointed to by the contents of the sub-address pointer register. The pointer register contents are determined by the previous bus write operation. In preparation for a bus read operation, it may be advantageous for a bus master to prematurely terminate a write transaction with a STOP or repeat START condition. The last transmitted byte then represents a pointer to the register of interest for the subsequent bus read operation.

The bus master reads status data from the LTC3337 with a START or repeat START condition followed by the LTC3337 read address. If the read address matches that of the LTC3337, the LTC3337 returns an acknowledge.

Following the acknowledgment of its read address, the LTC3337 returns one bit of status information for each of the next eight clock cycles from the register selected by the sub-address pointer (LSB first data byte). The SDA line stays high for 1-clock cycle after the first 8 bits and after LTC3337 returns the second data byte (MSB). Additional clock cycles from the master after the 2 data bytes have been read will leave the SDA line high. The LTC3337 will never acknowledge any bytes during a bus read operation except for its read address.

To read a different register, a write transaction must be initiated with a START or repeat START followed by the LTC3337 write address and sub-address pointer byte before the read transaction may be repeated.

When the contents of the sub-address pointer register point to write-only registers (A, H), the data returned in a bus read operation is the pending command data at that location if it had been modified since the last STOP condition. After a STOP condition, all pending data is copied to the command registers for immediate effect.

When the contents of the sub-address pointer register point to the writable and readable register B, the data returned in a bus read operation is data at that location, not the pending command data from the previous write operation. After a STOP condition, all pending data is copied to the command registers for immediate effect and a subsequent read operation can read the effect.

When the contents of the sub-address pointer register point to the read-only registers (C, D, E, F, G), the data returned is a snapshot of the state of the LTC3337 at a particular instant in time. If no interrupt requests are pending, the status data is sampled when the LTC3337 acknowledges its read address, just before the LTC3337 begins data transmission during a bus read operation. If the read address is acknowledged during an ADC conversion or I_{PEAK} pulse the status data reported is the one from the previous ADC conversion or end of the last I_{PEAK} pulse.

When an alarm/fault occurs, the $\overline{IRQ}$ pin is driven low and data is latched in bits C[3:0] of status register C at that moment. Any subsequent read operation from register C will return these frozen C[3:0] bits to facilitate determination of the cause of the interrupt request.

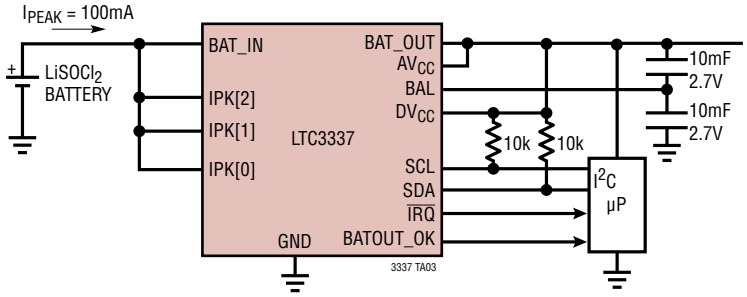
After the bus master clears the LTC3337 interrupt request, bits C[3:0] of the status latches are cleared. Bus read operations will then again return either a snapshot of the data at the time of the read address acknowledge, after an ADC conversion, after the I_{PEAK} pulse, or at the time of the next interrupt assertion, whichever comes first.

PC Board Layout

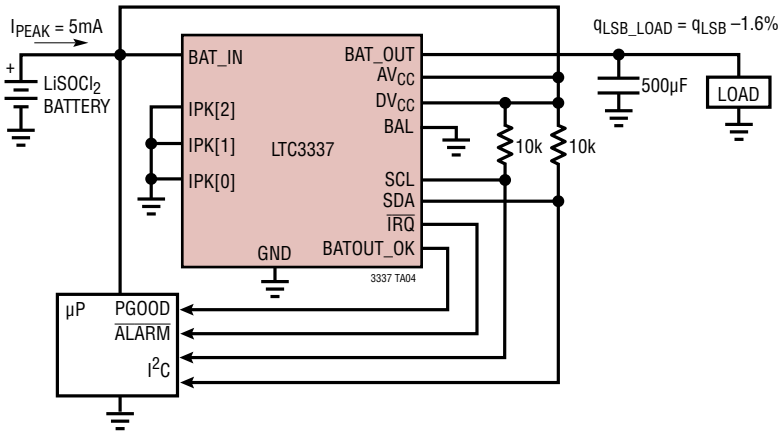
Despite its ultralow current operation, all high impedance nodes of the LTC3337 are inside the IC, and therefore, no special layout is needed. The positive terminals of the input and output capacitors should be connected as close as possible to the BAT_IN and BAT_OUT pins, respectively, and the negative terminals as close as possible to the GND pin.

TYPICAL APPLICATIONS

Microprocessor Application with High Load Peak Current and Supercapacitor

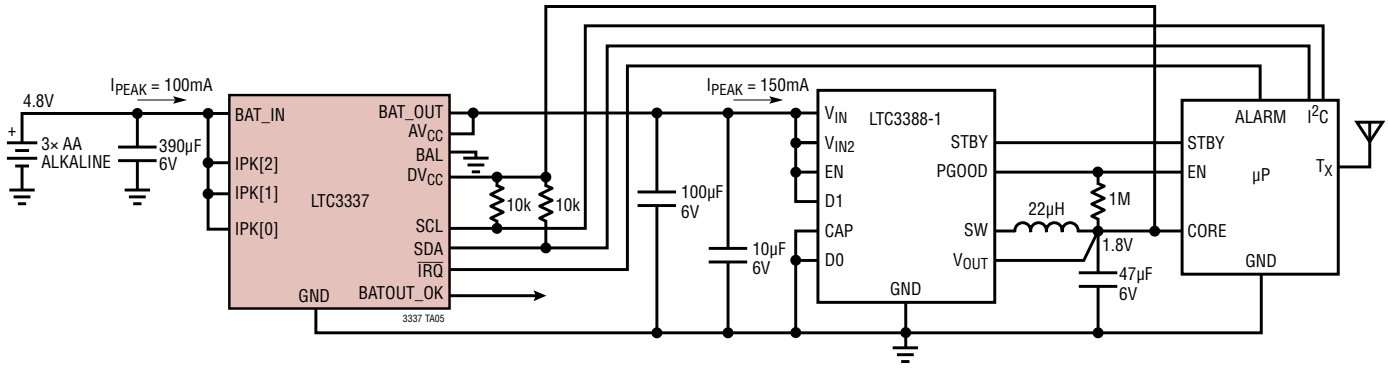


Output Power Metering Application

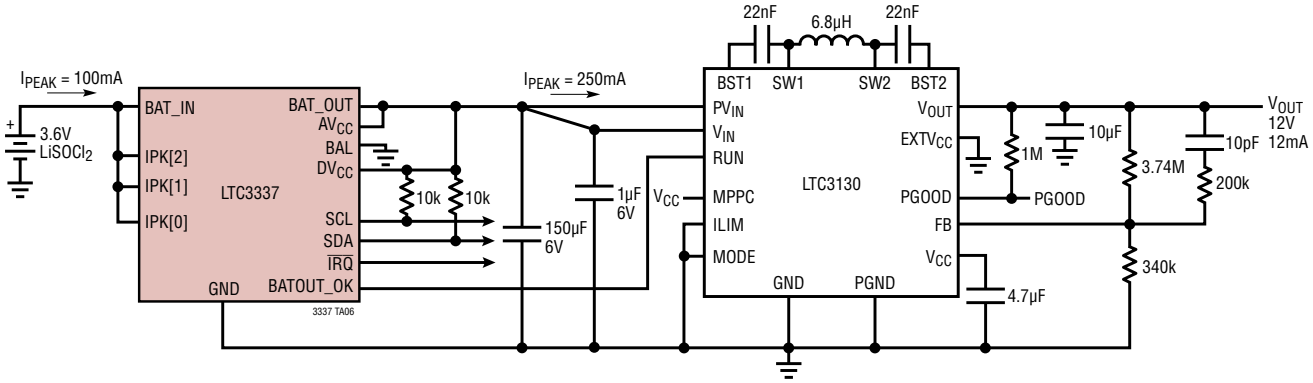


TYPICAL APPLICATIONS

Battery with High ESR Powering a Step-Down Converter and a Microprocessor with a Wireless Transmitter, All Coulombs Counted

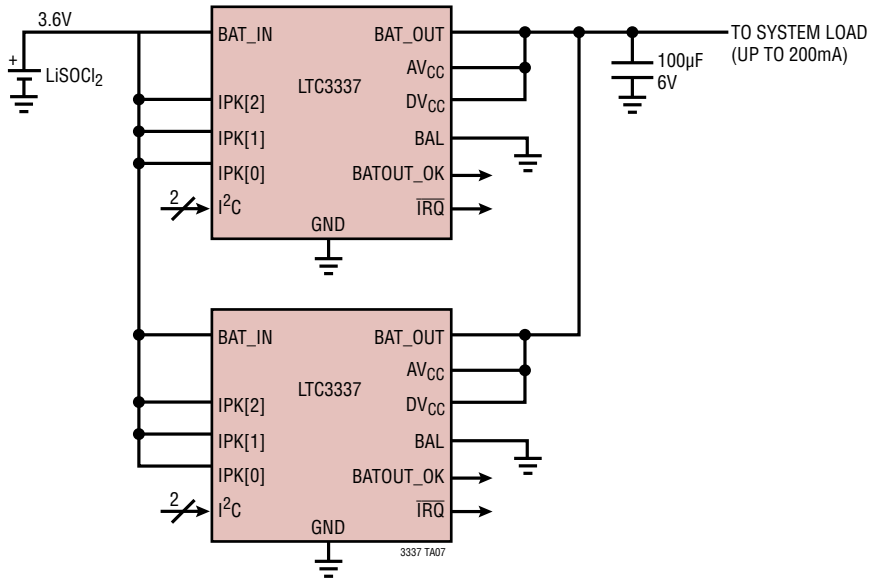


Primary Battery SOH Monitor with 12V Converter



TYPICAL APPLICATIONS

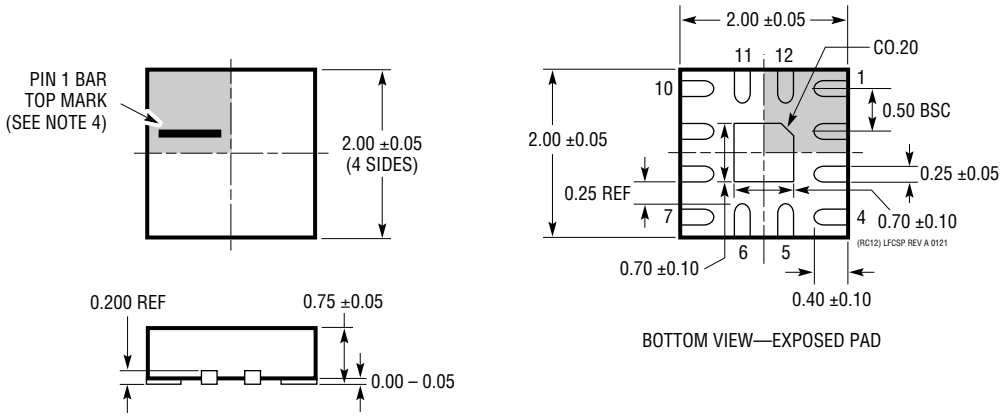
Paralleling Two LTC3337s for Higher Current Loads



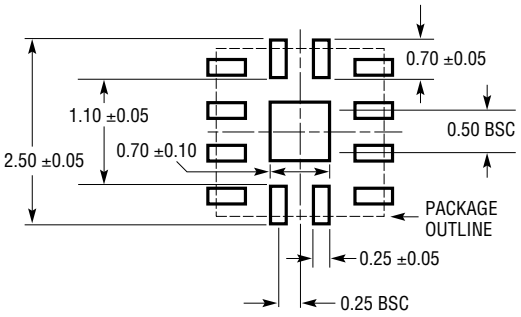
NOTE: SINCE THE TWO LTC3337 HAVE THE SAME I^2C ADDRESS, EXTERNAL CHIP SELECT LOGIC MUST BE IMPLEMENTED TO INDIVIDUALLY ADDRESS THEM.

PACKAGE DESCRIPTION

RC Package
12-Lead Plastic LFCSP (2mm × 2mm)
(Reference LTC DWG # 05-08-1784 Rev A)



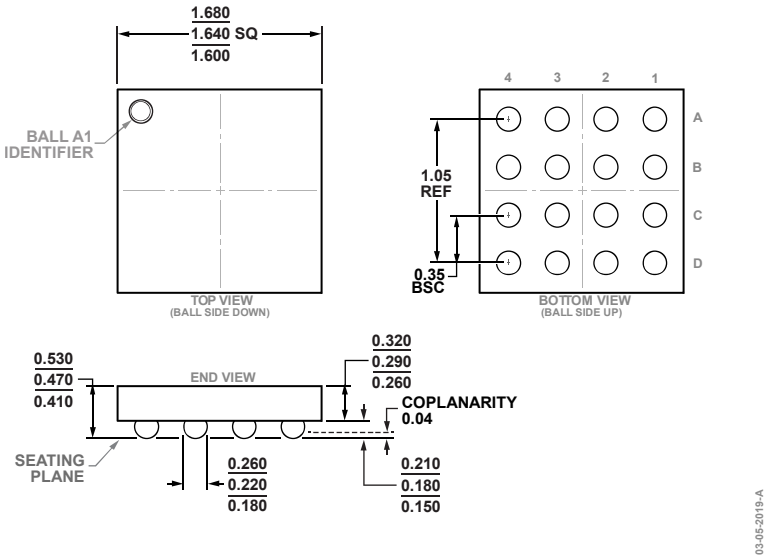
NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

PACKAGE DESCRIPTION

16-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-16-20)
Dimensions Shown in Millimeters

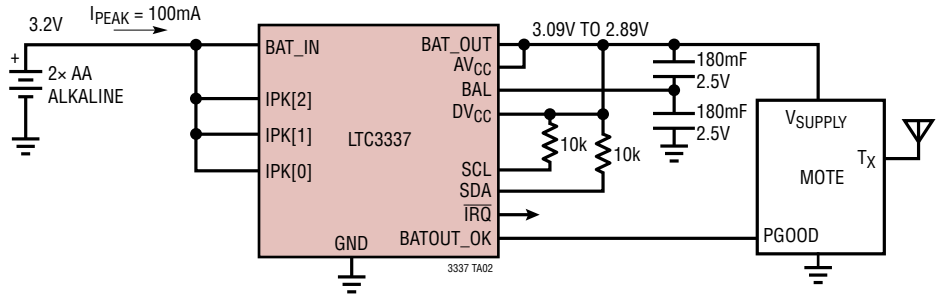


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/22	Added WLCSP package and references.	1–26
		Revised BAT Threshold spec.	3
		Revised I_{PEAK} Turn-Off Threshold spec.	4

TYPICAL APPLICATIONS

SmartMesh Mote with Supercapacitors for Wireless Mesh Networks



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2941	Battery Gas Gauge with I²C Interface	2.7V to 5.5V Operation; High Side R_{SENSE}; ±50mV Sense Voltage Range; 1% Charge Accuracy
LTC2941-1	1A I²C Battery Gas Gauge with Internal Sense Resistor	2.7V to 5.5V Operation; Integrated 50mΩ High Side R_{SENSE}; ±1A Sense Current Range; 1% Charge Accuracy
LTC2942	Battery Gas Gauge with Temperature, Voltage Measurement	14-Bit ΔΣ–ADC; Pin Compatible with LTC2941
LTC2942-1	1A Battery Gas Gauge with Internal Sense Resistor and Temperature/Voltage Measurement	14-Bit ΔΣ–ADC; Pin Compatible with LTC2941-1
LTC2943	Multicell Battery Gas Gauge with Temperature, Voltage, and Current Measurement	3.6V to 20V Operation; High Side R_{SENSE}; ±50mV Sense Voltage Range; 14-Bit ΔΣ–ADC; 1% Voltage, Current, and Charge Accuracy
LTC3129/ LTC3129-1	Micropower 200mA Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.42V to 15V, V_{OUT}: 1.4V to 15V, I_Q = 1.3μA, I_{SD} = 10nA, MSOP-16E, 3mm × 3mm QFN-16 Packages
LTC3130	25V, 600mA Buck-Boost DC/DC Converter with 1.6μA Quiescent Current	V_{IN}: 2.4V to 25V, V_{OUT}: 1V to 25V, I_Q = 1.2μA, I_{SD} = 500nA, 20-Lead 3mm × 4mm QFN and 16-Lead MSOP Packages
LTC3330	Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender	V_{IN}: 2.7V to 20V, BAT: 1.8V to 5.5V, 750nA I_Q 5mm × 5mm QFN-32 Package
LTC3331	Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Charger	V_{IN}: 2.7V to 20V, BAT Float: 3.45V/4V/4.1V/4.2V, 950nA I_Q 5mm × 5mm QFN-32 Package
LTC3335	Nanopower Buck-Boost DC/DC with Integrated Coulomb Counter	V_{IN}: 1.8V to 5.5V; 680nA I_Q, 3mm × 4mm QFN-20 Package
LTC3388-1/ LTC3388-3	20V, 50mA High Efficiency Nanopower Step-Down Regulator	V_{IN}: 2.7V to 20V, V_{OUT}: Fixed 1.1V to 5.5V, I_Q = 720nA, I_{SD} = 400nA, MSOP-10, 3mm × 3mm DFN-10 Packages
LTC3588-1/ LTC3588-2	Nanopower Energy Harvesting Power Supply with Up to 100mA of Output Current	V_{IN}: 2.7V to 20V, V_{OUT}: Fixed 1.8V to 5V, I_Q = 950nA, I_{SD} = 450nA, MSOP-10, 3mm × 3mm DFN-10 Packages
LTC4150	Coulomb Counter/Battery Gas Gauge	2.7V to 8.5V Operation; High Side R_{SENSE}; ±50mV Sense Voltage Range

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