

# Dual Synchronous 1.5A/1A 4MHz Step-Down DC/DC Regulator with POR

## FEATURES

- High Efficiency: Up to 95%
- 1.5A/1A Guaranteed Minimum Output Current
- Synchronizable to External Clock
- Power-On-Reset Output
- No Schottky Diodes Required
- Programmable Frequency Operation: 1.5MHz or Adjustable From 0.6MHz to 4MHz
- Low Ripple (< 35mV<sub>P-P</sub>) BurstMode® Operation
- Low R<sub>DS(ON)</sub> Internal Switches
- Short-Circuit Protected
- V<sub>IN</sub>: 2.25V to 5.5V
- Current Mode Operation for Excellent Line and Load Transient Response
- 125µA Quiescent Current in Sleep Mode
- Ultralow Shutdown Current: I<sub>Q</sub> < 1µA
- Low Dropout Operation: 100% Duty Cycle
- Phase Pin Selects 2nd Channel Phase Relationship with Respect to 1st Channel
- Internal Soft-Start with Individual Run Pin Control
- Available in Small Thermally Enhanced (3mm × 5mm) DFN and 20-Lead TSSOP Packages

## APPLICATIONS

- GPS/Navigation Systems
- Automotive Instrumentation
- PC Cards
- Industrial Power Supplies
- General Purpose Point of Load DC/DC

## DESCRIPTION

The LTC®3417A-1 is a dual constant frequency, synchronous step-down DC/DC converter. Intended for medium power applications, it operates from a 2.25V to 5.5V input voltage range and has a constant programmable switching frequency, allowing the use of tiny, low cost capacitors and inductors 2mm or less in height. Each output voltage is adjustable from 0.8V to 5V. Internal synchronous, low R<sub>DS(ON)</sub> power switches provide high efficiency without the need for external Schottky diodes.

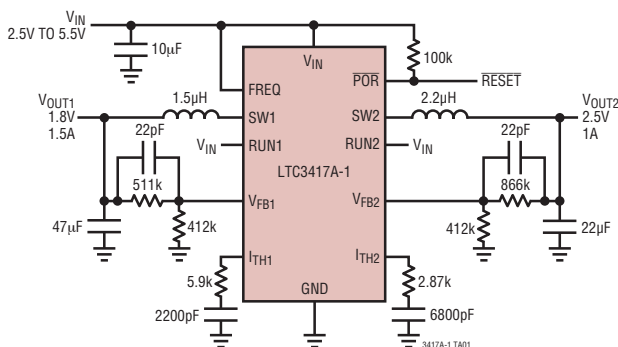
The open drain  $\overline{\text{POR}}$  pin goes low when either output voltage falls 6% below regulation. The output will remain low 150ms longer than the duration of the out of regulation condition.

A user selectable mode input allows the user to trade off ripple voltage for light load efficiency. Burst Mode operation provides high efficiency at light loads, while pulse skip mode provides low ripple noise at light loads. A phase mode pin allows the second channel to operate in-phase or 180° out-of-phase with respect to channel 1. Out-of-phase operation produces lower RMS current on V<sub>IN</sub> and thus lower stress on the input capacitor.

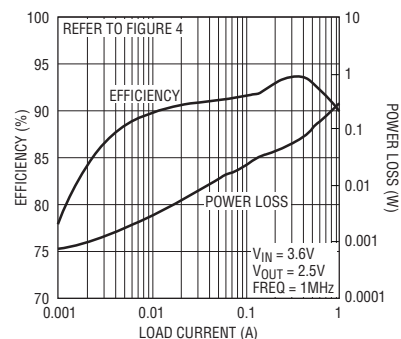
To further maximize battery life, the P-channel MOSFETs are turned on continuously in dropout (100% duty cycle) and both channels draw a total quiescent current of only 100µA. In shutdown, the device draws <1µA.

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## TYPICAL APPLICATION



**OUT2 Efficiency  
(Burst Mode Operation)**

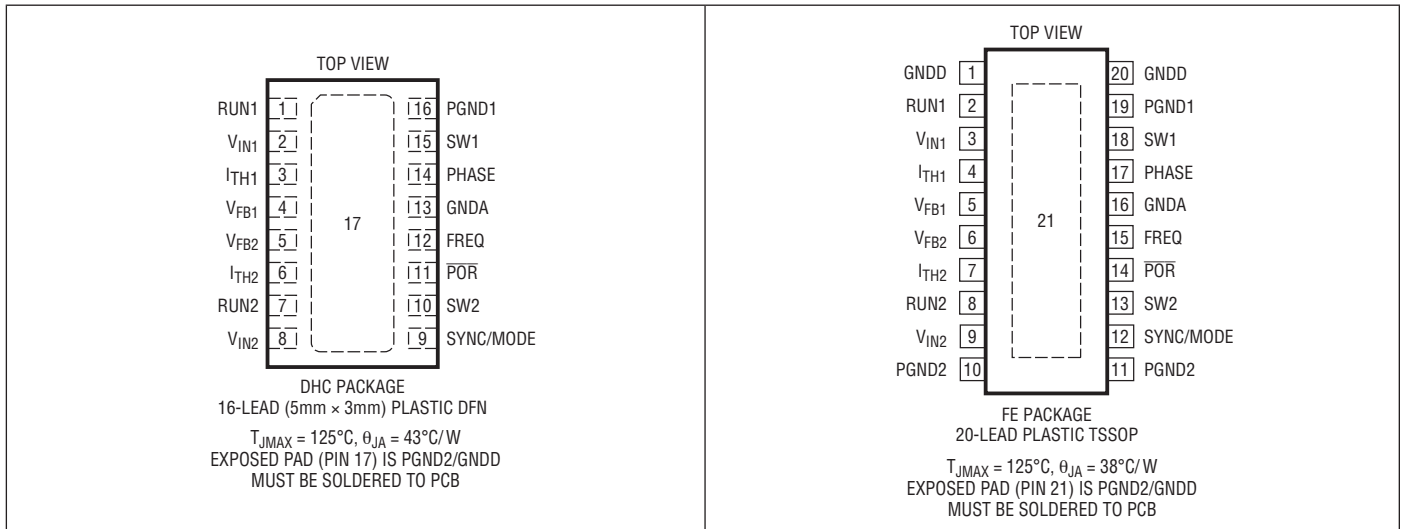


# LTC3417A-1

## ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{IN1}$ , $V_{IN2}$ Voltages.....	-0.3V to 6V	POR Voltage.....	-0.3V to 6V
SYNC/MODE, SW1, SW2, RUN1, RUN2, $V_{FB1}$ , $V_{FB2}$ , PHASE, FREQ, $I_{TH1}$ , $I_{TH2}$ Voltages.....	-0.3V to ( $V_{IN1}$ or $V_{IN2}$ ) + 0.3V	Operating Temperature Range (Note 2)	
$V_{IN1} - V_{IN2}$ , $V_{IN2} - V_{IN1}$ .....	0.3V	LTC3417AE-1 .....	-40°C to 85°C
		LTC3417AI-1 .....	-40°C to 125°C
		Junction Temperature (Notes 7, 8) .....	125°C
		Storage Temperature Range.....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3417AEDHC-1#PBF	LTC3417AEDHC-1#TRPBF	3417A1	16-Lead (3mm × 5mm) Plastic DFN	-40°C to 85°C
LTC3417AIDHC-1#PBF	LTC3417AIDHC-1#TRPBF	3417A1	16-Lead (3mm × 5mm) Plastic DFN	-40°C to 125°C
LTC3417AEFE-1#PBF	LTC3417AEFE-1#TRPBF	LTC3417AFE-1	20-Lead Plastic TSSOP	-40°C to 85°C
LTC3417AIFE-1#PBF	LTC3417AIFE-1#TRPBF	LTC3417AFE-1	20-Lead Plastic TSSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{IN} = 3.6\text{V}$  unless otherwise specified (Note 2).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN1}$ , $V_{IN2}$	Operating Voltage Range	$V_{IN1} = V_{IN2}$	2.25		5.5	V
$I_{FB1}$ , $I_{FB2}$	Feedback Pin Input Current	$V_{IN} = 6\text{V}$ Pin Under Test = 3V			± 0.1	μA

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## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 3.6\text{V}$  unless otherwise specified (Note 2).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{FB1}, V_{FB2}$	Feedback Voltage	(Note 3)	● 0.784	0.8	0.816	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation. %/V is the Percentage Change in $V_{OUT}$ with a Change in $V_{IN}$	$V_{IN} = 2.25\text{V to } 5\text{V}$ (Note 3)		0.02	0.2	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	$I_{TH1}, I_{TH2} = 0.36\text{V}$ (Note 3) $I_{TH1}, I_{TH2} = 0.84\text{V}$ (Note 3)		0.02 -0.02	0.2 -0.2	% %
$g_{m(EA)}$	Error Amplifier Transconductance	$I_{TH1}, I_{TH2(PINLOAD)} = \pm 5\mu\text{A}$ (Note 3)		1400		$\mu\text{S}$
$I_S$	Input DC Supply Current (Note 4) Active Mode	$V_{FB1} = V_{FB2} = 0.75\text{V}$ , $V_{SYNC/MODE} = V_{IN}$ , $V_{RUN1} = V_{RUN2} = V_{IN}$		400	600	$\mu\text{A}$
$I_S$	Half Active Mode ( $V_{RUN2} = 0\text{V}$ , 1.5A Only)	$V_{FB1} = 0.75\text{V}$ , $V_{SYNC/MODE} = V_{IN}$ , $V_{RUN1} = V_{IN}$		260	400	$\mu\text{A}$
	Half Active Mode ( $V_{RUN1} = 0\text{V}$ , 1A Only)	$V_{FB2} = 0.75\text{V}$ , $V_{SYNC/MODE} = V_{IN}$ , $V_{RUN2} = V_{IN}$		260	400	$\mu\text{A}$
	Both Channels in Sleep Mode	$V_{FB1} = V_{FB2} = 1\text{V}$ , $V_{SYNC/MODE} = V_{IN}$ , $V_{RUN1} = V_{RUN2} = V_{IN}$		125	250	$\mu\text{A}$
	Shutdown	$V_{RUN1} = V_{RUN2} = 0\text{V}$		0.01	1	$\mu\text{A}$
$f_{OSC}$	Oscillator Frequency	$V_{FREQ} = V_{IN}$	1.2	1.5	1.8	MHz
		$V_{FREQ}$ : $R_T = 143\text{k}$	0.85	1	1.25	MHz
		$V_{FREQ}$ : Resistor (Note 6)			4	MHz
$I_{LIM1}$	Peak Switch Current Limit on SW1 (1.5A)		2.1	2.5	A	
$I_{LIM2}$	Peak Switch Current Limit on SW2 (1A)		1.4	1.7	A	
$R_{DS(ON)1}$	SW1 Top Switch On-Resistance (1.5A)	$V_{IN1} = 3.6\text{V}$ (Note 5)		0.088		$\Omega$
	SW1 Bottom Switch On-Resistance	$V_{IN1} = 3.6\text{V}$ (Note 5)		0.084		$\Omega$
$R_{DS(ON)2}$	SW2 Top Switch On-Resistance (1A)	$V_{IN2} = 3.6\text{V}$ (Note 5)		0.16		$\Omega$
	SW2 Bottom Switch On-Resistance	$V_{IN2} = 3.6\text{V}$ (Note 5)		0.15		$\Omega$
$I_{SW1(LKG)}$	Switch Leakage Current SW1 (1.5A)	$V_{IN1} = 6\text{V}$ , $V_{RUN1} = 0\text{V}$		0.01	1	$\mu\text{A}$
$I_{SW2(LKG)}$	Switch Leakage Current SW2 (1A)	$V_{IN2} = 6\text{V}$ , $V_{RUN2} = 0\text{V}$		0.01	1	$\mu\text{A}$
$V_{UVLO}$	Undervoltage Lockout Threshold	$V_{IN1}, V_{IN2}$ Ramping Down	1.9	2.07	2.2	V
		$V_{IN1}, V_{IN2}$ Ramping Up	1.95	2.12	2.25	V
$V_{TH(POR)}$	Power-On-Reset Threshold Percentage Deviation of $V_{FB}$ Voltage from Steady State Value (Typically 0.8V)	$V_{FB1}$ or $V_{FB2}$ Ramping Up		-6		%
		$V_{FB1}$ or $V_{FB2}$ Ramping Down		-8		%
$R_{POR}$	Power-On-Reset Pull Down On-Resistance			120	300	$\Omega$
$t_{POR}$	Power-On-Reset De-Assertion Delay from Fault Removal	$FREQ = V_{IN}$		212,992		Clock Cycles
		$FREQ$ Tied to GND Through 143k Resistor		294,912		Clock Cycles
$V_{RUN1}, V_{RUN2}$	RUN1, RUN2 Threshold		0.3	0.85	1.5	V
$V_{PHASE}$	PHASE Threshold High-CMOS Levels		$V_{IN} - 0.5$			V
	PHASE Threshold Low-CMOS Levels				0.5	V
$I_{RUN1}, I_{RUN2}, I_{PHASE}, I_{SYNC/MODE}$	RUN1, RUN2, PHASE and SYNC/MODE Leakage Current	$V_{IN} = 6\text{V}$ , Pin Under Test = 3V		$\pm 0.01$	$\pm 1$	$\mu\text{A}$
$V_{T_{SYNC/MODE}}$	SYNC/MODE Threshold Voltage Low				0.5	V
$V_{T_{SYNC/MODE}}$	SYNC/MODE Threshold Voltage High		$V_{IN} - 0.5$			V
$V_{T_{FREQ}}$	FREQ Threshold Voltage High		$V_{IN} - 0.5$			V

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3417AE-1 is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the -40°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3417AI-1 is guaranteed to meet performance specifications over the -40°C to 125°C operating temperature range.

**Note 3:** The LTC3417A-1 is tested in feedback loop which serves  $V_{FB1}$  to the midpoint for the error amplifier ( $V_{ITH1} = 0.6V$ ) and  $V_{FB2}$  to the midpoint for the error amplifier ( $V_{ITH2} = 0.6V$ ).

**Note 4:** Total supply current is higher due to the internal gate charge being delivered at the switching frequency.

**Note 5:** Switch on-resistance is guaranteed by design and test correlation on the DHC package and by final test correlation on the FE package.

**Note 6:** Variable frequency operation with resistor is guaranteed by design but not production tested and is subject to duty cycle limitations.

**Note 7:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

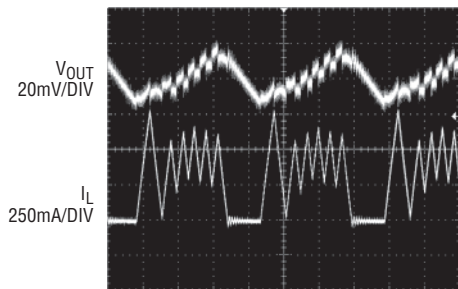
**Note 8:**  $T_J$  is calculated from the ambient temperature,  $T_A$ , and power dissipation,  $P_D$ , according to the following formula:

$$\text{LTC3417AEDHC-1: } T_J = T_A + (P_D \cdot 43^\circ\text{C/W})$$

$$\text{LTC3417AEFE-1: } T_J = T_A + (P_D \cdot 38^\circ\text{C/W})$$

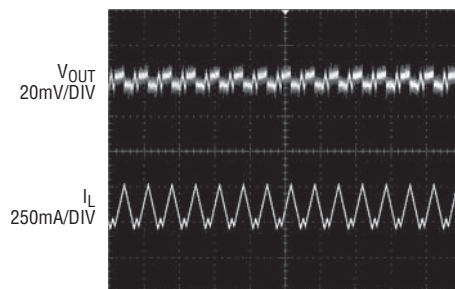
## TYPICAL PERFORMANCE CHARACTERISTICS

**OUT1 Burst Mode Operation**



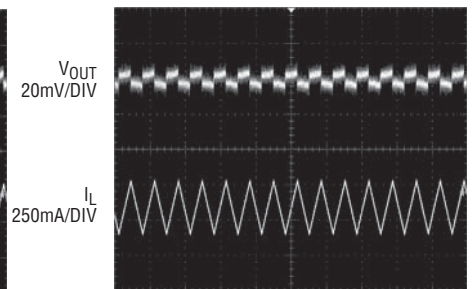
$V_{IN} = 3.6V$   
 $V_{OUT} = 1.8V$   
 $I_{LOAD} = 100mA$   
 REFER TO FIGURE 4

**OUT1 Pulse Skipping Mode Operation**



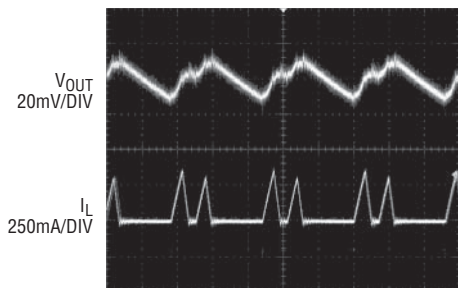
$V_{IN} = 3.6V$   
 $V_{OUT} = 1.8V$   
 $I_{LOAD} = 100mA$   
 REFER TO FIGURE 4

**OUT1 Forced Continuous Mode Operation**



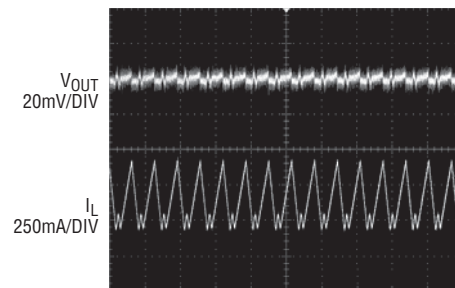
$V_{IN} = 3.6V$   
 $V_{OUT} = 1.8V$   
 $I_{LOAD} = 100mA$   
 REFER TO FIGURE 4

**OUT2 Burst Mode Operation**



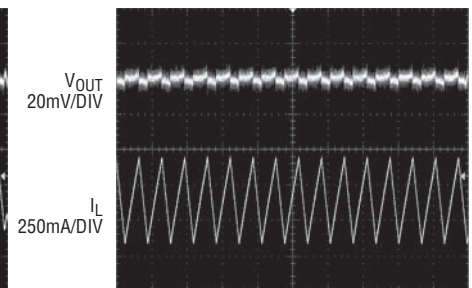
$V_{IN} = 3.6V$   
 $V_{OUT} = 2.5V$   
 $I_{LOAD} = 60mA$   
 REFER TO FIGURE 4

**OUT2 Pulse Skipping Mode Operation**



$V_{IN} = 3.6V$   
 $V_{OUT} = 2.5V$   
 $I_{LOAD} = 60mA$   
 REFER TO FIGURE 4

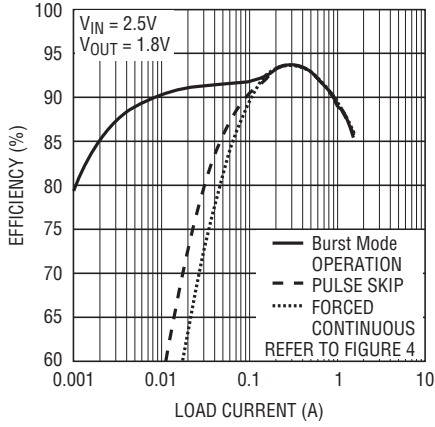
**OUT2 Forced Continuous Mode Operation**



$V_{IN} = 3.6V$   
 $V_{OUT} = 2.5V$   
 $I_{LOAD} = 60mA$   
 REFER TO FIGURE 4

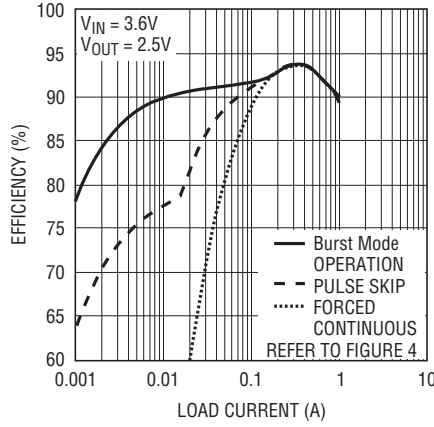
# TYPICAL PERFORMANCE CHARACTERISTICS

**OUT1 Efficiency vs Load Current**



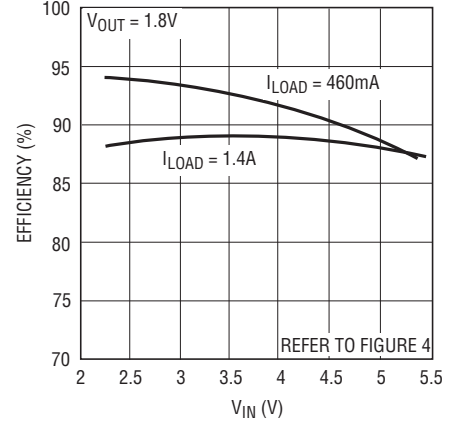
3417A-1 G07

**OUT2 Efficiency vs Load Current**



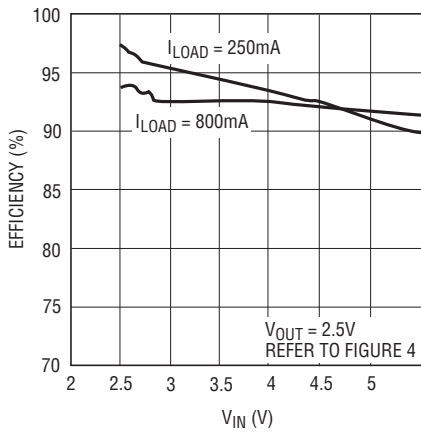
3417A-1 G08

**OUT1 Efficiency vs VIN (Burst Mode Operation)**



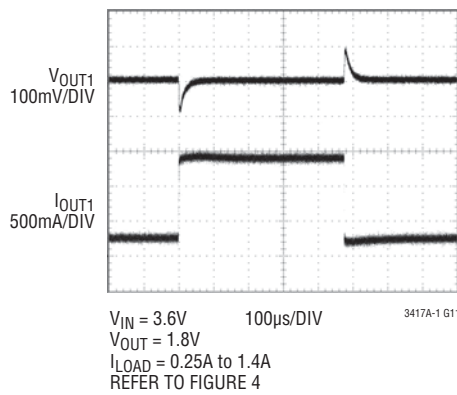
3417A-1 G09

**OUT2 Efficiency vs VIN (Pulse Skipping Mode)**



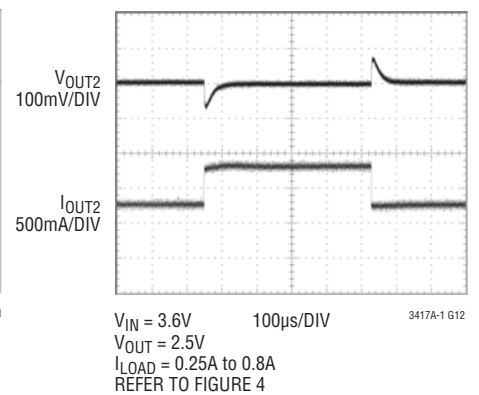
3417A-1 G10

**Load Step OUT1**



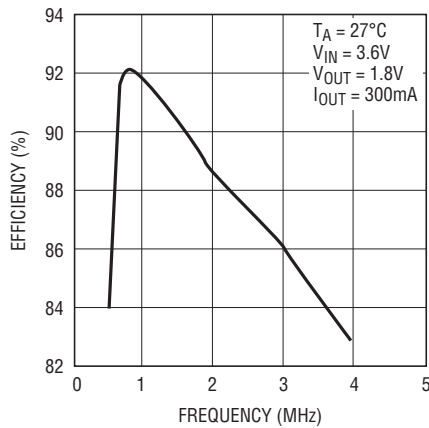
3417A-1 G11

**Load Step OUT2**



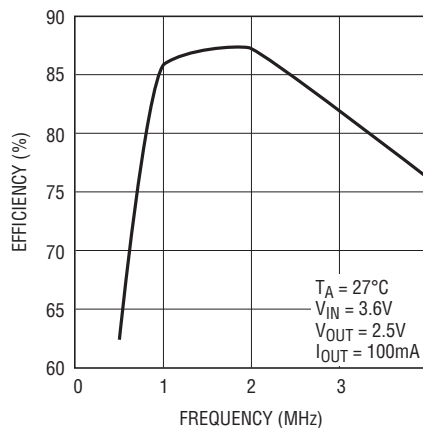
3417A-1 G12

**Efficiency vs Frequency OUT1**



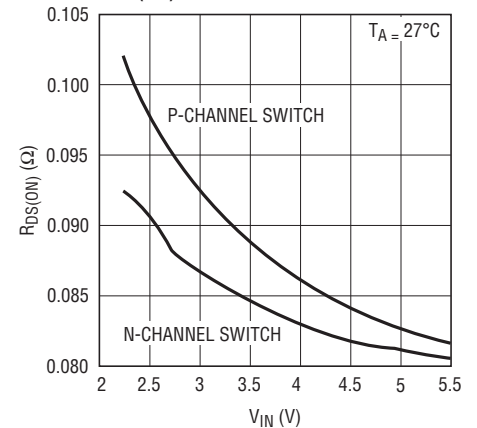
3417A-1 G13

**Efficiency vs Frequency OUT2**



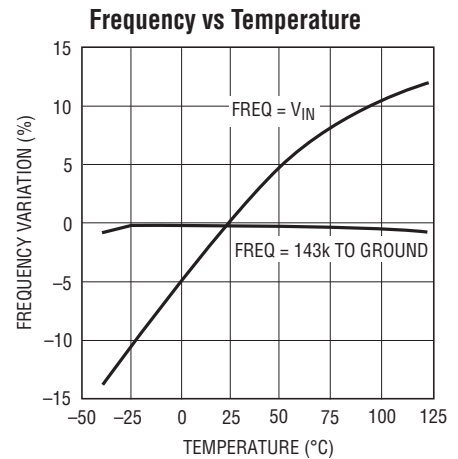
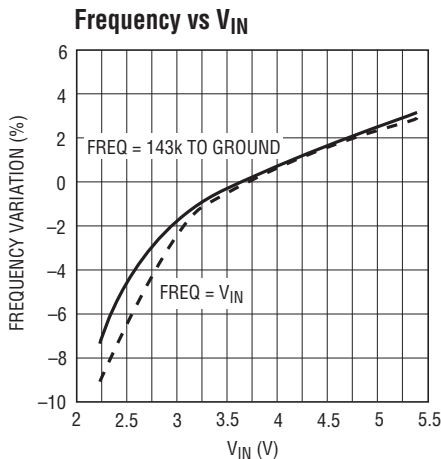
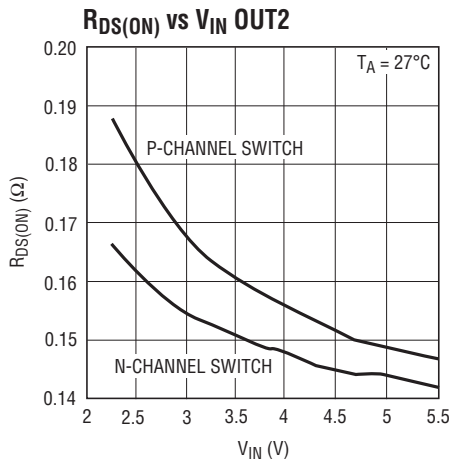
3417A-1 G14

**RDS(ON) vs VIN OUT1**



3417A-1 G15

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS (DFN/TSSOP)

**RUN1 (Pin 1/Pin 2):** Enable for 1.5A Regulator. When at Logic 1, 1.5A regulator is running. When at 0V, 1.5A regulator is off. When both RUN1 and RUN2 are at 0V, the part is in shutdown.

**V<sub>IN1</sub> (Pin 2/Pin 3):** Supply Pin for P-Channel Switch of 1.5A Regulator.

**I<sub>TH1</sub> (Pin 3/Pin 4):** Error Amplifier Compensation Point for 1.5A Regulator. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.5V.

**V<sub>FB1</sub> (Pin 4/Pin 5):** Receives the feedback voltage from external resistive divider across the 1.5A regulator output. Nominal voltage for this pin is 0.8V.

**V<sub>FB2</sub> (Pin 5/Pin 6):** Receives the feedback voltage from external resistive divider across the 1A regulator output. Nominal voltage for this pin is 0.8V.

**I<sub>TH2</sub> (Pin 6/Pin 7):** Error Amplifier Compensation Point for 1A regulator. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.5V.

**RUN2 (Pin 7/Pin 8):** Enable for 1A Regulator. When at Logic 1, 1A regulator is running. When at 0V, 1A regulator is off. When both RUN1 and RUN2 are at 0V, the part is in shutdown.

**V<sub>IN2</sub> (Pin 8/Pin 9):** Supply Pin for P-Channel Switch of 1A Regulator and Supply for Analog Circuitry.

**SYNC/MODE (Pin 9/Pin 12):** Combination Mode Selection and Oscillator Synchronization Pin. This pin controls the operation of the device. When the voltage on the SYNC/MODE pin is  $>(V_{IN} - 0.5V)$ , Burst Mode operation is selected. When the voltage on the SYNC/MODE pin is  $<0.5V$ , pulse skipping mode is selected. When the SYNC/MODE pin is held at  $V_{IN}/2$ , forced continuous mode is selected. The oscillation frequency can be synchronized to an external oscillator applied to this pin. When synchronized to an external clock, pulse skip mode is selected.

**SW2 (Pin 10/Pin 13):** Switch Node Connection to the Inductor for the 1A Regulator. This pin swings from  $V_{IN2}$  to PGND2.

**POR (Pin 11/Pin 14):** The Power-On-Reset Pin. This open drain-logic output is pulled to GND when the output voltage of either regulator falls 8% below regulation and goes high approximately 150ms after both regulators are above  $-6\%$  of regulation. If either RUN1 or RUN2 is low (the respective regulator is in sleep mode and therefore the output voltage is low), then  $\overline{\text{POR}}$  reflects the regulation of the running regulator.

**FREQ (Pin 12/Pin 15):** Frequency Set Pin. When FREQ is at  $V_{IN}$ , internal oscillator runs at 1.5MHz. When a resistor is connected from this pin to ground, the internal oscillator frequency can be varied from 0.6MHz to 4MHz.

**GNDA (Pin 13/Pin 16):** Analog Ground Pin for Internal Analog Circuitry.

## PIN FUNCTIONS

**PHASE (Pin 14/Pin 17):** Selects 1A regulator switching phase with respect to 1.5A regulator switching. Set to  $V_{IN1}$ , the 1.5A regulator and the 1A regulator are in phase. When PHASE is at 0V, the 1.5A regulator and the 1A regulator are switching 180 degrees out-of-phase. Do not float this pin.

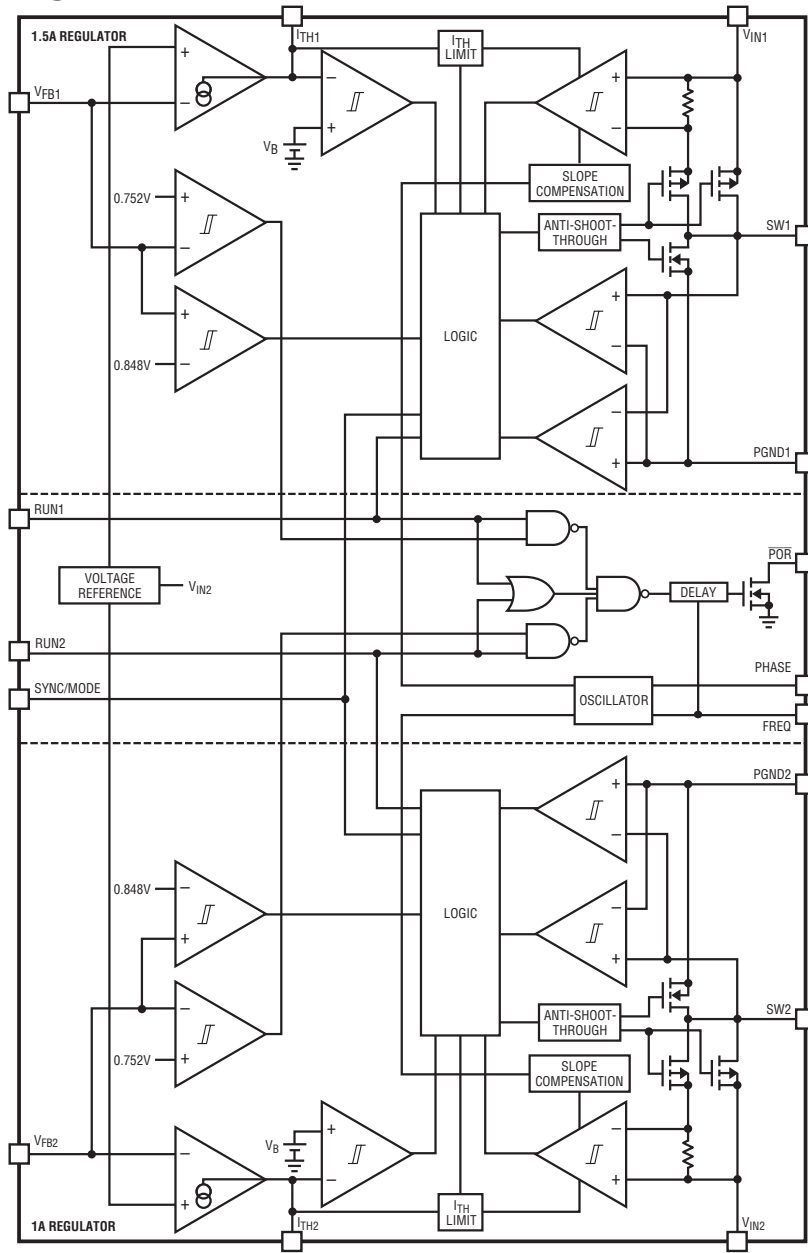
**SW1 (Pin 15/Pin 18):** Switch Node Connection to the Inductor for the 1.5A Regulator. This pin swings from  $V_{IN1}$  to PGND1.

**PGND1 (Pin 16/Pin 19):** Ground for SW1 N-Channel Driver.

**PGND2, GNDD (Pins 1,10,11,20):** TSSOP Package Only. Ground for SW2 N-channel driver and digital ground for circuit.

**Exposed Pad (Pin 17/Pin 21):** PGND2, GNDD. Ground for SW2 N-channel driver and digital ground for circuit. The Exposed Pad must be soldered to PCB ground.

## FUNCTIONAL DIAGRAM



3417A-1 BD

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## OPERATION

The LTC3417A-1 uses a constant frequency, current mode architecture. Both channels share the same clock frequency. The PHASE pin sets whether the channels are running in-phase or out of phase. The operating frequency is determined by connecting the FREQ pin to  $V_{IN}$  for 1.5MHz operation or by connecting a resistor from FREQ to ground for a frequency from 0.6MHz to 4MHz. To suit a variety of applications, the SYNC/MODE pin allows the user to trade off noise for efficiency.

The output voltages are set by external dividers returned to the  $V_{FB1}$  and  $V_{FB2}$  pins. An error amplifier compares the divided output voltage with a reference voltage of 0.8V and adjusts the peak inductor current accordingly. Undervoltage comparators will pull the  $\overline{POR}$  output low when either output voltage is 8% below its targeted value. The  $\overline{POR}$  output will go high after 212,992 cycles (when FREQ is high) or 294,912 cycles (when FREQ is tied to ground through an external resistor), or about 150ms, after both regulators are above -6% of the target output voltage.

### Main Control Loop

For each regulator, during normal operation, the P-channel MOSFET power switch is turned on at the beginning of a clock cycle when the  $V_{FB}$  voltage is below the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom N-channel MOSFET switch into the load until the next clock cycle.

The peak inductor current is controlled by the voltage on the  $I_{TH}$  pin, which is the output of the error amplifier. This amplifier compares the  $V_{FB}$  pin to the 0.8V reference. When the load current increases the  $V_{FB}$  voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the  $I_{TH}$  voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground. A digital soft-start is enabled after shutdown, which will slowly ramp the peak inductor current up over 1024 clock cycles.

### Low Current Operation

Three modes are available to control the operation of the LTC3417A-1 at low currents. Each of the three modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected. When the load is relatively light, the LTC3417A-1 automatically switches into Burst Mode operation in which the PMOS switches operate intermittently based on load demand. By running cycles periodically, the switching losses, which are dominated by the gate charge losses of the power MOSFETs, are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. The hysteresis voltage comparator trips when  $I_{TH}$  is below 0.24V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until  $I_{TH}$  exceeds 0.31V, turning on the switch and the main control loop which starts another cycle.

For lower output voltage ripple at low currents, pulse skipping mode can be used. In this mode, the LTC3417A-1 continues to switch at constant frequency down to very low currents, where it will begin skipping pulses used to control the power MOSFETs.

Finally, in forced continuous mode, the inductor current is constantly cycled creating a fixed output voltage ripple at all output current levels. This feature is desirable in telecommunications since the noise is a constant frequency and is thus easy to filter out. Another advantage of this mode is that the regulator is capable of both sourcing current into a load and sinking some current from the output.

The mode selection for the LTC3417A-1 is set using the SYNC/MODE pin. The SYNC/MODE pin sets the mode for both the 1A and the 1.5A step-down DC/DC converters.



## OPERATION

### Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100%. In this dropout condition, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and inductor.

### Low Supply Operation

The LTC3417A-1 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 2.07V to prevent unstable operation.

## APPLICATIONS INFORMATION

A general LTC3417A-1 application circuit is shown in Figure 4. External component selection is driven by the load requirement, and begins with the selection of the inductors L1 and L2. Once L1 and L2 are chosen,  $C_{IN}$ ,  $C_{OUT1}$  and  $C_{OUT2}$  can be selected.

### Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency,  $f_0$ , of the LTC3417A-1 is determined by pulling the FREQ pin to  $V_{IN}$  for 1.5MHz operation or by connecting an external resistor from FREQ to ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T \approx \frac{1.61 \cdot 10^{11}}{f_0} (\Omega) - 16.586k\Omega$$

for  $0.6\text{MHz} \leq f_0 \leq 4\text{MHz}$ . Alternatively, use Figure 1 to select the value for  $R_T$ .

The maximum operating frequency is also constrained by the minimum on-time and duty cycle. This can be calculated as:

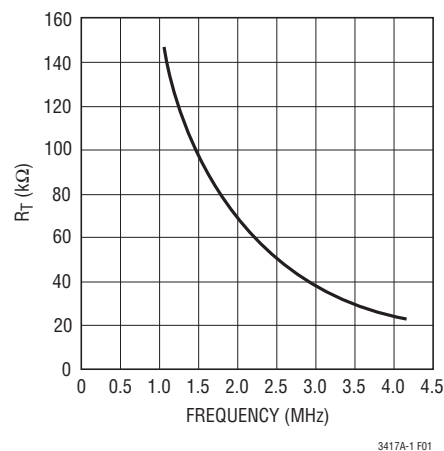


Figure 1. Frequency vs  $R_T$

$$f_{O(\text{MAX})} \approx 6.67 \left( \frac{V_{\text{OUT}}}{V_{\text{IN}(\text{MAX})}} \right) (\text{MHz})$$

The minimum frequency is limited by leakage and noise coupling due to the large resistance of  $R_T$ .

### Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current,  $\Delta I_L$ , decreases with higher inductance and increases with higher  $V_{IN}$  or  $V_{OUT}$ .

$$\Delta I_L = \frac{V_{\text{OUT}}}{f_0 \cdot L} \left( 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right)$$

Accepting larger values of  $\Delta I_L$  allows the use of low inductances, but results in higher output voltage ripple, greater core losses and lower output current capability.

## APPLICATIONS INFORMATION

A reasonable starting point for setting ripple current is  $\Delta I_L = 0.35 I_{LOAD(MAX)}$ , where  $I_{LOAD(MAX)}$  is the maximum current output. The largest ripple,  $\Delta I_L$ , occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_0 \cdot \Delta I_L} \left( 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductor values will cause the burst frequency to increase.

### Inductor Core Selection

Different core materials and shapes will change the size/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements of any radiated field/EMI requirements than on what the LTC3417A-1 requires to operate. Table 1 shows some

typical surface mount inductors that work well in LTC3417A-1 applications.

### Input Capacitor ( $C_{IN}$ ) Selection

In continuous mode, the input current of the converter can be approximated by the sum of two square waves with duty cycles of approximately  $V_{OUT1}/V_{IN}$  and  $V_{OUT2}/V_{IN}$ . To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. Some capacitors have a de-rating spec for maximum RMS current. If the capacitor being used has this requirement, it is necessary to calculate the maximum RMS current. The RMS current calculation is different if the part is used in "in phase" or "out of phase".

For "in phase", there are two different equations:

$V_{OUT1} > V_{OUT2}$ :

$$I_{RMS} = \sqrt{2 \cdot I_1 \cdot I_2 \cdot D2(1-D1) + I_2^2(D2-D2^2) + I_1^2(D1-D1^2)}$$

$V_{OUT2} > V_{OUT1}$ :

$$I_{RMS} = \sqrt{2 \cdot I_1 \cdot I_2 \cdot D1(1-D2) + I_2^2(D2-D2^2) + I_1^2(D1-D1^2)}$$

where:

$$D1 = \frac{V_{OUT1}}{V_{IN}} \quad \text{and} \quad D2 = \frac{V_{OUT2}}{V_{IN}}$$

**Table 1**

MANUFACTURER	PART NUMBER	VALUE ( $\mu$ H)	MAX DC CURRENT (A)	DCR	DIMENSIONS L x W x H (mm)
<b>L1 on OT1</b>					
Toko	A920CY-1R5M-D62CB	1.5	2.8	0.014	6 x 6 x 2.5
	A918CY-1R5M-D62LCB	1.5	2.9	0.018	6 x 6 x 2
Coilcraft	D01608C-152ML	1.5	2.6	0.06	6.6 x 4.5 x 2.9
Sumida	CDRH4D22/HP 1R5	1.5	3.9	0.031	5 x 5 x 2.4
Midcom	DUP-1813-1R4R	1.4	5.5	0.033	4.3 x 4.8 x 3.5
<b>L2 on OUT2</b>					
Toko	A915AY-2ROM-D53LC	2.0	3.9	0.027	5 x 5 x 3
Coilcraft	D01608C-222ML	2.2	2.3	0.07	6.6 x 4.5 x 2.9
Sumida	CDRH3D16/HP 2R2	2.2	1.75	0.047	4 x 4 x 1.8
		2.2	1.6	0.035	3.2 x 3.2 x 2
Midcom	DUP-1813-2R2R	2.2	3.9	0.047	4.3 x 4.8 x 3.5

## APPLICATIONS INFORMATION

When  $D_1 = D_2$  then the equation simplifies to:

$$I_{\text{RMS}} = (I_1 + I_2) \sqrt{D(1-D)}$$

or

$$I_{\text{RMS}} = (I_1 + I_2) \frac{\sqrt{V_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}})}}{V_{\text{IN}}}$$

where the maximum average output currents  $I_1$  and  $I_2$  equal the respective peak currents minus half the peak-to-peak ripple currents:

$$I_1 = I_{\text{LIM1}} - \frac{\Delta I_{\text{L1}}}{2}$$

$$I_2 = I_{\text{LIM2}} - \frac{\Delta I_{\text{L2}}}{2}$$

These formula have a maximum at  $V_{\text{IN}} = 2V_{\text{OUT}}$ , where  $I_{\text{RMS}} = (I_1 + I_2)/2$ . This simple worst case is commonly used to determine the highest  $I_{\text{RMS}}$ .

For “out of phase” operation, the ripple current can be lower than the “in phase” current.

In the “out of phase” case, the maximum  $I_{\text{RMS}}$  does not occur when  $V_{\text{OUT1}} = V_{\text{OUT2}}$ . The maximum typically occurs when  $V_{\text{OUT1}} - V_{\text{IN}}/2 = V_{\text{OUT2}}$  or when  $V_{\text{OUT2}} - V_{\text{IN}}/2 = V_{\text{OUT1}}$ . As a good rule of thumb, the amount of worst case ripple is about 75% of the worst case ripple in the “in phase” mode. Also note that when  $V_{\text{OUT1}} = V_{\text{OUT2}} = V_{\text{IN}}/2$  and  $I_1 = I_2$ , the ripple is zero.

Note that capacitor manufacturer’s ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1 $\mu\text{F}$  to 1 $\mu\text{F}$  ceramic capacitor is also recommended on  $V_{\text{IN}}$  for high frequency decoupling, when not using an all ceramic capacitor solution.

### Output Capacitor ( $C_{\text{OUT1}}$ and $C_{\text{OUT2}}$ ) Selection

The selection of  $C_{\text{OUT1}}$  and  $C_{\text{OUT2}}$  is driven by the required ESR to minimize voltage ripple and load step transients.

Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ( $\Delta V_{\text{OUT}}$ ) is determined by:

$$\Delta V_{\text{OUT}} \approx \Delta I_{\text{L}} \left( \text{ESR}_{\text{COUT}} + \frac{1}{8 \cdot f_0 \cdot C_{\text{OUT}}} \right)$$

where  $f_0$  = operating frequency,  $C_{\text{OUT}}$  = output capacitance and  $\Delta I_{\text{L}}$  = ripple current in the inductor. The output ripple is highest at maximum input voltage, since  $\Delta I_{\text{L}}$  increases with input voltage. With  $\Delta I_{\text{L}} = 0.35 I_{\text{LOAD(MAX)}}$ , the output ripple will be less than 100mV at maximum  $V_{\text{IN}}$  and  $f_0 = 1\text{MHz}$  with:

$$\text{ESR}_{\text{COUT}} < 150\text{m}\Omega$$

Once the ESR requirements for  $C_{\text{OUT}}$  have been met, the RMS current rating generally far exceeds the  $I_{\text{RIPPLE(P-P)}}$  requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it has a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost but also have the lowest capacitance density, high voltage and temperature coefficient and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic specialty polymer (SP) capacitors.

## APPLICATIONS INFORMATION

In most cases, 0.1 $\mu$ F to 1 $\mu$ F of ceramic capacitors should also be placed close to the LTC3417A-1 in parallel with the main capacitors for high frequency decoupling.

### Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Because the LTC3417 control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the  $V_{IN}$  pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop,  $V_{DROOP}$ , is usually about 2 to 3 times the linear droop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 2.5 \frac{\Delta I_{OUT}}{f_0 \cdot V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10 $\mu$ F ceramic capacitor is usually enough for these conditions.

### Setting the Output Voltage

The LTC3417A-1 develops a 0.8V reference voltage between the feedback pins,  $V_{FB1}$  and  $V_{FB2}$ , and the signal ground as shown in Figure 4. The output voltages are set by two resistive dividers according to the following formulas:

$$V_{OUT1} \approx 0.8V \left( 1 + \frac{R1}{R2} \right)$$

$$V_{OUT2} \approx 0.8V \left( 1 + \frac{R3}{R4} \right)$$

Keeping the current small (<5 $\mu$ A) in these resistors maximizes efficiency, but making the current too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor,  $C_F$ , may also be used. Great care should be taken to route the  $V_{FB}$  node away from noise sources, such as the inductor or the SW line.

### Power-On Reset

The  $\overline{POR}$  pin is an open-drain output which pulls low when either regulator is out of regulation. When both output voltages are above -6% of regulation, a timer is started which allows the POR output to go high after 212,992 clock cycles (when FREQ is tied to  $V_{IN}$ ) or 294,912 clock cycles (when FREQ is tied to ground through an external resistor). This results in a delay of approximately 150ms when the oscillator is set to 2MHz. When either channel is shut down, the  $\overline{POR}$  output reflects the condition of the running regulator.

## APPLICATIONS INFORMATION

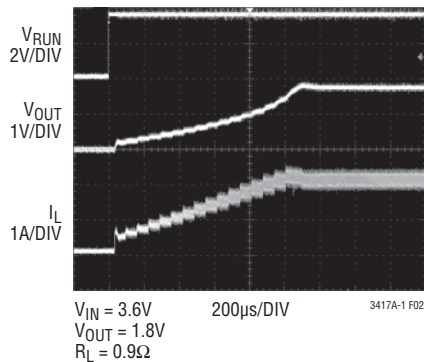


Figure 2. Digital Soft-Start OUT1

### Soft-Start

Soft-start reduces surge currents from  $V_{IN}$  by gradually increasing the peak inductor current. Power supply sequencing can also be accomplished by controlling the  $I_{TH}$  pin. The LTC3417A-1 has an internal digital soft-start for each regulator output, which steps up a clamp on  $I_{TH}$  over 1024 clock cycles, as can be seen in Figures 2 and 3. As the voltage on  $I_{TH}$  ramps through its operating range, the internal peak current limit is also ramped at a proportional linear rate.

### Mode Selection

The SYNC/MODE pin is a multipurpose pin which provides mode selection and frequency synchronization. Connecting this pin to  $V_{IN}$  enables Burst Mode operation for both regulators, which provides the best low current efficiency at the cost of a higher output voltage ripple. When SYNC/MODE is connected to ground, pulse skipping operation is selected for both regulators, which provides the lowest output voltage and current ripple at the cost of low current efficiency. Applying a voltage that is more than 1V from either supply results in forced continuous mode for both regulators, which creates a fixed output ripple and allows the sinking of some current (about  $1/2\Delta I_L$ ). Since the switching noise is constant in this mode, it is also the easiest to filter out. In many cases, the output voltage can be simply connected to the SYNC/MODE pin, selecting the forced continuous mode except at start-up.

The LTC3417A-1 can be synchronized to an external clock signal by the SYNC/MODE pin. The internal oscillator frequency should be set to 20% lower than the external clock frequency to ensure adequate slope compensation, since slope compensation is derived from the internal oscillator. During synchronization, the mode is set to pulse skipping and the top switch turn-on is synchronized to the rising edge of the external clock.

When using an external clock, with the PHASE pin low, the switching of the two channels occur at the edges of the external clock. A 50% duty cycle will therefore produce 180° out-of-phase operation.

### Checking Transient Response

The  $I_{TH}$  pin compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the  $I_{TH}$  pin not only allows optimization of the control loop behavior, but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated using the percentage of overshoot seen at this pin or by examining the rise time at this pin.

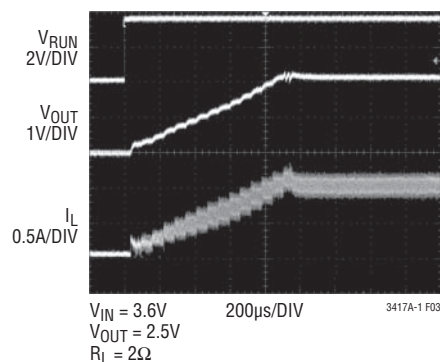


Figure 3. Digital Soft-Start OUT2

## APPLICATIONS INFORMATION

The  $I_{TH}$  external components shown in the Figure 4 circuit will provide an adequate starting point for most applications. The series RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because of various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of  $1\mu\text{s}$  to  $10\mu\text{s}$  will produce output voltage and  $I_{TH}$  pin waveforms that will give a sense of overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{OUT}$  immediately shifts by an amount equal to  $\Delta I_{LOAD} \cdot ESR_{C_{OUT}}$ , where  $ESR_{C_{OUT}}$  is the effective series resistance of  $C_{OUT}$ .  $\Delta I_{LOAD}$  also begins to charge or discharge  $C_{OUT}$  generating a feedback error signal used by the regulator to return  $V_{OUT}$  to its steady-state value. During this recovery time,  $V_{OUT}$  can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with  $R_{ITH}$  and the bandwidth of the loop increases with decreasing  $C_{ITH}$ . If  $R_{ITH}$  is increased by the same factor that  $C_{ITH}$  is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, feedforward capacitors, C1 and C2, can be added to improve the high frequency response, as shown in Figure 4. Capacitor C1 provides phase lead by creating a high frequency zero with R1 which improves the phase margin for the 1.5A SW1 channel. Capacitor C2 provides phase lead by creating a high frequency zero with R3 which improves the phase margin for the 1A SW2 channel.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage  $V_{IN}$  drops toward  $V_{OUT}$ , the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta, or single inductor, positive buck boost.

In some applications, a more severe transient can be caused by switching in loads with large ( $>1\mu\text{F}$ ) input capacitors. The discharged input capacitors are effectively put in parallel with  $C_{OUT}$ , causing a rapid drop in  $V_{OUT}$ . No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (P1 + P2 + P3 + \dots)$$

where P1, P2, etc. are the individual losses as a percentage of input power.

Hot Swap is a trademark of Linear Technology Corporation.

## APPLICATIONS INFORMATION

Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3417A-1 circuits: 1) LTC3417A-1  $I_S$  current, 2) switching losses, 3)  $I^2R$  losses, 4) other losses.

- 1) The  $I_S$  current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents.  $I_S$  current results in a small (<0.1%) loss that increases with  $V_{IN}$ , even at no load.
- 2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge moves from  $V_{IN}$  to ground. The resulting charge over the switching period is a current out of  $V_{IN}$  that is typically much larger than the DC bias current. The gate charge losses are proportional to  $V_{IN}$  and thus their effects will be more pronounced at higher supply voltages.
- 3)  $I^2R$  losses are calculated from the DC resistances of the internal switches,  $R_{SW}$ , and the external inductor,  $R_L$ . In continuous mode, the average output current flowing through inductor L is “chopped” between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET  $R_{DS(ON)}$  and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The  $R_{DS(ON)}$  for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain  $I^2R$  losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

where  $R_L$  is the resistance of the inductor.

- 4) Other “hidden” losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these “system” level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that  $C_{IN}$  has adequate charge storage and very low  $ESR_{COUT}$  at

the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

### Thermal Considerations

The LTC3417A-1 requires the package Exposed Pad (PGND2/GNDD pin) to be well soldered to the PC board. This gives the DFN and TSSOP packages exceptional thermal properties, compared to similar packages of this size, making it difficult in normal operation to exceed the maximum junction temperature of the part. In a majority of applications, the LTC3417A-1 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3417A-1 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both switches in both regulators will be turned off and the SW nodes will become high impedance.

To prevent the LTC3417A-1 from exceeding its maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \cdot \theta_{JA}$$

where  $P_D$  is the power dissipated by the regulator and  $\theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature,  $T_J$ , is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3417A-1 is in dropout in both regulators at an input voltage of 3.3V with load currents of 1.5A and 1A. From the Typical Performance Characteristics graph of Switch Resistance, the  $R_{DS(ON)}$  resistance of the 1.5A P-channel switch is 0.09Ω and the  $R_{DS(ON)}$  of the 1A P-channel switch is 0.163Ω.

## APPLICATIONS INFORMATION

The power dissipated by the part is:

$$PD = I_1^2 \cdot R_{DS(ON)1} + I_2^2 \cdot R_{DS(ON)2}$$

$$PD = 1.5^2 \cdot 0.09 + 1^2 \cdot 0.163$$

$$PD = 366\text{mW}$$

The DFN package junction-to-ambient thermal resistance,  $\theta_{JA}$ , is about  $43^\circ\text{C/W}$ . Therefore, the junction temperature of the regulator operating in a  $70^\circ\text{C}$  ambient temperature is approximately:

$$T_J = 0.366 \cdot 43 + 70$$

$$T_J = 85.7^\circ\text{C}$$

Remembering that the above junction temperature is obtained from an  $R_{DS(ON)}$  at  $25^\circ\text{C}$ , we might recalculate the junction temperature based on a higher  $R_{DS(ON)}$  since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of  $125^\circ\text{C}$ .

### Design Example

As a design example, consider using the LTC3417A-1 in a portable application with a Li-Ion battery. The battery provides a  $V_{IN}$  from 2.8V to 4.2V. One load requires 1.8V at 1.5A in active mode, and 1mA in standby mode. The other load requires 2.5V at 1A in active mode, and 500 $\mu\text{A}$  in standby mode. Since both loads still need power in standby, Burst Mode operation is selected for good low load efficiency ( $\text{SYNC/MODE} = V_{IN}$ ).

First, determine what frequency should be used. Higher frequency results in a lower inductor value for a given  $\Delta I_L$  ( $\Delta I_L$  is estimated as  $0.35I_{LOAD(MAX)}$ ). Reasonable values for wire wound surface mount inductors are usually in the range of  $1\mu\text{H}$  to  $10\mu\text{H}$ .

CONVERTER OUTPUT	$I_{LOAD(MAX)}$	$\Delta I_L$
SW1	1.5A	525mA
SW2	1A	350mA

Using the 1.5MHz frequency setting ( $\text{FREQ} = V_{IN}$ ), we get the following equations for L1 and L2:

$$L1 = \frac{1.8\text{V}}{1.5\text{MHz} \cdot 525\text{mA}} \left( 1 - \frac{1.8\text{V}}{4.2\text{V}} \right) = 1.3\mu\text{H}$$

Use  $1.5\mu\text{H}$ .

$$L2 = \frac{2.5\text{V}}{1.5\text{MHz} \cdot 350\text{mA}} \left( 1 - \frac{2.5\text{V}}{4.2\text{V}} \right) = 1.9\mu\text{H}$$

Use  $2.2\mu\text{H}$ .

$C_{OUT}$  selection is based on load step droop instead of ESR requirements. For a 2.5% output droop:

$$C_{OUT1} = 2.5 \cdot \frac{1.5\text{A}}{1.5\text{MHz}(5\% \cdot 1.8\text{V})} = 28\mu\text{F}$$

$$C_{OUT2} = 2.5 \cdot \frac{1\text{A}}{1.5\text{MHz}(5\% \cdot 2.5\text{V})} = 13\mu\text{F}$$

The closest standard values are  $47\mu\text{F}$  and  $22\mu\text{F}$ .

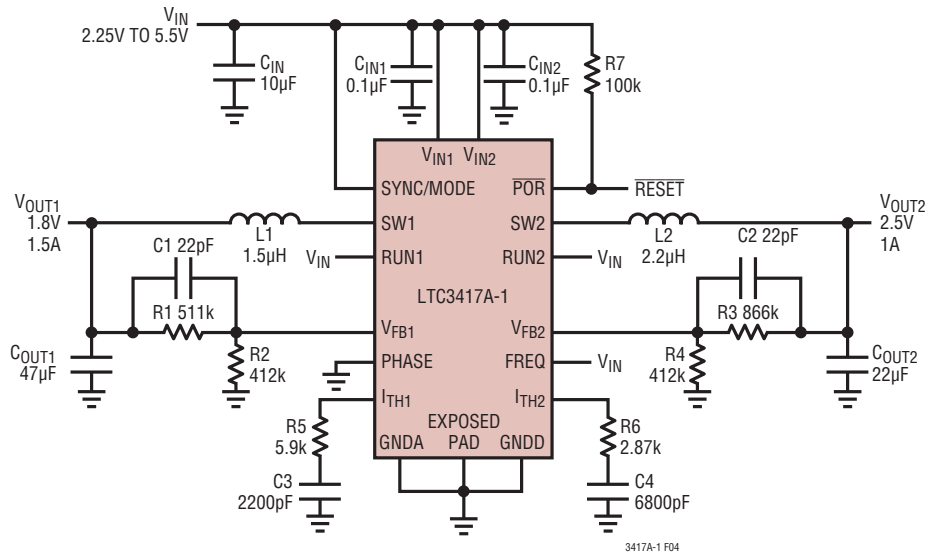
The output voltages can now be programmed by choosing the values of R1, R2, R3, and R4. To maintain high efficiency, the current in these resistors should be kept small. Choosing  $2\mu\text{A}$  with the 0.8V feedback voltages makes R2 and R4 equal to 400k. A close standard 1% resistor is 412k. This then makes R1 = 515k. A close standard 1% is 511k. Similarly, with R4 at 412k, R3 is equal to 875k. A close 1% resistor is 866k.

The compensation should be optimized for these components by examining the load step response, but a good place to start for the LTC3417A-1 is with a  $5.9\text{k}\Omega$  and  $2200\text{pF}$  filter on  $I_{TH1}$  and  $2.87\text{k}$  and  $6800\text{pF}$  on  $I_{TH2}$ . The output capacitor may need to be increased depending on the actual undershoot during a load step.

The  $\overline{\text{POR}}$  pin is an open drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed. Figure 4 shows a complete schematic for this design.



APPLICATIONS INFORMATION



L1: MIDCOM DUS-5121-1R5R  
 C\_OUT1: KEMET C1210C226K8PAC

L2: MIDCOM DUS-5121-2R2R  
 C\_OUT2, C\_IN: KEMET C1206C106K4PAC

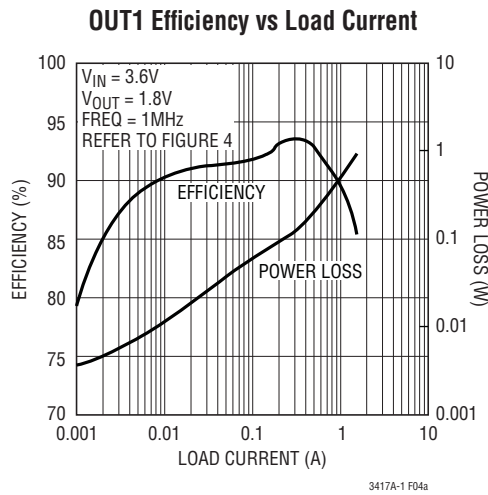


Figure 4. 1.8V at 1.5A/2.5V at 1A Step-Down Regulators

## APPLICATIONS INFORMATION

### Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3417A-1. These items are also illustrated graphically in the layout diagram of Figure 5. Check the following in your layout.

1. Does the capacitor  $C_{IN}$  connect to the power  $V_{IN1}$  (Pin 2),  $V_{IN2}$  (Pin 8), and PGND2/GNDD (Pin 17) as close as possible (DFN package)? It may be necessary to split  $C_{IN}$  into two capacitors. This capacitor provides the AC current to the internal power MOSFETs and their drivers.
2. Are the  $C_{OUT1}$ ,  $L_1$  and  $C_{OUT2}$ ,  $L_2$  closely connected? The (-) plate of  $C_{OUT1}$  returns current to PGND1, and the (-) plate of  $C_{OUT2}$  returns current to the PGND2/GNDD and the (-) plate of  $C_{IN}$ .
3. The resistor divider, R1 and R2, must be connected between the (+) plate of  $C_{OUT1}$  and a ground line terminated near GNDA. The resistor divider, R3 and R4,

must be connected between the (+) plate of  $C_{OUT2}$  and a ground line terminated near GNDA. The feedback signals  $V_{FB1}$  and  $V_{FB2}$  should be routed away from noise components and traces, such as the SW lines, and its trace should be minimized.

4. Keep sensitive components away from the SW pins. The input capacitor  $C_{IN}$ , the compensation capacitors  $C_{C1}$ ,  $C_{C2}$ ,  $C_{ITH1}$  and  $C_{ITH2}$  and all resistors R1, R2, R3, R4,  $R_{ITH1}$  and  $R_{ITH2}$  should be routed away from the SW traces and the inductors L1 and L2.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GNDA pin at one point which is then connected to the PGND2/GNDD pin.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies.

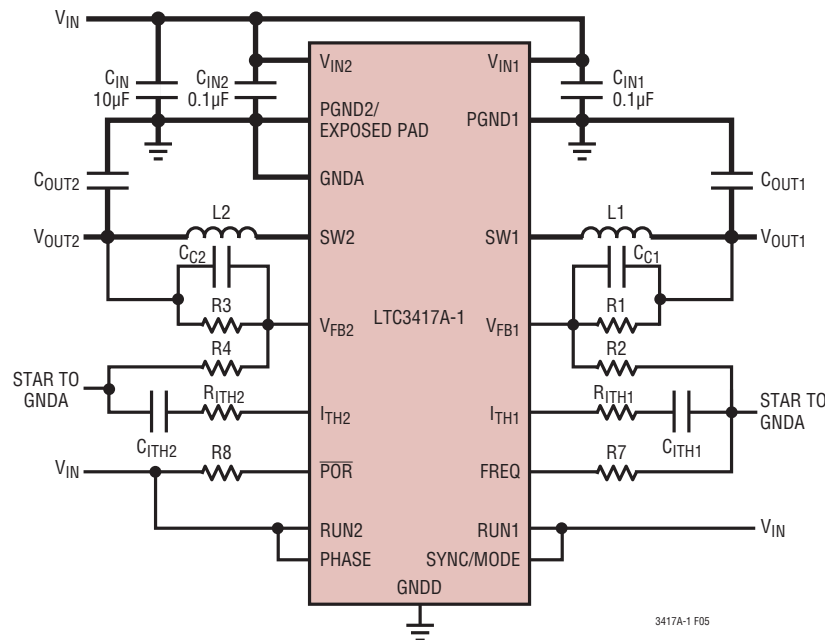
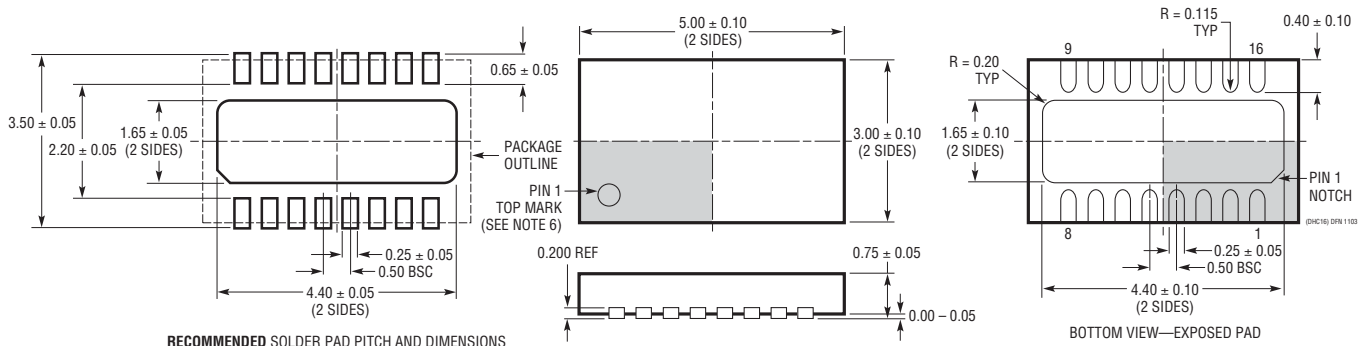


Figure 5. Layout Guideline

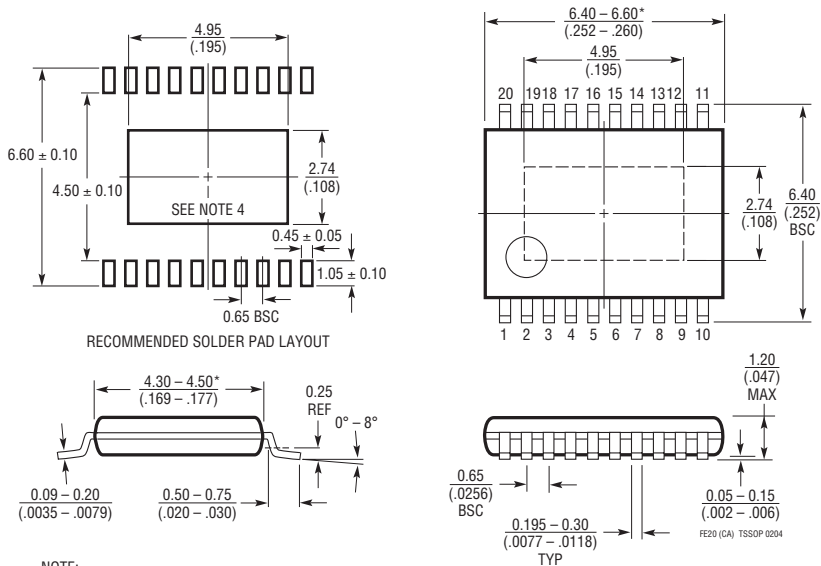
**PACKAGE DESCRIPTION**

**DHC Package**  
**16-Lead Plastic DFN (5mm × 3mm)**  
 (Reference LTC DWG # 05-08-1706)



- NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

**FE Package**  
**20-Lead Plastic TSSOP (4.4mm)**  
 (Reference LTC DWG # 05-08-1663)  
**Exposed Pad Variation CA**



- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
  2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
  3. DRAWING NOT TO SCALE
  4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
- \*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

# LTC3417A-1

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3406A/B	600mA, 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 20 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, ThinSOT™ Package
LTC3407A	Dual 600mA/600mA 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, MS10E, 3mm × 3mm DFN-10 Package
LTC3409	600mA, 1.7/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN(MIN)}$ : 1.6V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 65 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 3mm DFN-8 Package
LTC3410/B	300mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 26 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, SC70 Package
LTC3411A	1.25A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, MS10, 3mm × 3mm DFN-10 Package
LTC3412A	2.5A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 4mm × 4mm QFN-16, TSSOP-16E Package
LTC3414	4A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.25V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 64 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, TSSOP-20E Package
LTC3416	4A, 4MHz, Synchronous Step-Down DC/DC Converter with Tracking	95% Efficiency, $V_{IN(MIN)}$ : 2.25V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 64 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, TSSOP-20E Package
LTC3417	Dual 1.4A/800mA, 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 125 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 5mm DFN-16, TSSOP-20E Packages
LTC3417A	Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.3V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 125 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, TSSOP-16E, 3mm × 3mm DFN-16 Package
LTC3417A-2	Dual 1.5A/1A ( $I_{OUT}$ ) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.25V to 5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 125 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 5mm DFN-16, TSSOP-20E Packages
LTC3418	8A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.25V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 380 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 5mm × 7mm QFN-38 Package
LTC3419/-1	Dual 600mA/600mA 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 35 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, MS10, 3mm × 3mm DFN-10 Package
LTC3438	800mA, 1MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.4V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 1.5V to 5.25V, $I_Q$ = 35 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 2mm × 3mm DFN-8 Package
LTC3440	600mA, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 2.5V to 5.5V, $I_Q$ = 25 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, MS10, 3mm × 3mm DFN-10 Package
LTC3441/2/3	1.2A, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.4V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 2.4V to 5.25V, $I_Q$ = 50 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 4mm DFN-12 Package
LTC3530	600mA, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 1.8V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 1.8V to 5.5V, $I_Q$ = 40 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, MS10, 3mm × 3mm DFN-10 Package
LTC3531/-3/3.3	200mA, 1.5MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 1.8V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 2V to 5V, $I_Q$ = 16 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, ThinSOT, 3mm × 3mm DFN-6 Package
LTC3542	500mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 26 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 2mm × 2mm DFN-6, ThinSOT Package
LTC3544/B	Quad 100/200/200/300mA, 2.25MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.3V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 70 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 3mm QFN-16 Package
LTC3545/-1	Triple, 800mA × 3, 2.25MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.3V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 58 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 3mm QFN-16 Package
LTC3547/B	Dual 300mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, DFN-8 Package
LTC3548/-1/-2	Dual 400mA & 800mA $I_{OUT}$ , 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, MS10E, 3mm × 3mm DFN-10 Package
LTC3560	800mA 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 16 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, ThinSOT Package
LTC3561	1.25A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.5V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 240 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 3mm DFN-8 Package
LTC3562	Quad, I <sup>2</sup> C Interface, 600/600/400/400mA, 2.25MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ : 2.9V, $V_{IN(MAX)}$ : 5.5V, $V_{OUT(MIN)}$ = 0.425V, $I_Q$ = 100 $\mu$ A, $I_{SD}$ < 1 $\mu$ A, 3mm × 3mm QFN-20 Package

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