2A Wide Input Voltage Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Regulated Output with Input Voltages Above, Below or Equal to the Output**
- **1.8V to 5.5V (Input) and 5.25V (Output) Voltage Range**
- **0.8A Continuous Output Current: V_{IN} > 1.8V**
- **2A Continuous Output Current: V_{IN} > 3V**
- **Single Inductor**
- Synchronous Rectification: Up to 96% Efficiency
- Programmable Burst Mode® Operation: I_Q = 40µA
- Output Disconnect in Shutdown
- Programmable Frequency from 300kHz to 2MHz
- <1µA Shutdown Current
- Small Thermally Enhanced 14-Lead (3mm × 4mm × 0.75mm) DFN package

APPLICATIONS

- GSM Modems
- Handheld Instruments
- Digital Cameras
- Smart Phones
- Media Players
- Miniature Hard Disk Drive Power

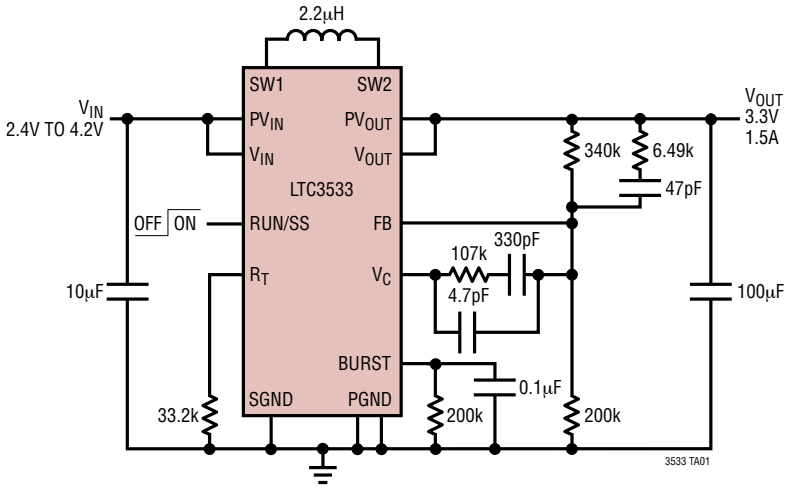
DESCRIPTION

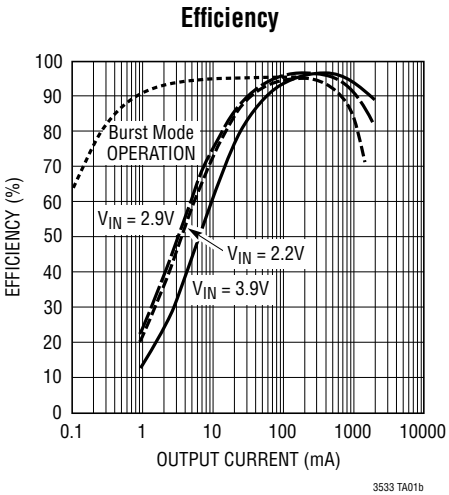
The LTC®3533 is a wide V_{IN} range, highly efficient, fixed frequency, buck-boost DC/DC converter that operates from input voltages above, below or equal to the output voltage. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for single cell lithium-ion/polymer or multi-cell alkaline/NiMH applications where the output voltage is within the input voltage range.

The LTC3533 features programmable Burst Mode operation, extended V_{IN} and V_{OUT} ranges down to 1.8V, and increased output current. Switching frequencies up to 2MHz are programmed with an external resistor. The Burst Mode threshold is programmed with a single resistor from the BURST pin to GND.

Other features include 1µA shutdown current, short circuit protection, programmable soft-start, current limit and thermal shutdown. The LTC3533 is housed in the thermally enhanced 14-lead (3mm × 4mm × 0.75mm) DFN package.

TYPICAL APPLICATION



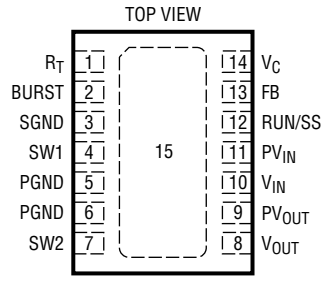


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, PV_{IN} Voltages.....–0.3 to 6V
V_{OUT}, PV_{OUT} Voltages.....–0.3 to 6V
SW1, SW2 Voltages
DC.....–0.3 to 6V
Pulsed < 100ns.....–0.3 to 7V
V_C, FB, RUN/SS, BURST Voltages.....–0.3 to 6 V
Operating Temperature Range (Note 2).... –40°C to 85°C
Maximum Junction Temperature (Note 3)..... 125°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3533#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3533EDE#PBF	LTC3533EDE#TRPBF	3533	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3533EDE	LTC3533EDE#TR	3533	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available i n 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{OUT} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Range		●	1.8		5.5	V
Output Voltage Adjust Range		●	1.8		5.25	V
Feedback Voltage		●	1.196	1.22	1.244	V
Feedback Input Current	V_{FB} = 1.22V			1	50	nA
Quiescent Current – Burst Mode Operation	V_C = 0V, V_{BURST} = 0V (Note 4)			40	50	µA
Quiescent Current – Shutdown	V_{RUN} = 0V, Not Including Switch Leakage			0.1	1	µA
Quiescent Current – Active	V_C = 0V, BURST = 3.6V (Note 4)			700	1100	µA
Input Current Limit		●	3.5	4.5		A
Peak Current Limit				7		A
Reverse Current Limit				0.5		A
NMOS Switch Leakage	Switches B and C			0.1	5	µA
PMOS Switch Leakage	Switches A and D			0.1	10	µA
NMOS Switch On Resistance	Switches B and C			60		mΩ
PMOS Switch On Resistance	Switches A and D			80		mΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{OUT} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle	Boost (% Switch C On) Buck (% Switch A On)	● ●	80 100	90		% %
Minimum Duty Cycle		●			0	%
Frequency Accuracy	R_T = 33.2k	●	0.7	1	1.3	MHz
Error Amp AVOL				80		dB
Error Amp Source Current				–20		µA
Error Amp Sink Current				250		µA
Burst Threshold				1		V
Burst Input Current	V_{BURST} = 5.5V, V_{IN} = 5.5V				8	µA
RUN/SS Threshold	When IC is Enabled When EA is at Maximum Boost Duty Cycle	●	0.4	0.7 1.3	1.4	V V
RUN/SS Input Current	V_{RUN} = 5.5V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

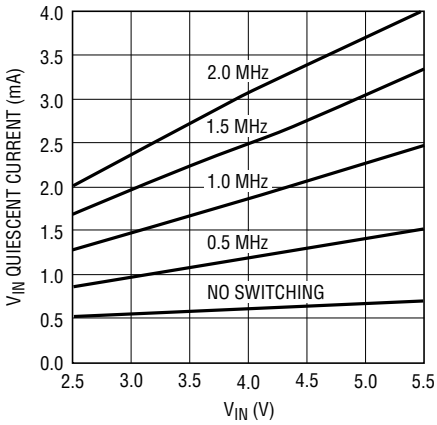
Note2: The LTC3533EDE is guaranteed to meet performance specifications from 0ºC to 85ºC. Specifications over the –40ºC to 85ºC operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: Current Measurements are performed when the outputs are not switching.

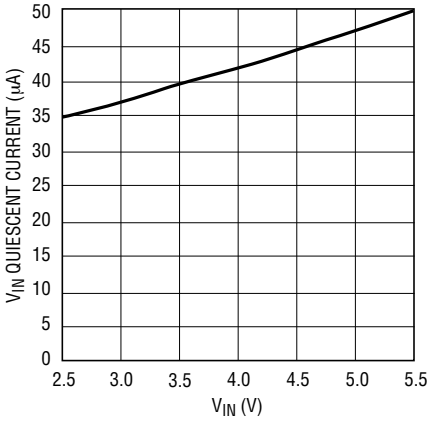
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

Quiescent Current vs V_{IN} (Fixed Frequency Mode)



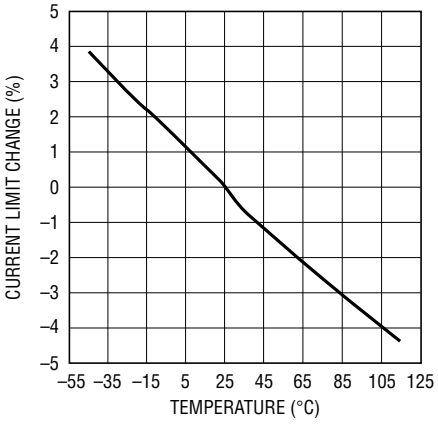
3533 G01

Burst Mode Quiescent Current



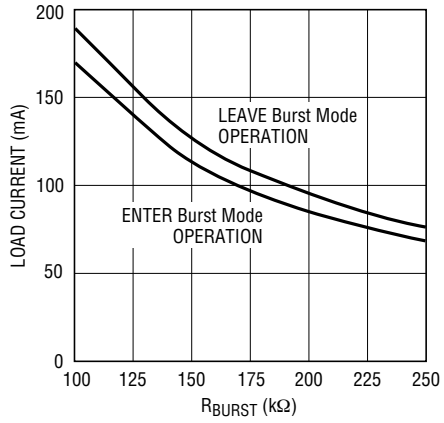
3530 G02

Peak Current Limit vs Temperature



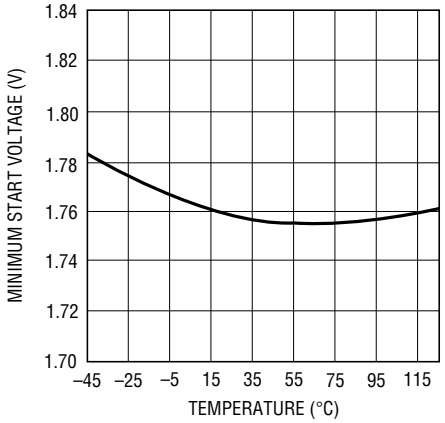
3533 G03

Automatic Burst Mode Threshold vs R_{BURST}



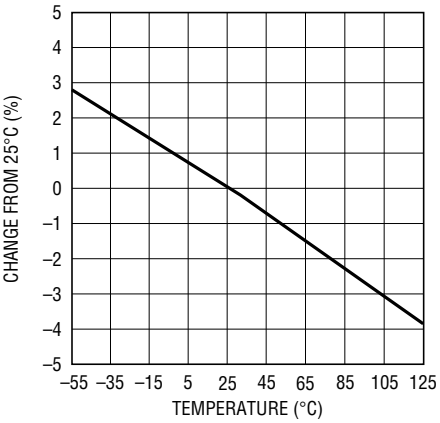
3533 G04

Minimum Start Voltage vs Temperature



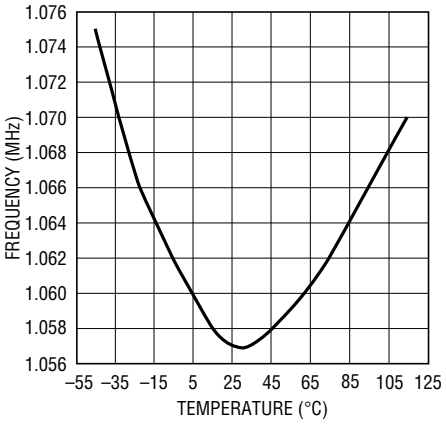
3533 G05

Average Input Current Limit vs Temperature



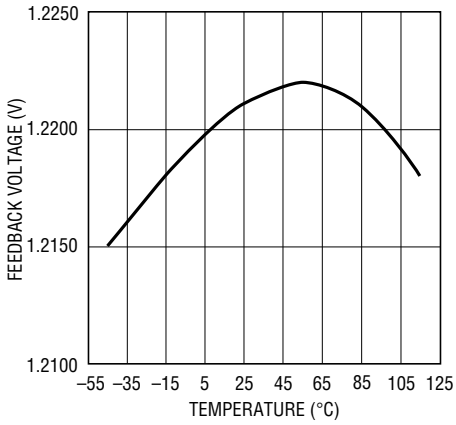
3533 G06

Frequency Change vs Temperature



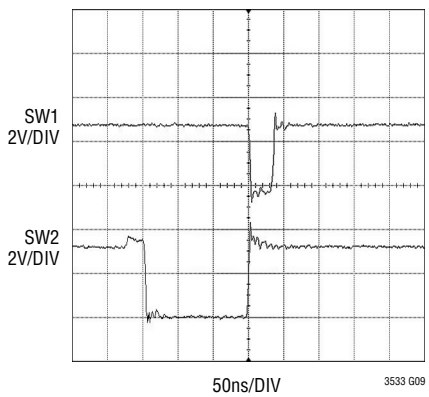
3533 G07

Feedback Voltage vs Temperature



3533 G08

Switch Pins Before Entering Boost Mode

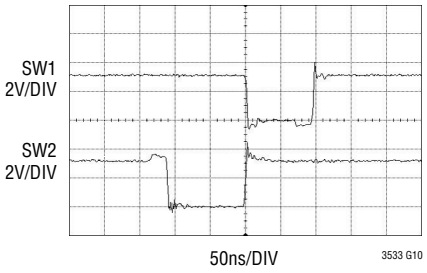


3533 G09

V_{IN} = 2.9V
V_{OUT} = 3.3V AT 500mA

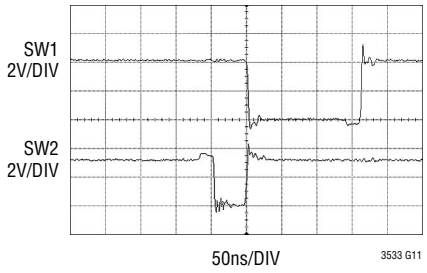
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

Switch Pins in Buck-Boost Mode



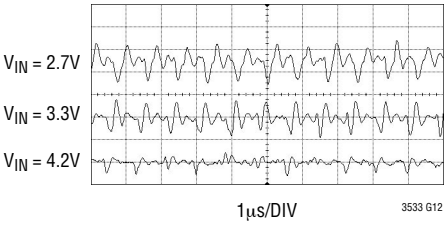
V_{IN} = 3.3V
V_{OUT} = 3.3V AT 500mA

Switch Pins Entering Buck-Boost Mode



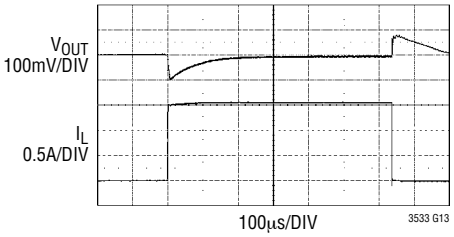
V_{IN} = 4.2V
V_{OUT} = 3.3V AT 500mA

Output Ripple at 1A Load



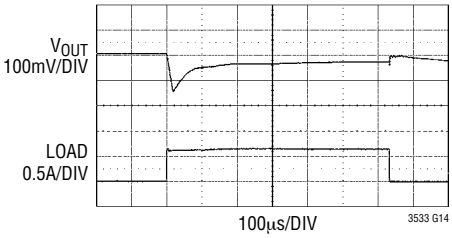
V_{OUT} = 3.3V, 20mV/DIV
C_{OUT} = 100µF CERAMIC

Load Transient Response in Fixed Frequency Mode, No Load to 1.5A



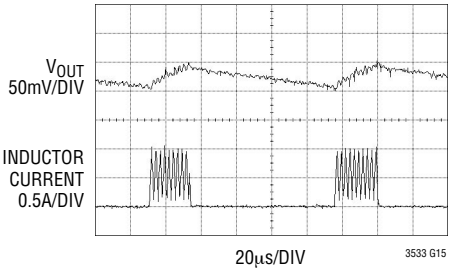
V_{IN} = 3.6V
V_{OUT} = 3.3V
C_{OUT} = 100µF X5R CERAMIC

Load Transient Response in Auto Burst Mode, No Load to 600mA



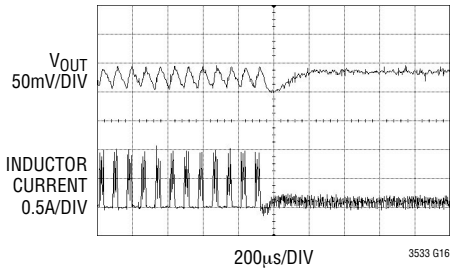
V_{IN} = 3.6V
V_{OUT} = 3.3V
C_{OUT} = 100µF X5R CERAMIC +
100µF LOW ESR TANTALUM

Burst Mode Operation



C_{OUT} = 100µF CERAMIC

Transition from Burst Mode Operation to Fixed Frequency Mode



C_{OUT} = 100µF CERAMIC

PIN FUNCTIONS

R_T (Pin 1): Programs the Frequency of the Internal Oscillator. Connect a resistor from R_T to ground.

$$f(kHz) = 33{,}170/R_T\ (k\Omega)$$

BURST (Pin 2): Used to set the Automatic Burst Mode Threshold. Connect a resistor and capacitor in parallel from this pin to ground. See the Applications Information section for component value selection. For manual control, ground the pin to force Burst Mode operation, connect to V_{IN} to force fixed frequency PWM mode.

SGND (Pin 3): Signal ground for the IC.

SW1 (Pin 4): Switch Pin where Internal Switches A and B are Connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from SW1 to ground for a moderate efficiency improvement. Minimize trace length to reduce EMI.

PGND1, PGND2 (Pins 5, 6): Power Ground for the Internal NMOS Power Switches.

SW2 (Pin 7): Switch Pin where Internal Switches C and D are Connected. An optional Schottky diode can be connected from SW2 to V_{OUT} for a moderate efficiency improvement. For applications with output voltages over 4.3V, this Schottky diode is required to ensure the SW2 pin does not exhibit excess voltage. Minimize trace length to reduce EMI.

V_{OUT} (Pin 8): Voltage Sensing Pin for PV_{OUT} and Input Supply Pin for Internal Circuitry Powered by PV_{OUT}. A filter capacitor is placed from V_{OUT} to GND. A ceramic bypass capacitor is recommended as close to the V_{OUT} and GND pins as possible.

PV_{OUT} (Pin 9): Output of the Synchronous Rectifier. A filter capacitor is placed from PV_{OUT} to PGND. A ceramic bypass capacitor is recommended as close to the PV_{OUT} and PGND pins as possible.

V_{IN} (Pin 10): Input Supply Pin. Internal V_{CC} for the IC.

PV_{IN} (Pin 11): Power V_{IN} Supply Pin. A 10µF ceramic capacitor is recommended as close to the PV_{IN} and PGND pins as possible.

RUN/SS (Pin 12): Combined Enable and Soft-Start. Applied voltage <0.4V shuts down the IC. Tie to >1.4V to enable the IC and >1.6V to ensure the error amp is not clamped from soft-start. An RC from the shutdown command signal to this pin will provide a soft-start function by limiting the rise time of V_C

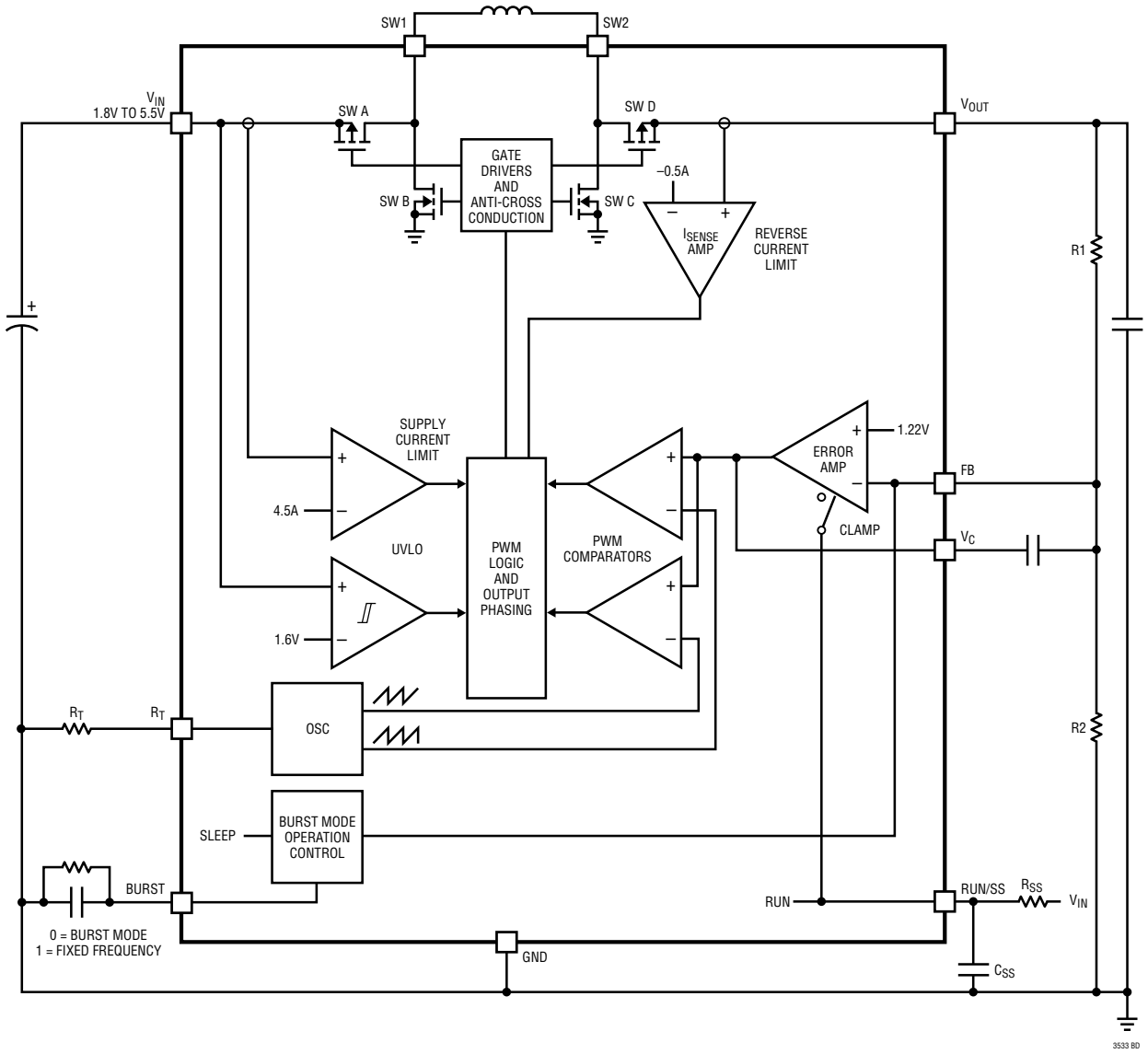
FB (Pin 13): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 1.8V to 5.25V. The feedback reference voltage is typically 1.22V.

$$V_{OUT} = 1.22 \bullet \frac{R1+R2}{R2}$$

V_C (Pin 14): Error Amp Output. An R-C network is connected from this pin to FB for loop compensation. Refer to “Closing the Feedback Loop” section for component selection guidelines. During Burst Mode operation, V_C is internally connected to a hold circuit.

Exposed Pad (Pin 15): IC Substrate Ground. This pin must be soldered to the PCB ground to provide both electrical contact and a good thermal contact to the PCB.

BLOCK DIAGRAM



OPERATION

The LTC3533 provides high efficiency, low noise power for a wide variety of handheld electronic devices. The LTC proprietary topology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amplifier output voltage on V_C determines the output duty cycle of the switches. Since V_C is a filtered signal, it provides rejection of frequencies well below the switching frequency. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. High efficiency is achieved at light loads when Burst Mode operation is entered and the LTC3533's quiescent current drops to a low 40µA.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation is programmed by an external resistor from R_T to ground, according to the following equation:

$$f(kHz) = 33{,}170/R_T(k)$$

Error Amplifier

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier (from FB to V_C) to obtain stability of the converter. For improved bandwidth, an additional RC feed-forward network can be placed across the upper feedback divider resistor. The voltage on the RUN/SS pin clamps the error amplifier output, V_C, to provide a soft-start function.

Supply Current Limits

There are two different supply current limit circuits in the LTC3533, working consecutively, each having internally fixed thresholds which vary inversely with V_{IN}.

The first circuit is a current limit amplifier, sourcing current into FB to drop the output voltage, should the peak input current exceed 4.5A typical. This method provides a closed loop means of clamping the input current. During conditions where V_{OUT} is near ground, such as during a short circuit or startup, this threshold is cut to 750mA, providing a fold-back feature. For this current limit feature to be most effective, the Thevenin resistance from FB to ground should be greater than 100k.

Should the peak input current exceed 7A typical, the second circuit, a high speed peak current limit comparator, shuts off PMOS switch A. The delay to output of this comparator is typically 50ns.

Reverse Current Limit

During fixed frequency operation, the LTC3533 operates in forced continuous conduction mode. The reverse current limit comparator monitors the inductor current from the output through switch D. Should this negative inductor current exceed 500mA typical, the LTC3533 shuts off switch D.

Four-Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, V_{IN}, V_{OUT} and GND.Figure 2 shows the regions of operation for the LTC3533 as a function of the control voltage, V_C.

Dependent on V_C's magnitude, the LTC3533 will operate in either buck, buck/boost or boost mode. The four power switches are properly phased so the transfer between operating modes is continuous, smooth and transparent to the user. When V_{IN} approaches V_{OUT} the buck/boost region is entered, where the conduction time of the four switch region is typically 150ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

OPERATION

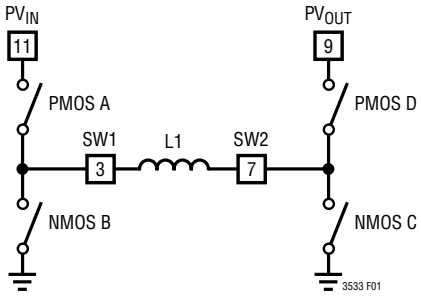


Figure 1. Simplified Diagram of Output Switches

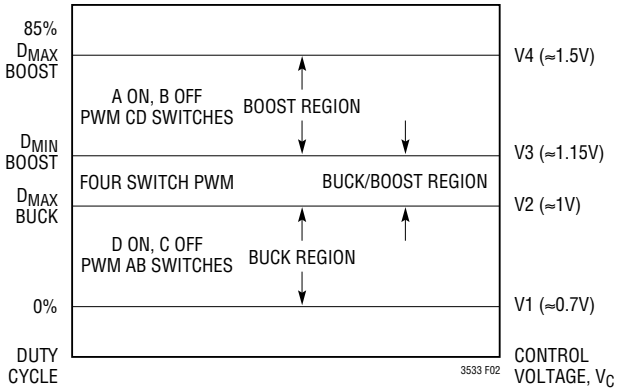


Figure 2. Switch Control vs Control Voltage, V_C

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the control voltage, V_C, is above voltage V1, switch A begins to switch. During the off time of switch A, synchronous switch B turns on for the remainder of the period. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in buck mode reaches D_{MAX_BUCK}, given by:

$$D_{MAX\_BUCK} = 100 - D4_{SW}\ \%$$

where $D4_{SW}$ = duty cycle % of the four switch range.

$$D4_{SW} = (150ns \bullet f) \bullet 100\ \%$$

where f = operating frequency, Hz.

Beyond this point the “four switch,” or buck/boost region is reached.

Buck/Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the control voltage, V_C, is above voltage V2, switch pair AD remain on for duty cycle D_{MAX_BUCK}, and switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When V_C reaches the edge of the buck/boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$. The input voltage, V_{IN}, where the four switch region begins is given by:

$$V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 150ns \bullet f)\ V$$

The point at which the four switch region ends is given by:

$$V_{IN} = \frac{V_{OUT}}{1 - (150ns \bullet f)}\ V$$

where f = operating frequency, Hz.

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the control voltage, V_C, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 90% typical and is reached when V_C is above V4.

OPERATION

BURST MODE OPERATION

Burst Mode operation reduces the LTC3533's quiescent current consumption at light loads and improves overall conversion efficiency, increasing battery life. During Burst Mode operation the LTC3533 delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the quiescent current drops to 40µA. In this mode the output ripple has a variable frequency component that depends upon load current, and will typically be about 2% peak-to-peak. Burst Mode operation ripple can be reduced slightly by using more output capacitance. Another method of reducing Burst Mode operation ripple is to place a small feed-forward capacitor across the upper resistor in the V_{OUT} feedback divider network (as in Type III compensation).

During the period where the device is delivering energy to the output, the peak switch current will rise to 900mA typical and the inductor current will terminate at zero current for each cycle. In this mode, the typical maximum average output currents are given by:

$I_{MAX(BURST)BUCK} \approx 450mA;\ V_{OUT} < V_{IN}$

$I_{MAX(BURST)BOOST} \approx 450mA \bullet (V_{IN}/V_{OUT});\ V_{OUT} > V_{IN}$

$I_{MAX(BURST)BUCK\text{-}BOOST} \approx 700mA;\ V_{OUT} \approx V_{IN}$, since the input and output are connected together for most of the cycle.

The efficiency below 1mA becomes dominated primarily by the quiescent current. The Burst Mode operation efficiency is given by:

$$Efficiency \cong \frac{\eta \bullet I_{LOAD}}{40\mu A + I_{LOAD}}$$

where η is typically 90% during Burst Mode operation

Programmable Automatic Burst Mode Operation

Burst Mode operation can be automatic or digitally controlled with a single pin. In automatic mode, the LTC3533 enters Burst Mode operation at the programmed threshold and returns to fixed frequency operation when the load demand increases. The load current at which the mode transition occurs is programmed using a single external resistor from BURST to ground, according to the following equations:

$$\text{Enter Burst Mode Operation: } I_{BURST} = \frac{17}{R_{BURST}}$$

$$\text{Exit Burst Mode Operation: } I_{BURST} = \frac{19}{R_{BURST}}$$

Where R_{BURST} is in kΩ and I_{BURST} is the load transition current in Amps. Do not use values of R_{BURST} greater than 250kΩ.

For automatic operation a filter capacitor must also be connected from BURST to ground. The equation for the minimum capacitor value is:

$$C_{BURST(MIN)} \geq \frac{C_{OUT} \bullet V_{OUT}}{60,000}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF.

In the event that a load transient causes FB to drop by more than 4% from the regulation value while in Burst Mode operation, the LTC3533 will immediately switch to fixed frequency mode and an internal pull-up will be momentarily applied to BURST, rapidly charging C_{BURST}. This prevents the IC from immediately re-entering Burst mode operation once the output achieves regulation.

OPERATION

Manual Burst Mode Operation

For manual control of Burst Mode operation, the RC network connected to BURST can be eliminated. To force fixed frequency mode, BURST should be connected to V_{IN}. To force Burst Mode operation, BURST should be grounded. When commanding Burst Mode operation manually, the circuit connected to BURST should be able to sink up to 2mA.

For optimum transient response with large dynamic loads, the operating mode should be controlled digitally by the host. By commanding fixed frequency operation prior to a sudden increase in load, output voltage droop can be minimized. Note that if the load current applied during forced Burst Mode operation (BURST pin is grounded) exceeds the current that can be supplied, the output voltage will start to droop and the LTC3533 will automatically come out of Burst Mode operation and enter fixed frequency mode, raising V_{OUT}. Once regulation is achieved, the LTC3533 will then enter Burst Mode operation once again (since the user is still commanding this by grounding BURST), and the cycle will repeat, resulting in about 4% output ripple.

Burst Mode Operation to Fixed Frequency Transient Response

In Burst Mode operation, the compensation network is not used and V_C is disconnected from the error amplifier. During long periods of Burst Mode operation, leakage currents in the external components or on the PC board could cause the compensation capacitor to charge (or discharge), which could result in a large output transient when returning to fixed frequency mode of operation, even at the same load current. To prevent this, the LTC3533 incorporates an active clamp circuit that holds the voltage on V_C at an optimal voltage during Burst Mode operation. This minimizes any output transient when returning to fixed frequency mode operation. For optimum transient response, Type 3 compensation is also recommended to broad band the control loop and roll off past the two pole response of the output LC filter. (See Closing the Feedback Loop).

Soft-Start

The soft-start function is combined with shutdown. When the RUN/SS pin is brought above 1V typical, the LTC3533 is enabled but the error amplifier duty cycle is clamped from V_C. A detailed diagram of this function is shown in Figure 3. The components R_{SS} and C_{SS} provide a slow ramping voltage on RUN/SS to provide a soft-start function. To ensure that V_C is not being clamped, RUN/SS must be raised above 1.6V.

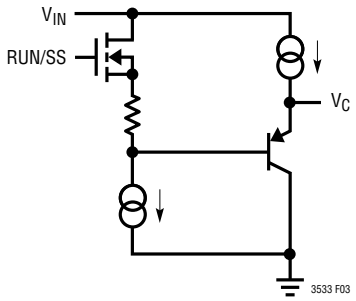


Figure 3.

APPLICATIONS INFORMATION

COMPONENT SELECTION

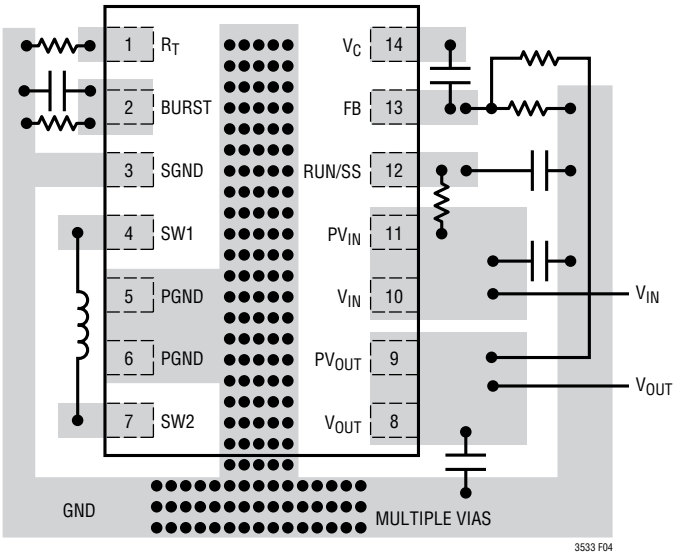


Figure 4. Recommended Component Placement. Traces Carrying High Current Should be Short and Wide. Trace Area at FB and V_C Pins are Kept Low. Lead Length to Battery Should be Kept Short. PV_{OUT} and PV_{IN} Ceramic Capacitors Close to the IC Pins.

Inductor Selection

The high frequency operation of the LTC3533 allows the use of small surface mount inductors. The inductor ripple current is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)} \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet \Delta I_L \bullet V_{OUT}} H$$

$$L_{BUCK} > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet \Delta I_L \bullet V_{IN(MAX)}} H$$

where f = switching frequency, Hz

ΔI_L = maximum allowable inductor ripple current

$V_{IN(MIN)}$ = minimum input voltage

$V_{IN(MAX)}$ = maximum input voltage

V_{OUT} = output voltage

For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 4A to 6A region. To minimize radiated noise, use a shielded inductor. See Table 1 for a suggested list of inductor suppliers.

Output Capacitor Selection

The bulk value of the output filter capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\%Ripple\_Boost = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)}) \bullet 100}{C_{OUT} \bullet V_{OUT}^2 \bullet f} \%$$

$$\%Ripple\_Buck = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet 100}{8L\ C_{OUT} \bullet V_{IN(MAX)} \bullet f^2} \%$$

where C_{OUT} = output filter capacitor

$I_{OUT(MAX)}$ = maximum output load current

The output capacitance is usually many times larger than the minimum value in order to handle the transient response

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
CoEv Magnetics	(800) 227-7040	(650) 361-2508	www.circuitprotection.com/magnetics.asp
Murata	(814) 237-1431 (800) 831-9172	(814) 238-0409	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81(3) 3607-5111	USA: (847) 956-0702 Japan: 81(3) 3607-5144	www.sumida.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
TOKO	(847) 297-0070	(847) 699-7864	www.tokoam.com

APPLICATIONS INFORMATION

requirements of the converter. As a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden or TDK ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended. See Table 2 for contact information.

Input Capacitor Selection

Since PV_{IN} is the supply voltage for the IC it is recommended to place at least a 4.7µF, low ESR ceramic bypass capacitor close to PV_{IN} and GND. It is also important to minimize any stray resistance from the converter to the battery or other power source.

Optional Schottky Diodes

Schottky diodes across the synchronous switches B and D are not required, but do provide a lower drop during the break-before-make time (typically 15ns), thus improving efficiency. Use a surface mount Schottky diode such as an MBRM120T3 or equivalent. Do not use ordinary rectifier diodes since their slow recovery times will compromise efficiency.

Output Voltage < 1.8V

The LTC3533 can operate as a buck converter with output voltages as low as 400mV. The part is specified at 1.8V minimum to allow operation without the requirement of a Schottky diode; Since synchronous switch D is powered from PV_{OUT}, and the $R_{DS(ON)}$ will increase at low output voltages, a Schottky diode is required from SW2 to V_{OUT} to provide the conduction path to the output. Note that Burst Mode operation is inhibited at output voltages below 1V typical.

Output Voltage > 4.3V

A Schottky diode from SW2 to V_{OUT} is required for output voltages over 4.3V. The diode must be located as close to the pins as possible in order to reduce the peak voltage on SW2 due to parasitic lead and trace inductances.

Input Voltage > 4.5V

For applications with input voltages above 4.5V which could exhibit an overload or short-circuit condition, a 2Ω/1nF series snubber is required between SW1 and GND. A Schottky diode from SW1 to PV_{IN} should also be added as close to the pins as possible. For the higher input voltages, V_{IN} bypassing becomes more critical. Therefore, a ceramic bypass capacitor as close to the PV_{IN} and GND pins as possible is also required.

Operating Frequency Selection

Higher operating frequencies allow the use of a smaller inductor and smaller input and output filter capacitors, thus reducing board area and component height. However, higher operating frequencies also increase the IC's total quiescent current due to the gate charge of the four switches, as given by:

Buck: $I_Q = (600e - 12 \bullet V_{IN} \bullet f)$ mA

Boost: $I_Q = [800e - 12 \bullet (V_{IN} + V_{OUT}) \bullet f]$ mA

Buck/Boost: $I_Q = [(1400e - 12 \bullet V_{IN} + 400e - 12 \bullet V_{OUT}) \bullet f]$ mA

where f = switching frequency in Hz. Therefore frequency selection is a compromise between the optimal efficiency and the smallest solution size.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com

APPLICATIONS INFORMATION

Closing the Feedback Loop

The LTC3533 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck/boost), but is usually no greater than 15. The output filter exhibits a double pole response, as given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

(in buckm ode)

$$f_{FILTER\_POLE} = \frac{V_{IN}}{2 \bullet V_{OUT} \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

(in boostm ode)

where L is in Henries and C_{OUT} is in Farads.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

A troublesome feature in boost mode is the right-half plane zero (RHP), given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} Hz$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop, but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin using Type I compensation, the loop must be crossed over a decade before the LC double pole. Referring to Figure 5, the unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{P1}} Hz$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required, providing two zeros to compensate for the double-pole response of the output filter. Referring to Figure 6, the location of the poles and zeros are given by:

$$f_{POLE1} = \frac{1}{2 \bullet \pi \bullet 10e^3 \bullet R1 \bullet C_{P1}} Hz$$

(which is a very low frequency)

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P1}} Hz$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}} Hz$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P2}} Hz$$

where resistance is in Ohms and capacitance is in Farads.

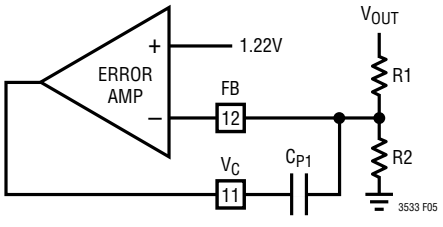


Figure 5. Error Amplifier with Type I Compensation

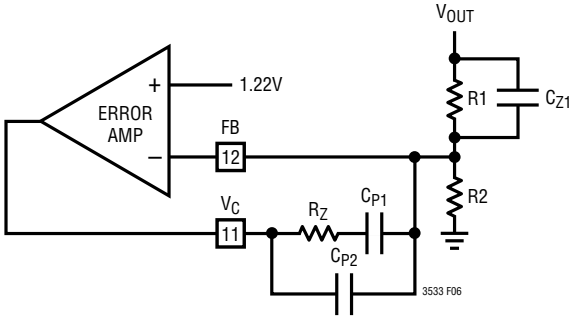
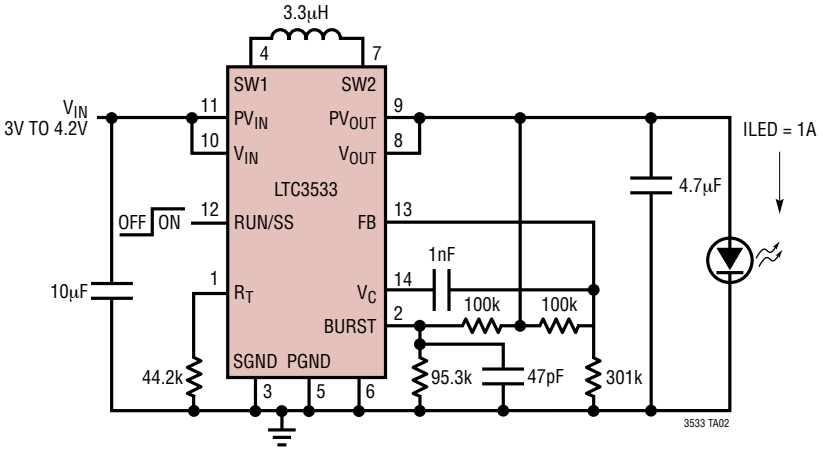


Figure 6. Error Amplifier with Type III Compensation

TYPICAL APPLICATIONS

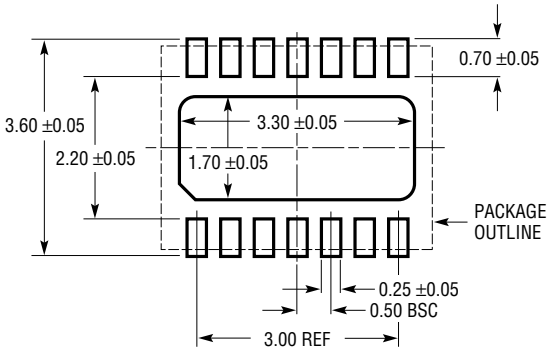
High Efficiency, High Current LED Driver



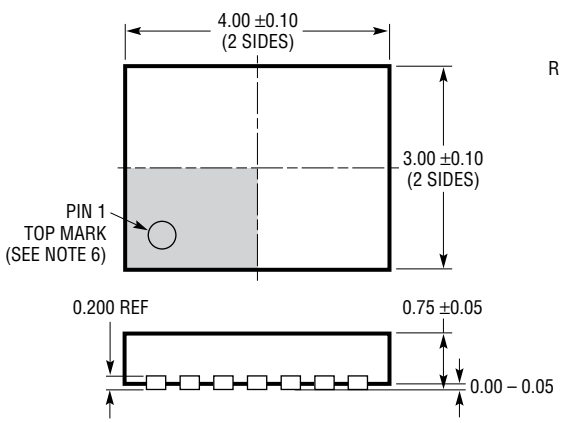
PACKAGE DESCRIPTION

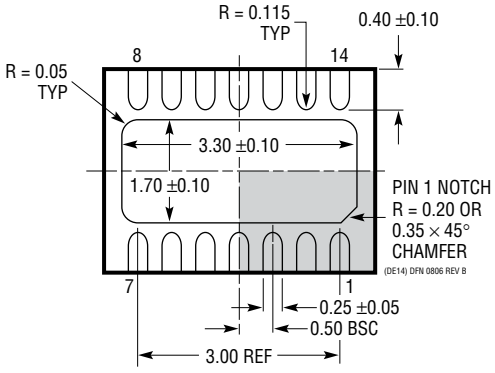
Please refer to http://www.linear.com/product/LTC3533#packaging for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

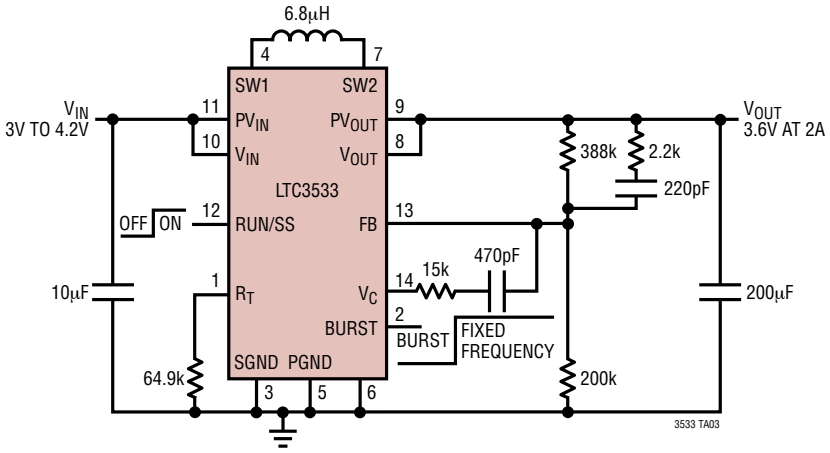
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	01/16	Corrected part number in Order Information	2
		Modified Burst Mode Operation	10
		Moved application circuit to back page	18
C	08/16	Corrected part number in Order Information	2

TYPICAL APPLICATION

1MHz Li-Ion to 3.6V at 2A, Pulsed, with Manual Mode Control



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3113	3A Low Noise Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.5V, I_Q = 300µA, I_{SD} < 1µA, 20-Pin TSSOP Package, 4mm × 5mm DFN
LTC3127	1A Buck-Boost DC/DC Converter with Programmable Input Current Limit	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 35µA, I_{SD} < 4mA, 12-Pin MSOP Package, 3mm × 3mm DFN
LTC3401/LT3402	1A/2A (I_{SW}), 3MHz Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 6V, I_Q = 38mA, I_{SD} < 1µA, MS Package
LTC3411	1.25A (I_{OUT}), 4MHz Synchronous Step-Up DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} ≤ 1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz Synchronous Step-Up DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} ≤ 1µA, TSSOP16E Package
LTC3421	3A (I_{SW}), 3MHz Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, QFN Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MAX)}$: 2.5V to 5.5V, I_Q = 25µA, I_{SD} < 1µA, MS, DFN Package
LTC3441	1.2A (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MAX)}$: 2.4V to 5.5V, I_Q = 25µA, I_{SD} < 1µA, DFN Package
LTC3442/LTC3443	1.2A (I_{OUT}), Synchronous Buck-Boost DC/DC Converters, LTC3442 (1MHz), LTC3443 (600kHz)	V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$: 2.4V to 5.25V, I_Q = 28µA, I_{SD} < 1µA, DFN Package
LTC3444	500mA (I_{OUT}), Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.7V to 5.5V, V_{OUT} = 0.5V to 5V, DFN Package, Internal Compensation
LTC3530	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 40µA, I_{SD} < 1µA, 10-Pin MSOP Package, 3mm × 3mm DFN
LTC3532	500mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.5V, I_Q = 35µA, I_{SD} < 1µA, 10-Pin MSOP Package, 3mm × 3mm DFN
LTC3536	1A (I_{OUT}) Low Noise Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.5V, I_Q = 32µA, I_{SD} < 1µA, 12-Pin MSOP Package, 3mm × 3mm DFN

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