

Dual Monolithic 300mA Synchronous Step-Down Regulator

FEATURES

- High Efficiency Dual Step-Down Outputs: Up to 96%
- 300mA Output Current per Channel at $V_{IN} = 3V$
- Automatic Low Ripple Burst Mode Operation (20mV_{p-p})
- Only 40μA Quiescent Current During Operation (Both Channels)
- 2.25MHz Constant-Frequency Operation
- 2.5V to 5.5V Input Voltage Range
- Low Dropout Operation: 100% Duty Cycle
- Internally Compensated for All Ceramic Capacitors
- Independent Internal Soft-Start for Each Channel
- Current Mode Operation for Excellent Line and Load Transient Response
- 0.6V Reference Allows Low Output Voltages
- Short-Circuit Protected
- Ultralow Shutdown Current: $I_Q < 1\mu A$
- Low Profile (0.75mm) 8-Lead 3mm × 2mm DFN Package

APPLICATIONS

- Cellular Telephones
- Digital Still Cameras
- Wireless and DSL Modems
- PDAs/Palmtop PCs
- Portable Media Players

DESCRIPTION

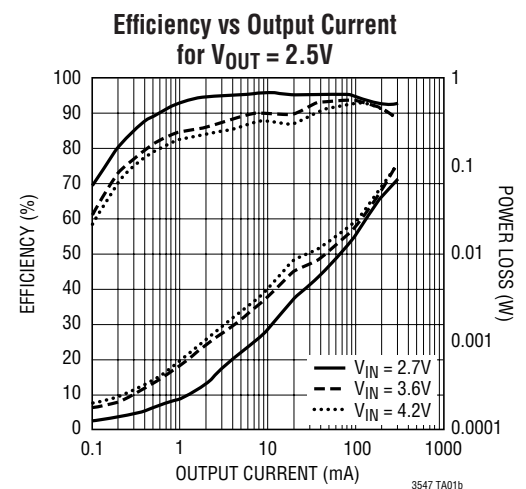
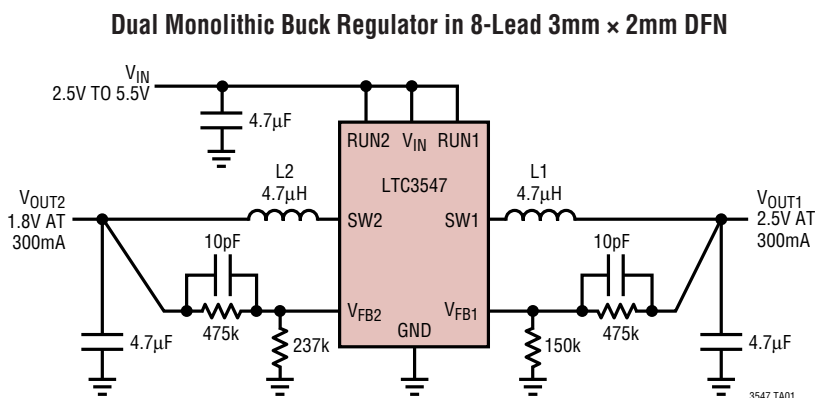
The LTC[®]3547 is a dual, 2.25MHz, constant-frequency, synchronous step-down DC/DC converter in a tiny 3mm × 2mm DFN package. 100% duty cycle provides low dropout operation, extending battery life in portable systems. Low output voltages are supported with the 0.6V feedback reference voltage. Each regulator can supply 300mA continuous output current.

The input voltage range is 2.5V to 5.5V, making it ideal for Li-Ion and USB powered applications. Supply current during operation is only 40μA and drops to < 1μA in shutdown. Automatic Burst Mode[®] operation increases efficiency at light loads, further extending battery life.

An internally set 2.25MHz switching frequency allows the use of tiny surface mount inductors and capacitors. Internal soft-start reduces inrush current during start-up. All outputs are internally compensated to work with ceramic capacitors. The LTC3547 is available in a low profile (0.75mm) 3mm × 2mm DFN package. The LTC3547 is also available in a fixed output voltage configuration, eliminating the need for the external feedback networks (see Table 2).

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TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}	-0.3V to 6V
V_{FB1}, V_{FB2}	-0.3V to $V_{IN} + 0.3V$
RUN1, RUN2	-0.3V to $V_{IN} + 0.3V$
SW1, SW2 (DC)	-0.3V to $V_{IN} + 0.3V$
P-Channel Switch Source Current (DC)	500mA
N-Channel Switch Sink Current (DC)	500mA
Peak SW Sink and Source Current (Note 5)	700mA
Ambient Operating Temperature Range ...	-40°C to 85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	-65°C to 125°C

PACKAGE/ORDER INFORMATION

<p style="text-align: center;">DDB PACKAGE 8-LEAD (3mm × 2mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 76^{\circ}C/W$ EXPOSED PAD (PIN 9) IS GND MUST BE SOLDERED TO PCB</p>	
ORDER PART NUMBER	DDB PART MARKING
LTC3547EDDB LTC3547EDDB-1	LCDP LCPC
Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/	

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_{IN} = 3.6V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{IN}	V_{IN} Operating Voltage		● 2.5		5.5	V	
V_{UV}	V_{IN} Undervoltage Lockout	V_{IN} Low to High	●	2.0	2.5	V	
I_{FB}	Feedback Pin Input Current	LTC3547, $V_{FB} = V_{FBREG}$ LTC3547-1, $V_{FB} = V_{FBREG}$	●	3	30	nA	
V_{FBREG1}	Regulated Feedback Voltage (V_{FB1})	LTC3547, $0^{\circ}C \leq T_A \leq 85^{\circ}C$ LTC3547, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ LTC3547-1, $0^{\circ}C \leq T_A \leq 85^{\circ}C$ LTC3547-1, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$	●	0.590 0.588 1.770 1.764	0.600 0.600 1.800 1.800	0.610 0.612 1.830 1.836	V
V_{FBREG2}	Regulated Feedback Voltage (V_{FB2})	LTC3547, $0^{\circ}C \leq T_A \leq 85^{\circ}C$ LTC3547, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ LTC3547-1, $0^{\circ}C \leq T_A \leq 85^{\circ}C$ LTC3547-1, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$	●	0.590 0.588 1.180 1.176	0.600 0.600 1.200 1.200	0.610 0.612 1.220 1.224	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	$V_{IN} = 2.5V$ to $5.5V$		0.3	0.5	%/V	
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	$I_{LOAD} = 0mA$ to $300mA$		0.5		%	
I_S	Input DC Supply Current Active Mode (Note 3) Sleep Mode Shutdown	$V_{FB1} = V_{FB2} = 0.95V \times V_{FBREG}$ $V_{FB1} = V_{FB2} = 1.05V \times V_{FBREG}, V_{IN} = 5.5V$ RUN1 = RUN2 = 0V, $V_{IN} = 5.5V$		450 40 0.1	700 60 1	μA μA μA	
f_{OSC}	Oscillator Frequency	$V_{FB} = 0.6V$	●	1.8	2.25	2.7	MHz
I_{LIM}	Peak Switch Current Limit Channel 1 (300mA) Channel 2 (300mA)	$V_{IN} = 3V, V_{FB} < V_{FBREG},$ Duty Cycle < 35%		400 400	550 550	mA mA	

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 3.6\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$R_{DS(ON)}$	Channel 1 (Note 4)	$V_{IN} = 3.6\text{V}$, $I_{SW} = 100\text{mA}$		0.8	1.05	Ω
	Top Switch On-Resistance					
	Bottom Switch On-Resistance	$V_{IN} = 3.6\text{V}$, $I_{SW} = 100\text{mA}$		0.75	1.05	Ω
	Channel 2 (Note 4)	$V_{IN} = 3.6\text{V}$, $I_{SW} = 100\text{mA}$		0.8	1.05	Ω
Top Switch On-Resistance						
	Bottom Switch On-Resistance	$V_{IN} = 3.6\text{V}$, $I_{SW} = 100\text{mA}$		0.75	1.05	Ω
$I_{SW(LKG)}$	Switch Leakage Current	$V_{IN} = 5\text{V}$, $V_{RUN} = 0\text{V}$		0.01	1	μA
$t_{SOFTSTART}$	Soft-Start Time	V_{FB} From 10% to 90% Full-Scale	0.450	0.650	0.850	ms
V_{RUN}	RUN Threshold High		● 0.4	1	1.2	V
I_{RUN}	RUN Leakage Current			● 0.01	1	μA
V_{BURST}	Output Ripple in Burst Mode Operation	$V_{OUT} = 1.5\text{V}$, $C_{OUT} = 4.7\mu\text{F}$		20		mV _{P-P}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3547E is guaranteed to meet specified performance from 0°C to 85°C . Specifications over the -40°C and 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

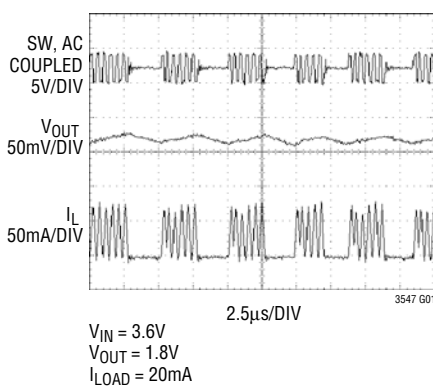
Note 4: The DFN switch on-resistance is guaranteed by correlation to wafer level measurements.

Note 5: Guaranteed by long term current density limitations.

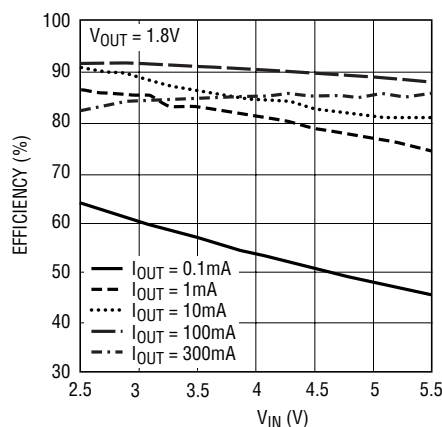
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

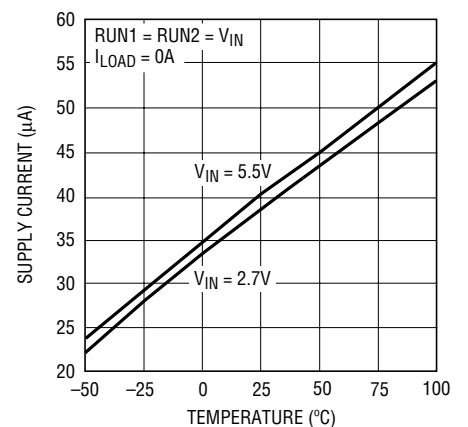
Burst Mode Operation



Efficiency vs Input Voltage

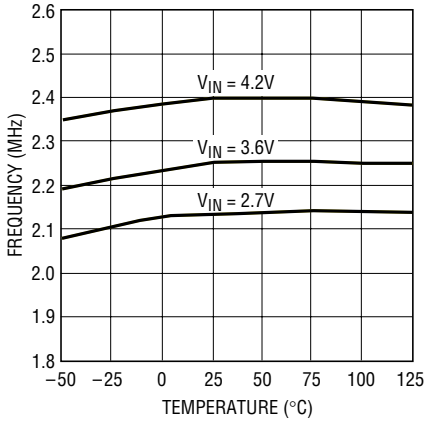


Supply Current vs Temperature



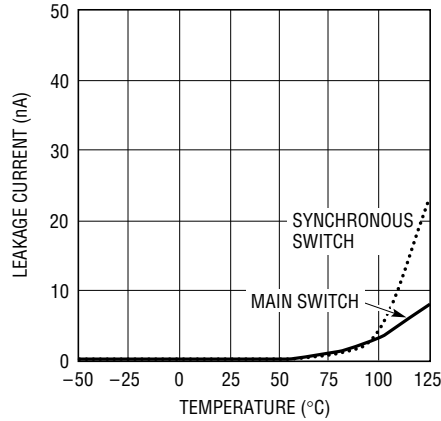
TYPICAL PERFORMANCE CHARACTERISTICS

Oscillator Frequency vs Temperature



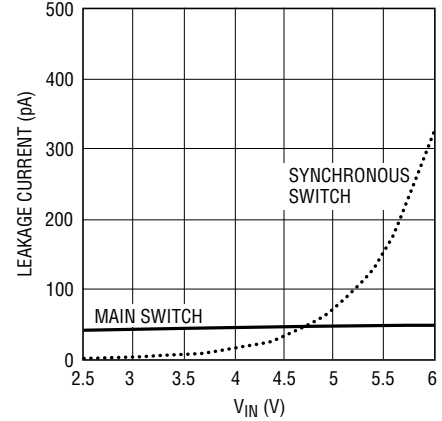
3547 G04

Switch Leakage vs Temperature



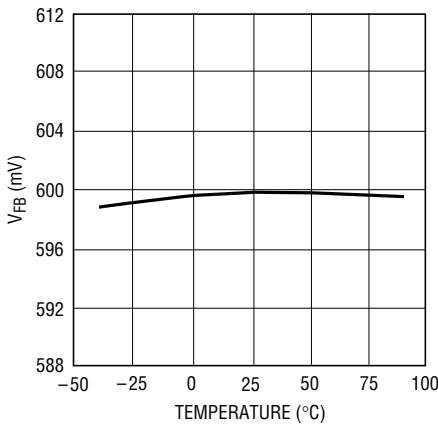
3547 G05

Switch Leakage vs Input Voltage



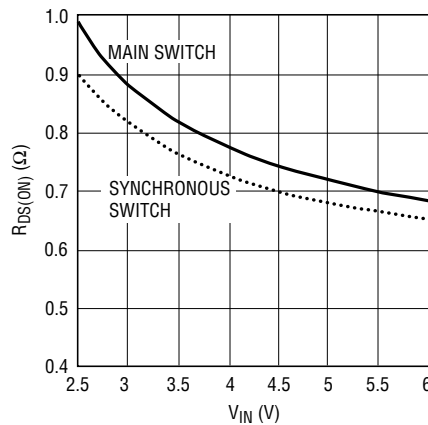
3547 G06

Reference Voltage vs Temperature



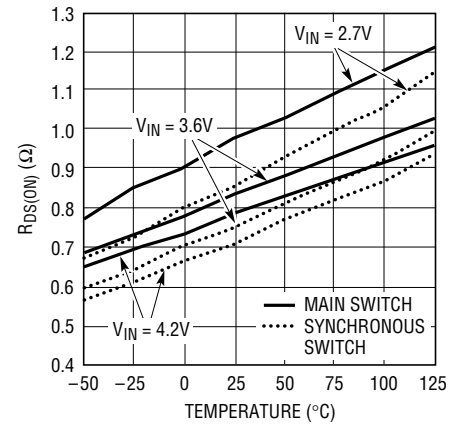
3547 G07

R_{DS(ON)} vs Input Voltage



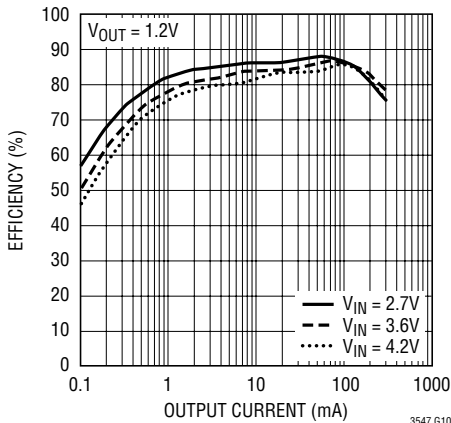
3547 G08

R_{DS(ON)} vs Temperature



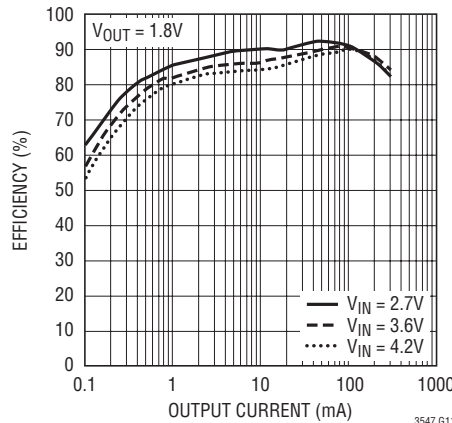
3547 G09

Efficiency vs Load Current



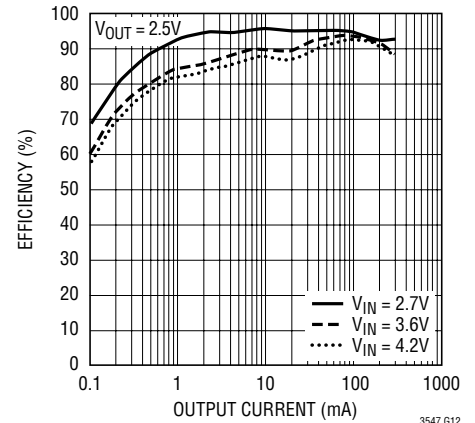
3547 G10

Efficiency vs Load Current



3547 G11

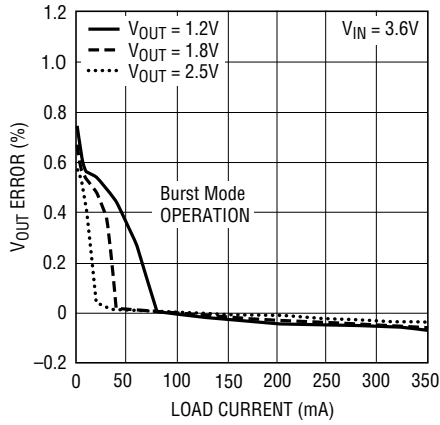
Efficiency vs Load Current



3547 G12

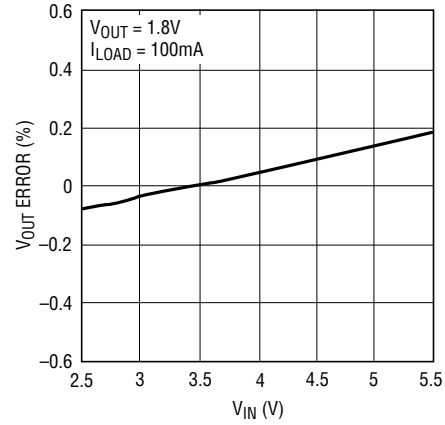
TYPICAL PERFORMANCE CHARACTERISTICS

Load Regulation



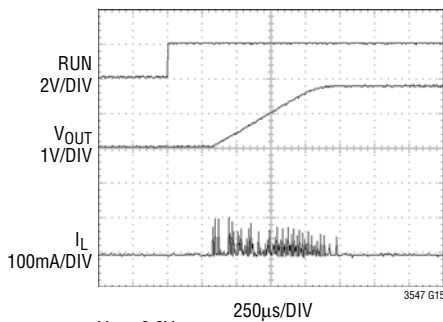
3547 G13

Line Regulation



3547 G14

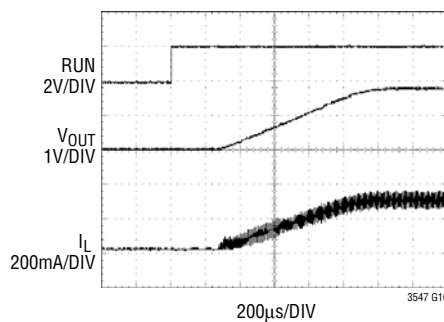
Start-Up From Shutdown



3547 G15

$V_{IN} = 3.6V$
 $V_{OUT} = 1.8V$
 $I_{LOAD} = 0A$

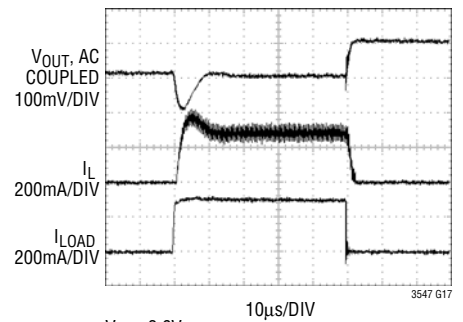
Start-Up From Shutdown



3547 G16

$V_{IN} = 3.6V$
 $V_{OUT} = 1.8V$
 $I_{LOAD} = 300mA$

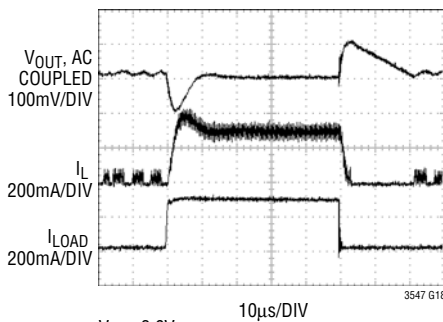
Load Step



3547 G17

$V_{IN} = 3.6V$
 $V_{OUT} = 1.8V$
 $I_{LOAD} = 0mA$ TO $300mA$

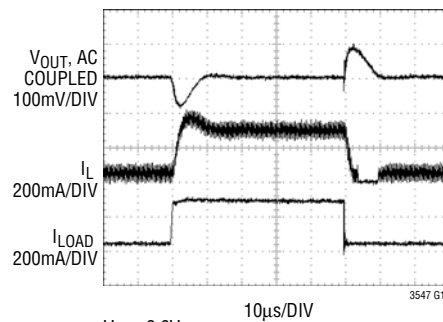
Load Step



3547 G18

$V_{IN} = 3.6V$
 $V_{OUT} = 1.8V$
 $I_{LOAD} = 20mA$ TO $300mA$

Load Step



3547 G19

$V_{IN} = 3.6V$
 $V_{OUT} = 1.8V$
 $I_{LOAD} = 50mA$ TO $300mA$

PIN FUNCTIONS

V_{FB1} (Pin 1): Regulator 1 Output Feedback. Receives the feedback voltage from the external resistor divider across the regulator 1 output. Nominal voltage for this pin is 0.6V.

RUN1 (Pin 2): Regulator 1 Enable. Forcing this pin to V_{IN} enables regulator 1, while forcing it to GND causes regulator 1 to shut down.

V_{IN} (Pin 3): Main Power Supply. Must be closely decoupled to GND.

SW1 (Pin 4): Regulator 1 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

GND (Pin 5): Ground. Connect to the (-) terminal of C_{OUT}, and the (-) terminal of C_{IN}.

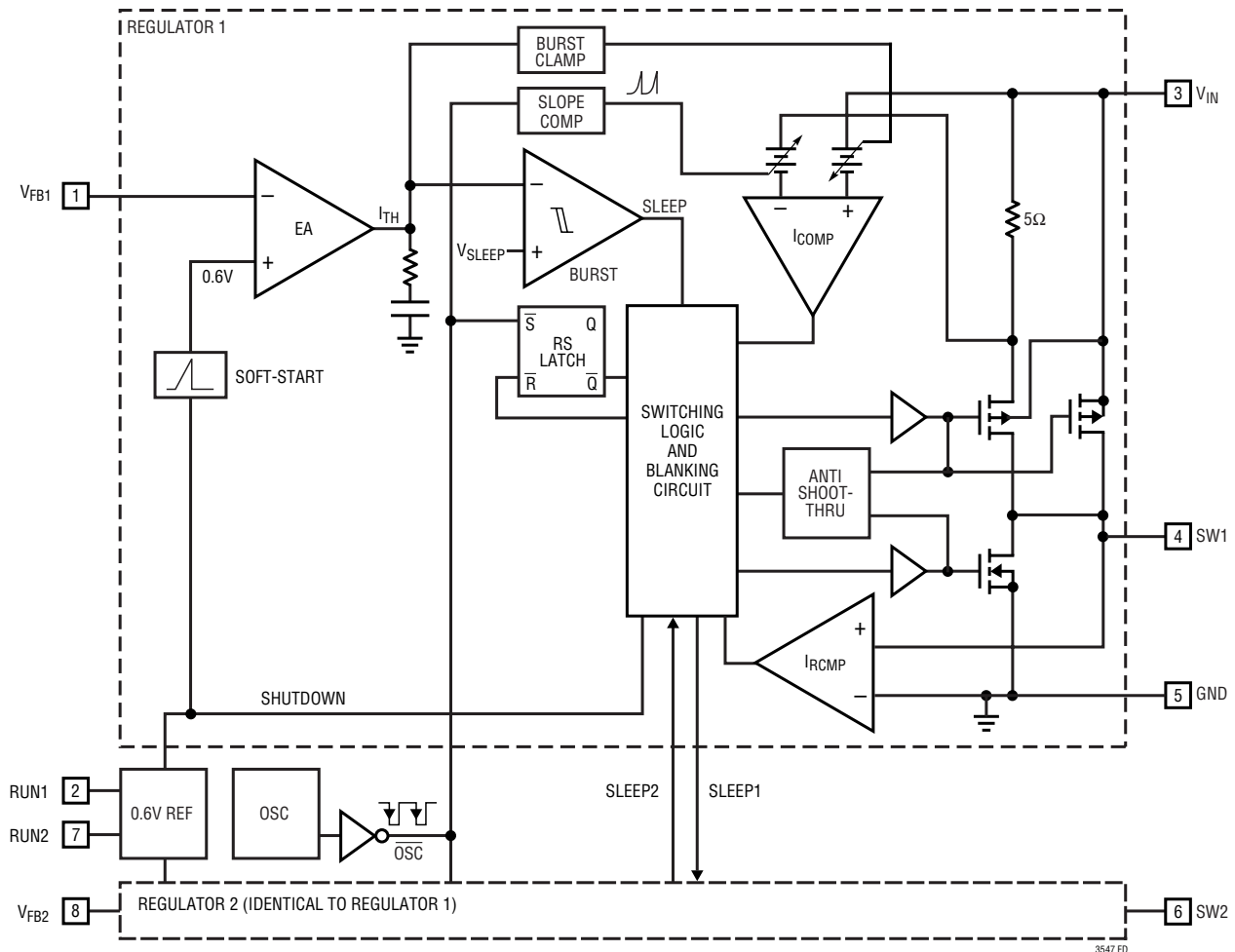
SW2 (Pin 6): Regulator 2 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

RUN2 (Pin 7): Regulator 2 Enable. Forcing this pin to V_{IN} enables regulator 2, while forcing it to GND causes regulator 2 to shut down.

V_{FB2} (Pin 8): Regulator 2 Output Feedback. Receives the feedback voltage from the external resistor divider across the regulator 2 output. Nominal voltage for this pin is 0.6V.

Exposed Pad (Pin 9): Electrically Connected to GND. Must be soldered to the PCB for optimum thermal performance.

FUNCTIONAL DIAGRAM



3547 FD

3547fa

OPERATION (Refer to Functional Diagram)

The LTC3547 uses a constant-frequency current mode architecture. The operating frequency is set at 2.25MHz. Both channels share the same clock and run in-phase.

The output voltage is set by an external resistor divider returned to the V_{FB} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and regulates the peak inductor current accordingly.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the peak inductor current (controlled by I_{TH}) is reached. The RS latch turns off the synchronous switch and energy stored in the inductor is discharged through the bottom switch (N-channel MOSFET) into the load until the next clock cycle begins, or until the inductor current begins to reverse (sensed by the I_{RCMP} comparator).

The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier. This amplifier regulates the V_{FB} pin to the internal 0.6V reference by adjusting the peak inductor current accordingly.

Burst Mode Operation

To optimize efficiency, the LTC3547 automatically switches from continuous operation to Burst Mode operation when the load current is relatively light. During Burst Mode operation, the peak inductor current (as set by I_{TH}) remains fixed at approximately 60mA and the PMOS switch operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized.

The duration of each burst event can range from a few cycles at light load to almost continuous cycling with short sleep intervals at moderate loads. During the sleep intervals, the load current is being supplied solely from the output capacitor. As the output voltage droops, the error amplifier output rises above the sleep threshold, signaling the burst comparator to trip and turn the top MOSFET on. This cycle repeats at a rate that is dependent on load demand.

Dropout Operation

When the input supply voltage decreases toward the output voltage the duty cycle increases to 100%, which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (see Typical Performance Characteristics). Therefore, the user should calculate the worst-case power dissipation when the LTC3547 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information Section).

Soft-Start

In order to minimize the inrush current on the input bypass capacitor, the LTC3547 slowly ramps up the output voltage during start-up. Whenever the RUN1 or RUN2 pin is pulled high, the corresponding output will ramp from zero to full-scale over a time period of approximately 650 μ s. This prevents the LTC3547 from having to quickly charge the output capacitor and thus supplying an excessive amount of instantaneous current.

Short-Circuit Protection

When either regulator output is shorted to ground, the corresponding internal N-channel switch is forced on for a longer time period for each cycle in order to allow the inductor to discharge, thus preventing current runaway. This technique has the effect of decreasing switching frequency. Once the short is removed, normal operation resumes and the regulator output will return to its nominal voltage.

APPLICATIONS INFORMATION

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN} . To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad (2)$$

Where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1 μ F to 1 μ F ceramic capacitor is also recommended on V_{IN} for high frequency decoupling when not using an all-ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (3)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

If tantalum capacitors are used, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3547 control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN} . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} , large enough to damage the part. For more information, see Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

APPLICATIONS INFORMATION

Setting the Output Voltage

The LTC3547 regulates the V_{FB1} and V_{FB2} pins to 0.6V during regulation. Thus, the output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V \left(1 + \frac{R2}{R1} \right) \quad (4)$$

Keeping the current small ($< 5\mu A$) in these resistors maximizes efficiency, but making it too small may allow stray capacitance to cause noise problems or reduce the phase margin of the error amp loop.

To improve the frequency response of the main control loop, a feedback capacitor (C_F) may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Fixed output versions of the LTC3547 (e.g. LTC3547-1) include an internal resistive divider, eliminating the need for external resistors. The resistor divider is chosen such that the V_{FB} input current is $3\mu A$. For these versions the V_{FB} pin should be connected directly to V_{OUT} . Table 2 lists the fixed output voltages available for the LTC3547-1.

Table 2. Fixed Output Voltage Versions

PART NUMBER	V_{OUT1}	V_{OUT2}
LTC3547	Adjustable	Adjustable
LTC3547-1	1.8V	1.2V

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When

a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \cdot ESR$, where ESR is the effective series resistance of C_{OUT} . ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used to determine the phase margin. In addition, feedback capacitors (C_{F1} and C_{F2}) can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large ($> 1\mu F$) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT} , causing a rapid drop in V_{OUT} . No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

APPLICATIONS INFORMATION

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four sources usually account for the losses in LTC3547 circuits: 1) V_{IN} quiescent current, 2) switching losses, 3) I^2R losses, 4) other system losses.

- 1) The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN} , even at no load.
- 2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and

bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

- 3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW} , and external inductor, R_L . In continuous mode, the average output current flows through inductor L, but is “chopped” between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP}) \cdot (DC) + (R_{DS(ON)BOT}) \cdot (1 - DC) \quad (5)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2 \cdot (R_{SW} + R_L)$$

- 4) Other “hidden” losses, such as copper trace and internal battery resistances, can account for additional efficiency degradations in portable systems. It is very important to include these “system” level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses, including diode conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

APPLICATIONS INFORMATION

Thermal Considerations

In a majority of applications, the LTC3547 does not dissipate much heat due to its high efficiency. In the unlikely event that the junction temperature somehow reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

The goal of the following thermal analysis is to determine whether the power dissipated causes enough temperature rise to exceed the maximum junction temperature (125°C) of the part. The temperature rise is given by:

$$T_{\text{RISE}} = P_D \cdot \theta_{\text{JA}} \quad (6)$$

Where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J , is given by:

$$T_J = T_{\text{RISE}} + T_{\text{AMBIENT}} \quad (7)$$

As a worst-case example, consider the case when the LTC3547 is in dropout on both channels at an input voltage of 2.7V with a load current of 300mA and an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{\text{DS(ON)}}$ of the main switch is 0.9Ω. Therefore, power dissipated by each channel is:

$$P_D = I_{\text{OUT}}^2 \cdot R_{\text{DS(ON)}} = 81\text{mW}$$

Given that the thermal resistance of a properly soldered DFN package is approximately 76°C/W, the junction temperature of an LTC3547 device operating in a 70°C ambient temperature is approximately:

$$T_J = (2 \cdot 0.081\text{W} \cdot 76\text{°C/W}) + 70\text{°C} = 82.3\text{°C}$$

which is well below the absolute maximum junction temperature of 125°C.

PC Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3547. These items are also illustrated graphically in the layout diagrams of Figures 2 and 3. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 3) and GND (Pin 5) as closely as possible? This capacitor provides the AC current of the internal power MOSFETs and their drivers.
2. Are the respective C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN} .
3. The resistor divider, R1 and R2, must be connected between the (+) plate of $C_{\text{OUT}1}$ and a ground sense line terminated near GND (Pin 5). The feedback signals $V_{\text{FB}1}$ and $V_{\text{FB}2}$ should be routed away from noisy components and traces, such as the SW lines (Pins 4 and 6), and their trace length should be minimized.
4. Keep sensitive components away from the SW pins if possible. The input capacitor C_{IN} and the resistors R1, R2, R3 and R4 should be routed away from the SW traces and the inductors.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at a single point. These ground traces should not share the high current path of C_{IN} or C_{OUT} .
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.

APPLICATIONS INFORMATION

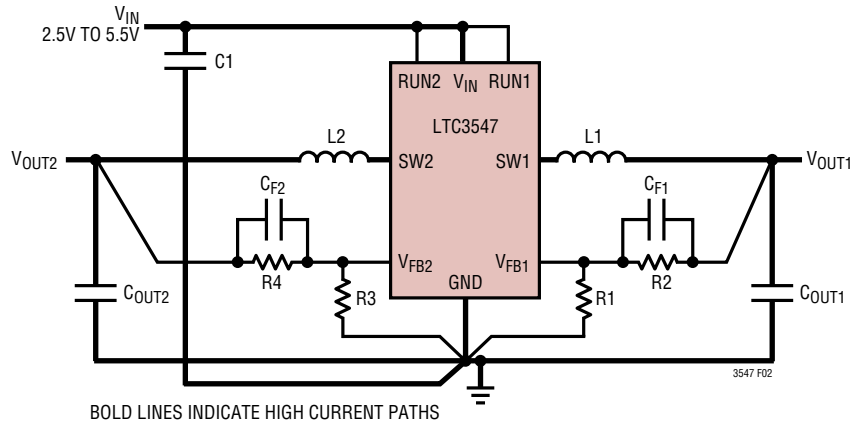


Figure 2. LTC3547 Layout Diagram (See Board Layout Checklist)

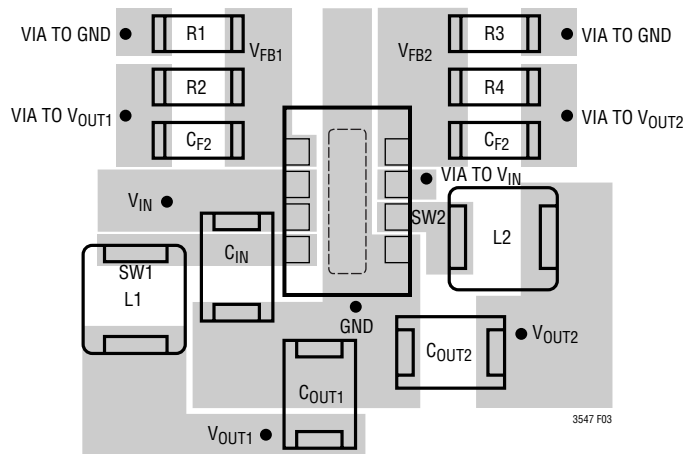


Figure 3. LTC3547 Suggested Layout

APPLICATIONS INFORMATION

Design Example

As a design example, consider using the LTC3547 in a portable application with a Li-Ion battery. The battery provides a V_{IN} ranging from 2.8V to 4.2V. The load on each channel requires a maximum of 300mA in active mode and 2mA in standby mode. The output voltages are $V_{OUT1} = 2.5V$ and $V_{OUT2} = 1.8V$.

Start with channel 1. First, calculate the inductor value for about 40% ripple current (120mA in this example) at maximum V_{IN} . Using a derivation of Equation 1:

$$L1 = \frac{2.5V}{2.25MHz \cdot (120mA)} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 3.75\mu H$$

For the inductor, use the closest standard value of 4.7 μH . A 4.7 μF capacitor should be more than sufficient for this output capacitor. As for the input capacitor, a typical value of $C_{IN} = 4.7\mu F$ should suffice, as the source impedance of a Li-Ion battery is very low.

The feedback resistors program the output voltage. To maintain high efficiency at light loads, the current in these resistors should be kept small. Choosing 2 μA with the 0.6V feedback voltage makes $R1 \sim 300k$. A close standard 1% resistor is 280k. Using Equation 4:

$$R2 = \left(\frac{V_{OUT}}{0.6} - 1\right) \cdot R1 = 887k$$

An optional 10pF feedback capacity (C_{F1}) may be used to improve transient response.

Using the same analysis for channel 2 ($V_{OUT2} = 1.8V$), the results are:

$$L2 = 3.81\mu H$$

$$R3 = 280k$$

$$R4 = 560k$$

Figure 4 shows the complete schematic for this example, along with the efficiency curve and transient response.

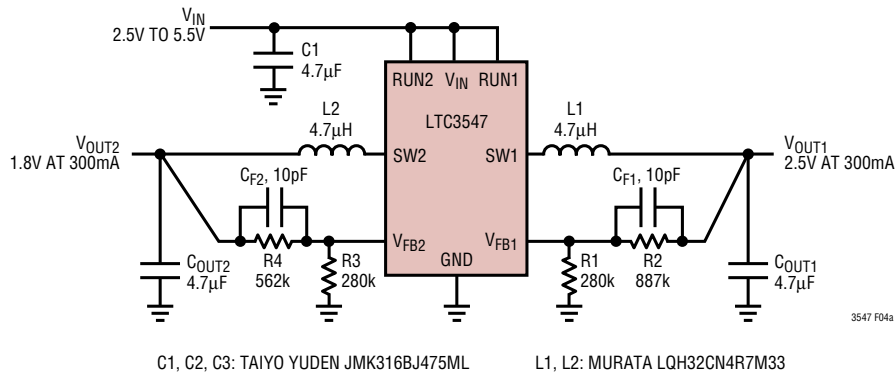


Figure 4a. Design Example Circuit

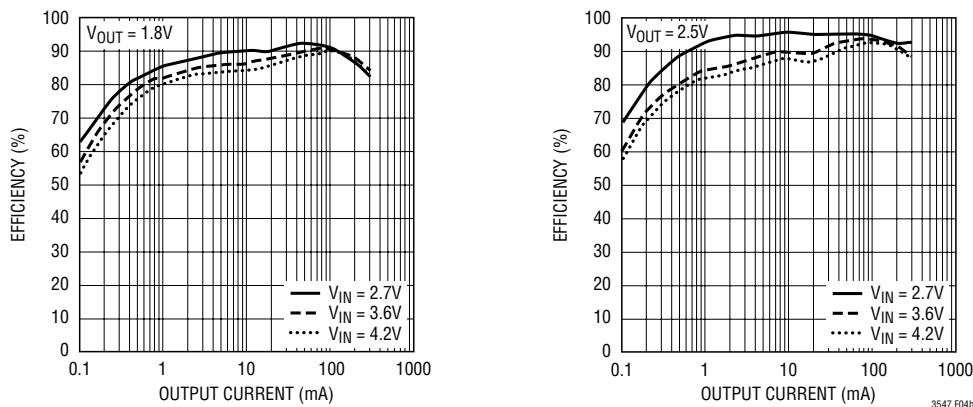


Figure 4b. Efficiency vs Output Current

APPLICATIONS INFORMATION

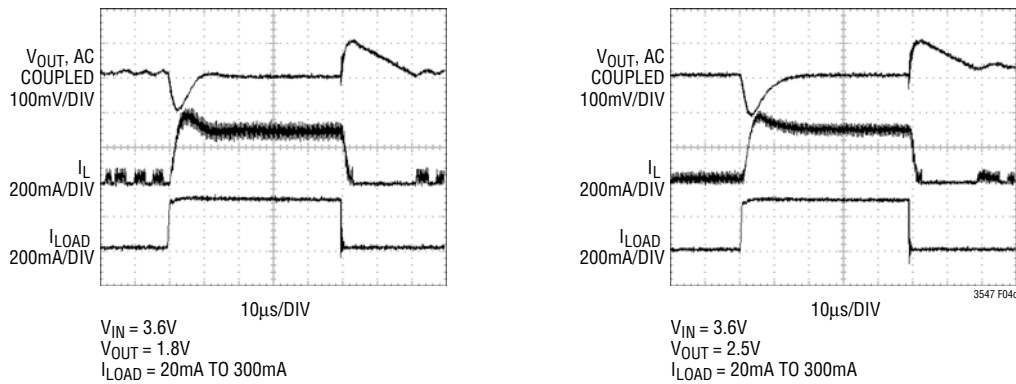
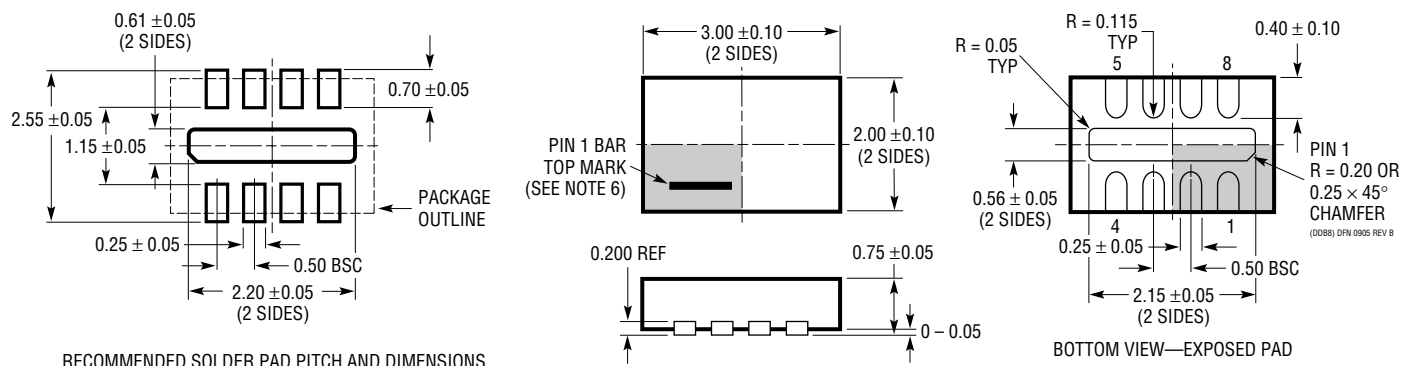


Figure 4c. Transient Response

PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
 (Reference LTC DWG # 05-08-1702 Rev B)

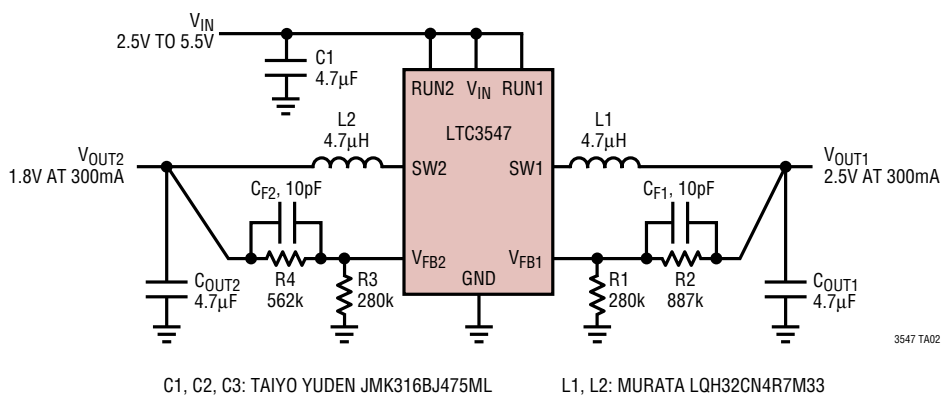


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

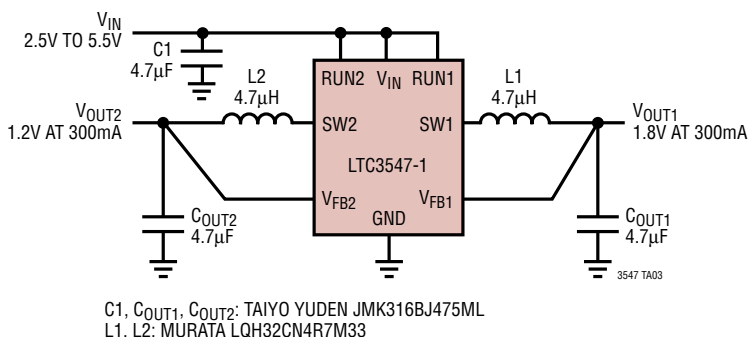
- NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Dual 300mA Buck Converter



1.8V/1.2V Dual 300mA Buck Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN} : 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA (I_{OUT}), 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, DFN Packages
LTC3409	600mA (I_{OUT}), 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN} : 1.6V to 5.5V, V_{OUT} = 0.6V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LTC3410/LTC3410B	300mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70 Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS10, DFN Packages
LTC3531/LTC3531-3/ LTC3531-3.3	200mA (I_{OUT}), 1.5MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} : 1.8V to 5.5V, V_{OUT} : 2V to 5V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT, DFN Packages
LTC3532	500mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} : 2.4V to 5.5V, V_{OUT} : 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, MS10, DFN Packages
LTC3548/LTC3548-1/ LTC3548-2	Dual 400mA and 800mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, DFN Packages

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