

# Single-Phase, High Efficiency DC/DC Controller for Intel Mobile CPUs

## FEATURES

- **Wide Input Voltage Range: 4V to 30V**
- **±1% Output Voltage Accuracy**
- **6-Bit IMVP-IV VID Code:  $V_{OUT} = 0.7V$  to  $1.708V$**
- **Intel Compatible Power Saving Mode (PSIB)**
- **Power Good Output with Adaptive Masking**
- **Lossless Voltage Positioning**
- **Resistor Programmable  $V_{OUT}$  at Boot-Up and Deeper Sleep State**
  - Resistor Programmable Deep Sleep Offset
  - Programmable Fixed Frequency: 210kHz to 550kHz
  - Adjustable Soft-Start Current Ramping
  - Foldback Output Current Limit
  - Short-Circuit Shutdown Timer with Defeat Option
  - Overvoltage Protection
- Available in 32-Lead 5mm × 5mm × 0.8mm (Profile) QFN Package

## APPLICATIONS

- Mobile and Desktop Computers
- Internet Servers

## DESCRIPTION

The LTC<sup>®</sup>3734 is a single-phase synchronous step-down switching regulator controller that drives all N-channel power MOSFETs in a constant frequency architecture. The output voltage is programmable by six VID bits during normal operation and by external resistors during initial boot-up and deeper sleep state. The LTC3734 drives its output stage at frequencies up to 550kHz. Powerful on-chip gate drivers eliminate the need for external gate driver ICs, thus simplifying the design.

An Intel compatible PSIB input is provided to select between two modes of operation. Fully enhanced synchronous mode achieves a very small output ripple and very fast transient response while power saving mode realizes very high efficiency. OPTI-LOOP<sup>®</sup> compensation allows the transient response to be optimized for a wide range of output capacitance and ESR values.

The LTC3734 is available in a small 5mm × 5mm QFN package. For 2-phase applications refer to the LTC3735.

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## TYPICAL APPLICATION

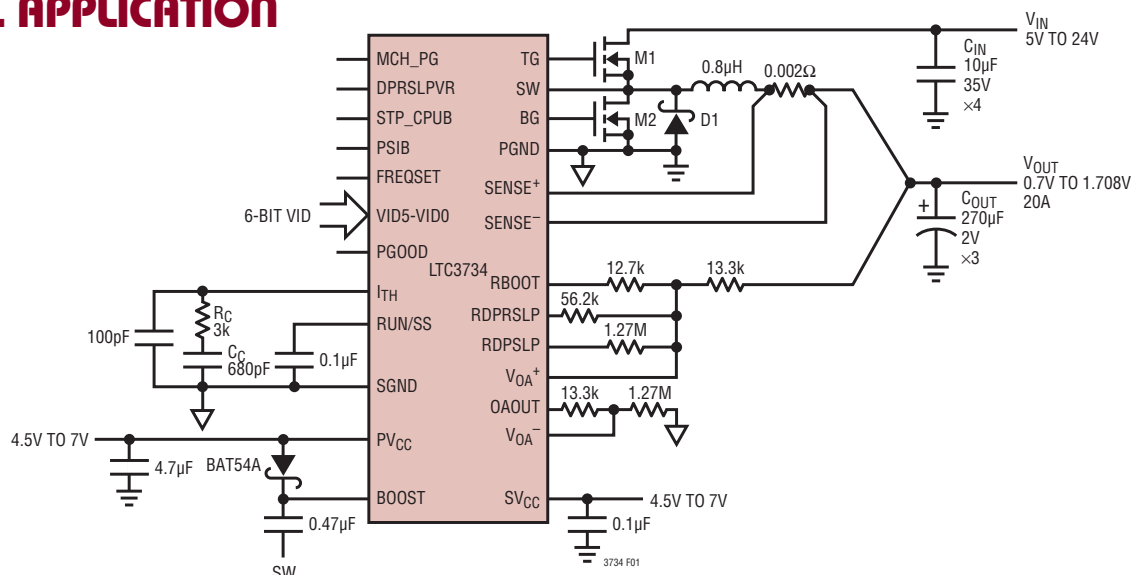


Figure 1. High Current Step-Down Converter

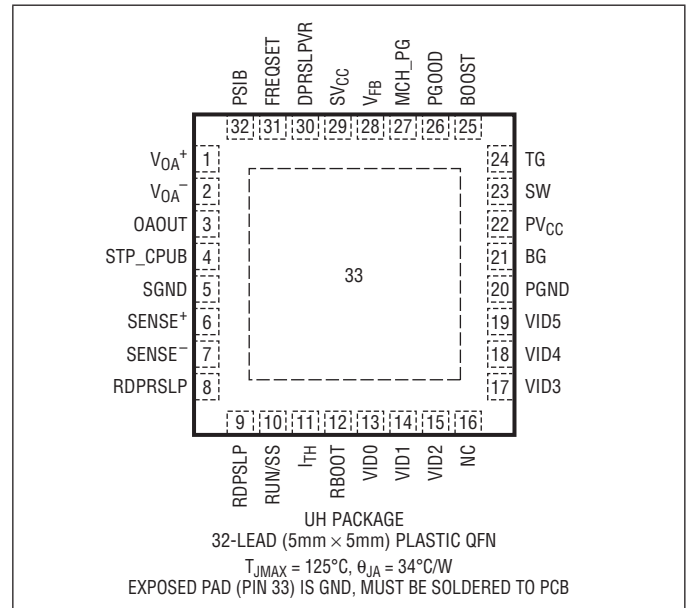
# LTC3734

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ( $PV_{CC}$ , $SV_{CC}$ )	7V to -0.3V
Topside Driver Voltages (BOOST)	38V to -0.3V
Switch Voltage (SW)	32V to -5V
Boosted Driver Voltages (BOOST-SW)	7V to -0.3V
DPRSLPVR, STP_C PUB, MCH_PG, PGOOD, RDPRSLP, RDPSLP, RBOOT Voltages	5V to -0.3V
RUN/SS, FREQSET, PSIB Voltages	7V to -0.3V
VID0-VID5 Voltages	5V to -0.3V
$V_{FB}$ Voltage	2V to -0.3V
$V_{OA}^+$ , $V_{OA}^-$ Voltage	3.6V to -0.3V
Peak Gate Drive Current <math><1\mu s</math> (TG, BG)	5A
Operating Ambient Temperature Range (Note 2)	-40°C to 85°C
Junction Temperature (Note 3)	125°C
Storage Temperature Range	-65°C to 125°C
Reflow Peak Body Temperature	245°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3734EUH#PBF	LTC3734EUH#TRPBF	3734	32-Lead Plastic (5mm x 5mm) QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{PVCC} = V_{SVCC} = 5\text{V}$ ,  $V_{RUN/SS} = 5\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Main Control Loop</b>						
Reference	Regulated Feedback Voltage	$I_{TH}$ Voltage = 0.5V; Measured at $V_{FB}$ (Note 4)		0.600		V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	$I_{TH}$ Voltage = Max; $V_{CM} = 1.7\text{V}$	● 59	72	85	mV
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, $\Delta I_{TH}$ Voltage: 1.2V to 0.7V Measured in Servo Loop, $\Delta I_{TH}$ Voltage: 1.2V to 2V	●	0.1	0.5	%
			●	-0.1	-0.5	%
$V_{REFLNREG}$	Reference Voltage Line Regulation	$V_{PVCC} = V_{SVCC} = 4.5\text{V to }7\text{V}$		0.02	0.1	%/V
$V_{PSIB}$	Forced Continuous Threshold		0.57	0.6	0.63	V
$I_{PSIB}$	Forced Continuous Current	$V_{PSIB} = 0\text{V}$		-0.5	-1	$\mu\text{A}$
$V_{OVL}$	Output Overvoltage Threshold	Measured with Respect to $V_{FB} = 0.6\text{V}$	0.64	0.66	0.68	V
$g_m$	Transconductance Amplifier $g_m$	$I_{TH} = 1.2\text{V}$ , Sink/Source 25 $\mu\text{A}$ (Note 4)	● 4.5	6	7.5	mmho
$g_{mOL}$	Transconductance Amplifier Gain	$I_{TH} = 1.2\text{V}$ , ( $g_m \cdot Z_L$ ; No Ext Load) (Note 4)		3		V/mV
$V_{ACTIVE}$	Output Voltage in Active Mode	VID = 010110, $I_{TH} = 0.5\text{V}$ (0°C - 85°C) VID = 010110, $I_{TH} = 0.5\text{V}$ (Note 2)	● 1.342	1.356	1.370	V
			● 1.336	1.356	1.376	V

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## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_Q$	Input DC Supply Current Normal Mode Shutdown	(Note 5)		2	3	mA
		$V_{RUN/SS} = 0\text{V}$		20	100	$\mu\text{A}$
UVR	Undervoltage RUN/SS Reset	$V_{CC}$ Lowered Until the RUN/SS Pin is Pulled Low	3.2	3.7	4.2	V
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS} = 1.9\text{V}$	-2.3	-1.5	-0.8	$\mu\text{A}$
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising	1.0	1.5	1.9	V
$V_{RUN/SSARM}$	RUN/SS Pin Latchoff Arming	$V_{RUN/SS}$ Rising from 3V		3.9		V
$V_{RUN/SSLO}$	RUN/SS Pin Latchoff Threshold	$V_{RUN/SS}$ Ramping Negative		3.2		V
$I_{SCL}$	RUN/SS Discharge Current	Soft Short Condition $V_{FB} = 0.375\text{V}$ , $V_{RUN/SS} = 4.5\text{V}$	-5	-1.5		$\mu\text{A}$
$I_{SDLHO}$	Shutdown Latch Disable Current	$V_{FB} = 0.375\text{V}$ , $V_{RUN/SS} = 4.5\text{V}$		1.5	5	$\mu\text{A}$
$I_{SENSE}$	Total Sense Pins Source Current	$V_{SENSE^-} = V_{SENSE^+} = 0\text{V}$	-85	-60		$\mu\text{A}$
DF <sub>MAX</sub>	Maximum Duty Factor	In Dropout	95	98.5		%
TG $t_r$ TG $t_f$	Top Gate Transition Time: Rise Time Fall Time	(Note 6) $C_{LOAD} = 3300\text{pF}$ $C_{LOAD} = 3300\text{pF}$		30	90	ns
				40	90	ns
BG $t_r$ BG $t_f$	Bottom Gate Transition Time: Rise Time Fall Time	(Note 6) $C_{LOAD} = 3300\text{pF}$ $C_{LOAD} = 3300\text{pF}$		60	90	ns
				50	90	ns
TG/BG $t_{1D}$	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	$C_{LOAD} = 3300\text{pF}$ (Note 6)		50		ns
BG/TG $t_{2D}$	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	$C_{LOAD} = 3300\text{pF}$ (Note 6)		60		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 7)		100		ns
<b>VID Parameters</b>						
$R_{ATTEN}$	VID Top Resistance			5.33		$\text{k}\Omega$
ATTEN <sub>ERR</sub>	Resistive Divider Error	(Note 8)	● -0.25		0.25	%
VID <sub>THLOW</sub>	VID0 to VID5 Logic Threshold Low				0.3	V
VID <sub>THHIGH</sub>	VID0 to VID5 Logic Threshold High		0.7			V
VID <sub>LEAK</sub>	VID0 to VID5 Leakage				$\pm 1$	$\mu\text{A}$
<b>Oscillator</b>						
$I_{FREQSET}$	FREQSET Input Current	$V_{FREQSET} = 0\text{V}$		-2	-1	$\mu\text{A}$
$f_{NOM}$	Nominal Frequency	$V_{FREQSET} = 1.2\text{V}$	320	355	390	kHz
$f_{LOW}$	Lowest Frequency	$V_{FREQSET} = 0\text{V}$	190	210	240	kHz
$f_{HIGH}$	Highest Frequency	$V_{FREQSET} \geq 2.4\text{V}$	490	550	610	kHz
<b>PGOOD Output</b>						
$V_{PGL}$	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$		0.1	0.3	V
$I_{PGOOD}$	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$			$\pm 1$	$\mu\text{A}$
$V_{PG}$	PGOOD Trip Level	$V_{FB}$ with Respect to Set Output Voltage $V_{FB}$ Ramping Negative $V_{FB}$ Ramping Positive	-7	-10	-13	%
			7	10	13	%
$t_{MASK}$	PGOOD Mask Timer		100	110	120	$\mu\text{s}$
$t_{DELAY}$	MCH_PG Delay Time			15		cycles

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Operational Amp</b>						
$I_B$	Input Bias Current			15	200	nA
$V_{OS}$	Input Offset Voltage Magnitude	$V_{OA^+} = V_{OA^-} = 1.2\text{V}$ , $I_{OUT} = 1\text{mA}$		0.8	5	mV
CM	Common Mode Input Voltage Range		0		$PV_{CC} - 1.4$	V
CMRR	Common Mode Rejection Ratio	$I_{OUT} = 1\text{mA}$	46	70		dB
$I_{CL}$	Output Source Current		10	35		mA
$A_{VOL}$	Open-Loop DC Gain	$I_{OUT} = 1\text{mA}$		30		V/mV
GBP	Gain-Bandwidth Product	$I_{OUT} = 1\text{mA}$		2		MHz
SR	Slew Rate	$R_L = 2\text{k}$		5		V/ $\mu\text{s}$
$V_{O(MAX)}$	Maximum High Output Voltage	$I_{OUT} = 1\text{mA}$	$PV_{CC} - 1.2$	$PV_{CC} - 0.9$		V

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3734E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formula:

$$T_{J(LTC3734EUH)} = T_A + (P_D \cdot 34^\circ\text{C/W})$$

**Note 4:** The LTC3734 is tested in a feedback loop that servos  $V_{ITH}$  to a specified voltage and measures the resultant  $V_{FB}$ .

**Note 5:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

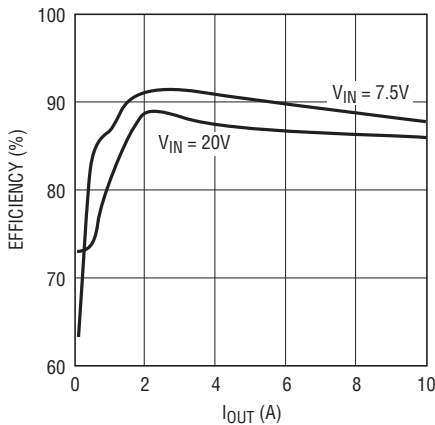
**Note 6:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

**Note 7:** The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current  $\geq 40\%$   $I_{MAX}$  (see Minimum On-Time Considerations in the Applications Information section).

**Note 8:** The  $ATTEN_{ERR}$  specification is in addition to the output voltage accuracy specified at VID code = 010110.

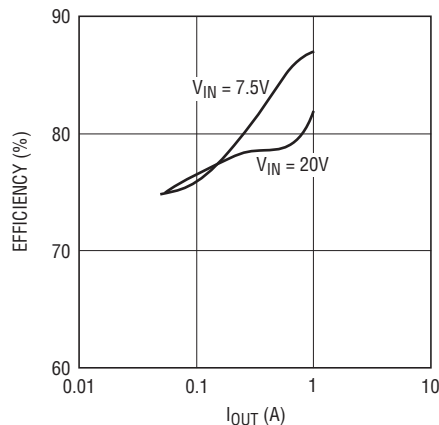
## TYPICAL PERFORMANCE CHARACTERISTICS

**Active Mode Efficiency (VID = 1.186V, PSI = 0) (Figure 9)**



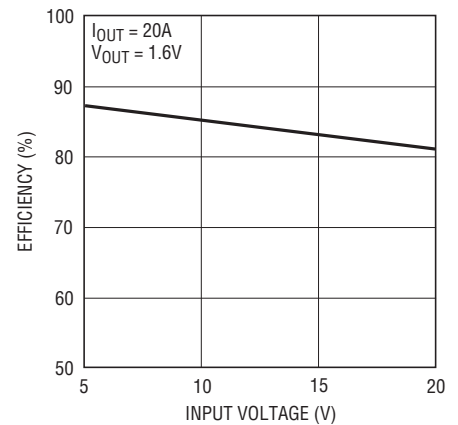
3735 601

**Deeper Sleep Mode Efficiency (Figure 9)**



3734 602

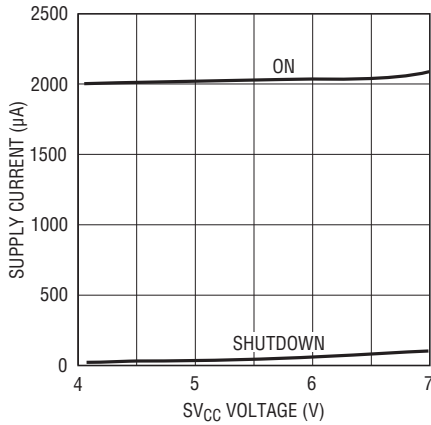
**Efficiency vs Input Voltage (Figure 9)**



3734 603

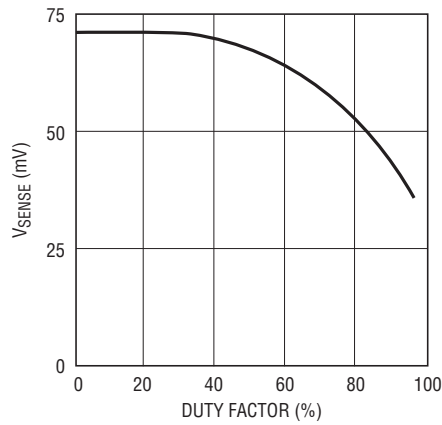
# TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs  $S_{V_{CC}}$  Voltage and Mode**



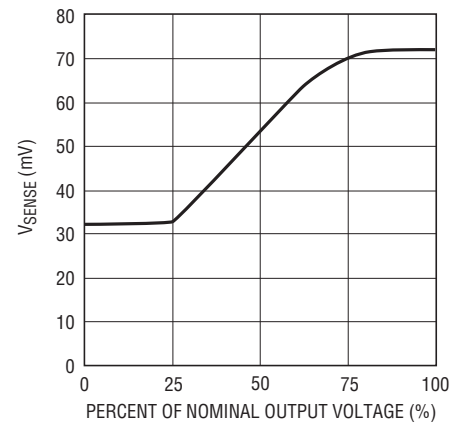
3734 G04

**Maximum Current Sense Threshold vs Duty Factor**



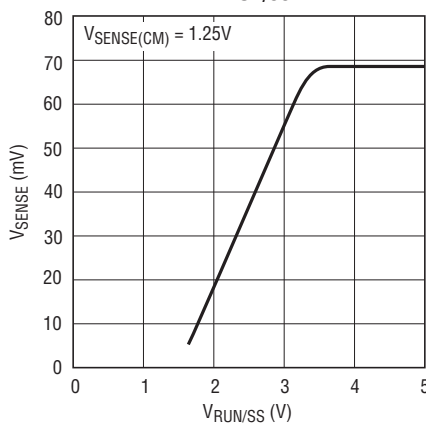
3734 G05

**Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)**



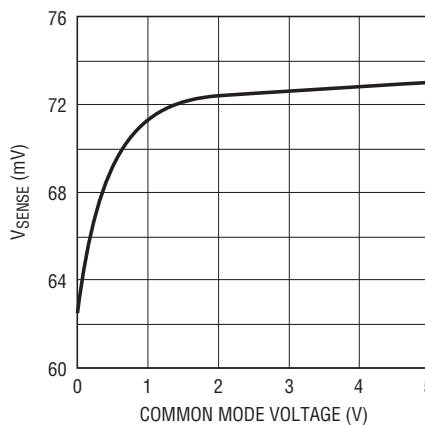
3734 G06

**Maximum Current Sense Threshold vs  $V_{RUN/SS}$  (Soft-Start)**



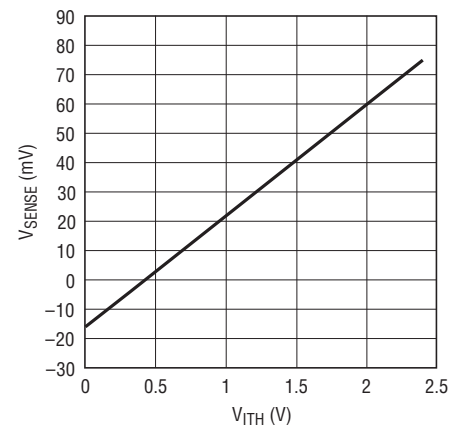
3734 G07

**Maximum Current Sense Threshold vs Sense Common Mode Voltage**



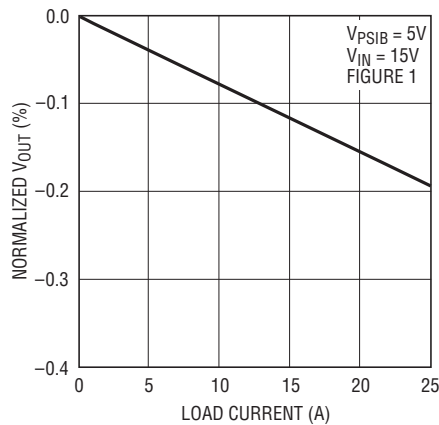
3734 G08

**Current Sense Threshold vs  $I_{TH}$  Voltage**



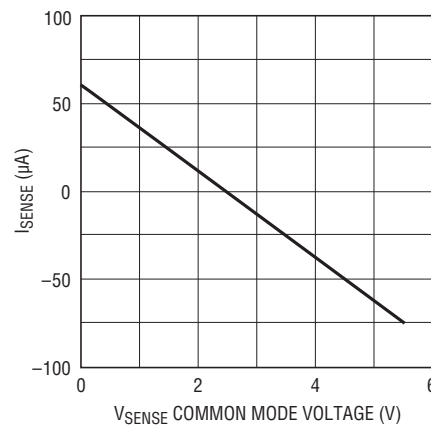
3734 G09

**Load Regulation (without AVP)**



3734 G10

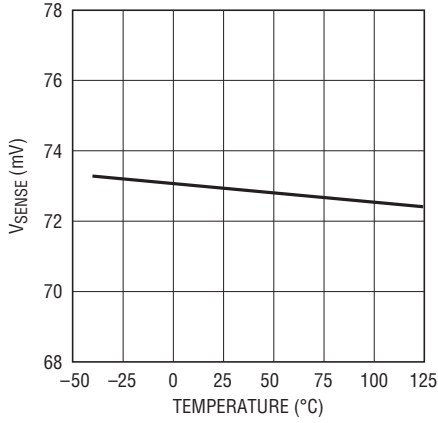
**SENSE Pins Total Source Current**



3734 G12

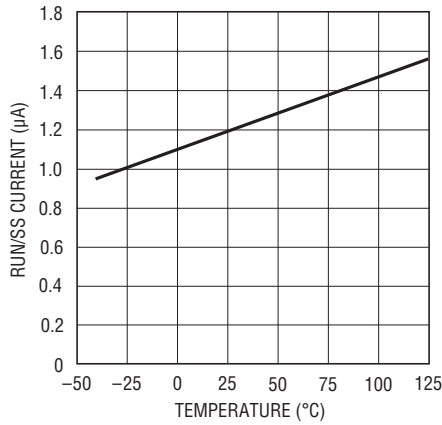
## TYPICAL PERFORMANCE CHARACTERISTICS

**Maximum Current Sense Threshold vs Temperature**



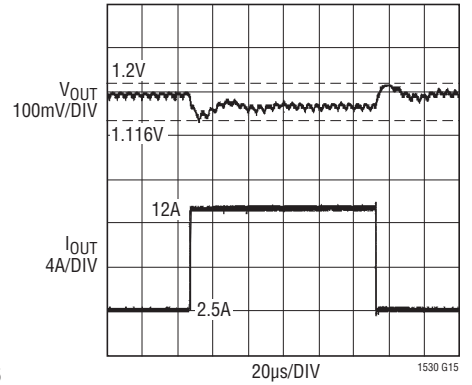
3734 G13

**RUN/SS Current vs Temperature**

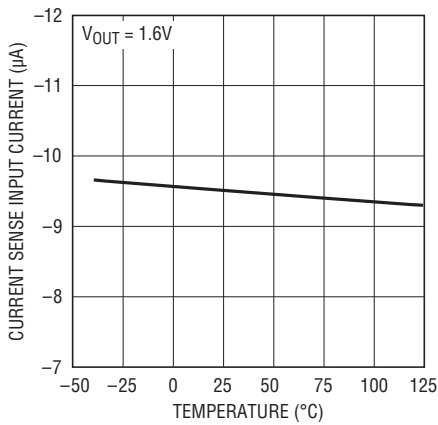


3734 G14

**Load Step (Figure 9)**

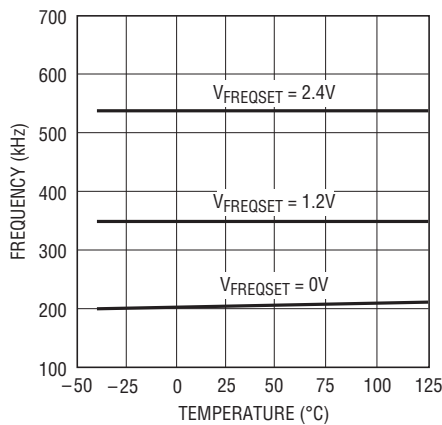


**Current Sense Pin Input Current vs Temperature**



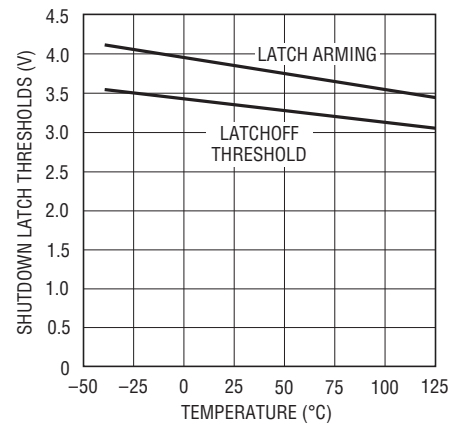
3734 G16

**Oscillator Frequency vs Temperature**



3734 G17

**V<sub>RUN/SS</sub> Shutdown Latch Thresholds vs Temperature**



3734 G19

## PIN FUNCTIONS

**$V_{OA}^+$ ,  $V_{OA}^-$  (Pins 1, 2):** Inputs to the Internal Operational Amplifier.

**OAOUT (Pin 3):** Output of the Internal Operational Amplifier.

**STP\_CPUB (Pin 4):** Deep Sleep State Input. When the signal to this pin is low, the voltage regulator enters deep sleep state and its output voltage is a certain percentage lower than the VID commands. This offset percentage is set by the resistor connected to the RDPSLP pin. When the signal to this pin is high, the voltage regulator exits deep sleep state.

**SGND (Pin 5):** Signal Ground. All small-signal components and compensation components should connect to this ground which, in turn, connects to PGND at one point.

**SENSE<sup>+</sup> (Pin 6):** The (+) Input to the Differential Current Comparator. The  $I_{TH}$  pin voltage and built-in offsets between SENSE<sup>-</sup> and SENSE<sup>+</sup> pins in conjunction with  $R_{SENSE}$  set the current trip threshold.

**SENSE<sup>-</sup> (Pin 7):** The (-) Input to the Differential Current Comparator.

**RDPSLP (Pin 8):** Deeper Sleep State Resistor Pin. Connect a resistor from this pin to  $V_{OA}^+$ . This resistor in conjunction with the RDPSLP resistor sets the output voltage of the regulator in deeper sleep state.

**RDPSLP (Pin 9):** Deep Sleep Resistor Pin. Connect a resistor from this pin to  $V_{OA}^+$ . This resistor sets the percentage offset of output voltage in deep sleep state.

**RUN/SS (Pin 10):** Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output. Forcing this pin below 1V causes the IC to shut down all internal circuitry. All functions are disabled in shutdown.

**$I_{TH}$  (Pin 11):** Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's threshold increases with this control voltage. The normal voltage range of this pin is from 0V to 2.4V

**RBOOT (Pin 12):** Boot-Up Resistor Pin. Connect a resistor from this pin to  $V_{OA}^+$ . This resistor sets the output voltage during the initial boot-up.

**VID0–VID5 (Pins 13, 14, 15, 17, 18, 19):** VID Control Logic Input Pins.

**NC (Pin 16):** Not Connected.

**PGND (Pin 20):** Driver Power Ground. Connect to sources of bottom N-channel MOSFETs and the (-) terminals of  $C_{IN}$ .

**BG (Pin 21):** High Current Gate Drive for Bottom N-Channel MOSFETs. Voltage swing at this pin is from ground to  $PV_{CC}$ .

**$PV_{CC}$  (Pin 22):** Power Supply Pin. The on chip gate drivers are powered from this voltage source. Decouple to PGND with a minimum of 4.7 $\mu$ F X5R/X7R ceramic capacitor placed directly adjacent to the IC.

## PIN FUNCTIONS

**SW (Pin 23):** Switch Node Connection to Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to  $V_{IN}$ .

**TG (Pin 24):** High Current Gate Drive for Top N-Channel MOSFETs. This is the output of a floating driver with a voltage swing equal to  $PV_{CC}$  superimposed on the switch node voltage SW.

**BOOST (Pin 25):** Bootstrapped Supply to the Topside Floating Driver. External capacitor is connected between the BOOST and SW pins, and a Schottky diode is connected between the BOOST and  $PV_{CC}$  pins.

**PGOOD (Pin 26):** Power Good Indicator Output. This pin is open drain when output is within  $\pm 10\%$  of its set point. When output is not within the  $\pm 10\%$  window, this pin is pulled to ground. An internal timer watches over VID, state transitions, overvoltage or undervoltage conditions, then masks PGOOD from going low for 110 $\mu$ s.

**MCH\_PG (Pin 27):** MCH Power Good Input. Output voltage remains VBOOT for 15 clock cycles after the assertion of MCH\_PG. This delay is only sensitive to the rising edge of the MCH\_PG logic signal.

**V<sub>FB</sub> (Pin 28):** Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage.

**SV<sub>CC</sub> (Pin 29):** Signal Power Pin. The internal control circuits are powered from this voltage source.

**DPRSLPVR (Pin 30):** Deeper Sleep State Input. When the signal to this pin is high, the voltage regulator enters deeper sleep state and its output is determined by the parallel resistor value of RDPRSLP and RDPSLP. When the signal is low, the voltage regulator exits deeper sleep state.

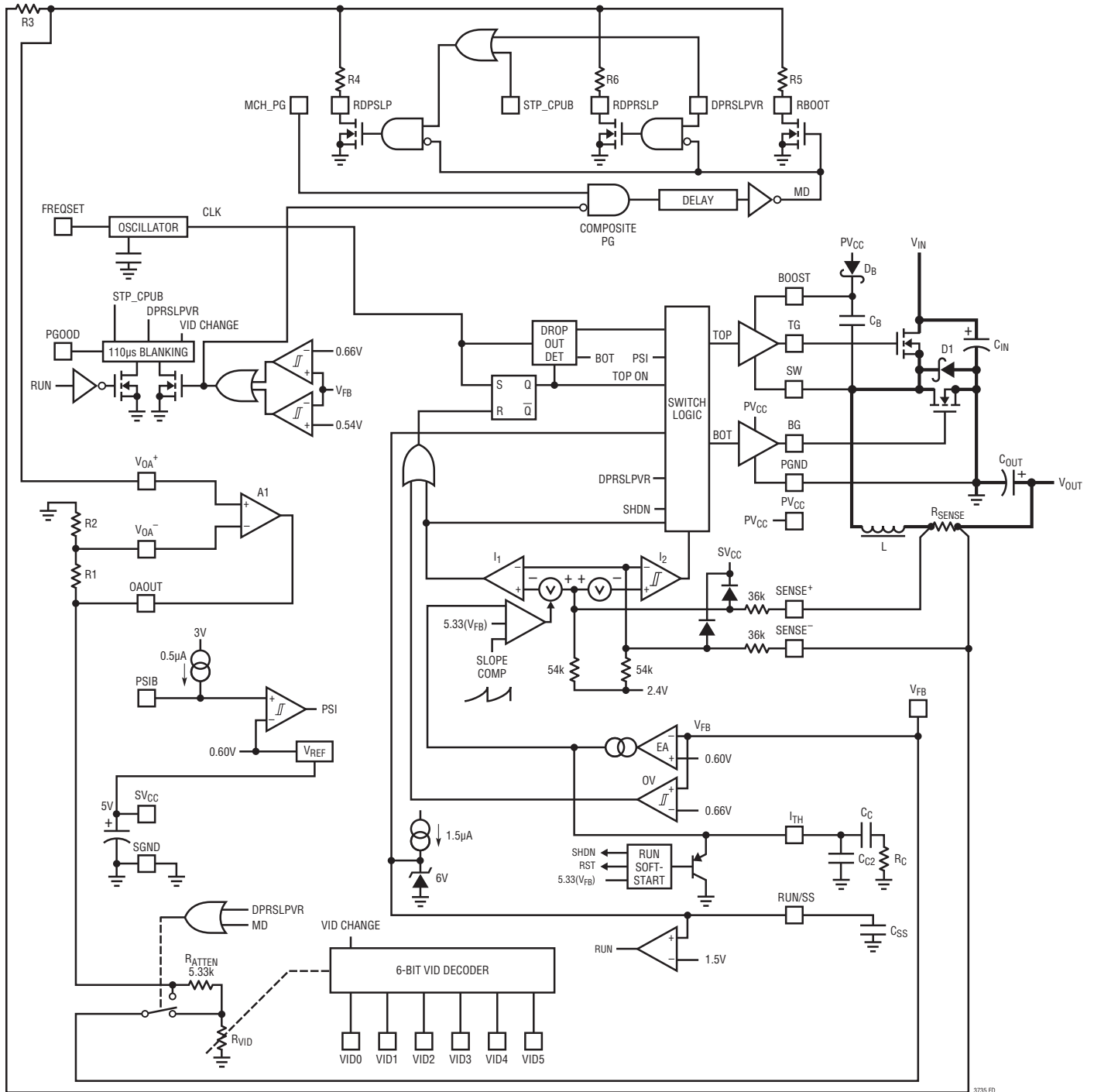
**FREQSET (Pin 31):** Frequency Set Pin. Apply a DC voltage between 0V and 5V to set the operating frequency of the internal oscillator. This frequency is the switching frequency of the controller.

**PSIB (Pin 32):** Power Status Indicator Input. When the signal to this pin is high, the controller operates in fully synchronous switching mode for fastest transient and lowest ripple. When the signal is low, controller enters power saving mode, providing high efficiency at light load.

**SGND (Exposed Pad Pin 33):** Signal Ground. Must be soldered to the PCB.



# FUNCTIONAL DIAGRAM



3735 FD

## OPERATION (Refer to Functional Diagram)

### Main Control Loop

The LTC3734 uses a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on when the clock sets the RS latch, and turned off when the main current comparator,  $I_1$ , resets the RS latch. The peak inductor current at which  $I_1$  resets the RS latch is controlled by the voltage on the  $I_{TH}$  pin, which is the output of error amplifier EA. The  $V_{FB}$  pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in EA inverting input node relative to the 0.6V reference, which in turn causes the  $I_{TH}$  voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator  $I_2$ , or the beginning of the next cycle.

The top MOSFET driver is biased from a floating bootstrap capacitor  $C_B$ , which normally is recharged during each off cycle through an external diode when the top MOSFET turns off. As  $V_{IN}$  decreases to a voltage close to  $V_{OUT}$ , the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 500ns every sixth cycle to allow  $C_B$  to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.5 $\mu$ A current source to charge soft-start capacitor  $C_{SS}$ . When  $C_{SS}$  reaches 1.5V, the main control loop is enabled with the internal  $I_{TH}$  voltage clamped at approximately 30% of its maximum value. As  $C_{SS}$  continues to charge, the internal  $I_{TH}$  voltage is gradually released allowing normal, full-current operation.

### Frequency Programming

The switching frequency of the LTC3734 is determined by the DC voltage at the FREQSET pin. A DC voltage ranging from 0V to 2.4V moves the internal oscillator frequency from 210kHz to 550kHz.

### Low Current Operation (PSIB)

The PSIB pin selects between two modes of operation. When PSIB is above 0.6V, the controller operates in full synchronous switching mode. Bottom driver (BG) is kept on once it is turned on until the oscillator sets the RS latch. The inductor current can therefore go from output back to input power supply and could potentially boost the input supply to dangerous voltage levels—BEWARE! This mode of operation is also of lower efficiency and much current can circulate between input and output. However, this mode provides constant switching frequency.

When PSIB is below 0.6V, the bottom driver (BG) is turned off if the inductor current starts to reverse. This mode of operation prevents current going from output back to input and eliminates the conduction power loss related to circulating current. The circuit may skip switching cycles at very light load conditions.

### Output Voltage at Start-Up and at Deeper Sleep State

Under normal conditions, the output voltage of the regulator is commanded by six VID bits, except at start-up and at deeper sleep state. At start-up, the RUN/SS capacitor starts to charge up and its voltage limits the inrush current from the input power source. This linearly rising current limit provides a controlled output voltage rise. During start-up, the VID command is ignored and the output set point is determined by the value of the resistor connected to the RBOOT pin. The VID bits continue to be ignored for 15 switching cycles after the completion of the following two conditions: 1) output voltage has risen up and has regulated 2) MCH\_PG signal has asserted. After 15 switching cycles, output voltage is fully commanded by VID bits.

In deeper sleep state, the VID command is also ignored and the output set point is determined by the parallel value of the resistors at the RDPRSLP pin and RDPSLP pin.

## OPERATION (Refer to Functional Diagram)

### Operational Amplifier and Deep Sleep Offset

The internal operational amplifier provides a programmable output offset at deep sleep state (when the STP\_CPUB signal is low). The offset percentage is programmed by the resistor from RDPSLP to  $V_{OA}^+$  and the resistor from output to  $V_{OA}^+$ . The amplifier has an output slew rate of  $5V/\mu s$  and is capable of driving capacitive loads with an output RMS current typically up to 40mA. The open-loop gain of the amplifier is  $>120dB$  and the unity-gain bandwidth is 2MHz.

### Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots ( $>10\%$ ) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

### Power Good

The PGOOD pin is connected to the drain of an internal N-channel MOSFET. The MOSFET turns on when the output voltage is not within  $\pm 10\%$  of its nominal set point. When the output voltage is within  $\pm 10\%$  of its nominal set point, the MOSFET turns off and PGOOD is high impedance. PGOOD monitors the  $V_{BOOT}$  voltage when MCH\_PG is not asserted. During VID, deep sleep or deeper sleep

transitions, PGOOD is masked from going low for  $110\mu s$ , preventing the system from resetting during CPU mode changes. When VID bits, STP\_CPUB or DPRSLPVR signals change again after a previous transition, but before the timer expires, the internal timer resets.

### Short-Circuit Detection

The RUN/SS capacitor is used initially to limit the inrush current from the input power source. Once the controller has been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full-load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage the RUN/SS capacitor begins discharging assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latching can be overridden by providing a current  $>5\mu A$  to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latching circuit is enabled.

## APPLICATIONS INFORMATION

The basic LTC3734 application circuit is shown in Figure 1 on the first page of this data sheet. External component selection begins with the selection of the inductors based on ripple current requirements and continues with the current sensing resistors using the calculated peak inductor current and/or maximum current limit. Next, the power MOSFET, D1 is selected. The operating frequency and the inductor are chosen based mainly on the amount of ripple current. Finally,  $C_{IN}$  is selected for its ability to handle the input ripple current and  $C_{OUT}$  is chosen with low enough ESR to meet the output ripple voltage and load step specifications. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

### $R_{SENSE}$ Selection For Output Current

$R_{SENSE}$  is chosen based on the required peak output current. The LTC3734 current comparator has a maximum threshold of  $72\text{mV}/R_{SENSE}$  and an input common mode range of SGND to  $SV_{CC}$ . The current comparator threshold sets the peak inductor current, yielding a maximum average output current  $I_{MAX}$  equal to the peak value less half the peak-to-peak ripple current,  $\Delta I_L$ .

Allowing a margin for variations in the LTC3734 and external component values yields:

$$R_{SENSE} = (40\text{mV}/I_{MAX})$$

### Operating Frequency

The LTC3734 uses a constant frequency architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the DC voltage applied to the FREQSET pin. The FREQSET voltage is internally set to 1.2V. It is recommended that this pin is actively biased with a resistor divider to prevent noise getting into the system.

A graph for the voltage applied to the FREQSET pin vs frequency is given in Figure 2. As the operating frequency is increased the gate drive and switching losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 550kHz.

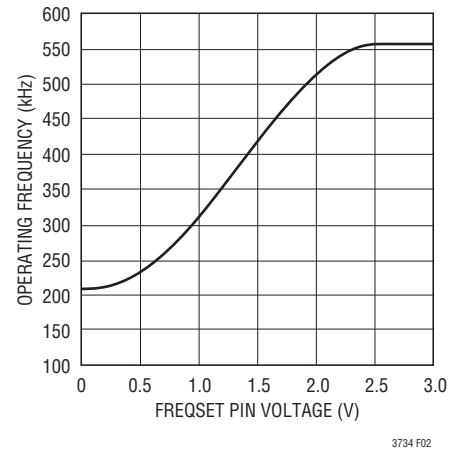


Figure 2. Operating Frequency vs  $V_{FREQSET}$

### Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are inter-related in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because MOSFET gate charge and transition losses increase directly with frequency. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current  $\Delta I_L$ , decreases with higher inductance or frequency and increases with higher  $V_{IN}$ :

$$\Delta I_L = \frac{V_{OUT}}{fL} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where  $f$  is the individual output stage operating frequency.

Accepting larger values of  $\Delta I_L$  allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is  $\Delta I_L = 0.4(I_{OUT})$ , where  $I_{OUT}$  is the maximum load current. Remember, the maximum  $\Delta I_L$  occurs at the maximum input voltage. The inductor ripple current is determined by the frequency, inductance, input and output voltages.

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### Inductor Core Selection

Once the value for L1 is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool M $\mu$  cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductor type selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. *Do not allow the core to saturate!*

A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Coilcraft, Coiltronics, Toko and Panasonic.

### Power MOSFET, D1 Selection

External power MOSFETs must be selected for output stage with the LTC3734: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the  $PV_{CC}$  voltage. This voltage typically ranges from 4.5V to 7V. Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the  $BV_{DSS}$  specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the “ON” resistance  $R_{DS(ON)}$ , gate charge  $Q_G$ , reverse transfer capacitance  $C_{RSS}$ , breakdown voltage  $BV_{DSS}$  and maximum continuous drain current  $I_{D(MAX)}$ .

When the LTC3734 operates at continuous mode in a step-down configuration, the duty cycles for the top and bottom MOSFETs are approximately:

$$\text{Top MOSFET Duty Cycle} = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$\text{Bottom MOSFET Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (2)$$

The conduction losses of the top and bottom MOSFETs are therefore:

$$P_{CONTOP} = \frac{V_{OUT}}{V_{IN}} \cdot (I_{OUT})^2 \cdot (1 + \delta \cdot \Delta T) \cdot R_{DS(ON)} \quad (3)$$

$$P_{CONBOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \cdot (I_{OUT})^2 \cdot (1 + \delta \cdot \Delta T) \cdot R_{DS(ON)} \quad (4)$$

where  $I_{OUT}$  is the maximum output current at full load,  $\Delta T$  is the difference between MOSFET operating temperature and room temperature, and  $\delta$  is the temperature dependency of  $R_{DS(ON)}$ .  $\delta$  is roughly 0.004/°C ~ 0.006/°C for low voltage MOSFETs.

The power losses of driving the top and bottom MOSFETs are simply:

$$P_{DRTOP} = Q_G \cdot PV_{CC} \cdot f \quad (5)$$

$$P_{DRBOT} = Q_G \cdot PV_{CC} \cdot f \quad (6)$$

Use  $Q_G$  data at  $V_{GS} = PV_{CC}$  in MOSFET data sheets.  $f$  is the switching frequency as described previously. Please notice that the above gate driving losses are usually not dissipated by the MOSFETs. Instead they are mainly dissipated on the internal drivers of the LTC3734, if there are no resistors connected between the drive pins (TG, BG) and the gates of the MOSFETs.

The calculation of MOSFET switching loss is complicated by several factors including the wide distribution of power

## APPLICATIONS INFORMATION

MOSFET threshold voltage, the nonlinearity of current rising/falling characteristic and the Miller Effect. Given the data in a typical power MOSFET data sheet, the switching losses of the top and bottom MOSFETs can only be estimated as follows:

$$P_{\text{SWTOP}} = V_{\text{IN}}^2 \cdot \frac{I_{\text{OUT}}}{2} \cdot f \cdot C_{\text{RSS}} \cdot R_{\text{DR}} \cdot \left( \frac{1}{V_{\text{DR}} - V_{\text{TH(MIN)}}} + \frac{1}{V_{\text{TH(MIN)}}} \right) \quad (7)$$

$$P_{\text{SWBOT}} \approx 0 \quad (8)$$

where  $R_{\text{DR}}$  is the effective driver resistance (of approximately  $2\Omega$ ),  $V_{\text{DR}}$  is the driving voltage ( $= PV_{\text{CC}}$ ) and  $V_{\text{TH(MIN)}}$  is the minimum gate threshold voltage of the MOSFET. Please notice that the switching loss of the bottom MOSFET is effectively negligible because the current conduction of the antiparalleling diode. This effect is often referred as zero-voltage-transition (ZVT). Similarly when the LTC3734 converter works under fully synchronous mode at light load, the reverse inductor current can also go through the body diode of the top MOSFET and make the turn-on loss to be negligible. However, equations 7 and 8 have to be used in calculating the worst-case power loss, which happens at highest load level.

The selection criteria of power MOSFETs start with the stress check:

$$V_{\text{IN}} < BV_{\text{DSS}}$$

$$I_{\text{MAX}} < I_{\text{D(MAX)}}$$

and

$$P_{\text{CONTOP}} + P_{\text{SWTOP}} < \text{top MOSFET maximum power dissipation specification}$$

$$P_{\text{CONBOT}} + P_{\text{SWBOT}} < \text{bottom MOSFET maximum power dissipation specification}$$

The maximum power dissipation allowed for each MOSFET depends heavily on MOSFET manufacturing and packaging, PCB layout and power supply cooling method. Maximum power dissipation data are usually specified in MOSFET data sheets under different PCB mounting conditions.

The next step of selecting power MOSFETs is to minimize the overall power loss:

$$P_{\text{OVL}} = P_{\text{TOP}} + P_{\text{BOT}} \\ = (P_{\text{CONTOP}} + P_{\text{DRTOP}} + P_{\text{SWTOP}}) + (P_{\text{CONBOT}} + P_{\text{DRBOT}} + P_{\text{SWBOT}})$$

For typical mobile CPU applications where the ratio between input and output voltages is higher than 2:1, the bottom MOSFET conducts load current most of the time while the main losses of the top MOSFET are for switching and driving. Therefore a low  $R_{\text{DS(ON)}}$  part (or multiple parts in parallel) would minimize the conduction loss of the bottom MOSFET while a higher  $R_{\text{DS(ON)}}$  but lower  $Q_{\text{G}}$  and  $C_{\text{RSS}}$  part would be desirable for the top MOSFET.

The Schottky diode, D1 in Figure 1, conducts during the dead-time between the conduction of the top and bottom MOSFETs. This helps reduce the current flowing through the body diode of the bottom MOSFET. A body diode usually has a forward conduction voltage higher than that of a Schottky and is thus detrimental to efficiency. The charge storage and reverse recovery of a body diode also cause high frequency rings at the switching nodes (the junction nodes between the top and bottom MOSFETs), which are again not desired for efficiency or EMI. Some power MOSFET manufacturers integrate a Schottky diode with a power MOSFET, eliminating the need to parallel an external Schottky. These integrated Schottky-MOSFETs, however, have smaller MOSFET die sizes than conventional parts and are thus not suitable for high current applications.

### $C_{\text{IN}}$ and $C_{\text{OUT}}$ Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle  $V_{\text{OUT}}/V_{\text{IN}}$ . A low ESR input capacitor sized for the maximum RMS current must be used. The RMS input ripple current is estimated to be:

$$I_{\text{RMS}} \cong I_{\text{OUT(MAX)}} \frac{V_{\text{OUT}}}{V_{\text{IN}}} \sqrt{\frac{V_{\text{IN}}}{V_{\text{OUT}}} - 1}$$

This formula has a maximum at  $V_{\text{IN}} = 2V_{\text{OUT}}$ , where  $I_{\text{RMS}} = I_{\text{OUT(MAX)}/2}$

## APPLICATIONS INFORMATION

This simple worst-case condition is commonly used for design, considering input/output variations and long term reliability. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR). Typically once the ESR requirement has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirements. The steady state output ripple ( $\Delta V_{OUT}$ ) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

Where  $f$  = operating frequency of each stage,  $C_{OUT}$  = output capacitance and  $\Delta I_L$  is inductor peak-to-peak ripple current.

The LTC3734 employs OPTI-LOOP technique to compensate the switching regulator loop with external components (through  $I_{TH}$  pin). OPTI-LOOP compensation speeds up regulator's transient response, minimizes output capacitance and effectively removes constraints on output capacitor ESR. It opens a much wider selection of output capacitor types and a variety of capacitor manufactures are available for high current, low voltage switching regulators.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce the inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer (SP) surface

mount capacitors from Panasonic offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KE-MET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, POSCAPs, Kemet AO-CAPs, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.

### PV<sub>CC</sub> and SV<sub>CC</sub> Decoupling

The PV<sub>CC</sub> pin supplies power to the bottom gate driver and therefore must be bypassed to power ground with a minimum of 4.7 $\mu$ F ceramic or tantalum capacitor. Since the gate driving currents are of high amplitude and high slew rate, this bypassing capacitor should be placed very close to the PV<sub>CC</sub> and PGND pins to minimize the parasitic inductance. Do NOT apply greater than 7V to the PV<sub>CC</sub> pin.

The SV<sub>CC</sub> pin supplies current to the internal control circuitry of the LTC3734. This supply current is much lower than that of the current for the external MOSFET gate drive. Ceramic capacitors are very good for high frequency filtering and a 0.1 $\mu$ F ~ 1 $\mu$ F ceramic capacitor should be placed adjacent to the SV<sub>CC</sub> and SGND pins.

### Topside MOSFET Driver Supply ( $C_B, D_B$ ) (Refer to Functional Diagram)

External bootstrap capacitor  $C_B$  connected to the BOOST pin supplies the gate drive voltages for the topside MOSFETs. Capacitor  $C_B$  in the Functional Diagram is charged through diode  $D_B$  from PV<sub>CC</sub> when the SW pin is low. When the topside MOSFET turns on, the driver places the  $C_B$  voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to  $V_{IN}$  and the BOOST pin rises to  $V_{IN} + PV_{CC}$ . The value of the boost capacitor  $C_B$  needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of  $D_B$  must be greater than  $PV_{CC(MAX)}$ .

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### VID Output Voltage Programming

After  $27\mu\text{s} \sim 71\mu\text{s}$   $t_{\text{BOOT}}$  delay, the output voltage of the regulator is digitally programmed as defined in Table 1 using the VID0 to VID5 logic input pins. The VID logic inputs program a precision, 0.25% internal feedback resistive divider. The LTC3734 has an output voltage range of 0.700V to 1.708V in 16mV steps.

Referring to the Functional Diagram, there is a resistor,  $R_{\text{VID}}$ , from  $V_{\text{FB}}$  to ground. The value of  $R_{\text{VID}}$  is controlled by the six VID input pins. Another internal resistor, 5.33k ( $R_{\text{ATTEN}}$ ), completes the resistive divider. The output voltage is thus set by the ratio of  $(R_{\text{VID}} + 5.33\text{k})$  to  $R_{\text{VID}}$ .

Each VID digital pin is a high impedance input. Therefore they must be actively pulled high or pulled low. The logic low threshold of the VID pins is 0.3V; the logic high threshold is 0.7V.

### Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) run/shutdown, 2) soft-start and 3) an optional short-circuit latching timer. Soft-start reduces the input power source's surge currents by gradually increasing the controller's current limit. The latching timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current ( $>5\mu\text{A}$ ) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. The following paragraph describes how the functions operate.

An internal  $1.5\mu\text{A}$  current source charges up the soft-start capacitor,  $C_{\text{SS}}$ . When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from  $25\text{mV}/R_{\text{SENSE}}$  to  $72\text{mV}/R_{\text{SENSE}}$ . The output current thus ramps up slowly, eliminating the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{\text{DELAY}} = \frac{1.5\text{V}}{1.5\mu\text{A}} C_{\text{SS}} = (1\text{s}/\mu\text{F}) C_{\text{SS}}$$

The time for the output current to ramp up is then:

$$t_{\text{IRAMP}} = \frac{3\text{V} - 1.5\text{V}}{1.5\mu\text{A}} C_{\text{SS}} = (1\text{s}/\mu\text{F}) C_{\text{SS}}$$

By pulling the RUN/SS pin below 1V the LTC3734 is put into low current shutdown ( $I_{\text{Q}} < 100\mu\text{A}$ ). The RUN/SS pin can be driven directly from logic as shown in Figure 3. Diode D1 in Figure 3 reduces the start delay but allows  $C_{\text{SS}}$  to ramp up slowly providing the soft-start function. The RUN/SS pin has an internal 6V zener clamp (see Functional Diagram).

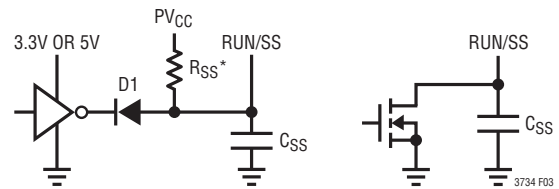


Figure 3. RUN/SS Pin Interfacing

### Start-Up Sequence (Refer to the Functional Diagram)

After soft-start, the output voltage of the regulator settles at a voltage level equal to  $V_{\text{BOOT}}$ .

$$V_{\text{BOOT}} = 0.6\text{V} \cdot \frac{R_2 \cdot (R_3 + R_5)}{R_5 \cdot (R_1 + R_2)}$$

By using different  $R_5$  resistors,  $V_{\text{BOOT}}$  can be programmed.

After the output voltage enters the  $\pm 10\%$  regulation window centered at  $V_{\text{BOOT}}$ , the internal power good comparator issues a logic high signal. Refer to the timing diagram in Figure 4. This signal then enters a logic AND gate, with MCH\_PG being the other input, and the output of the gate is PG shown in Figure 4. This composite PG signal is then delayed by  $t_{\text{BOOT}}$  amount of time and then becomes MD. As soon as MD is asserted, the output voltage changes from  $V_{\text{BOOT}}$  to  $V_{\text{VID}}$ , a voltage level totally controlled by the six VID bits. In the LTC3734, the time  $t_{\text{BOOT}}$  is set to be 15 switching cycles:

$$t_{\text{BOOT}} = 15 \frac{1}{f_s}$$

If  $f_s$  is set at 210kHz,  $t_{\text{BOOT}} = 71\mu\text{s}$

If  $f_s$  is set at 550kHz,  $t_{\text{BOOT}} = 27\mu\text{s}$



## APPLICATIONS INFORMATION

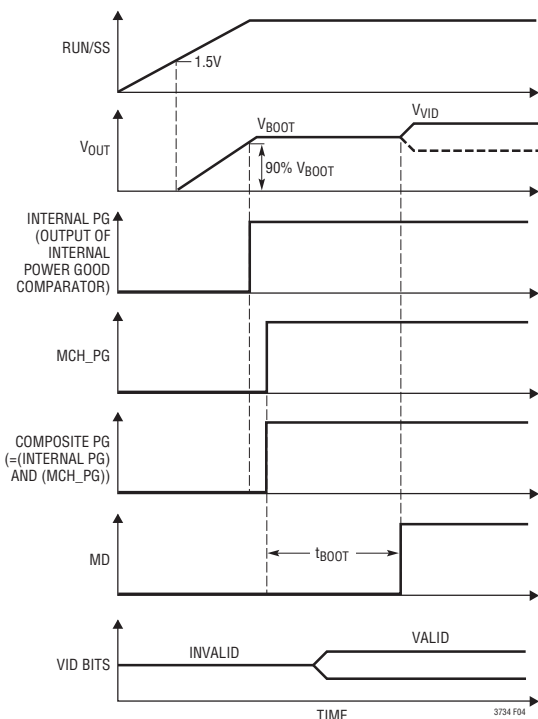


Figure 4. Start-Up Timing Diagram

### Output Voltage Set in Deep Sleep and Deeper Sleep States (Refer to the Functional Diagram)

The output voltage can be offset by the STP\_CPUB signal. When STP\_CPUB becomes low, the output voltage will be a certain percentage lower than that set by the VID bits in Table 1. This state is defined to be the deep sleep state. Referring to the Functional Diagram, we can calculate the STP\_CPUB offset to be:

$$\text{STP}\% = -\frac{R3}{R3+R4} \cdot 100\%$$

By using different R4 resistors, STP\_CPUB offset can be programmed.

The output voltage could also be set by external resistors R4 and R6 when DPRSLPVR input is high. This state is defined to be the deeper sleep state. The output voltage is set to  $V_{\text{DPRSLPVR}}$ , regardless of the VID setting:

$$V_{\text{DPRSLPVR}} = 0.6V \cdot \frac{R2 \cdot (R3 + R6 \parallel R4)}{(R6 \parallel R4) \cdot (R1 + R2)}$$

where  $R6 \parallel R4$  is the parallel combination of R4 and R6.

By using different value R6 resistors,  $V_{\text{DPRSLPVR}}$  can be programmed.

(The digital input threshold voltage is 1.8V for STP\_CPUB, DPRSLPVR and MCH\_PG inputs.)

### Power Good Masking

The PGOOD output monitors  $V_{\text{OUT}}$ . When  $V_{\text{OUT}}$  is not within  $\pm 10\%$  of the set point, PGOOD is pulled low with an internal MOSFET. When  $V_{\text{OUT}}$  is within the regulation window, PGOOD is of high impedance. PGOOD should be pulled up by an external resistor.

During VID changes, deep sleep and deeper sleep transitions, the output voltage can initially be out of the  $\pm 10\%$  window of the newly set regulation point. To avoid nuisance indications from PGOOD, a timer masks PGOOD for 110 $\mu\text{s}$ . If output is still out of regulation after this blanking time, PGOOD goes low. Any overvoltage or undervoltage condition is also masked for 110 $\mu\text{s}$  before it is reported by PGOOD.

The masking circuitry also adaptively tracks VID and state changes. If a new change in VID or state happens before the 110 $\mu\text{s}$  masking timer expires, the timer resets and starts a fresh count of 110 $\mu\text{s}$ . This prevents the system from rebooting under frequent output voltage transitions. Refer to Figure 5 for the PGOOD timing diagram.

During start up, PGOOD is actively pulled low until the RUN/SS pin voltage reaches its arming voltage, which

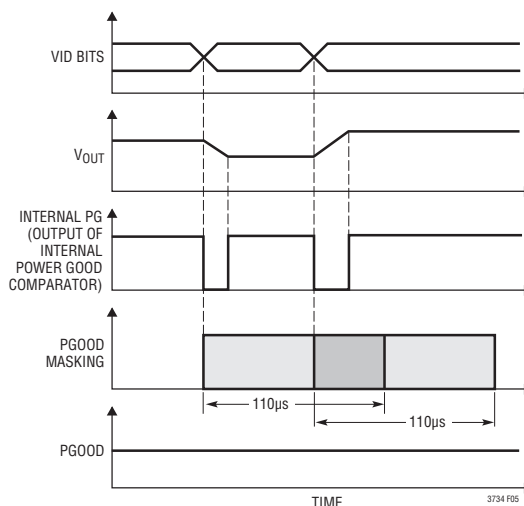


Figure 5. PGOOD Timing Diagram

## APPLICATIONS INFORMATION

Table 1. VID Output Voltage Programming

VID5	VID4	VID3	VID2	VID1	VID0	LTC3734
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V

VID5	VID4	VID3	VID2	VID1	VID0	LTC3734
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

is 4.2V typically. Only then is the PGOOD pull-low signal released.

When RUN/SS goes low, PGOOD goes low simultaneously.

### Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to latch off the controller when an overcurrent condition is detected. The

RUN/SS capacitor,  $C_{SS}$ , is used initially to limit the inrush current. After the controller has been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value after  $C_{SS}$  reaches 4.2V,  $C_{SS}$  begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long

## APPLICATIONS INFORMATION

enough period as determined by the size of the  $C_{SS}$ , the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO}^1 \approx (C_{SS} \cdot 0.7V)/(1.5\mu A) = 4.6 \cdot 10^5 (C_{SS})$$

If the overload occurs after start-up, the voltage on  $C_{SS}$  will continue charging and will provide additional time before latching off:

$$t_{LO}^2 \approx (C_{SS} \cdot 2V)/(1.5\mu A) = 1.3 \cdot 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor,  $R_{SS}$ , to the RUN/SS pin as shown in Figure 3. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. When deriving the  $5\mu A$  current from  $PV_{CC}$  as in the figure, current latchoff is always defeated.

Why should you defeat current latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor  $C_{SS}$  may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

A recommended soft-start capacitor of  $C_{SS} = 0.1\mu F$  will be sufficient for most applications.

### Minimum On-Time Considerations

Minimum on-time,  $t_{ON(MIN)}$ , is the smallest time duration that the LTC3734 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate

charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3734 will begin to skip cycles resulting in variable frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC3734 is generally less than 150ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger ripple current and ripple voltage.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has a low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current equal to or greater than 15% of  $I_{OUT(MAX)}$  at  $V_{IN(MAX)}$ .*

### Active Voltage Positioning

Active voltage positioning can be used to minimize peak-to-peak output voltage excursion under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Active voltage positioning can easily be added to the LTC3734. Figure 6 shows the equivalent circuit for implementing AVP. The load line slope is estimated to be:

$$AVP \cong -35.5 \cdot \frac{R_{SENSE}}{m} \cdot \frac{R3}{R_{AVP}}, \quad (9)$$

$$\text{if } g_m \cdot R3 > 10 \cdot \frac{V_{OUT}}{0.6V}$$

## APPLICATIONS INFORMATION

where

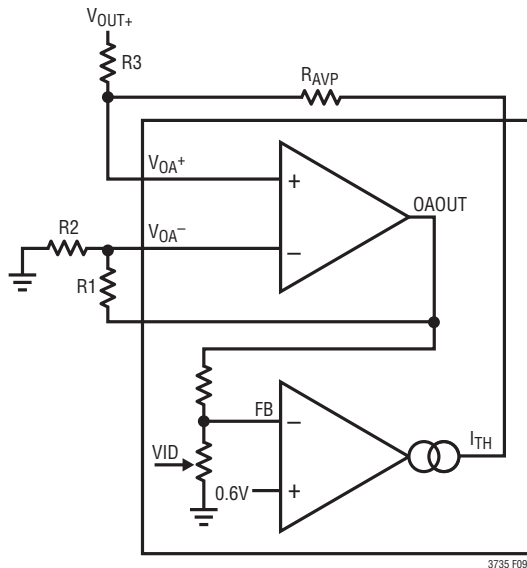
AVP is the slope, in mV/A

R<sub>SENSE</sub> is the current sense resistor

m is the number of phases, m = 1 for LTC3734

R3 and R<sub>AVP</sub> are defined in Figure 6

g<sub>m</sub> is the transconductance gain for the error amplifier, it is about 4.5mmho for LTC3734.



**Figure 6. Simplified Schematic Diagram for AVP Design in LTC3734**

Rewriting equation (9) we can estimate the AVP resistor to be:

$$R_{AVP} \cong \frac{35.5 \cdot R3 \cdot R_{SENSE}}{m \cdot |AVP|} \quad (10)$$

We also adopt the current sense resistors as part of voltage positioning slopes. So the total load line slope is estimated to be:

$$AVP \cong -35.5 \cdot \frac{R_{SENSE}}{m} \cdot \frac{R3}{R_{AVP}} - \frac{R_{SENSE}}{m}, \quad (11)$$

$$\text{if } g_m \cdot R3 \gg \frac{V_{OUT}}{0.6V}$$

Rewriting this equation, we can estimate the R<sub>AVP</sub> value to be:

$$R_{AVP} \cong \frac{35.5 \cdot R3}{\frac{m \cdot |AVP|}{R_{SENSE}} - 1} \quad (12)$$

Typically the calculation results based on these equations have  $\pm 10\%$  tolerance. So the resistor values need to be fine tuned.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3734 circuits: 1) I<sup>2</sup>R losses, 2) Topside MOSFET transition losses, 3) P<sub>VCC</sub> supply current and 4) C<sub>IN</sub> loss.

1) I<sup>2</sup>R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, and current sense resistor. In continuous mode the average output current flows through L and R<sub>SENSE</sub>, but is “chopped” between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same R<sub>DS(ON)</sub>, then the resistance of one MOSFET can simply be summed with the resistances of L, R<sub>SENSE</sub> and ESR to obtain I<sup>2</sup>R losses. For example, if each R<sub>DS(ON)</sub> = 10mΩ, R<sub>L</sub> = 10mΩ, and R<sub>SENSE</sub> = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A per output stage for a 5V output, or a 3% to 12% loss per output stage for a 3.3V

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output. Efficiency varies as the inverse square of  $V_{OUT}$  for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

2) Transition losses apply only to the topside MOSFET(s), and are significant only when operating at high input voltages (typically 12V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = V_{IN}^2 \cdot \frac{I_{OUT}}{2} \cdot f \cdot C_{RSS} \cdot R_{DR} \cdot \left( \frac{1}{V_{DR} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}} \right)$$

3)  $PV_{CC}$  drives both top and bottom MOSFETs. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge  $dQ$  moves from  $PV_{CC}$  to ground. The resulting  $dQ/dt$  is a current out of  $PV_{CC}$  that is typically much larger than the control circuit current. In continuous mode,  $I_{GATECHG} = (Q_T + Q_B)f$ , where  $Q_T$  and  $Q_B$  are the gate charges of the topside and bottom side MOSFETs and  $f$  is the switching frequency.

4) The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC  $I^2R$  loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including  $C_{OUT}$  ESR loss, Schottky diode conduction loss during dead time, inductor core loss and internal control circuitry supply current generally account for less than 2% additional loss.

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs,  $V_{OUT}$  shifts by an amount equal to  $\Delta I_{LOAD}(ESR)$ , where ESR is the effective

series resistance of  $C_{OUT}$ .  $\Delta I_{LOAD}$  also begins to charge or discharge  $C_{OUT}$  generating the feedback error signal that forces the regulator to adapt to the current change and return  $V_{OUT}$  to its steady-state value. During this recovery time  $V_{OUT}$  can be monitored for excessive overshoot or ringing, which would indicate a stability problem. *The availability of the  $I_{TH}$  pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The  $I_{TH}$  external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The  $I_{TH}$  series  $R_C$ - $C_C$  filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon first because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of  $<1\mu s$  will produce output voltage and  $I_{TH}$  pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the  $I_{TH}$  pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing  $R_C$  and the bandwidth of the loop will be increased by decreasing  $C_C$ . If  $R_C$  is increased by the same factor that  $C_C$  is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

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### Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 7 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC3734 has a maximum input voltage of 32V, most applications will be limited to 30V by the MOSFET  $BV_{DSS}$ .

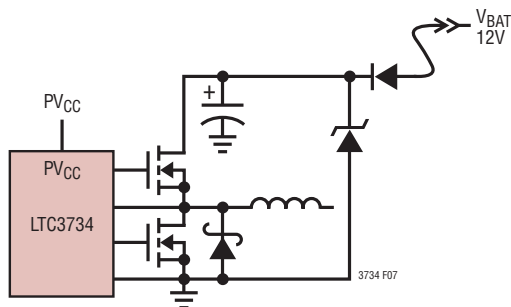


Figure 7. Automotive Application Protection

### Design Example

As a design example, assume  $V_{IN} = 12V$  (nominal),  $V_{IN} = 21V$  (max),  $V_{OUT} = 1.5V$ ,  $I_{MAX} = 20A$ , and  $f = 350kHz$ .

The inductance value is chosen first based on a 40% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. The minimum inductance for 40% ripple current is:

$$L \geq \frac{V_{OUT}}{f \cdot \Delta I} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{1.5V}{350kHz \cdot (40\% \cdot 20A)} \cdot \left(1 - \frac{1.5V}{21V}\right) = 0.5\mu H$$

The peak inductor current will be the maximum DC current plus one half of the ripple current, or 24A.

Tie the FREQSET pin to 1.2V, resistively divided down from  $SV_{CC}$  to have 350kHz operation.

The minimum on-time also occurs at maximum input voltage:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN} \cdot f} = \frac{1.5V}{21V \cdot 350kHz} = 204ns$$

which is larger than 150ns, the typical minimum on time of the LTC3734.

$R_{SENSE}$  can be calculated by using a conservative maximum sense voltage threshold of 40mV and taking into account of the peak current:

$$R_{SENSE} = \frac{40mV}{24A} = 0.002\Omega$$

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The power loss dissipated by the top MOSFET can be calculated with equations 3 and 7. Using a Fairchild FDS7760 as an example:  $R_{DS(ON)} = 8\text{m}\Omega$ ,  $Q_G = 55\text{nC}$  at  $5\text{V } V_{GS}$ ,  $C_{RSS} = 307\text{pF}$ ,  $V_{TH(MIN)} = 1\text{V}$ . At maximum input voltage with  $T_J(\text{estimated}) = 85^\circ\text{C}$  at an elevated ambient temperature:

$$P_{TOP} = \frac{1.5\text{V}}{21\text{V}} \cdot 20\text{A}^2 \cdot (1 + 0.005 \cdot (85^\circ\text{C} - 25^\circ\text{C})) \cdot (0.008\Omega + 21\text{V}^2 \cdot \frac{20\text{A}}{2} \cdot 350\text{kHz} \cdot 307\text{pF} \cdot 2\Omega \cdot (\frac{1}{5\text{V} - 1\text{V}} + \frac{1}{1\text{V}})) = 1.48\text{W}$$

Equation 4 gives the worst-case power loss dissipated by the bottom MOSFET (assuming FDS7760 and  $T_J = 85^\circ\text{C}$  again):

$$P_{BOT} = \frac{21\text{V} - 1.5\text{V}}{21\text{V}} \cdot 20\text{A}^2 \cdot (1 + 0.005 \cdot (85^\circ\text{C} - 25^\circ\text{C})) \cdot 0.008\Omega = 3.86\text{W}$$

Therefore, it is necessary to have two FDS7760s in parallel to split the power loss for both the top and bottom MOSFETS.

A short-circuit to ground will result in a folded back current of about:

$$I_{SC} = \frac{25\text{mV}}{0.002\Omega} + \frac{1}{2} \cdot \left( \frac{200\text{ns} \cdot 21\text{V}}{0.5\mu\text{H}} \right) = 16.7\text{A}$$

The worst-case power dissipation by the bottom MOSFET under short-circuit conditions is:

$$P_{BOT} = \frac{\frac{1}{350\text{kHz}} - 200\text{ns}}{1} \cdot 16.7\text{A}^2 \cdot (1 + 0.005 \cdot (85^\circ\text{C} - 25^\circ\text{C})) \cdot 0.008\Omega = 2.7\text{W}$$

which is less than normal, full load conditions.

The RMS input ripple current will be:

$$I_{INRMS} = 20\text{A}/2 = 10\text{A}$$

An input capacitor(s) with a 10A RMS current rating is required.

The output capacitor ripple current is calculated. The output ripple will be highest at the maximum input voltage:

$$\Delta I_{OUT(MAX)} = \frac{1.5\text{V}}{350\text{kHz} \cdot 0.5\mu\text{H}} \cdot \left( 1 - \frac{1.5}{2.1} \right) = 8\text{A}_{P-P}$$

Assuming the ESR of output capacitor(s) is  $5\text{m}\Omega$ , the output ripple voltage is:

$$\Delta V_{OUT} \approx 8\text{A}_{P-P} \left( 5\text{m}\Omega + \frac{1}{8 \cdot 350\text{kHz} \cdot (4 \cdot 270\mu\text{F})} \right) = 42.6\text{mV}_{P-P}$$

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### PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3734. Check the following in your layout:

1) Are the signal and power grounds segregated? Keep the SGND at one end of a PC board to prevent MOSFET currents from traveling under the IC. The IC signal ground pin (Pin 5) should be used to hook up all control circuitry on one side of the IC, routing the copper through SGND, under the IC covering the “shadow” of the package, connecting to the PGND pin (Pin 20) and then continuing on to the (–) plate of  $C_{OUT}$ .

2) Is the  $PV_{CC}$  decoupling capacitor connected immediately adjacent to the  $PV_{CC}$  and PGND pins? A  $1\mu\text{F}$  ceramic capacitor of the X7R or X5R material is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the power MOSFETs. An additional  $4.7\mu\text{F} \sim 10\mu\text{F}$  of ceramic, tantalum or other low ESR capacitor is recommended in order to keep  $PV_{CC}$  stable. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes, and (–) plates of  $C_{IN}$ , which should have the shortest trace length possible.

3) Are the  $SENSE^-$  and  $SENSE^+$  leads routed together with minimum PC trace spacing? The filter capacitors between  $SENSE^+$  and  $SENSE^-$  pin pairs should be as close as possible to the LTC3734. Ensure accurate current sensing with Kelvin connections at the current sense resistor. See Figure 8.

4) Does the (+) plate of  $C_{IN}$  connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs. Keep the input current path formed by the input capacitor, top and bottom MOSFETs, and the Schottky diode on the same side of the PC board in a tight loop to minimize conducted and radiated EMI.

5) Keep the “noisy” nodes, SW, BOOST, TG and BG away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC3734.

It is critical to keep the high-switching-current paths to a small physical size. High electric and magnetic fields will radiate from these “loops” just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the “noise” generated by a switching regulator. The ground terminations of the synchronous MOSFETs and Schottky diodes should return to the negative plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the negative plate(s) of the input capacitor(s) should be used to tie in the IC power ground pin (PGND) and the signal ground pin (SGND). This technique keeps inherent signals generated by high current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

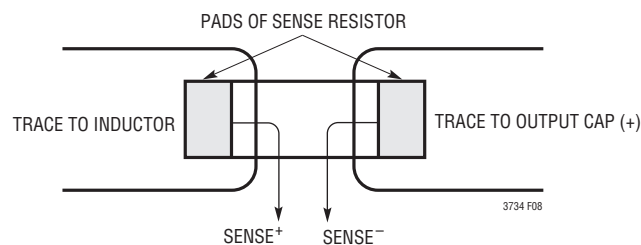


Figure 8. Proper Current Sense Connections



## TYPICAL APPLICATION

Figure 9 shows a typical application using the LTC3734 to power the mobile CPU core. The input can vary from 5V to 24V; the output voltage can be programmed from 0.7V to 1.708V with a maximum current of 20A. By only modifying the external MOSFET and inductor selection, higher load current capability can be achieved.

The power supply in Figure 9 receives a VRON signal for ON/OFF control. After soft-start, the output voltage is set at 1.2V until the assertion of the MCH\_PG signal. After about a 50 $\mu$ s delay, the VID5-VID0 bits gain the control over the output voltage and program it between 0.7V and

1.708V. When the STP\_CPUB signal is low, a deep sleep state is indicated and the output voltage is decreased by about 1.04%. When the DPRSLPVR signal is high, a deeper sleep state is indicated and the output voltage becomes 0.748V regardless of the states of the VID bits. Active voltage positioning is accomplished with a resistive divider across the I<sub>TH</sub> pin. Lower resistance yields a steeper AVP slope while higher resistance provides a flatter slope. Finally, the PGOOD output is masked for 110 $\mu$ s during VID change or state transition.

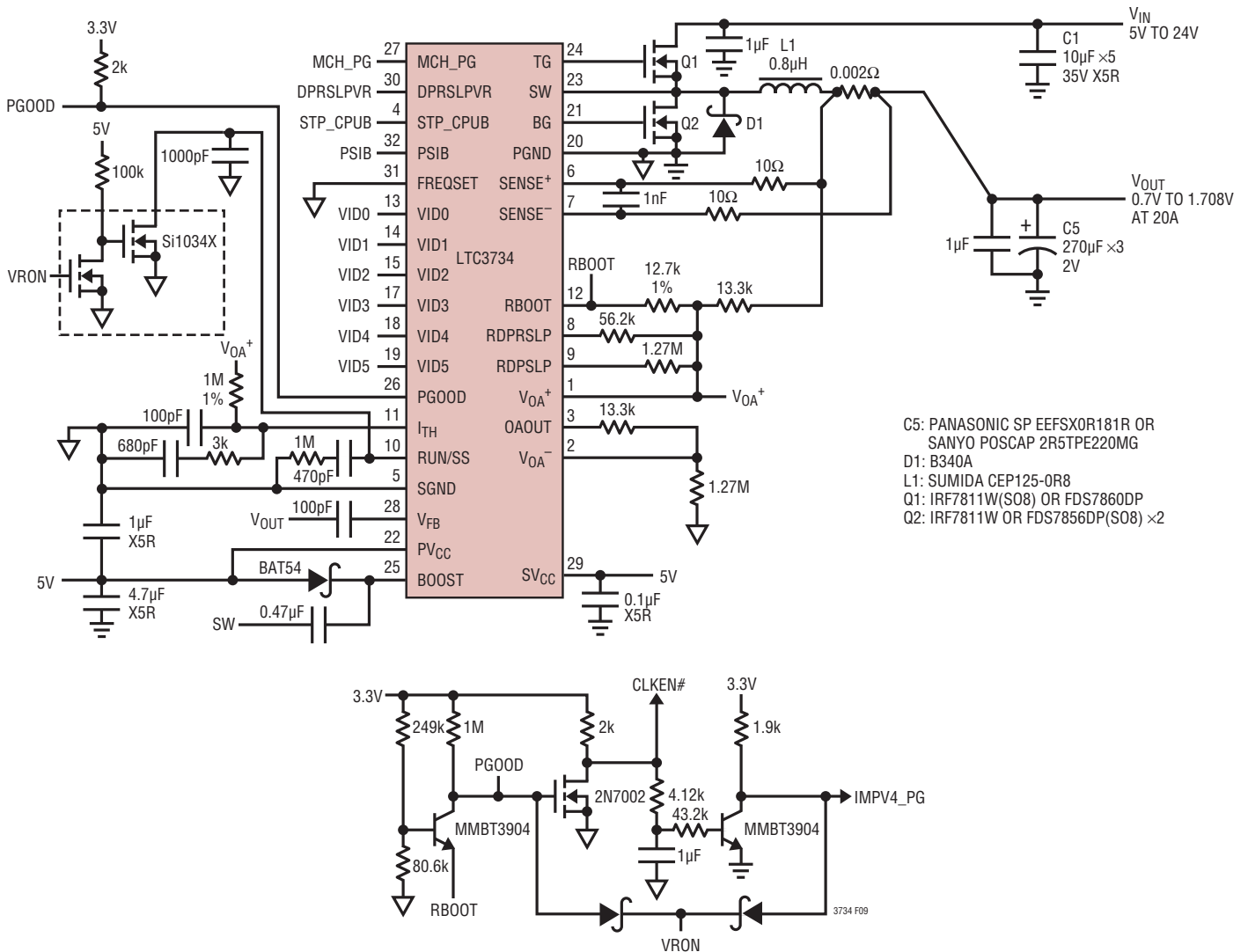
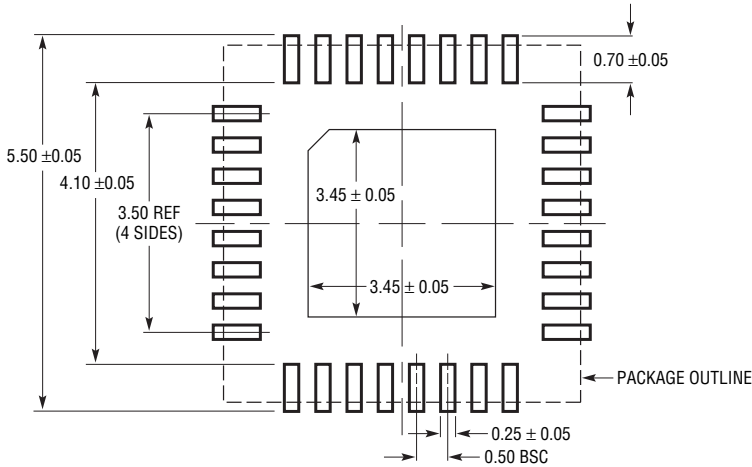


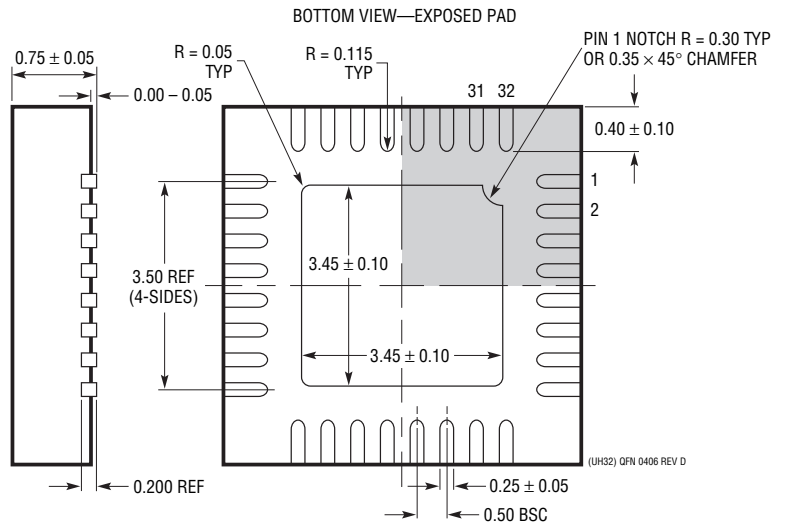
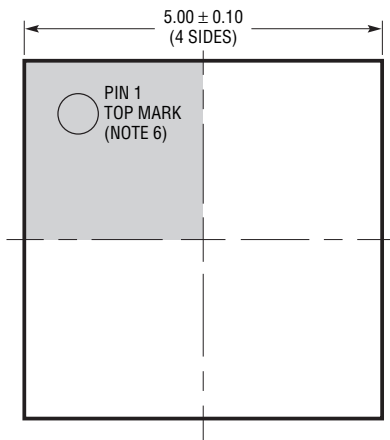
Figure 9. 5V to 24V Input, 0.7V to 1.708V Output, 20A IMVP-IV Compatible Power Supply

**PACKAGE DESCRIPTION**

**UH Package**  
**32-Lead Plastic QFN (5mm × 5mm)**  
 (Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



- NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE MO-220 VARIATION WHHD-(X) (TO BE APPROVED)
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/11	Updated Figure 9	25
		Updated Related Parts	28

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3816	Single Phase DC/DC Controller for Intel IMVP-6/6+/6.5 CPUs	7-Bit IMVP-6 VID: $0.00V \leq V_{OUT} \leq 1.50V$ , $4.5V \leq V_{IN} \leq 36V$ , Very Low Duty Cycle Capable
LTC3732	3-Phase, 5-Bit VID, 600kHz, Synchronous Controller	5-Bit VRM 9/9.1: $1.10V \leq V_{OUT} \leq 1.85V$ , $4.5V \leq V_{IN} \leq 32V$ , Stage Shedding™ or Burst Mode® Operation
LTC3735	2-Phase, High Efficiency DC/DC Controller for Intel Mobile CPUs	6-Bit IMVP-4 VID: $0.70V \leq V_{OUT} \leq 1.708V$ , $4.5V \leq V_{IN} \leq 30V$ , Lossless Voltage Positioning
LTC3869/LTC3869-2	Dual, 2-Phase Synchronous Step-Down DC/DC Controllers with Excellent Current Share when Paralleled	Phase-Lockable Fixed 250kHz to 780kHz Frequency, $4V \leq V_{IN} \leq 38V$ , $0.8V \leq V_{OUT} \leq 12.5V$
LTC3856	2-Phase, Single Output Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	Phase-Lockable Fixed 250kHz to 770kHz Frequency, $4.5V \leq V_{IN} \leq 38V$ , $0.8V \leq V_{OUT} \leq 5V$
LTC3850/LTC3850-1 LTC3850-2	Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controller, R <sub>SENSE</sub> or DCR Current Sensing and Tracking	Phase-Lockable Fixed 250kHz to 780kHz Frequency, $4V \leq V_{IN} \leq 30V$ , $0.8V \leq V_{OUT} \leq 5.25V$
LTC3860	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and Three-State Output Drive	Operates with Power Blocks, DR MOS Devices or External Drivers/MOSFETs, $3V \leq V_{IN} \leq 24V$ , $t_{ON(MIN)} = 20ns$
LTC3855	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	Phase-Lockable Fixed Frequency 250kHz to 770kHz, $4.5V \leq V_{IN} \leq 38V$ , $0.8V \leq V_{OUT} \leq 12V$
LTC3829	3-Phase, Single Output Synchronous Step-Down Controller with Diff Amp and DCR Temperature Compensation	Phase-Lockable Fixed 250kHz to 770kHz Frequency, $4.5V \leq V_{IN} \leq 38V$ , $0.8V \leq V_{OUT} \leq 5V$
LTC3853	Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R <sub>SENSE</sub> or DCR Current Sensing and Tracking	Phase-Lockable Fixed 250kHz to 750kHz Frequency, $4V \leq V_{IN} \leq 24V$ , $V_{OUT3}$ Up to 13.5V

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