High Voltage High Current Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion into Live Backplane**
- **Wide Operating Voltage Range: 6.5V to 80V**
- **Drives Two Gates for High Power Applications**
- **Configurable Parallel, Staged Start or Single MOSFET Modes**
- Adjustable Precision Current Limit: 6mV to 20mV
- Current Foldback Limits MOSFET Power
- SOA Timer Optimizes MOSFET Capability
- Monitors V_{GS} and V_{DS} for MOSFET Health
- 12V Gate Drive for Lower MOSFET $R_{DS(ON)}$
- Parallelable Controllers for Very High Current Levels
- Available in 24-Lead Narrow SSOP and 24-Pin 4mm × 5mm QFN Packages

APPLICATIONS

- Live Board Insertion in 12V, 24V and 48V Systems
- Industrial High Side Switch/Circuit Breaker
- Computers, Servers
- Vehicle Electrical Systems

DESCRIPTION

The LTC®4238 is a high voltage high current Hot Swap controller that allows a board to be safely inserted and removed from a live backplane. Dual 12V gate drive is well suited for high power applications to either share safe operating area across parallel MOSFETs or support a 2-stage start-up that first charges the load capacitance followed by enabling a low on-resistance path to the load.

The device features active current limiting (ACL) with two foldback options as V_{DS} increases. The constant power profile limits the power dissipation to be no higher than a fixed value, while the high power profile allows the part to ride through large input steps during operation.

The LTC4238 notifies when output power is good. In addition, it has protection features that respond to input undervoltage, overvoltage; and generate a fault when there is an overcurrent or FET bad condition.

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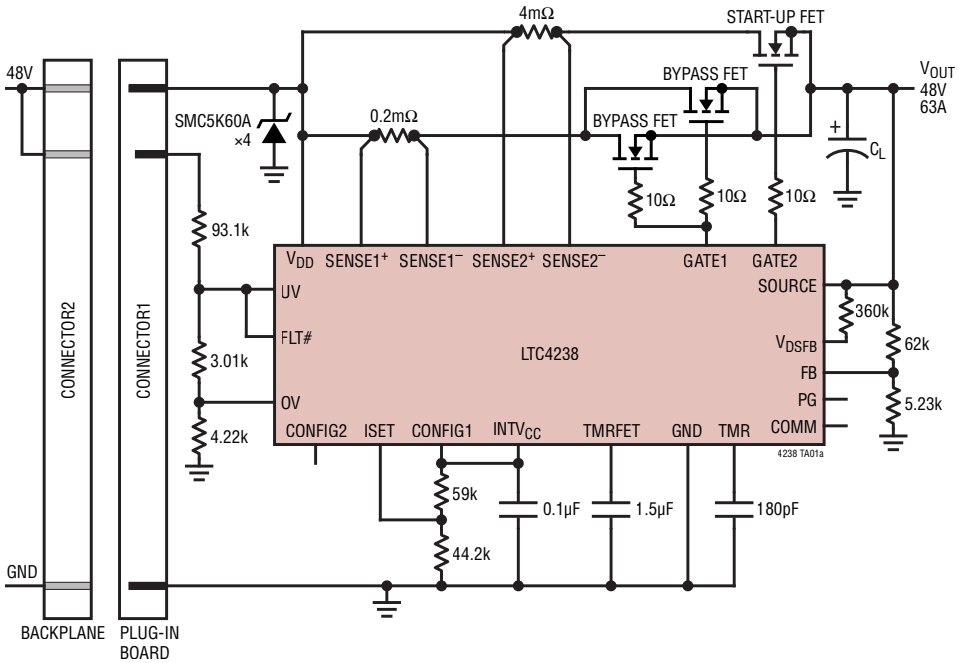
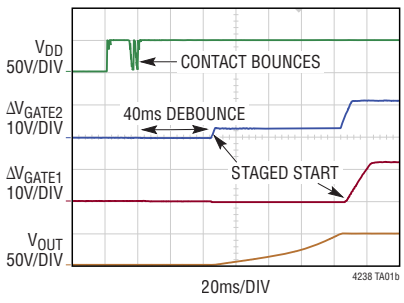
TYPICAL APPLICATION

48V, 63A Hot Swap Controller in Low Stress Staged Start Mode



Start-Up Behavior



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltages
- V_{DD} ..... –0.3V to 100V
- $INTV_{CC}$ ..... –0.3V to 5.5V

Input Voltages
- GATE – SOURCE (Note 3) ..... –0.3V to 10V
- SENSE1+, SENSE1–, SENSE2+, SENSE2– ..... V_{DD} – 4.5V to V_{DD} + 0.3V
- SOURCE, FB, OV, UV, ... –0.3V to 100V
- V_{DSFB} ..... –0.3V to V_{DD} +0.3V
- TMR, TMRFET, ISET, CONFIG1, CONFIG2 ..... –0.3V to $INTV_{CC}$ + 0.3V

Output Voltages
- GATE, PG, FLT# ..... –0.3V to 100V
- COMM ..... –0.3V to 5.5V

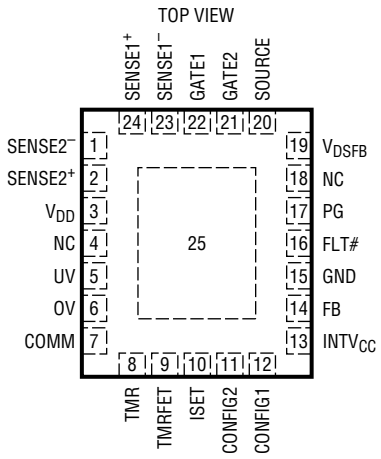
Output Currents
- $INTV_{CC}$ 10mA

Operating Junction Temperature Range
- LTC4238C ..... 0°C to 70°C
- LTC4238I ..... –40°C to 85°C
- LTC4238H ..... –40°C to 125°C

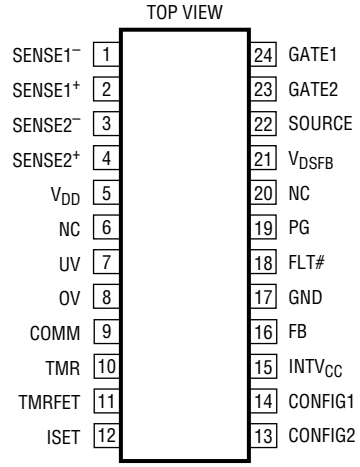
Storage Temperature Range
- GN Package ..... –65°C to 150°C
- UFD Package ..... –65°C to 125°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN
$T_{J(MAX)}$ = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 25) PCB GND
ELECTRICAL CONNECTION OPTIONAL



GN24 PACKAGE
24-LEAD PLASTIC SSOP
$T_{J(MAX)}$ = 150°C, θ_{JA} = 85°C/W

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4238CUFD#PBF	LTC4238CUFD#TRPBF	4238	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4238IUFD#PBF	LTC4238IUFD#TRPBF	4238	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4238HUFD#PBF	LTC4238HUFD#TRPBF	4238	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC4238CGN#PBF	LTC4238CGN#TRPBF	LTC4238GN	24-Lead Plastic SSOP	0°C to 70°C
LTC4238IGN#PBF	LTC4238IGN#TRPBF	LTC4238GN	24-Lead Plastic SSOP	–40°C to 85°C
LTC4238HGN#PBF	LTC4238HGN#TRPBF	LTC4238GN	24-Lead Plastic SSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Input Supply Range		●	6.5		80	V
I_{DD}	Input Supply Current		●		3	5	mA
$V_{DD(UVLO)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	5.8	6	6.2	V
$V_{DD(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●		500		mV
$INTV_{CC}$	Internal 5V Supply Voltage	I_{LOAD} = 0mA to 10mA	●	4.5	5.0	5.5	V
$INTV_{CC(UVLO)}$	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising	●	3.75	4	4.25	V
$INTV_{CC(HYST)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis		●		110		mV
Current Limit							
$\Delta V_{SNS(TH)}$	Current Limit Sense Voltage Threshold ($SENSE^+ – SENSE^–$)	ISET= 0V ISET = $INTV_{CC}$	● ●	5.8 19.5	6 20	6.2 20.5	mV mV
	10% Current Limit Foldback, Start-Up Only	ISET = 0V ISET = $INTV_{CC}$	● ●	0.18 1.6	0.6 2	0.9 2.4	mV mV
	30% Current Limit Foldback, Normal	$V_{DD} – V_{DSFB}$ =12V ISET = 0V ISET = $INTV_{CC}$	 ● ●	 1.5 5.6	 1.8 6	 2.1 6.4	 mV mV
	Current Limit Threshold DAC INL		●		0	±60	µV
$\Delta V_{SNS1} – \Delta V_{SNS2}$	Current Limit Channel Voltage Mismatch	V_{SENSE1}+, V_{SENSE2}+ = 48V	●		0	±300	µV
$\alpha_{ILIM(FAST)}$	Ratio of Fast Current Limit to Nominal $\Delta V_{SNS(TH)}$		●	2	3	4	
I_{SENSE1}+	$SENSE1^+$ Input Current	V_{SENSE1}+ = 48V, $V_{SNS1} \leq$ 20mV	●	0		150	µA
$I_{SENSE1}–$	$SENSE1^–$ Input Current, $V_{SENSE1}– = V_{SENSE2}–$ = 48V	HSSS Mode with CH2 Off	●	3	5	7	µA
		Parallel, LSSS Mode, HSSS Mode with CH2 On	●		0	±1	µA
I_{SENSE2}+	$SENSE2^+$ Input Current	V_{SENSE2}+ = 48V	●	0		70	µA
$I_{SENSE2}–$	$SENSE2^–$ Input Current	V_{SENSE2}+ = $V_{SENSE2}–$ = 48V	●		0	±1	µA
Gate Drive							
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} – V_{SOURCE}$)	V_{DD} = 6.5V to 80V, I_{GATE} = –5µA (Note 3)	●	10	12	14	V
$\Delta V_{GATE(TH)}$	Gate Threshold for FET-Bad and Power Good		●	6	8	10	V
$I_{GATE(UP)}$	GATE1, GATE2 Pull-Up Current	Gate On, GATE = 0V	●	–35	–50	–70	µA
$I_{GATE(DN)}$	GATE1, GATE2 Fast Pull-Down Current	ΔV_{SNS} = 100mV, ΔV_{GATE} = 6V			0.8		A
	Gate Off Pull-Down Current to SOURCE	ΔV_{GATE} = 6V	●	6	10	16	mA
	Gate Off Pull-Down Current to Ground	ΔV_{GATE} = 6V	●	0.5	1.5	2.5	mA
$t_{PHL(SENSE)}$	ΔV_{SNS} High to GATE Low Propagation Delay	ΔV_{SNS} = 0mV to 100mV Step, C = 10nF	●		0.5	1	µs
$t_{PHL(GATE)}$	UV, OV Turn Off Propagation Delay	GATE < 6V, Gate Open	●	0.3	1	3	µs
$t_{PHL(STRESS)}$	Propagation Delay to Turn Off Low Stress MOSFET in HSSS Mode	Gate Open	●		6	13	µs
Comparator Inputs							
V_{TH}	UV, OV, FB Threshold Voltage	Rising	●	2.5	2.56	2.62	V
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	280	360	440	mV
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	25	46	85	mV
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	60	80	100	mV
V_{TH}	UV Reset Threshold Voltage	Falling	●	0.95	1.00	1.05	V
$\Delta V_{UVR(HYST)}$	UV Reset Threshold Hysteresis		●	50	100	150	mV
I_{INPUT}	UV, OV, FB Input Current	V = 2.56V	●		0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FETBAD(TH)}$	V_{DD} – SOURCE FET-Bad Threshold		●	80	100	120	mV
$V_{STRESS(TH)}$	V_{DD} – SOURCE Low Stress Threshold		●	1.6	2	2.4	V
I_{SOURCE}	SOURCE Input Current	V_{SOURCE} = 48V	●	10	40	300	µA
$t_{DL(UV)}$	Debounce Turn-On Propagation Delay	UV Turn-On	●	30	40	50	ms
$t_{DL(OV)}$	Turn-On Propagation Delay	OV Turn-On	●		25	50	µs
$t_{DL(PG)}$	Power Good Delay		●		1	3	µs
$V_{CONFIG1/2}$	Input High Threshold		●	$INTV_{CC}$ – 0.8	$INTV_{CC}$ – 0.5	$INTV_{CC}$ – 0.2	V
	Input Low Threshold		●	0.2	0.5	0.8	V
I_{CONFIG}	CONFIG Sink or Source Current	CONFIG = 0 to $INTV_{CC}$	●			±20	µA
$V_{ISET(TH)}$	ISET Threshold Error	(Note 4)	●			±150	mV
I_{ISET}	ISET Input Current	V = 0, 5V	●		0	±1	µA
Other Pin and Functions							
V_{OL}	PG, FLT# Output Low Voltage	I = 2mA	●		0.3	0.4	V
I_{OH}	PG, FLT# Leakage Current	V = 80V	●		0	±1	µA
R_{VDSFB}	Resistance Between V_{DD} and V_{DSFB} Pins	Gate On	●	90	120	150	kΩ
I_{VDSFB}	V_{DSFB} Input Current	Gate Off	●		0	±1	µA
I_{COMM}	COMM Source Current	V = 2.5V, Gate On and in Current Limit	●	–3.5	–5	–6.5	µA
	COMM Sink Current	V = 2.5V, Gate Off	●	3			mA
$V_{COMM(SERVO)}$	COMM Servo Voltage	LSSS Start-Up	●	0.35	0.8	0.9	V
		Gate Fully On, Not in Current Limit	●	2.3	2.5	2.7	V
$V_{COMM(TH)}$	COMM High Threshold	In Current Limit	●	$INTV_{CC}$ – 2	$INTV_{CC}$ – 1.5	$INTV_{CC}$ – 0.85	V
	COMM Low Threshold	Gates On, Not in LSSS	●	0.9	1.4	1.9	V
	COMM LSSS Threshold	Gate On, in LSSS	●	0.1	0.2	0.3	V
$V_{TMR(H)}$	TMR, TMRFET High Threshold	Rising (Note 5)	●	2.50	2.56	2.62	V
$V_{TMR(L)}$	TMR, TMRFET Low Threshold	Falling (Note 5)	●	0.16	0.2	0.24	V
$I_{TMR(UP)}$	TMR (ILIM), TMRFET Pull Up Current	V_{TIMER} = 0V	●	–16.5	–20	–22	µA
	TMR (SOA) Pull Up Current	ΔV_{SNS} = 0V and $V_{DD} – V_{VDSFB}$ = 0V	●			±1	µA
		ΔV_{SNS} = 10mV and $V_{DD} – V_{VDSFB}$ = 6V	●	–90	–100	–110	µA
		ΔV_{SNS} = 20mV and $V_{DD} – V_{VDSFB}$ = 50mV	●	–2.5	–1.4	1	µA
$I_{TMR(DN)}$	TMR(ILIM) Pull Down Current	V_{TMR} = 2.56V	●	3	5	7	µA
$I_{TMRFET(DN)}$	TMRFET Pull Down Current	V_{TMRFET} = 2.56V	●	0.2	0.5	0.8	mA
D_{OC}	Overcurrent Auto-Retry Duty Cycle		●	0.04	0.08	0.12	%
D_{FETBAD}	FETBAD Auto-Retry Duty Cycle		●	0.8	1.6	2.4	%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive. All voltages are referenced to GND unless otherwise specified.

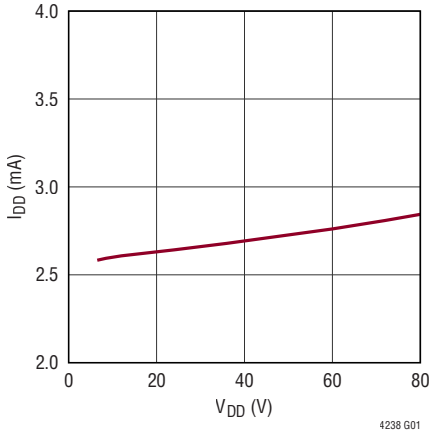
Note 3: Internal clamps limit the GATE pin to a minimum of 10V above or 0.3V below SOURCE. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: See Table 1 for more details.

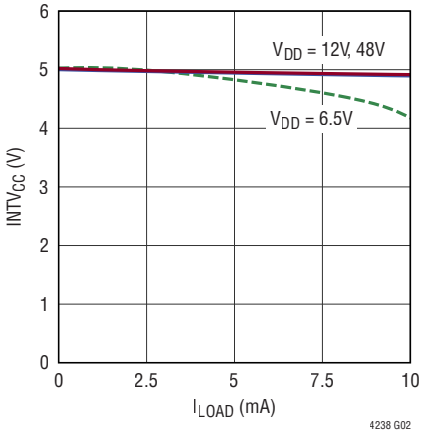
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 48V unless otherwise noted.

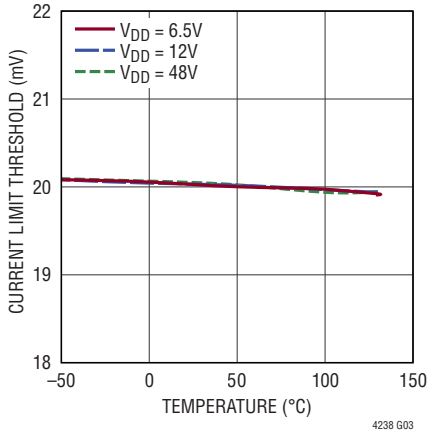
Supply Current vs Voltage



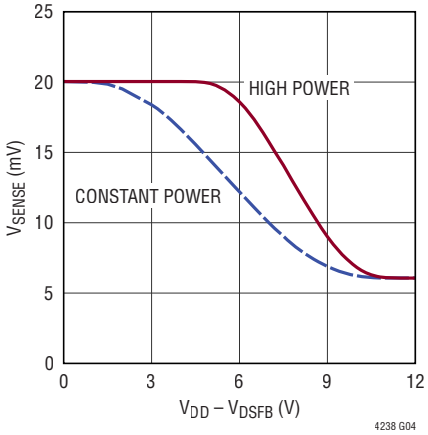
INTVCC Load Regulation



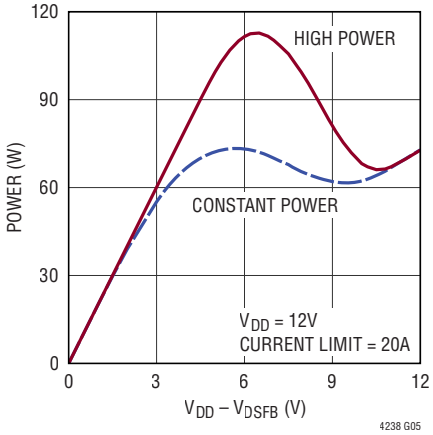
Current Limit Threshold vs Temperature



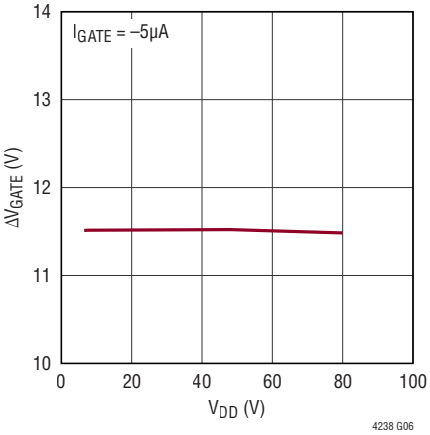
Current Limit Foldback Profiles



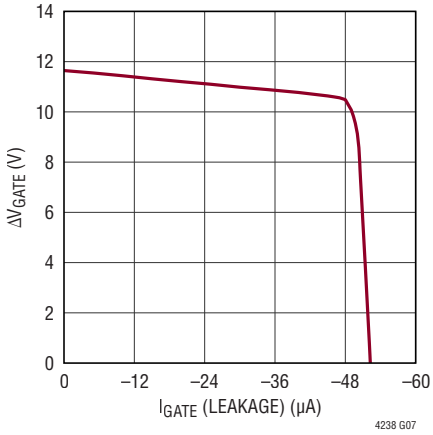
MOSFET Power Limit



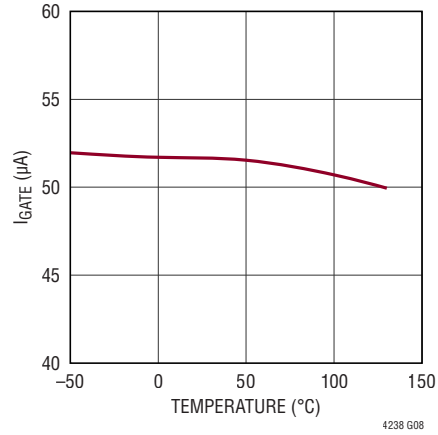
MOSFET Gate Drive vs V_{DD}



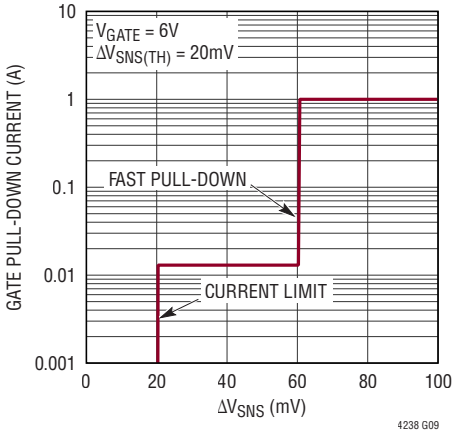
MOSFET Gate Drive vs Gate Leakage Current



MOSFET Gate Drive Pull-Up Current vs Temperature



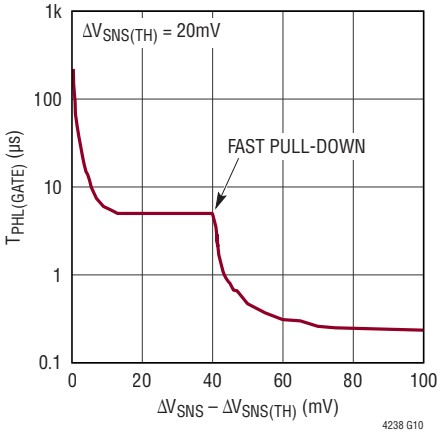
Gate Pull-Down Current vs Sense Input Voltage



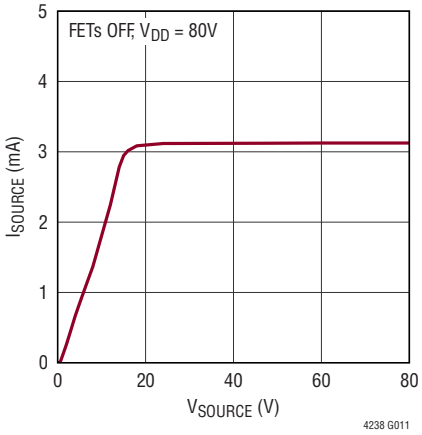
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 48V unless otherwise noted.

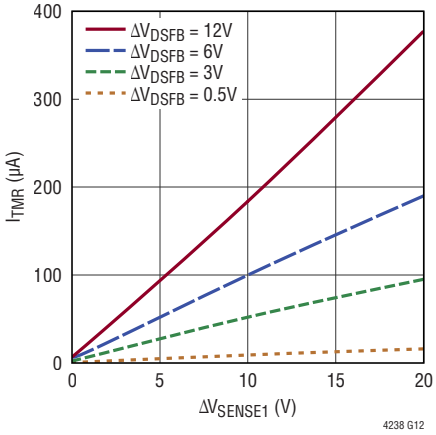
Current Limit Propagation Delay vs Overdrive



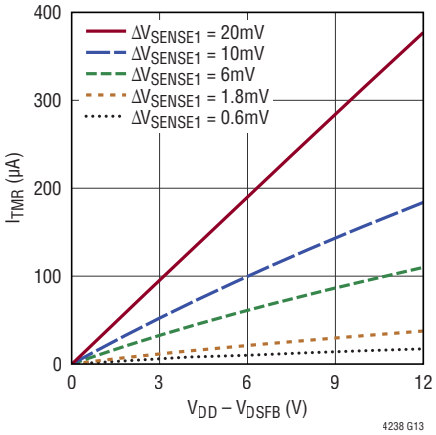
Source Pin Current vs Source Voltage



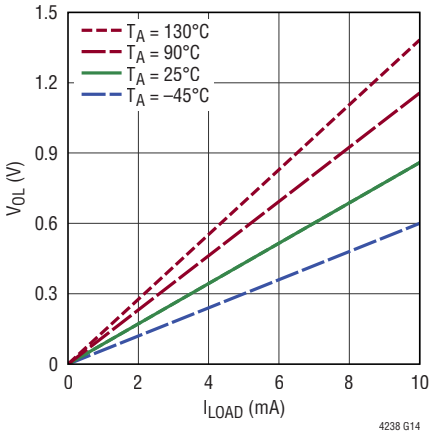
SOA Timer Pull-Up Current vs ΔV_{SENSE1}



SOA Timer Pull-Up Current vs $V_{DD} - V_{DSFB}$



PG and FLT# Output Low Voltage vs Load Current



PIN FUNCTIONS

COMM: Communication Input/Output. Coordinates turn on, turn off, and overcurrent faults between parts. Directly connect the COMM pins of a group of parts to operate them together. COMM may also be used as an ON status or current limit status indicator. May be pulled to ground with an open drain output to turn off the part. Leave open if unused.

CONFIG1, CONFIG2: Three State Configuration Inputs. Decoded to select one of nine possible configurations. These include single FET, High Stress Staged Start (HSSS), Parallel or Low Stress Staged Start (LSSS) modes, current limit profile and timer type for TMR pin (see Table 3).

FB: Power Good Comparator Input. Connect this pin to an external resistive divider from SOURCE to GND. If the FB voltage falls below 2.48V, the PG pin will pull low to indicate the power is bad.

FLT#: Over Current or FET Bad Fault Output. An open drain output that pulls low when the FET bad timer or current limit/SOA timer expires. Tie FLT# and UV together through a resistor to $INTV_{CC}$ to enable auto-retry (see Applications Information for details).

GATE1, GATE2: Gate Drives for External N-Channel MOSFETs. Internal 50µA current sources charge the gates of the MOSFETs. No compensation capacitors are required on the GATE pins, but a resistor-capacitor (RC) network from these pins to ground may be used to set the turn-on output voltage slew rate. During turn-off there is a 10mA pull-down current to SOURCE and a 1mA pull-down current to GND. During a short-circuit or undervoltage lockout (V_{DD} or $INTV_{CC}$), a 0.8A pull-down between GATE1/GATE2 and SOURCE is activated. If only one MOSFET is used, leave the GATE2 pin open and connect $SENSE2^+$ and $SENSE2^-$ to V_{DD}.

GND: Device Ground.

$INTV_{CC}$: Internal Supply Decoupling Output. Connect a capacitor no smaller than 0.1µF from this pin to ground. Up to 10mA may be drawn from this pin to power application circuitry. This pin is current limited and will drop to GND to reduce heating in an overcurrent condition. Overloading this pin can disrupt internal operation. This pin can be driven by an external supply that can only source, but not sink current.

ISET: Current Limit Adjustment Input. The ISET voltage is compared with seven threshold voltages generated by a resistive voltage divider from $INTV_{CC}$. The result sets the current limit voltage to be one of eight discrete values from 6mV to 20mV in 2mV increments. When ISET is connected to ground, the current limit threshold is set to 6mV. When ISET is connected to $INTV_{CC}$, current limit threshold is set to 20mV (see Table 1).

NC: No Connection. Not Internally connected.

OV: Overvoltage Comparator Input. Connect OV to an external resistive voltage divider from V_{DD} to GND. An overvoltage fault is detected if this pin rises above the 2.56V threshold. When the OV pin voltage falls back below the 2.51V falling threshold, the GATE pins will turn on again immediately. Tie to GND if unused.

PG: Power Good Output. An open drain output that pulls low when the FB pin drops below 2.48V indicating the power is bad. If the FB pin rises above 2.56V, $V_{DD} – V_{SOURCE}$ is lower than 2V, and the GATEs are fully enhanced, the open-drain pull-down releases the PG to go high.

$SENSE1^+$, $SENSE2^+$: Positive Kelvin Current Sense Input. Connect these pins to the V_{DD} side of the current sense resistor(s).

$SENSE1^–$, $SENSE2^–$: Negative Kelvin Current Sense Input. Connect this pin to the MOSFET side of the current sense resistor(s). The current limit circuit controls the GATE pin to limit the sense voltage between the $SENSE^+$ and $SENSE^–$ pins to the value selected by the ISET pin or less; depending on the voltage at the V_{DSFB} pin. Tie $SENSE2^–$ to V_{DD} when unused.

SOURCE: N-Channel MOSFET Source Connection. Connect this pin to the source of the external N-channel MOSFET switch. This pin provides a return for the gate pull-down circuit and is used as an input to the 100mV and 2V V_{DS} comparators which are used for FET-BAD faults and staged start timing, respectively.

PIN FUNCTIONS

TMR: Current Limit Timer or SOA Timer Output. The mode of operation is set by the state of CONFIG pins. In current limit timer mode, connect a capacitor between this pin and ground to set a 128ms/µF duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following a cool-down time of 150s/µF, resulting in a 0.08% duty cycle. In SOA timer mode, connect a RC network between this pin and ground. The current charging the RC network is proportional to the power dissipation in the powerpath, which is equal to ΔV_{SENSE1} multiplied by the voltage difference between the V_{DD} and SOURCE pins as measured at the V_{DSFB} pin.

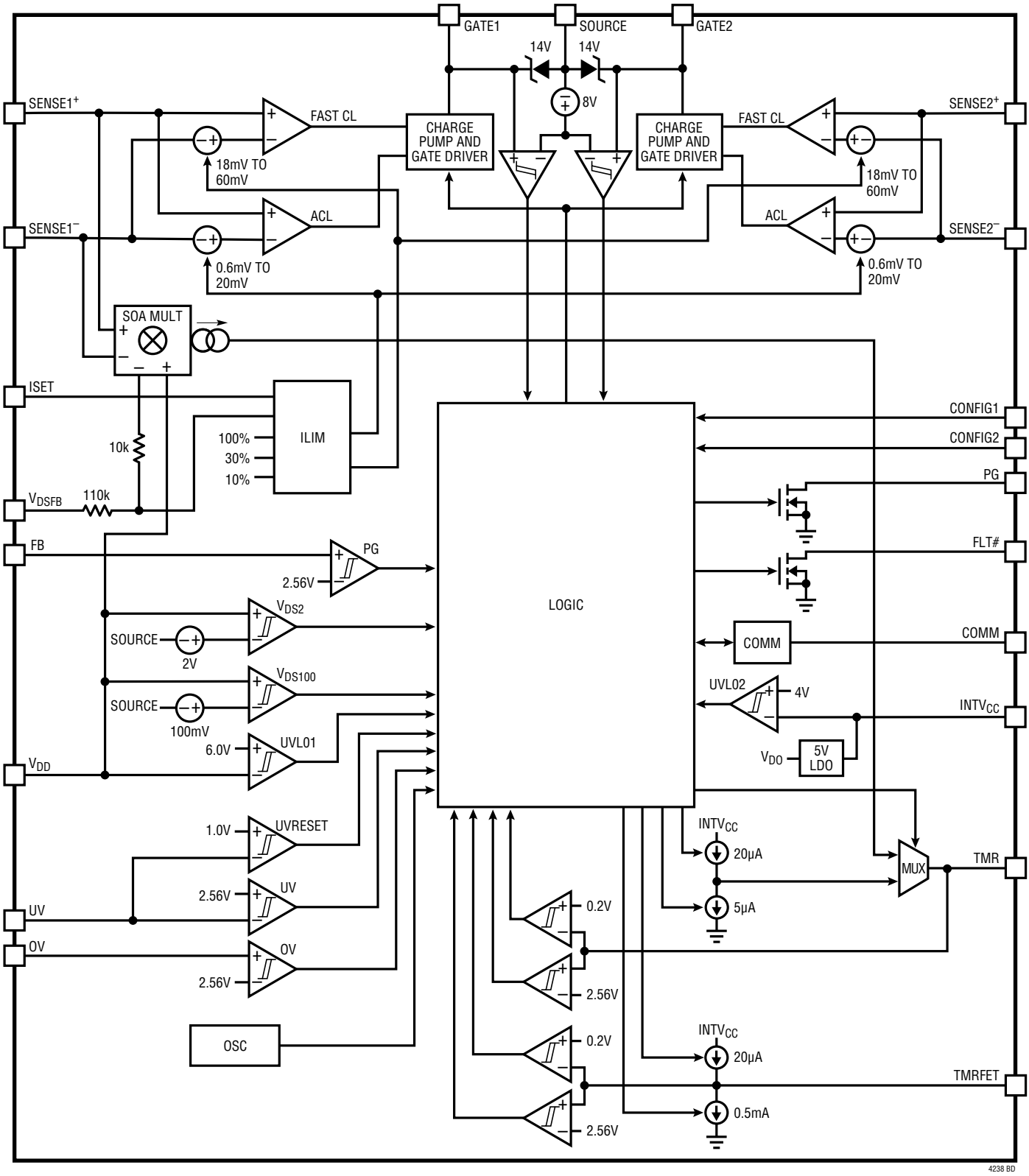
TMRFET: FET-Bad Timer Input. Connect a capacitor between this pin and ground to set a 128ms/µF duration for a FET-bad condition before the switch is turned off due to a FET-bad fault. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following a cool down time of 8s/µF, resulting in a 1.6% duty cycle. Tie to GND if unused.

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD} to GND. If the UV pin falls below 2.2V, an undervoltage is detected and the switch turns off. Pulling this pin below 1V resets the overcurrent and FET-bad faults and allows the switch to turn back on (see Applications Information for details). If overcurrent auto-retry is desired, then tie this pin to the FLT# pin. Tie to $INTV_{CC}$ if unused.

V_{DD}: Supply Voltage Input. This pin has an undervoltage lockout threshold of 6V. V_{DD} is an input for the FET-bad comparator with a 100mV threshold. It is also an input for the stress comparator with a 2V threshold.

V_{DSFB}: V_{DS} Foldback Sense Input. This pin is used to monitor the drain to source voltage of the external MOSFETs, which is used by the SOA timer to monitor MOSFET power, as well as set the foldback current limit. 12V systems may connect V_{DSFB} directly to the SOURCE pin. 48V systems will require an additional R_{VDSFB} resistor of 10kΩ/V for input voltage over 12V to set the proper gain of the SOA timer and foldback circuits.

BLOCK DIAGRAM



OPERATION

The LTC4238 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The device features four distinct operation modes: single driver mode, parallel mode, high stress staged start mode (HSSS), and low stress staged start mode (LSSS). Each of these modes addresses specific application requirements for Safe Operating Area (SOA), $R_{DS(ON)}$, and cost.

The Block Diagram shows the monitoring blocks of the LTC4238. First, two undervoltage lockout circuits, UVLO1 and UVLO2, validate the input supply and the internally generated 5V supply, INTVCC. UVLO2 also generates the power-up initialization to the logic. The undervoltage (UV), and overvoltage (OV) comparators determine if the external conditions are valid prior to turning on the GATEs.

In normal operation, the LTC4238 turns on the external N-channel MOSFETs after a startup debounce delay, passing power to the load. A precise current limit value can be set from 6mV to 20mV in 2mV steps using the ISET voltage. During startup, the voltage between $SENSE^+$ and $SENSE^-$ may be controlled to be no higher than 10% of the current limit threshold or to the current limit threshold with foldback. The startup current may be set to even lower values with an external gate RC network.

An overcurrent fault at the output may result in excessive MOSFET power dissipation during Active Current Limiting (ACL). To limit this power in each channel, the ACL amplifiers regulate the voltage between $SENSE1^+$, $SENSE1^-$ and $SENSE2^+$, $SENSE2^-$ pins by reducing the GATE-to-SOURCE voltages in an active control loop when the sense voltages exceed the current limit value. When the MOSFET's drain to source voltage is high, power dissipation is further reduced by folding back the current limit to 30% of nominal based on foldback. In the event of a catastrophic output short, fast current limit comparators immediately pull the GATE pins down with 0.8A when the sensed current is three times the nominal current limit.

The LTC4238 provides two ways of limiting the time the system is exposed to overstress conditions: a MOSFET SOA timer or a current limit timer. The timer selection is made via the CONFIG pins. If the MOSFET SOA timer is chosen, the TMR pin is pulled up by a current that is proportional to the power dissipation in the MOSFET driven by GATE1. With an RC network representing the thermal behavior of this MOSFET, the TMR voltage is proportional to the MOSFET temperature rise. When the TMR voltage reaches its threshold of 2.56V (representing $T_{J(MAX)}$ of the MOSFET), the overcurrent fault is triggered. Both GATEs turn off to protect the MOSFETs based on their SOA. If the current limit timer is chosen, the TMR pin is configured to drive a single capacitor and ramps up with 20µA when active current limiting is engaged. If the TMR pin reaches its 2.56V threshold, the LTC4238 turns off both GATEs and FLT# pin pulls low to indicate a fault. Then the TMR pin ramps down using a 5µA current source until the voltage drops below 0.2V. After that, the TMR pin will ramp up and down 256 times with 20µA/5µA to allow the pass transistor to cool down. If overcurrent auto-retry is enabled by tying the FLT# pin to the UV pin, the LTC4238 will turn on again at the end of 256 timer cycles.

The output voltage is monitored using the FB pin and the Power Good (PG) comparator to determine if the power is ready for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

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A typical LTC4238 application is a high availability system in which a positive voltage supply is distributed to power individual hot-swapped cards.

In the following sections, the parallel mode is first chosen to demonstrate common functions and basic hot-swap applications. The unique features and applications of each operation mode are then described separately. A basic 48V, 40A LTC4238 application circuit is shown in Figure 1. The power supply on a board is controlled by using two pairs of N-channel pass transistors, M1A-B and M2A-B, placed in the power path. Resistors R_{S1} and R_{S2} sense current through M1A-B and M2A-B. Resistors R1, R2 and R3 define undervoltage and overvoltage levels. R_{G1-4} prevent high frequency self-oscillations in the MOSFETs. R7 and R8 set the power good threshold, and R6 scales current limit foldback to the intended operating voltage.

The following sections cover turn-on, turn-off and various faults that the LTC4238 detects and acts upon. External component selection is discussed in detail in the Design Examples section.

Turn-On Sequence

Several conditions must be met before the external MOSFETs turn on. First the external supply, V_{DD}, must exceed its 6.0V undervoltage lockout level. Next, the internally generated supply, $INTV_{CC}$, must cross its 4V undervoltage threshold. This generates a power-on-reset pulse.

After a power-on-reset pulse, the UV and OV pins verify that input power is within the acceptable range. The state of the UV comparator must be stable for at least 40ms to qualify for turn-on. The MOSFETs are then turned on by charging up the GATE pins with 50µA current sources. When the GATE voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on and the SOURCE voltage then follows the GATE voltages as it increases.

While the MOSFETs are turning on, the power dissipation in current limit for each MOSFET is limited to the

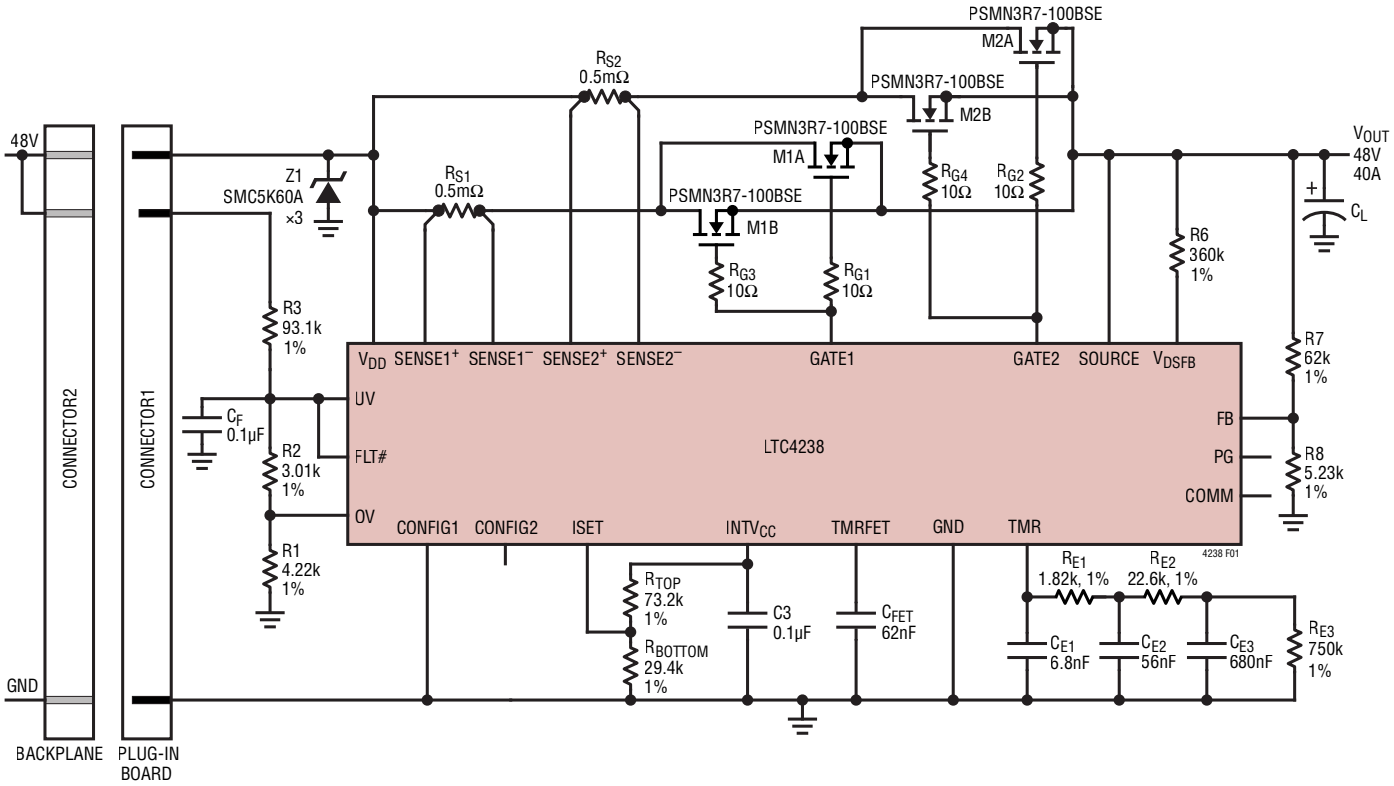

Figure 1. 48V, 40A Hot Swap Controller with SOA Timer in Parallel Mode

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foldback profile as shown in Figure 2. As the SOURCE voltage rises, the V_{DSFB} and FB pins follow as set by R6, R7 and R8. Once the MOSFET drain to source voltage is lower than its 2V threshold, both GATE pins are higher than their 8V thresholds, and the FB pin has exceeded its

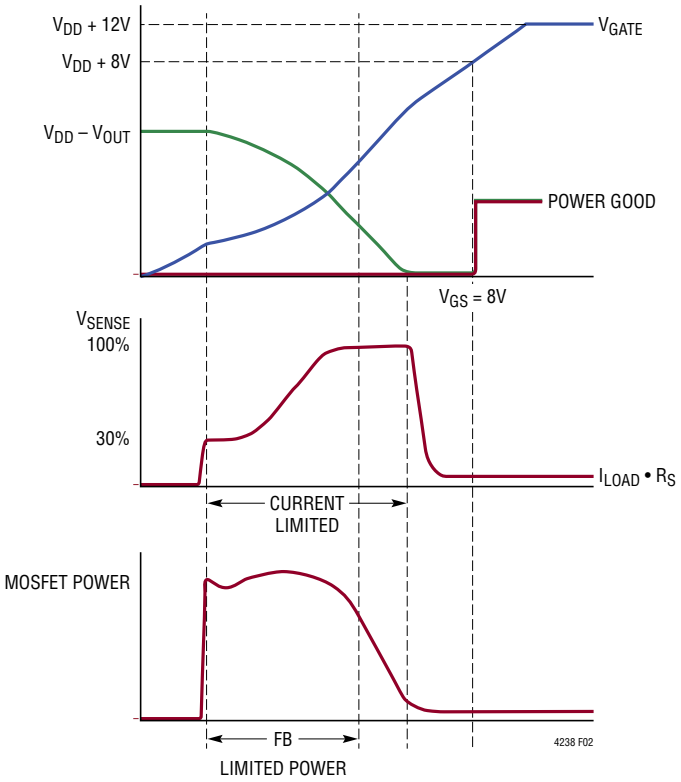

Figure 2. Power-Up Waveforms

2.56V threshold, then the PG pin releases high to indicate power is good and the load may be activated.

In normal operation, the minimum GATE-to-SOURCE (ΔV_{GATE}) drive voltage is 10V. The ΔV_{GATE} voltage is clamped below 14V to protect the gates of 20V N-channel MOSFETs. A curve of ΔV_{GATE} drive versus V_{DD} is shown in the typical performance characteristics.

Turn-Off Sequence

A normal turn-off sequence is initiated by card removal when the backplane connector short pin opens, causing the UV or OV comparator output to change state. Additionally, several fault conditions can turn off the GATEs. These include an input overvoltage, input undervoltage, overcurrent or FET-bad fault.

The MOSFETs are turned off with 10mA from GATE to SOURCE and with 1mA currents pulling the GATE pins to ground. With the MOSFET turned off, the SOURCE and FB voltages drop as the load capacitance discharges. When the FB voltage crosses below its threshold, PG pulls low to indicate that the output power is no longer good. If the V_{DD} pin falls below 5.5V or $INTV_{CC}$ drops below the undervoltage lockout falling threshold of 3.89V, a fast shut down of the MOSFET is initiated. The GATE pins are then pulled down with 0.8A currents to the SOURCE pin.

Overcurrent Protection

The LTC4238 features two levels of protection from short-circuit and overcurrent conditions. Load current is monitored by the $SENSE^+$ and $SENSE^-$ pins across the current sense resistors. There are two distinct thresholds for the current sense voltages, an active current limit threshold and a fast current limit comparator threshold. The fast current limit comparator threshold is always three times the nominal current limit threshold. If the sense voltage of a channel reaches the current limit threshold, the corresponding GATE is pulled down until the associated active current limit loop is engaged. In the event of a catastrophic short-circuit or a sudden input step, where the sense voltage of a channel reaches the fast current limit comparator threshold, the corresponding GATE is immediately pulled to SOURCE to limit peak current through the MOSFET. When the sense voltage drops to the current limit threshold, the active current limit loop is engaged.

Current Limit Foldback

The LTC4238 features an adjustable current limit with foldback that protects the MOSFETs from excessive power dissipation. During active current limiting, the available current is reduced as a function of the voltage across MOSFET sensed by V_{DD} and V_{DSFB} pins. The higher the voltage across MOSFET, the lower the current limit threshold will be. The lowest foldback value after start-up is 30% of the nominal voltage.

The nominal voltage of the LTC4238 current limit threshold is set between 6mV and 20mV in 2mV steps via the ISET pin (Table 1). This can be used to achieve a given current limit with the limited selection of standard sense

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resistor values available around 1mΩ. Threshold values as low as 6mV reduce power dissipation in sense resistors for high current applications.

Two current limit foldback profiles are available to meet different application needs, constant power and high power. Refer to Table 3 for foldback configurations. The constant power profile is shaped such that the power in the MOSFET is constant while current limiting, regardless of V_{DS}. This simplifies the SOA design of the application and makes the safe dissipation time a constant for various voltage and current conditions. This works well with the current limit timer on the TMR pin. However, the constant power foldback profile starts to fold back at small V_{DS}, which could occur during an input step. For that reason the high power profile is also available. It doesn't start to fold back until the V_{DS} is around 50% of the nominal input voltage. This prevents the current limit from folding back after an input step and collapsing the output because it is less than the load current. Since the power dissipation in the MOSFET is not constant for the high power profile, the worst-case power dissipation usually occurs when half of the nominal supply voltage is across the MOSFET. Graphs in the Typical Performance Characteristics show the current limit and power versus voltage across the MOSFETs.

Additionally, to ease start-up, the LTC4238 features a configurable option for a start-up current at 10% of the full current limit. The LTC4238 stays at 10% until the conditions for power good are met, at which point it will switch to the normal foldback profile and current limit. In many cases this will eliminate the need for an RC network on the GATEs of the MOSFETs to limit the inrush current. Configurations using the 10% current limit for start-up all use the SOA timer. This timer provides the flexibility to allow a long current limit timeout at low power levels during start-up, and a short current limit timeout during a fault after start-up.

Constant Current Start-Up Using GATE RC Networks

An optional series RC network from GATE to GND (R_G and C_G in Figure 5) provides an inrush current less than the current limit by limiting the slew rate of the GATE pin. The current limit timer will not run since the current limit is not engaged during start-up. Thus, a small timer capacitor may be used which allows the use of MOSFETs with smaller SOA. Power good will signal when the FB pin crosses its 2.56V threshold and the ΔV_{GATE} voltages cross their 8V thresholds. When both those conditions are met and the impedance back to the supply through the MOSFET is low, the output voltage is suitable for the load to be turned on. PG voltage goes high to indicate power is good. R_G should be chosen such that $I_{GATE} \bullet R_G$ is less than the threshold voltage of the MOSFET to avoid an initial inrush current spike. But increasing R_G improves the stability of the current limit servo loop (see Applications Information on current limit stability). If the voltage of the 50µA I_{GATE} current across R_G is higher than MOSFET's threshold, a diode may be added in parallel with the large R_G to limit its voltage while charging up C_G (see Figure 5). For the staged-start architectures, an RC network may be used on a trickle MOSFET or stress MOSFET. In the parallel architecture, identical RC networks may be used on both MOSFETs. Bypass MOSFETs don't need the current

Table 1. ISET Pin Voltage* vs Current Limit Thresholds and Suggested 1% Resistor Values

$\Delta V_{SNS(TH)}$ (mV)	V_{ISET} (V)	I_{SET} Thresholds Compared with		R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	$R_{BOTTOM}/(R_{TOP} + R_{BOTTOM})$
		Lower (V)	Upper (V)			
6	0		0.357	Open	Short	0.000
8	0.714	0.357	1.071	88.7	14.7	0.143
10	1.429	1.071	1.786	73.2	29.4	0.286
12	2.143	1.786	2.5	59.0	44.2	0.429
14	2.857	2.5	3.214	44.2	59.0	0.571
16	3.571	3.214	3.929	29.4	73.2	0.714
18	4.286	3.929	4.643	14.7	88.7	0.857
20	5	4.643		Short	Open	1.000

*$INTV_{CC}$ = 5V is used for this table.

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limiting function of an RC network, but an RC network may be used in low stress staged start to improve the undershoot recovery time of the bypass MOSFET(s).

Current Limit Stability

For many applications the LTC4238 current limit loop is stable without additional components. However, there are certain conditions where additional components may be needed to improve stability. The dominant pole of the current limit circuit is set by the capacitance at the gate of the external MOSFET, and larger gate capacitance makes the current limit loop more stable. Usually a total of 10nF GATE-to-SOURCE capacitance is sufficient for stability and is provided by inherent MOSFET C_{GS}. The stability of the loop is degraded by reducing the size of the resistor on a gate RC network if one is used, which may necessitate additional GATE-to-SOURCE capacitance. The worst case for current limit stability occurs when the output is shorted to ground after a normal start-up. Board level short-circuit testing is highly recommended as board layout can also affect transient performance.

Parasitic MOSFET Oscillations

Not all circuit oscillations can be ascribed to the current limit loop. Some higher frequency oscillations can arise from the MOSFETs themselves. (See Rarely Asked Questions 151, High-Side Current Sensing). There are two possible parasitic oscillation mechanisms. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with gate resistors RG1 – RG4 as shown in Figure 1. In some applications, one may find that these resistors help in short-circuit transient recovery as well. However, too large of a resistor will slow down the turn-off time. The recommended RG1 – RG4 range is between 5Ω and 500Ω. 10Ω provides stability without affecting turn-off time. These resistors must be located next to the MOSFET gate pin with no other connections between them.

A second type of parasitic oscillation occurs at frequencies between 200kHz and 800kHz when the MOSFET source is loaded with less than 10µF, and the drain is fed with an inductive impedance such as contributed by wiring inductance. To prevent this second type of oscillation, load the source with more than 10µF and bypass the input supply with a series 10Ω, 100nF snubber to ground.

Overcurrent Fault with a Basic Current Limit Timer

During active current limit, the power dissipation in the MOSFET is large. If this power dissipation persists, the MOSFET can reach temperatures that cause damage. A basic current limit timer has a single capacitor connected between TMR pin and GND and sets a maximum time for the MOSFET to operate in a current limit mode. When this timer expires, an over current fault is generated and the MOSFET is turned off to protect it from overheating.

Current limiting begins when the current sense voltage between the $SENSE^+$ and $SENSE^-$ pins reaches the current limit threshold level (which depends on foldback and the voltage of the ISET pin). The corresponding GATE pin is then pulled down and regulated to limit the current sense voltage to the current limit value. In parallel mode, if either GATE is in current limit during start-up then the current limit timer starts to run. The external timer capacitor at the TMR pin will be charged with a 20µA pull-up current. After start-up, only when both GATE pins are regulated in current limit will the current limit timer start to run. If at least one of the GATE pins stops limiting current before the TMR pin reaches the 2.56V threshold, then the TMR pin will discharge with 5µA. For HSSS, LSSS or Single Driver Modes, if the current sense voltage between the $SENSE1^+$ and $SENSE1^-$ pins reaches the current limit threshold level, then the current limit timer will start to run. For a given current limit time delay, t_{ACL}, use Equation 1 for setting the timing capacitor's value:

$$C_{TMR} = t_{ACL} \bullet 8[nF/ms] \quad (1)$$

When the TMR pin reaches its 2.56V threshold, the LTC4238 turns off both GATEs and generates an overcurrent fault. The MOSFETs are turned off with a 10mA current from GATE to SOURCE and a 1mA current from GATE to ground. Open-drain output FLT# also pulls low. After the fault, the TMR pin begins discharging with a 5µA pull-down current. When the TMR pin reaches its 200mV low threshold, it will cycle up with 20µA and down with 5µA 256 times to give the MOSFETs time to cool.

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An overcurrent fault may be cleared by pulling the UV pin below its 1V UV reset threshold, which happens automatically if FLT# is tied to the UV pin. Once the TMR completes the cool down delay, the MOSFETs turn on if the fault has been cleared. The cool down time is 150s/µF, resulting in a 0.08% duty cycle.

MOSFET manufacturers specify the safe limits on operating voltage, current and time as a set of curves referred to as the Safe Operating Area (SOA). The proper timer capacitance must be set to allow the worst-case operating condition to stay within the SOA limits. The worst-case operating condition could be completely charging a large bypass capacitor at the output during start-up, or riding through a large input step. With a basic current limit timer, once a timer capacitance is set, the MOSFET must be selected to withstand the worst-case SOA condition that occurs during any possible normal operating condition or fault condition.

The waveform in Figure 3 shows how the output turns off following a short circuit.

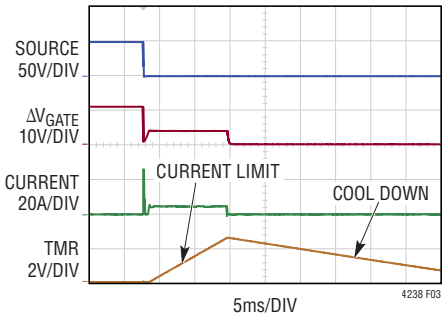

Figure 3. GATE1, SOURCE, TMR Current vs Time

Overcurrent Fault with the SOA Timer

The LTC4238 features another mode for the TMR pin, SOA Timer, which better protects the MOSFET(s) when the power dissipated in the MOSFET varies widely. Instead of a constant 20µA current, the TMR outputs a current proportional to the power dissipation in the MOSFET driven by GATE1 and the 5µA internal TMR pull-down current is disabled. The assumption is made that in parallel mode the MOSFETs of both channels see the similar stresses. In other modes, the MOSFET at channel 1 sees more stress. The mode of TMR pin is configured using the CONFIG pins.

The SOA timer requires an RC network representing the MOSFET thermal model to be connected to TMR (Figure 1). At least two resistors and two capacitors are required for minimum accuracy of the thermal behavior. More RC elements provide better accuracy. Thus, the cost and board area are larger than the single-capacitor timer. The SOA timer voltage represents the real time rise in the junction temperature of the channel 1 MOSFET and its trip threshold 2.56V represents the maximum allowable peak temperature of the MOSFET. With the SOA timer, the selection of MOSFETs is much simpler: they just need to meet the worst-case operation requirements. In fault conditions such as output short, the SOA timer automatically protects the MOSFETs by turning them off once the maximum allowable peak temperature is reached (TMR tripped). With the single capacitor timer, the minimum capacitor must first be selected to keep the MOSFETs on during worst-case operating conditions, then the MOSFETs must be selected to withstand the worst-case SOA conditions during normal operating and fault conditions. The cost of MOSFETs selected based on the single capacitor timer for parallel mode or high stress staged start mode may be substantially higher than that using the SOA timer. It is recommended to use the SOA timer for high power applications using parallel mode or high stress staged start mode, especially for those with large input steps.

During all modes of operation an internal multiplier drives TMR with a current proportional to V_{SENSE1} multiplied by the voltage difference between V_{DD} and SOURCE pin as measured the V_{DSFB} pin (Equation 2).

$$I_{TMR} = \frac{400\mu A \bullet V_{SENSE1} \bullet (V_{DD} - V_{DSFB})}{20mV \bullet 12V} \quad (2)$$

For example, it produces 100µA when V_{SENSE1} = 10mV and $V_{DD} - V_{DSFB}$ = 6V. When the TMR voltage crosses its 2.56V threshold, the MOSFETs are shut off and an overcurrent fault is detected. When the multiplier output current is low, the TMR voltage drops as the RC network discharges. When it drops below 0.2V, Overcurrent Fault is cleared and MOSFETs can turn on if FLT# is connected to UV.

In order for the SOA timer to work properly, 12V is expected between V_{DD} and V_{DSFB} when V_{DD} is at its nominal and SOURCE is at ground. There is 120k of resistance

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internally from V_{DD} to V_{DSFB}. For 12V systems, V_{DSFB} should be simply connected to SOURCE. For input voltages larger than 12V, add a resistance of 10kΩ/V between the V_{DSFB} and SOURCE pins. For example, for 48V systems, a 360k resistor is required to be added between the two pins.

Note that the SOA timer is independent of the current limit set via the ISET pin. The current limit may be adjusted with the ISET pin without the need to modify the thermal RC network. However, if the sense resistor value is changed, a modified thermal RC network will be required. Using a large current limit threshold, such as 20mV, achieves the greatest accuracy and dynamic range from the SOA timer. Refer to Typical Performance Characteristics for the SOA TMR pull-up currents at different ΔV_{SENSE1} and different $V_{DD} – V_{DSFB}$ voltages.

The configuration of the thermal RC network for a particular MOSFET starts with the selection of a desired number of resistive and capacitive elements. Their values are decided based on the thermal impedance plot provided by the MOSFET manufacturer. Three resistors and three capacitors are usually enough to fit the plot fairly well from 10µs to 100ms (Figure 1), which covers the timing range of typical operating and fault conditions. If better fitting accuracy or wider fitting range is desired, more elements may be used. After the thermal RC network is configured, the thermal quantities are then converted to electric quantities according to Equation 3.

$$R_E = k \bullet R_\theta$$
$$C_E = \frac{C_\theta}{k} \quad (3)$$

where R_E and C_E are electric resistance and capacitance, respectively and R_θ and C_θ are thermal resistance and capacitance, respectively. The conversion constant k is given by Equation 4.

$$k = \frac{V_{DS,MAX} \bullet I_{D,MAX}}{I_{TIMER(UP),MAX}} \bullet \frac{V_{TIMER(TH)}}{\Delta T_{MAX}} \quad (4)$$

- $V_{DS,MAX}$ = The Maximum drain-to-source voltage that results in V_{DSFB} at 12V below V_{DD}.
- $I_{D,MAX}$ = $20mV/R_{SENSE1}$.
- $I_{TIMER(UP),MAX}$ = The TMR pull-up current corresponding to the maximum power dissipation.

  $P_{MAX} = V_{DS,MAX} \bullet I_{D,MAX}$
- $V_{TMR(TH)}$ = TMR rising threshold (2.56V).
- ΔT_{MAX} = The Maximum allowable temperature rise of the MOSFET.

For example, if $V_{DS,MAX}$ = 58V, $I_{D,MAX}$ = 40A, $I_{TMR(UP),MAX}$ = 400µA and ΔT_{MAX} = 110°C (175°C T_{JMAX} – 65°C T_A), k = $1.4 \bullet 10^5$ [V^2/°C]. A thermal RC network consisting of three resistors and capacitors that represent the thermal behavior of PSMN3R7-100BSE is shown in Figure 1.

FET-Bad Fault and Auto-Retry

A damaged MOSFET may have leakage from gate to drain or have degraded $R_{DS(ON)}$. Debris on the board may also produce leakage or a short from the GATE pin to the SOURCE pin, the MOSFET drain, or to ground. In these conditions the LTC4238 may not be able to pull the GATE pin high enough to fully enhance the MOSFET, or the MOSFET may not reach the intended $R_{DS(ON)}$ when the GATE pin is fully enhanced. This can put the MOSFET in a condition where the power in the MOSFET is higher than its continuous power handling capability, even though the current is below the current limit.

The LTC4238 monitors the integrity of the MOSFETs in two ways, and acts on both of them in the same manner. First, the LTC4238 monitors the voltage between the V_{DD} and SOURCE pins. A comparator detects a high DRAIN-to-SOURCE voltage (V_{DS}) whenever V_{DD} to SOURCE voltage is greater than 100mV. Second, the LTC4238 monitors the GATE voltage. The GATE voltage may not fully enhance with a damaged MOSFET. A gate low condition is detected if Gate-to-Source voltage is lower than 8V, and that channel is not in active current limit.

When either a high DRAIN-to-SOURCE voltage or a gate low condition is present for either or both MOSFETs while they are commanded on, the FET-bad timer starts to run. The logic determining FET-bad condition is in Figure 4. The external timer capacitor on the TMRFET pin is charged with a 20µA pull-up current. When the timer reaches the 2.56V rising threshold, a FET-bad fault condition is set, the

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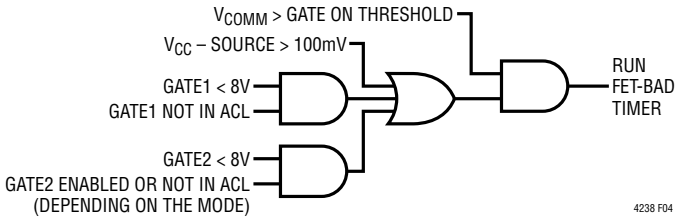

Figure 4. LOGIC Diagram for FET-Bad Timer

part turns off, and the GATE pins are pulled low with 10mA to SOURCE and 1mA to ground. If the DRAIN-to-SOURCE voltage falls below 100mV and the GATE low conditions are cleared before the TMRFET reaches 2.56V threshold, the TMRFET pin will discharge with 500µA. For a given FET-bad time delay, $t_{FET-BAD}$, use Equation 5 for setting the timing capacitor's value:

$$C_{TMRFET} = t_{FET-BAD} \bullet 8[nF/ms] \quad (5)$$

Note that during start-up, the V_{DS} high condition is present because the voltage from drain-to-source is greater than 100mV. To avoid undesired turn-off, the FET-bad timer duration must be long enough for the largest allowable load to start up. FET-bad faults are disabled by grounding the TMRFET pin.

The LTC4238 treats a FET-bad fault similar to an overcurrent fault. If a FET-bad fault is detected, the MOSFETs are turned off and the TMRFET pin begins discharging with a 500µA pull-down current. When the TMRFET pin reaches its 0.2V threshold, it will cycle up with 20µA and down with 500µA 64 times to allow the MOSFET time to cool down. When automatically retrying with FLT# pin tied to UV pin, the resulting FET-bad duty cycle is 1.6%. After the final time the TMRFET pin falls below its 0.2V low threshold the MOSFETs are allowed to turn on again.

Undervoltage and Overvoltage Faults

The UV pin can be used to monitor a supply undervoltage condition using an external resistive voltage divider. An undervoltage fault occurs when the UV voltage falls below its 2.2V falling threshold. An overvoltage fault occurs when the OV voltage goes above its rising threshold of 2.56V. When either an undervoltage or overvoltage fault occurs, the LTC4238 shuts off the GATE pins with a 10mA current to SOURCE and a 1mA current to ground.

If the UV voltage subsequently rises back above the threshold for 40ms, the GATEs can turn on again. If the OV voltage subsequently falls back below the threshold, the GATEs can turn on again immediately. The UV and OV signals may be filtered by placing a capacitor, C_F, between the UV pin and GND.

Dual Gate Operation Modes

The LTC4238 features dual gate drivers that are configured by the CONFIG1 and CONFIG2 pins into four distinct operation modes: single driver, parallel, high stress staged start (HSSS), and low stress staged start (LSSS). As shown in Table 2, each mode features specific SOA or $R_{DS(ON)}$ benefits, GATE(s) on/off behavior, power good signaling and fault detection logic.

All modes except LSSS support starting up with a resistive load such as a heating element or incandescent lamp. The modes of the dual gate drivers are selected together with the foldback profile and TMR behavior by the status of CONFIG1 and CONFIG2 pins as shown in Table 3.

Parallel

High current applications often demand several power MOSFETs in parallel to reach a target $R_{DS(ON)}$ under 1mΩ that is unavailable in a single MOSFET. In addition, dividing the load current amongst multiple devices alleviates the PCB current crowding problem with the use of a single MOSFET.

Parallel MOSFETs share current well when their GATE-to-SOURCE voltages are fully enhanced. However, when the MOSFETs are limiting current, the mismatch between gate thresholds will cause the MOSFET with the lowest threshold to carry more current than the others. Since threshold voltage has a negative temperature coefficient, as this MOSFET heats it may carry even more current. Eventually all the load current may be carried by a single MOSFET. For this reason, when a group of MOSFETs are operated in parallel only the SOA (Safe Operating Area) of a single MOSFET is guaranteed.

The LTC4238 resolves this problem by offering two gate drivers, each with an independent current limit circuit and associated current sense pins. For configuration 4, 7, 8, and 9 as shown in Table 3, these two gate drivers operate

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Table 2. LTC4238 Dual-Gate Operation Modes

MODE		SINGLE DRIVER	PARALLEL	HIGH STRESS STAGED START	LOW STRESS STAGED START
FEATURE		Simple	SOA Doubled, $R_{DS(ON)}$ Halved	GATE1 Drives High SOA MOSFET. GATE2 Drives Low $R_{DS(ON)}$ MOSFET	GATE1 Drives Low $R_{DS(ON)}$, Small SOA MOSFET. GATE2 Drives Small SOA MOSFET
TURN-ON SEQUENCE			GATE1 and GATE2 Turn on at the Same Time	GATE1 Turns on First. GATE2 Turns on after GATE1 Turns High and $V_{DD} - V_{SOURCE} < 2V$ and Channel 1 Is Not in ACL	GATE 2 Turns on First. GATE1 Turns on if $V_{FB} > 2.56V$ Once GATE2 Turns High
POWER GOOD LATCH	SET	V_{DD} – SOURCE < 2V, and $V_{FB} > 2.56V$, and $\Delta V_{GATE1} > 10V$, and ($\Delta V_{GATE2} > 10V$ or Disabled)			
	RESET	FB Drops Below 2.48V			FB Drops Below 2.48V or V_{COMM} Drops Below 0.2V
GATE1 TURN-OFF		$V_{COMM} < 1.4V$			$V_{COMM} < 0.2V$ or $V_{FB} < 2.56V$
GATE2 TURN-OFF		$\Delta V_{GATE1} < 8V$ or V_{DD} – SOURCE > 2V or Channel 1 is in ACL	$V_{COMM} < 1.4V$	$\Delta V_{GATE1} < 8V$ or V_{DD} – SOURCE > 2V or Channel is 1 in ACL	$V_{COMM} < 0.2V$
CURRENT LIMIT TIMER		Runs if $V_{COMM} > 3.5V$ or Channel 1 is in ACL	Runs if $V_{COMM} > 3.5V$ or During Start-Up: Either Channel Is in ACL After Start-Up: Both Channels are in ACL	Runs if $V_{COMM} > 3.5V$ or Channel 1 is in ACL	Runs if $V_{COMM} > 3.5V$ or Channel 1 is in ACL
FET BAD TIMER		Runs if $V_{COMM} > 1.4V$ and [(V_{DD} – SOURCE > 100mV) or ($\Delta V_{GATE1} < 8V$ and Not in ACL) or ($\Delta V_{GATE2} < 8V$ and Enabled)]	Runs if $V_{COMM} > 1.4V$ and [(V_{DD} – SOURCE > 100mV) or ($\Delta V_{GATE1} < 8V$ and Not in ACL) or ($\Delta V_{GATE2} < 8V$ and Not in ACL)]	Runs if $V_{COMM} > 1.4V$ and [(V_{DD} – SOURCE > 100mV) or ($\Delta V_{GATE1} < 8V$ and Not in ACL) or ($\Delta V_{GATE2} < 8V$ and Enabled)]	Runs if $V_{COMM} > 0.2V$ and [(V_{DD} – SOURCE > 100mV) or ($\Delta V_{GATE1} < 8V$ and Not in ACL) or ($\Delta V_{GATE2} < 8V$ and Not in ACL)]

Table 3. LTC4238 Configurations

CONFIGURATION	CONFIG2	CONFIG1	DUAL-GATE MODE	FOLDBACK PROFILE	TMR PIN TYPE	10% FOLDBACK DURING START-UP
1	Ground	Ground	HSSS/Single	High Power	Current Limit Timer	No
2	Ground	Open	HSSS/Single	Constant Power	SOA Timer	Yes
3	Ground	$INTV_{CC}$	HSSS/Single	High Power	SOA Timer	No
4	Open	Ground	Parallel	High Power	SOA Timer	No
5	Open	Open	LSSS	Constant Power	SOA Timer	No
6	Open	$INTV_{CC}$	LSSS	Constant Power	Current Limit Timer	No
7	$INTV_{CC}$	Ground	Parallel	Constant Power	SOA Timer	Yes
8	$INTV_{CC}$	Open	Parallel	Constant Power	SOA Timer	No
9	$INTV_{CC}$	$INTV_{CC}$	Parallel	High Power	Current Limit Timer	No

in parallel mode, in which GATE1 and GATE2 are turned on or off simultaneously. In this mode, the LTC4238 allows a group of parallel MOSFETs to be divided into two channels. During current limiting in an overcurrent event such as output short or input step, the independent gate control of the two channels divides the current evenly between them, resulting in twice the SOA performance of a Hot Swap controller with a single current limit circuit. This allows the use of smaller, less expensive MOSFETs, can start up a load twice as big, or increase SOA margins. In addition, multiple LTC4238s can be connected in parallel using the COMM pin to coordinate turn on, turn off, and fault behavior to further improve SOA.

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Figure 1 shows an application example providing 48V, 40A operating in the parallel mode. Two MOSFETs in each channel are used so that the power dissipation in each MOSFET is less than 1W when fully enhanced. After start-up, when the voltage across the MOSFETs drain and source is lower than 2V, the gate-to-source voltages for both MOSFETs are higher than 8V, and the FB voltage is higher than 2.56V, power is considered good. Open-drain output PG is then released to go high. After that, if the FB falls below 2.48V, PG will be reset to low.

If the current limit timer is selected with parallel mode (configuration 9), it will run if either channel is in current limit during start-up. Once start-up is finished and PG has been released, the current limit timer will run only if both channels are in current limit. If the SOA timer is selected, the RC network should represent the thermal behavior of a single MOSFET, since the TMR pull-up current is only related to the power dissipation in the channel 1 MOSFET. When TMR reaches 2.56V (representing the maximum allowable temperature rise in the MOSFET), both GATE1 and GATE2 are turned off and the overcurrent fault status will pull the FLT# pin low.

High Stress Stage Start

The two GATE drivers of the LTC4238 can also be configured to operate in high stress staged start mode by grounding the CONFIG2 pin (Table 3). In this mode GATE1 drives a high SOA MOSFET (M1) for start-up and to withstand overstresses; GATE2 drives less expensive bypass MOSFETs (M2A and M2B) with low $R_{DS(ON)}$ and relaxed SOA requirements to carry the load, as shown in Figure 5a. The high stress staged start mode works well for systems where large input steps or supply surges may occur. M1 must be selected with large enough SOA to withstand these conditions, in which M1 not only carries the full load current, but also needs to deliver the current to charge up the load capacitor.

At power up, GATE1 is turned on first to charge the load and GATE2 is held off. As illustrated in Figure 5b, GATE2 is turned on when GATE1 is fully enhanced (GATE1 is more than 8V higher than SOURCE pin), the MOSFET drain to source voltage is lower than 2V and channel 1 is not in current limit. After GATE2 is more than 8V higher than SOURCE pin, the open drain output PG pin is latched high given FB pin is higher than 2.56V. Most of the load current is delivered by M2A and M2B, which usually have much lower $R_{DS(ON)}$ than M1.

In this mode the current sense resistor is connected between $SENSE1^+$ and $SENSE1^-$, while $SENSE2^+$ and $SENSE2^-$ are connected to V_{DD} to disable the current limit circuit of GATE2. During overcurrent events such as an output short or an input step, the LTC4238 immediately switches off GATE2 to protect M2A and M2B from overstress, leaving the current limit of GATE1 to regulate the load current through M1. In this condition the TMR pull-up current is turned on. When the TMR voltage reaches 2.56V, GATE1 is turned off and an overcurrent fault is logged.

The high stress staged start mode decouples the SOA requirement from the $R_{DS(ON)}$ requirement. The MOSFET driven by GATE1 (M1) is selected so that its SOA is large enough to withstand stresses in all operating conditions. The $R_{DS(ON)}$ of M1 is not a major concern but needs to keep the MOSFET drain to source voltage lower than 2V when GATE2 is off, otherwise GATE2 will not be turned on. The MOSFETs driven by GATE2 (M2A and M2B) are selected so that their $R_{DS(ON)}$ minimizes the I^2R power dissipation, typically below or close to 1W. The SOA of M2A and M2B does not need to be large because GATE2 is switched off when either GATE1 is in current limit, GATE1 is low (GATE1 is less than 8V above SOURCE pin), or the MOSFET drain to source is higher than 2V. In this way the selection of MOSFET(s) for each channel is easier and the overall cost of MOSFETs may be lower than the parallel mode.

In the high stress staged start mode, the FET-bad timer starts to run when either GATE1 is low but channel 1 is not in active current limit, GATE2 is enabled but low, or the MOSFET drain to source voltage is higher than 100mV. When TMRFET rises above 2.56V, a FET-bad fault is triggered.

Low Stress Stage Start

The low stress staged start mode is well suited for applications with a tightly regulated supply voltage. In

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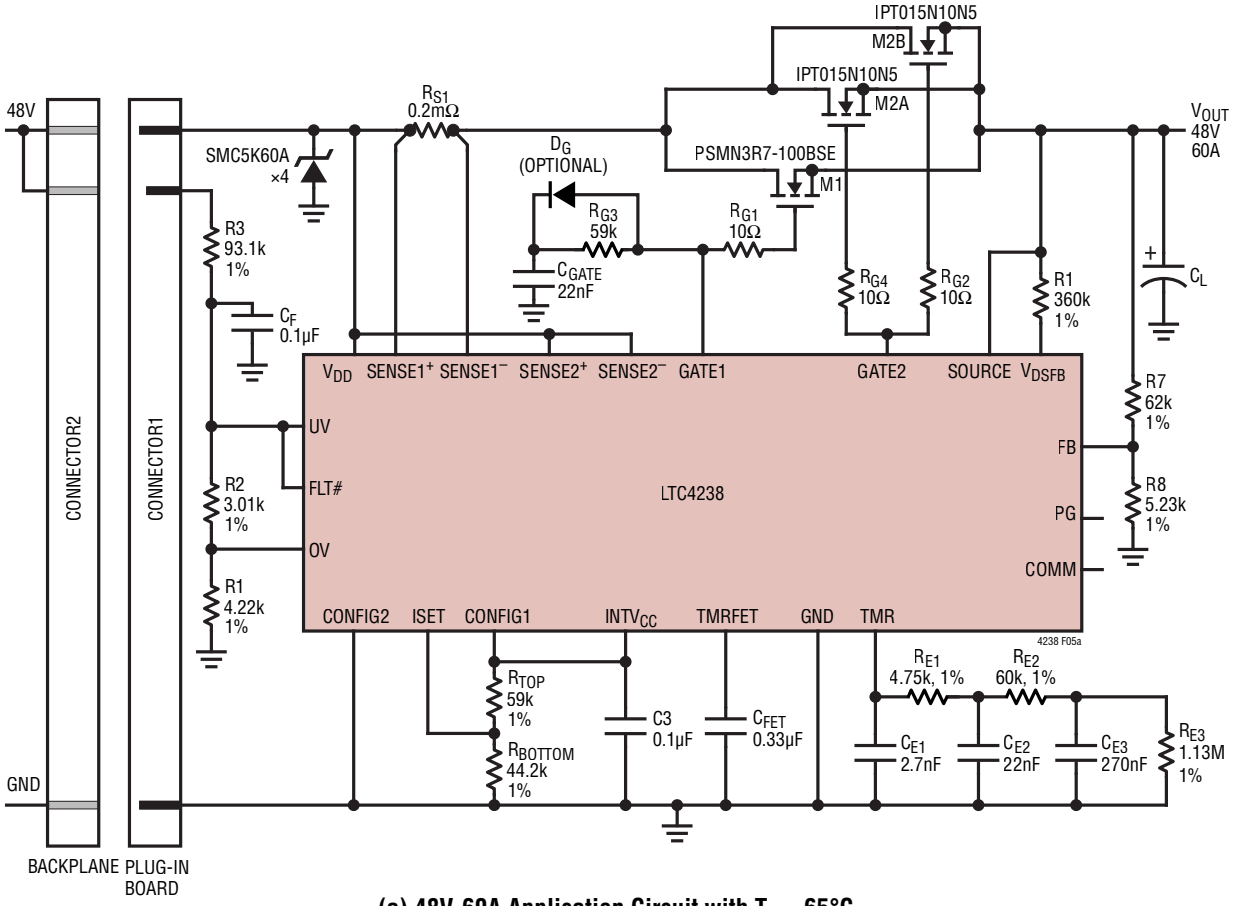
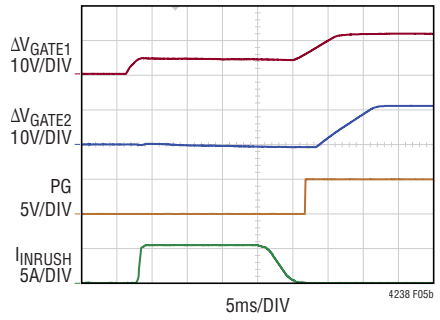
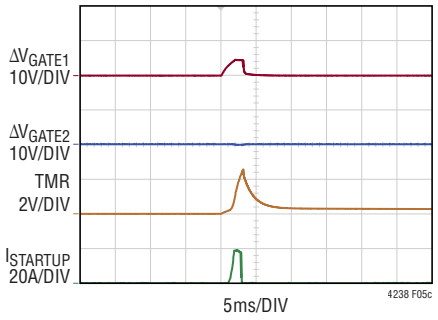
such a system without significant input voltage steps, the worst-case operating condition for the MOSFET SOA occurs when charging the load capacitance during start-up. By limiting the start-up inrush current to a very low level, the SOA demand for the start-up MOSFET is greatly alleviated. Additionally, the bypass path which turns on after start-up only needs inexpensive, switching regulator class MOSFETs. Therefore, this architecture minimizes



(a) 48V,60A Application Circuit with T_A = 65°C



(b) Normal Start-Up Waveform



(c) Start-Up into Short-Circuit

Figure 5. High Stress Staged Start Application

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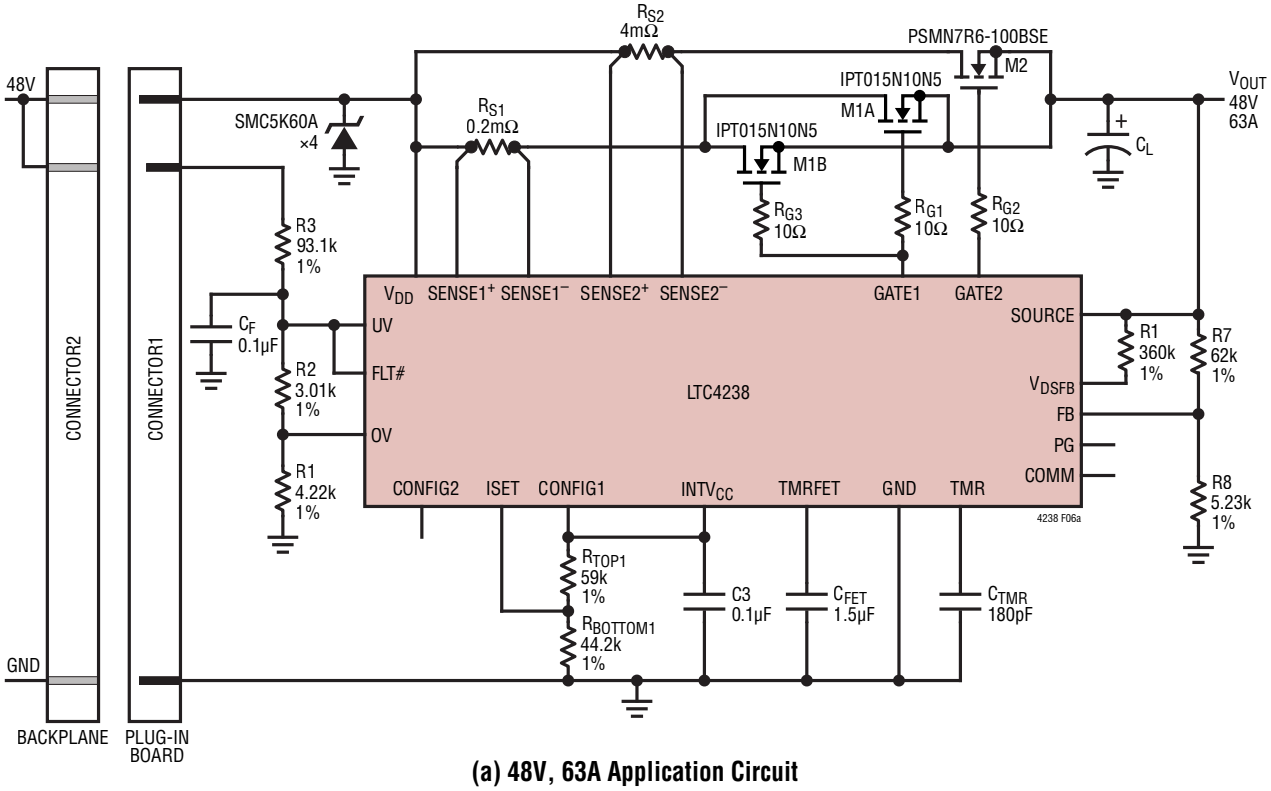
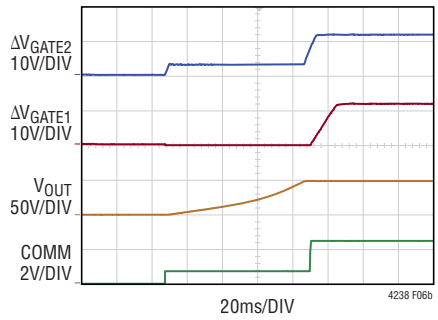
the cost of MOSFETs to achieve a given load current and $R_{DS(ON)}$. However, LSSS mode has limited capability to ride through an input step or a sustained load surge in current limit. Due to the low start-up current it also cannot start up a large resistive load such as a heating element or incandescent lamp.

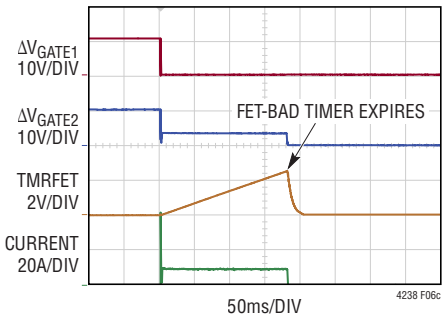
Figure 6a shows an application circuit for a 48V, 63A system operating in the low stress staged start mode. This mode is enabled by using configuration 5 or 6 in Table 3. In this mode GATE2 drives a compact, inexpensive MOSFET (M2) with small SOA as a trickle charging device for start-up. GATE1 drives parallel, low $R_{DS(ON)}$,



(a) 48V, 63A Application Circuit



(b) Normal Start-Up Waveform



(c) Start-Up into Short-Circuit

Figure 6. Low Stress Staged Start Application

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low SOA MOSFETs (M1A and M1B) with a high current limit to deliver the full load current. The turn-on sequence is the opposite of that in the high stress staged start mode as illustrated in Figure 5b: M2 turns on first and delivers a low inrush current due to the large sense resistor RS2. Once the load is fully charged (FB pin is higher than 2.56V) and the start-up MOSFET is fully enhanced (V_{GATE2} > 8V) and not in active current limit, GATE1 turns on. When the MOSFETs of both channels are fully enhanced, the drain-to-source voltage is lower than 2V and FB pin voltage is higher than 2.56V, power-good is asserted.

The current sense pins for both current limit circuits on GATE1 and GATE2 must be connected to their corresponding sense resistors. If an overcurrent event occurs, both GATE1 and GATE2 stay in current limit to share the stress. GATE1 turns off if the FB pin drops below 2.48V or GATE2 turns off due to a fault, which is different from the high stress staged start mode where GATE2 turns off if GATE1 is in current limit.

The condition to start the FET-bad fault timer in this mode is the same as in the parallel mode (see Table 2). Since the FET-bad fault timer is running during the trickle start-up while the load is slowly charged, the timer duration must be programmed long enough to avoid turning off M2 too early.

If the current limit timer is chosen, the TMR capacitor will be charged only when channel 1 is in current limit. A single, small TMR capacitor as shown in Figure 6a can be used to configure a brief delay, which should be within the worst SOA of M1A/M1B and M2. If the SOA timer is chosen, an RC network that represents the electric model for the thermal behavior of M1A or M1B should be connected to TMR. Note that during startup when M1A and M1B are turned off, the TMR pull-up current still relates to the power dissipation in M1A and M1B, which is zero. M2 should be selected so that its SOA allows it to be in current limit longer than M1A or M1B. In this way M2 is automatically protected when M1A and M1B turn off in an overcurrent condition.

Single Driver Mode

Figure 7 shows a single MOSFET application. Configured in high stress staged start mode, this implementation behaves as other single Hot Swap controllers like the LT4256 when the bypass MOSFETs are not stuffed and the GATE2 pin is open.

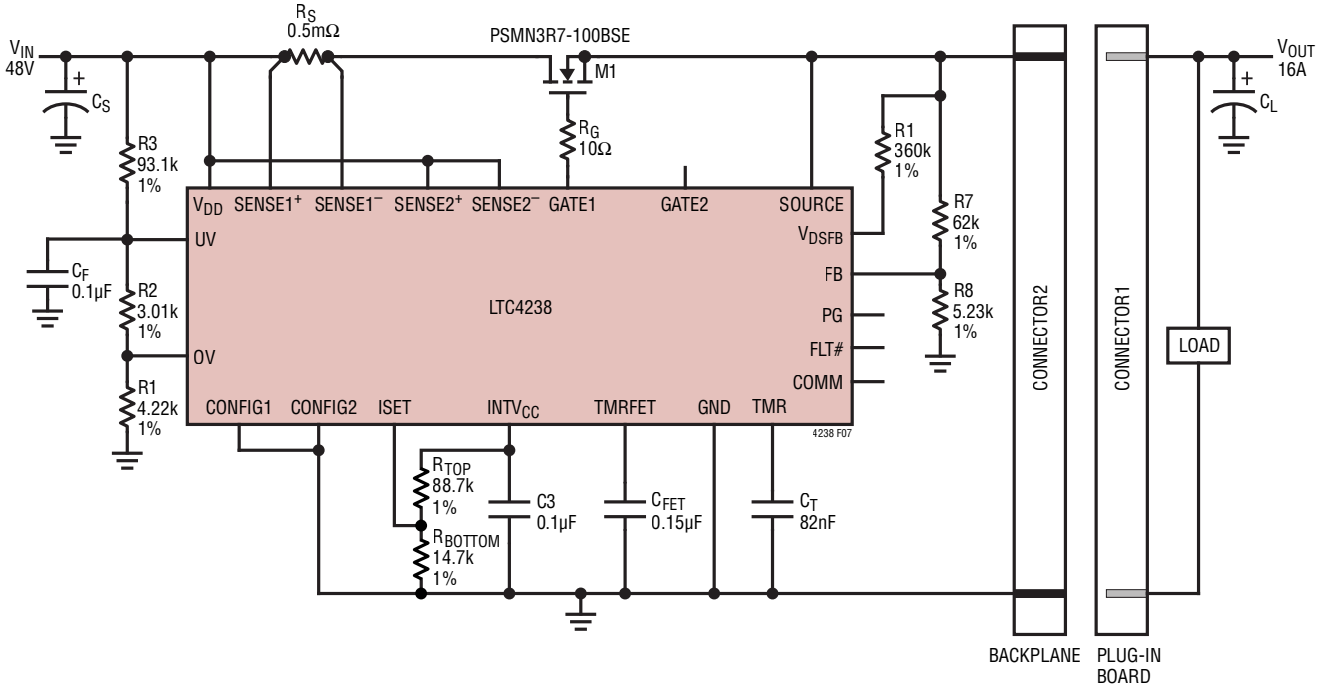

Figure 7. 48V, 16A A Single MOSFET Implementation with HSSS Mode

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On-Off Control

The LTC4238 can be configured to turn on automatically on insertion by connecting the UV/OV resistive voltage divider through a short pin on the connector. For an active high turn-on, the top of the divider is connected to the supply through the short pin as in Figure 8a; for active low turn-on, the bottom of the divider is connected to ground through the short pin as in Figure 8b. Both the UV and OV pins are rated to 100V so no additional protection is needed when pulled up to the supply.

An open-drain pull-down, or logic level NMOS may be connected to the UV pin to allow a logic signal to turn the LTC4238 on and off as shown in Figure 8c.

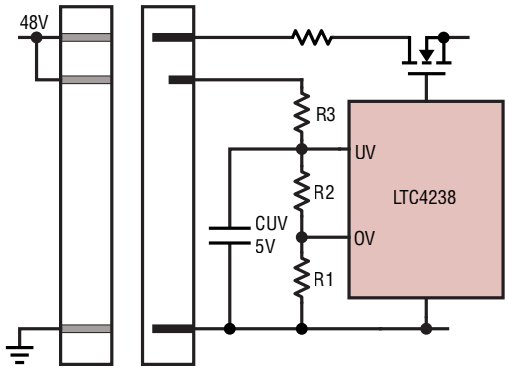
In addition the COMM pin may be used to turn off the LTC4238 by pulling it to GND with an open-drain pull-down. When COMM is released, the LTC4238 will turn on immediately provided no faults are present.

Parallel Controllers Using the COMM Pin

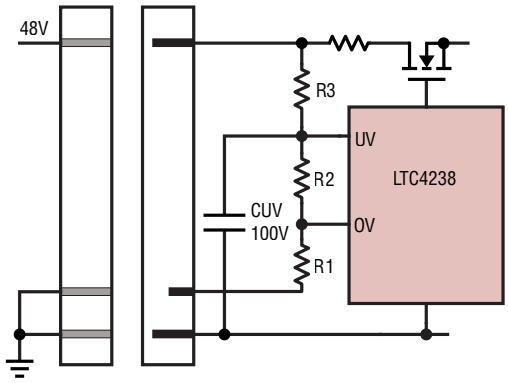
The LTC4238 has a COMM pin that communicates its status so that multiple LTC4238s can operate in parallel. Tie the COMM pins of a group of parts together to allow them to operate in tandem. A small capacitor may be connected to COMM node to improve noise immunity if necessary.

The COMM pin has 4 states.

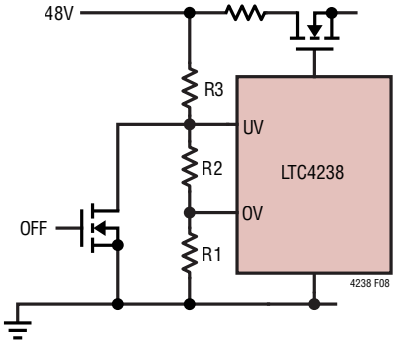
- Zero Volts mean none of the parts can turn on. Any part with a fault present will pull the pin to 0V to turn off the entire bank.
- 0.8V indicates only the start-up channel of the parts configured with LSSS mode are allowed to turn on. Those parts will regulate the COMM at 0.8V voltage with a 5µA pull-up current until the start-up MOSFET is fully enhanced.
- 2.5V at the COMM indicates that all the parts can turn on. The parts that have no faults present regulate at 2.5V with a 5µA pull-up current. The parts that are on and in current limit will disable the 2.5V regulator, allowing the COMM voltage to rise.
- 5V means all the parts are in current limit.



(a) Short Pin to Supply



(b) Short Pin to Ground



(c) On/Off Control by Logic Signal

Figure 8. On/Off Control with UV/OV Pins

When configured as a current limit timer, only one LTC4238 needs to have capacitor connected to the TMR pin. When the COMM voltage is within 1.5V of $INTV_{CC}$, the current limit TMR integrates. The remaining LTC4238s may have their TMR pins grounded to disable overcurrent

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faults. When using thermal networks, each individual part has its own thermal network and may generate a thermal fault regardless of the state of the COMM pin.

When multiple LTC4238s work together by having COMM pins connected, care must be taken to make sure all the LTC4238s see the same solid ground potential. Ground bounce could corrupt COMM function or possibly damage the LTC4238 if the absolute maximum rating is violated. Putting a current limiting resistor in series with the COMM pins, or putting a Schottky or capacitor between COMM and ground next to LTC4238 may mitigate ground noise.

The COMM pin may also be used as a current limit or processor hot (PROCHOTB) indicator for a single or multiple LTC4238s, if the group is in current limit, the pin is pulled to $INTV_{CC}$. A PNP and resistor circuit can convert this signal to a logic signal, as shown in Figure 9.

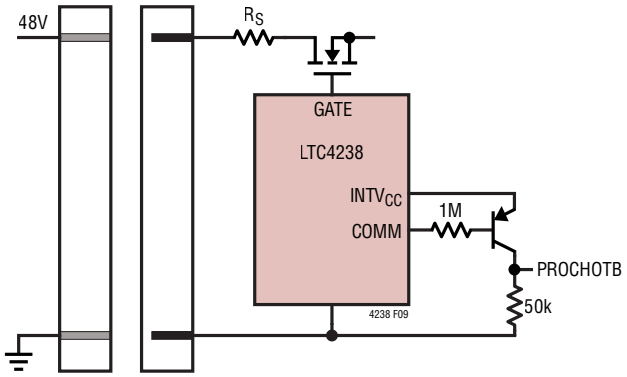

Figure 9. Current Limit/PROCHOT Indication Using the COMM Pin

Supply Transients

In card-resident applications, output short circuits working against the inductive nature of the supply can easily cause the input voltage to dip below the UV threshold.

In severe cases where the supply inductance is 500nH or more, the input can dip below the V_{DD} undervoltage lockout threshold of 5.5V. It is possible for the UV comparator or, the V_{DD} UVLO circuit to respond before the current reaches the current limit threshold. Adding a 100nF filter capacitor to the UV pin ensures that the UV comparator responds after current limiting commences. The fast current limit comparator engages at 3× the current limit threshold and has a propagation delay of 500ns. If the supply inductance is less than 2000nH in a 48V application, it is unlikely that the V_{DD} UVLO threshold will be breached and the fast di/dt rate allows the current to rise to the 3× level long before the UV pin responds.

Once the fast current limit comparator begins to arrest the short circuit current, the input voltage rapidly recovers and even overshoots its DC value. The LTC4238 is safe from damage up to 100V. In card-resident applications clamp the V_{DD} pin with a surge suppressor Z1, as shown in Figure 1. To minimize spikes in backplane resident applications, bypass the LTC4238 input supply with an electrolytic capacitor between V_{DD} and GND.

In the worst case, Z1 has to absorb the high current that triggers the fast current limit comparator. Several surge suppressors may be required to clamp this current for high power applications. In applications where a solid ground is not available to connect the surge suppressor, it may be connected from input to output, allowing the output capacitance to absorb spikes. In 12V applications, many 20V to 30V MOSFETs enter avalanche breakdown before 50V. In such a case, the MOSFET can also act as a surge suppressor and protect the Hot Swap controller from inductive input voltage surges.

Design Examples

The design flow starts with specifying the maximum load power and the operating voltage limits. If redundant supplies are used, the system usually has wide supply range and can experience large input steps when switching. An operation mode is then selected based on the approximate guideline in Table 4.

Table 4. The Guideline for Mode Selection

Mode	Power Level	Supply Range
Single Driver	<800W	Narrow or Wide
Parallel	<1500W	Narrow or Wide
HSSS	>1500W	Wide
LSSS	>1500W	Narrow
Two or More LTC4238 Using the COMM Pin	>3000W	

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Example 1: Parallel Mode with Current Limit Start-Up and SOA Timer

As a design example, take the following specifications: V_{IN} = 48V ±20%, the maximum load power of 1.4kW, start into active current limit and C_L = 1500µF. The parallel mode is chosen based on the guideline above. In the parallel mode, GATE1 and GATE2 drive two parallel channels of MOSFETs to charge the load capacitor simultaneously at startup, share the load current after startup, and turn off simultaneously upon a fault condition such as output overload or short-circuit. Since the input voltage varies between 38V and 58V, the high power profile is selected for foldback to better cope with input variations without folding back the current limit threshold. In addition, SOA Timer is picked for the TMR pin to protect the MOSFETs more effectively. This completed design is shown in Figure 1.

The maximum load current is calculated by:

$$I_{L(MAX)} = \frac{P_{L(MAX)}}{V_{UV(ON)}} = \frac{1400W}{38V} \approx 37A \quad (6)$$

Since there are two channels, the maximum current each channel carries is 18.5A.

Step 1. Configure current limit and select current sense resistors.

A 10mV sense voltage with a 0.5mΩ sense resistance is picked to provide 20A for each channel. When a specific design is actually built, there can be small inaccuracies in the current sensing owing to contact and copper trace resistances. An immediate remedy without changing sense resistors is to readjust the sense voltage in 2mV steps. For instance, moving sense voltage from 10mV to 12mV gives a 20% increase in current.

Some designers may use parallel sense resistors to achieve a specific resistance, in which case the averaging resistors, R_A, should be selected with the same ratio, k, as the sense resistors they connect to. See Figure 10. This allows the current limit circuit to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor should not exceed 1Ω.

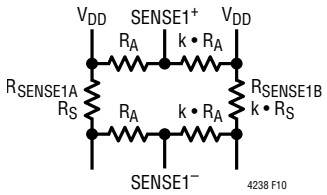

Figure 10. Weighted Averaging Sense Voltages

Step 2. Select the MOSFETs. The MOSFET should be sized to handle the power dissipation during the inrush charging of the load capacitor C_L. In addition, the $R_{DS(ON)}$ must be low enough to carry maximum load current. The method used to determine the power is the principle:

$$E_C = \text{Energy in } C_L = \text{Energy in M1+ Energy in M2} \quad (7)$$

Thus:

$$E_C = \frac{1}{2}CV^2 = \frac{1}{2}(1500\mu F) \bullet (58V)^2 \approx 2.5J \quad (8)$$

During start-up, current limit foldback will limit the power dissipation in MOSFET of each channel to:

$$P_{DISS,START\text{-}UP} = \frac{10mV \bullet 30\% \bullet 58V}{0.5m\Omega} \approx 348W \quad (9)$$

Calculate the time it takes to charge up C_L.

$$t_{CHARGEUP} = \frac{E_C}{P_{DISS,START\text{-}UP} \bullet 2MOSFETs} = \frac{2.5J}{348W \bullet 2} \approx 3.6ms \quad (10)$$

The SOA curves of candidate MOSFETs must be evaluated to ensure that heat capacity of the package can tolerate this power for 3.6ms. The SOA curve of the NXP PSMN3R7-100BSE shows it can sustain 9A with 60V across it for 10ms, satisfying this requirement. Additional MOSFETs in parallel may be required to keep power dissipation within limits at maximum load current, or to reduce the worst case MOSFET drain to source voltage. In this design a pair of PSMN3R7-100BSE is required for both channels. The worst-case MOSFET drain to SOURCE voltage with full load is:

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$$V_{DS,MAX} = \frac{I_{CH(MAX)} \bullet R_{DS(ON),MAX}}{2} = \frac{20A \bullet 3.7m\Omega}{2} = 37mV \quad (11)$$

There is enough margin with the full current load for V_{DD} – SOURCE before reaching FET bad threshold of 100mV.

Since PSMN3R7-100BSE has about 10nF of gate capacitance it is likely to be stable, but the short-circuit stability of the current limit loop should be checked and improved by adding capacitors from GATE to SOURCE if needed.

Step 3. Select the RC network for the SOA timer following the procedure as shown in the SOA Timer section. Three thermal capacitors and three thermal resistors provide fairly good curve fitting for the thermal impedance plot of the chosen MOSFET, PSMN3R7-100BSE in the range between 100µs and 100ms (wide enough for typical operating conditions of this application): $C_{\theta 1}$ = 0.001J/°C, $R_{\theta 1}$ = 0.013°C/W, $C_{\theta 2}$ = 0.008J/°C, $R_{\theta 2}$ = 0.16°C/W, $C_{\theta 3}$ = 0.1J/°C, $R_{\theta 3}$ = 0.27°C/W. The conversion constant is given by:

$$k = \frac{V_{DS,MAX} \bullet I_{D,MAX}}{I_{TMR(UP),MAX}} \bullet \frac{V_{TMR(TH)}}{\Delta T_{MAX}} = \frac{58V \bullet 20mV}{400\mu A \bullet 0.5m\Omega} \bullet \frac{2.56V}{175°C - 65°C} = 1.4 \bullet 10^5 \left[\frac{V^2}{°C}\right] \quad (12)$$

where ΔT_{MAX} is the maximum allowable temperature rise and chosen to be 110°C, which corresponds to a maximum MOSFET temperature of 175°C at an operating temperature of 65°C. The thermal R and C values are then converted to electric R and C values as shown in the SOA timer section. After the electrical R and C values are computed, choose the closest next-larger available resistor value and the closest next-smaller available capacitor value. Then the resistance corresponding to the thermal resistance of the board is added to the termination resistance (the largest one). Assuming a 5°C/W board thermal resistance in this application, it is converted to 5 • 1.4 • 10^5 = 700k. If the computed resistance for the board thermal resistance is over 1M, choose 1M. This avoids accuracy degradation due to board leakage currents. The resulting electrical capacitors and resistors are C_{E1} = 6.8nF, R_{E1} = 1.82k, C_{E2} = 56nF, R_{E2} = 22.6k, C_{E3} = 680nF, R_{E3} = 750k, as shown in Figure 1 and Figure 3. After the SOA timer is configured, run simulations in LTspice to ensure TMR does not reach its 2.56V trip point in any operating conditions including start-up and input step. When it trips in fault conditions such as output overload or short-circuit, verify the peak temperature of the MOSFET matches the proposed maximum temperature. Iterations of the above procedure may be needed before the RC network is finalized.

Step 4. Design the FET-bad timer. During start-up the FET-Bad Timer is running. The load capacitor must be fully charged before this timer expires, or the gate outputs will be turned off once a FET-bad fault is triggered. For a start-up time of 3.6ms and taking into account the tolerance of components, we choose having a 2× safety margin.

$$C_{FET} = 2 \bullet \frac{T_{START-UP}}{128ms/\mu F} = 2 \bullet \frac{3.6ms}{128ms/\mu F} \approx 56nF \quad (13)$$

The closest larger available capacitance 62nF is picked.

Step 5. $V_{UV(ON)}$ = 36V, $V_{UV(OFF)}$ = 60V, $V_{PWRGD(UP)}$ = 33V. Select resistive dividers for UV/OV and Power Good inputs. The UV and OV resistor string values can be solved in the following method. To keep the error due to 1µA of leakage to less than 1% choose a divider current of at least 200µA. R1 < 2.56V/200µA = 12.8kΩ. Then calculate:

$$R2 = \frac{V_{OV(OFF)}}{V_{UV(ON)}} \bullet R1 \bullet \frac{UV_{TH(RISING)}}{OV_{TH(FALLING)}} - R1 \quad (14)$$

$$R3 = \frac{V_{UV(ON)} \bullet (R1 + R2)}{UV_{TH(RISING)}} - R1 - R2 \quad (15)$$

In our case we choose R1 to be 4.22k to give a resistor string current greater than 200µA. Then, solving the equations results in R2 = 3.01k and R3 = 93.1k. A 0.1µF

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capacitor, C_F, is placed on the UV pin to prevent supply glitches from turning off the GATE via UV or OV.

The FB divider is solved by picking R8 and solving for R7, choosing 5.23k for R8.

$$R7 = \frac{V_{PWRGD(UP)}}{FB_{TH(RISING)}} \bullet R8 - R8 \quad (16)$$

resulting in R7 = 62k.

Since the fast-current limit comparator is engaged at 120A, the input TVS needs to be capable of clamping a 120A surge at a voltage above the OV threshold but below the 100V absolute maximum rating of the LTC4238 for about 1µs. The SMC5K60A clamps 51.7A at 96.8V for 1ms and can dissipate 23kW for 10µs. Three of them are required to sink 120A current.

In addition, a 0.1µF ceramic bypass capacitor is placed on the $INTV_{CC}$ pin. No bypass capacitor is required on the V_{DD} pin.

Example 2: Low Stress Staged Start Mode with Basic Timer

The second example has a line regulated 48V supply with the voltage variation of ±10%. The output is a 2.5kW constant power load. $V_{UV(ON)}$ = 36V and $V_{OV(OFF)}$ = 60V as shown in Figure 6. The load capacitance is specified as C_L = 2500µF. The low stress staged start mode is chosen for this example since the power exceeds 1500W and there is no concern of large input steps. In LSSS, the FET bad timer will run if GATE1 is low and not in ACL (Table 2), which could happen when the power good voltage hasn't been reached. Therefore, the power good voltage is recommended to be lower than the input UV voltage. In this example, $V_{PWRGD(UP)}$ is set to 33V. The current in channel 2 is usually only a small fraction of the maximum load current, such as 10% or less. For this reason, its current contribution during normal operation can be ignored for the first phase of the design. Later channel 2 can be accounted for or sized to make up for any shortfall in the high current (channel 1) path, so that full power (2500W) can be supplied at minimum input voltage (43V).

The maximum load current is calculated by Equation 17.

$$I_{L(MAX)} = P_{L(MAX)}/V_{S(MIN)} = 2500W/43V \approx 58A \quad (17)$$

With the two channels decoupled (channel 2 dedicated to start-up and channel 1 dedicated to passing the load current), the overall design flow and design considerations in some individual steps of the low stress staged start mode are different from the parallel mode.

Step 1. Select sufficient bypass MOSFETs to carry the maximum load current. For the maximum channel current of 58A, two IPT015N10N5 ($R_{DS(ON)}$ < 1.5mΩ) devices result in 1.26W per package, an acceptable dissipation with airflow.

With full load, the worst-case voltage across the MOSFET is about 58A • (1.5/2)mΩ = 43.5mV. The threshold for starting the FET-bad timer is 100mV. There is sufficient margin to account for inaccuracies before enabling the TMRFET pull-up current. See detailed design considerations in Example 1, Step 2.

Step 2. Configure the current limit and select the current sense resistors. The current limit in this example should cover the maximum load current, with enough margin to account for device tolerances. Pick the minimum resistance available for a single sense resistor, 200µΩ, which is a metal element resistor. Select the current limit threshold voltage by first assuming channel 1 carries the maximum load current, then add a small current carried by the start-up channel for the margin.

$$\Delta V_{SENSE(MIN)} = RS1 \bullet I_{L(MAX)} = 200\mu\Omega \bullet 58A \approx 12mV \quad (18)$$

The resistor power dissipation of channel 1 is given by Equation 21.

$$PS1 = \Delta V_{SENSE(MIN)} \bullet I_{L(MAX)} = 12mV \bullet 58A = 696mW \quad (19)$$

Which is well within the power limit of several Watts for a metal element sense resistor.

As a last step, a 4mΩ sense resistor is chosen for a channel 2 current:

$$I_{LIM1} = \frac{\Delta V_{SENSE}}{RS2} = \frac{12mV}{4m\Omega} = 3A \quad (20)$$

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so that the total current limit is calculated by Equation 21.

$$I_{LIM} = I_{LIM1} + I_{LIM2} = \frac{12mV}{200\mu\Omega} + 3A = 63A \quad (21)$$

Taking all tolerances into account, this provides sufficient margin for the maximum load current of 58A.

Step 3. Design the TMR behavior. Since there is no concern about a large input step, a short timer delay is chosen for overcurrent turn-off. In the low stress staged start mode the TMR function is a filtered circuit breaker and a single timer capacitor on TMR works for this purpose. Channel 1 dictates the timer capacitor selection since it carries most of the load current. All of the channel 1 current could be concentrated into a single MOSFET. The current limit of channel 1 is 60A in this example, and the MOSFET (IPT015N10N5) can handle 50V and 60A for 80µs. It has been found that 20µs of circuit breaker filtering is sufficient to reject noise encountered in most systems, so the chosen MOSFET is up to the task. The TMR pull-up current is 20µA, with a voltage threshold of 2.56V. Compute the timer capacitance for 20µs filter delay using Equation 22.

$$C_{TMR} = \frac{I_{TMR(UP),MAX} \bullet t_{FILTER}}{V_{TMR(TH)}} = \frac{20\mu A \bullet 20\mu s}{2.56V} = 156pF \quad (22)$$

Select the next-larger available capacitance: C_{TMR} = 180pF.

Step 4. Design the start-up channel (channel 2) and FET-bad timer. At start-up in low stress staged start mode, channel 2 charges the load capacitance with a small trickle current. The necessary start-up time for a 2500µF load capacitor is:

$$t_{CHAREGUP} = \frac{\frac{1}{2} C_L \bullet V^2}{P_{DISS,START\text{-}UP}} = \frac{\frac{1}{2} \bullet 2500\mu F \bullet (53V)^2}{3A \bullet 30\% \bullet 53V} = 74ms \quad (23)$$

The FET bad timer must be set longer than the startup time for the load capacitor to be fully charged. Meanwhile, FET-bad timer should be short enough that the FET picked for channel 2 can handle the start-up current with the full drain to source voltage for this duration. With a 2× safety margin, we choose:

$$C_{FET} = \frac{2 \bullet t_{START\text{-}UP} \bullet I_{TMRFET(UP)}}{2.56V} = \frac{2 \bullet 74ms \bullet 20\mu A}{2.56V} = 1.2\mu F \quad (24)$$

The next larger available capacitance, 1.5µF, is used. Since the start-up current is relatively low, a small, low cost device may be used. PSMN7R6-100B, which can stand the 30% foldback of 3A at 48V as a DC condition is selected for this trickle channel. Its $R_{DS(ON)}$ is no higher than 7.6mΩ. After startup, the worst-case power dissipation in this channel is $(3A)^2 \bullet 7.6m\Omega$ = 68mW, well within the MOSFET capability.

Step 5. Run simulations to verify temperature rises in both the channel 1 and channel 2 MOSFETs under all operating and fault conditions. This is a necessary step when using a single capacitor current limit timer as selected in Step 3.

First, check the temperature rise in the channel 2 MOSFET (M2) during startup. The conditions include normal startup into current limit to fully charge the 2500µF load capacitor at the maximum input voltage. If the temperature rise is too high in normal startup condition, a larger MOSFET can be selected for channel 2. For the fault condition, the worst-case power dissipated in MOSFET is same as the max voltage (53V) across the MOSFET with 30% of full current limit since the constant power profile is selected for foldback. If the temperature rise is too high, the startup current limit may be reduced by selecting a larger sense resistor R_{S2}. Using the conditions of this example, it is found the worst-case temperature rise in M2 either in normal startup condition or with fault resistors is lower than 50°C. This verifies the selected channel 2 MOSFET, PSMN7R6-100B, has more than enough SOA to handle the worst-case dissipation.

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Second, check the temperature rise in channel 1 after startup when TMR times out under different overload conditions. In this example, IPT015N10N5 can take 60A with 40V across it for 100µs. The temperature rise in 20µs is insignificant under overload conditions. If the worst-case temperature rise in channel 1 is too high, better SOA MOSFET(s) must be selected for it.

Layout Considerations

For high current applications, PCB layout plays a critical role in minimizing current congestion as well as partitioning the current between two channels. In parallel mode, to achieve the even split of current flow between the two channels, the two high current paths should have very similar layouts for the R_{SENSE} and MOSFET placements.

To achieve accurate current sensing, Kelvin connections are also required. The SENSE$^+$ and SENSE$^-$ lines should be laid out as differential signal pair. Their trace lengths to LTC4238 pins should be as short as possible. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/□. Small resistances add up quickly in high current applications.

To improve noise immunity, place the resistive voltage dividers for the UV, OV and FB pins close to the device and keep traces to V_{DD} and GND short. It is also important to put the $INTV_{CC}$ bypass capacitor as close as possible between the $INTV_{CC}$ and GND pins. A 0.1µF capacitor, C_F, from the UV pin (and OV pin through resistor R2) to GND also helps reject supply noise. Figure 11 shows a layout that addresses these issues. Note that a surge suppressor, Z1, is placed between supply and ground using wide traces.

It is advised to avoid placing the ground plane under the power MOSFETs. If the MOSFETs overheat, the insulation could fail between the input voltage at their drains and an underlying ground plane. This could create a catastrophic short across the supply.

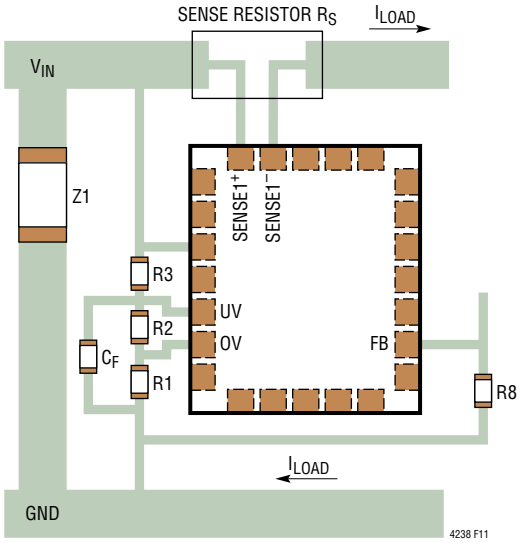
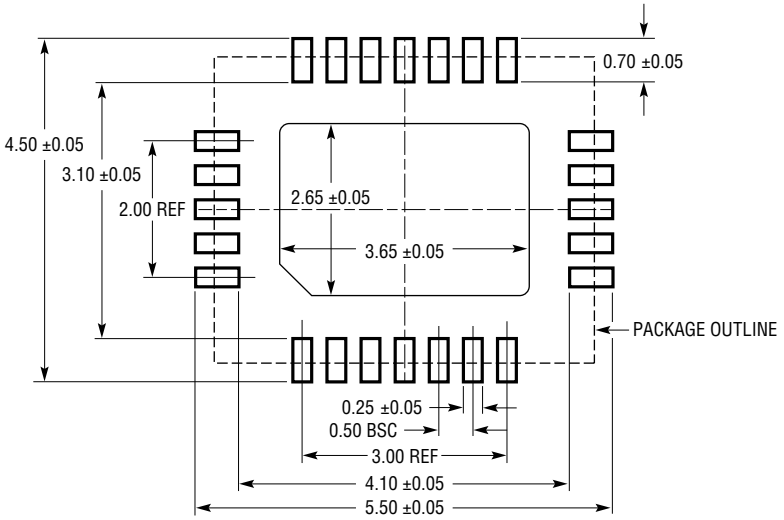


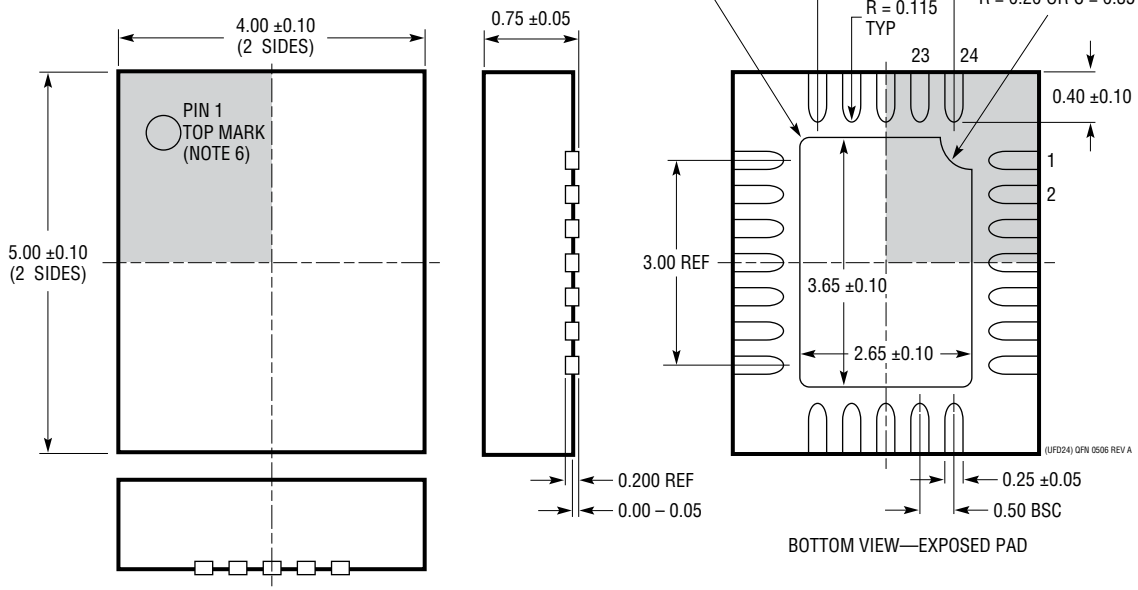
Figure 11. Recommended PCB Layout

PACKAGE DESCRIPTION

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

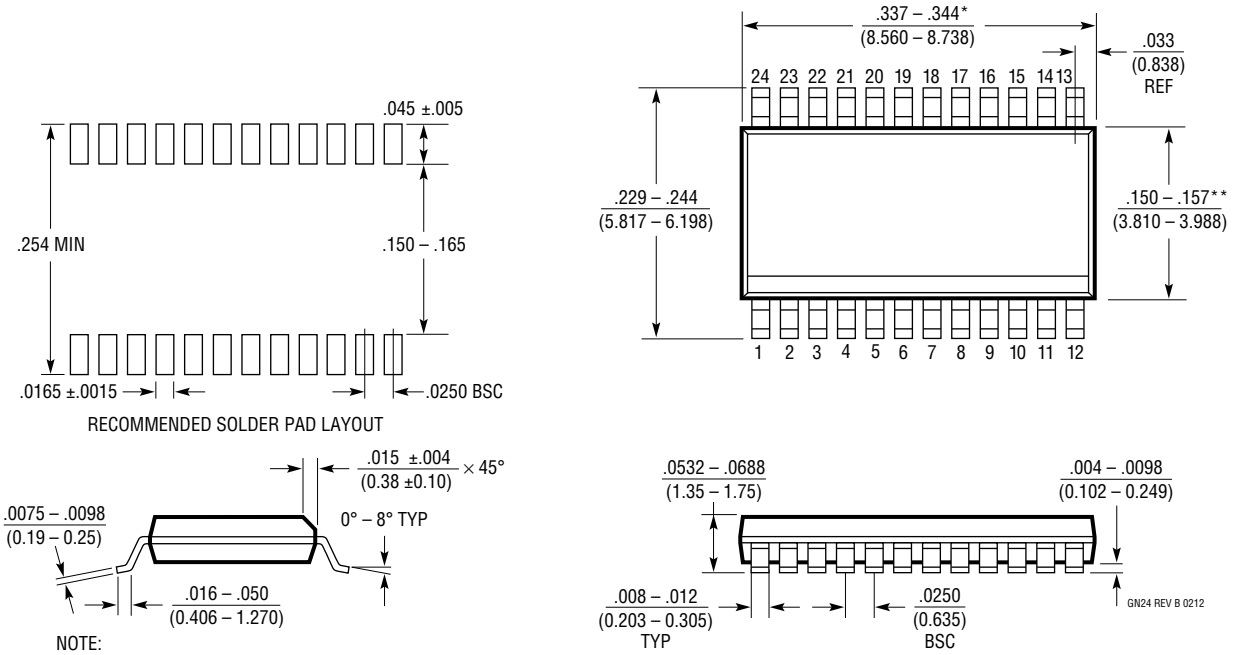


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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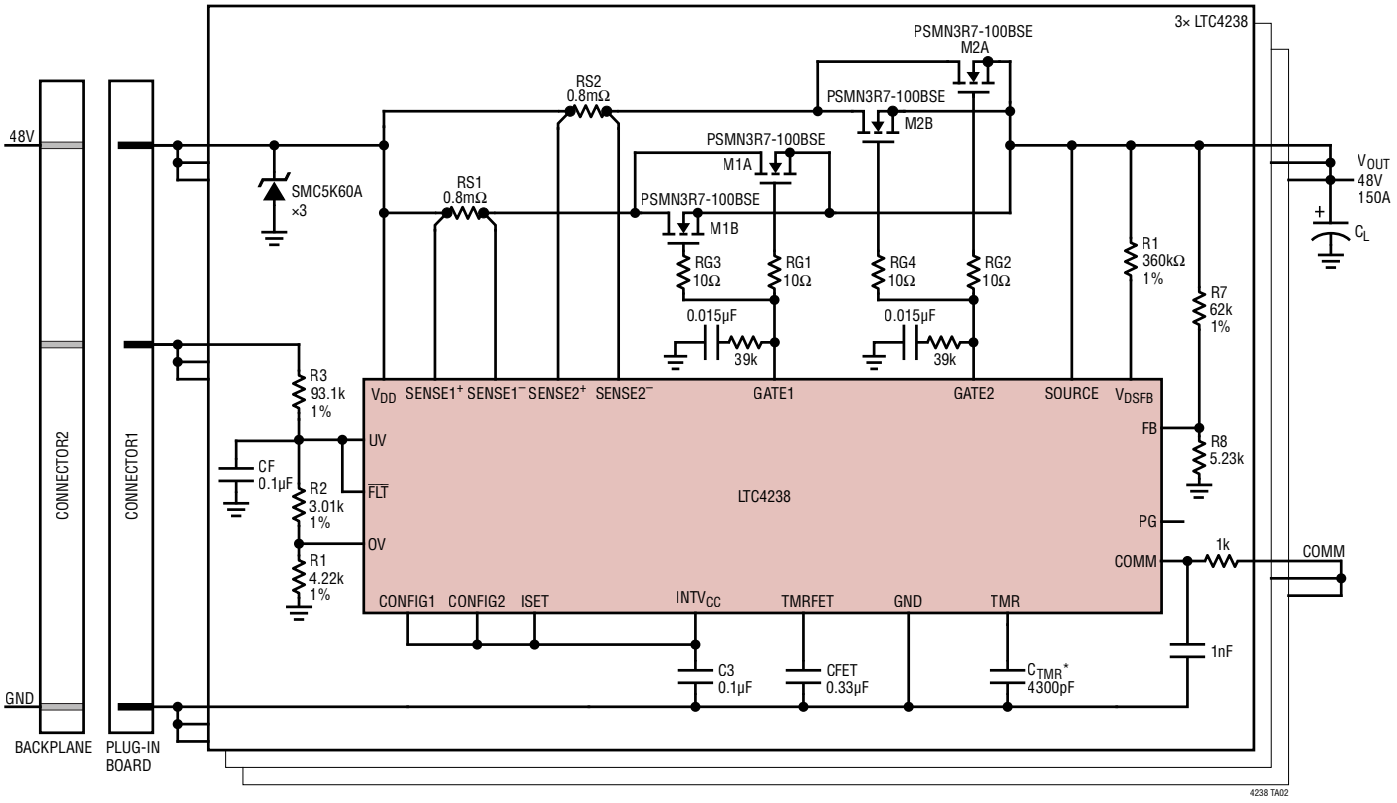
TYPICAL APPLICATION

48V, 150A Hot Swap Controllers Using the COMM Pin



*ONLY ONE OF ALL THE LTC4238s NEEDS TO HAVE A CAPACITOR CONNECTED TO THE TMR PIN.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1641-1/ LT1641-2	Positive High Voltage Hot Swap Controllers	Active Current Limiting, Supplies from 9V to 80V
LT4256-1/ LT4256-2	Positive 48V Hot Swap Controller with Open-Circuit Detect	Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply
LTC4281	Positive Voltage Hot Swap Controller with I²C Compatible Monitoring	12-/16-Bit ADC Monitors Current, Voltage, Power and Energy, Internal EEPROM, I²C, Supplies from 2.9V to 33V
LTC4282	High Current Positive Voltage Hot Swap Controller with I²C Compatible Monitoring	Dual Gate Drive, 12-/16-Bit ADC Monitors Current, Voltage, Power and Energy, Internal EEPROM, I²C, Supplies from 2.9V to 33V
LTC4283	–48V Hot Swap Controller with Energy Monitor	SOA Timer, 8-Bit to 16-Bit ADC Monitors Current, Voltage, Power and Energy, Internal EEPROM, I²C or Single-Wire Broadcast
LTC4284	–48V High Current Hot Swap Controller with Energy Monitor	Dual Gate Drive, SOA Timer, 8-Bit to 16-Bit ADC Monitors Current, Voltage, Power and Energy, Internal EEPROM, I²C or Single-Wire Broadcast
LTC4237	Positive High Voltage Hot Swap Controllers	Active Current Limiting, Foldback Current Limiting, SOA Timer, FET Health Monitor, Supplies from 6.5V to 80V

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