SmartMesh IP Node 2.4GHz 802.15.4e Wireless Mote-on-Chip

NETWORK FEATURES

- Complete Radio Transceiver, Embedded Processor, and Networking Software for Forming a Self-Healing Mesh Network
- SmartMesh® Networks Incorporate:
  - Time Synchronized Network-Wide Scheduling
  - Per Transmission Frequency Hopping
  - Redundant Spatially Diverse Topologies
  - Network-Wide Reliability and Power Optimization
  - NIST Certified Security
- SmartMesh Networks Deliver
  - >99.999% Network Reliability Achieved in the Most Challenging RF Environments
  - Sub 50µA Routing Nodes
- Compliant to 6LoWPAN Internet Protocol (IP) and IEEE 802.15.4e Standards

LTC5800-IPM FEATURES

- Industry-Leading Low Power Radio Technology
  - 4.5mA to Receive a Packet
  - 9.7mA to Transmit at 8dBm
- PCB Module Versions Available (LTP5901/ LTP5902-IPM) with RF Modular Certifications
- 2.4GHz, IEEE 802.15.4e System-on-Chip
- 72-Pin 10mm × 10mm QFN Package
- Micrium µCOS-II Real Time Operating System based On-Chip Software Development Kit

DESCRIPTION

SmartMesh IP™ wireless sensor networks are self managing, low power internet protocol (IP) networks built from wireless nodes called motes. The LTC®5800-IPM is the IP mote product in the Eterna®* family of IEEE 802.15.4e System-on-Chip (SoC) solutions, featuring a highly-integrated, low power radio design by Dust Networks® as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh IP networking software.

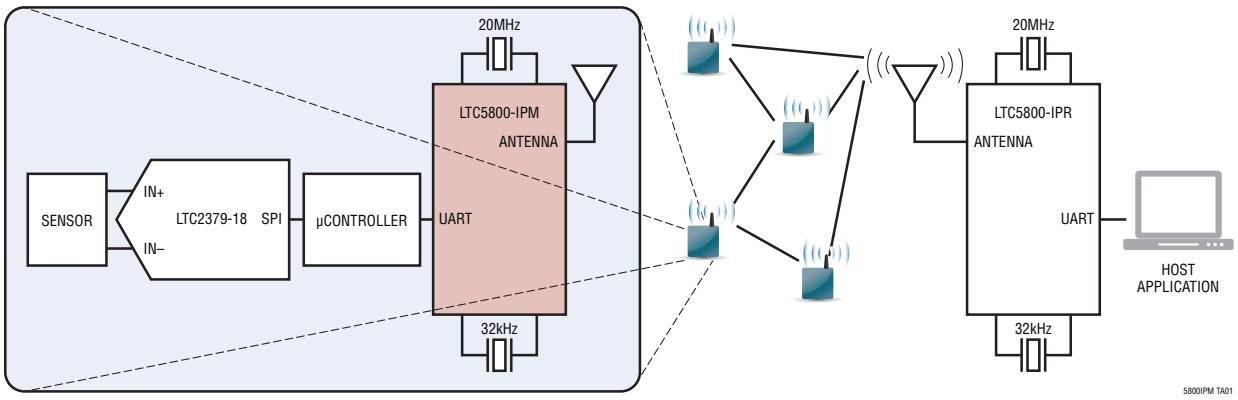
The LTC5800-IPM SoC features an on-chip power amplifier (PA) and transceiver, requiring only power supply decoupling, crystals, and antenna with matching circuitry to create a complete wireless node.

With Dust's time-synchronized SmartMesh IP networks, all motes in the network may route, source or terminate data, while providing many years of battery powered operation. The SmartMesh IP software provided with the LTC5800-IPM is fully tested and validated, and is readily configured via a software Application Programming Interface.

SmartMesh IP motes deliver a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

* Eterna is Dust Networks' low power radio SoC architecture.

TYPICAL APPLICATION



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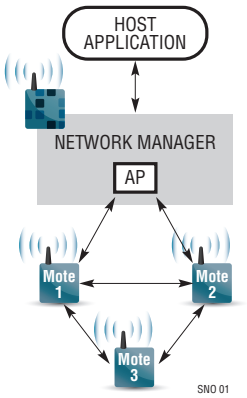
SMARTMESH NETWORK OVERVIEW

A SmartMesh network consists of a self-forming multi-hop mesh of nodes, known as motes, which collect and relay data, and a network manager that monitors and manages network performance and security, and exchanges data with a host application.

SmartMesh networks communicate using a time slotted channel hopping (TSCH) link layer, pioneered by Dust Networks. In a TSCH network, all motes in the network are synchronized to within less than a millisecond. Time in the network is organized into time slots, which enables collision-free packet exchange and per-transmission channel-hopping. In a SmartMesh network, every device has one or more parents (e.g. mote 3 has motes 1 and 2 as parents) that provide redundant paths to overcome communications interruption due to interference, physical obstruction or multi-path fading. If a packet transmission fails on one path, the next retransmission may try on a different path and different RF channel.

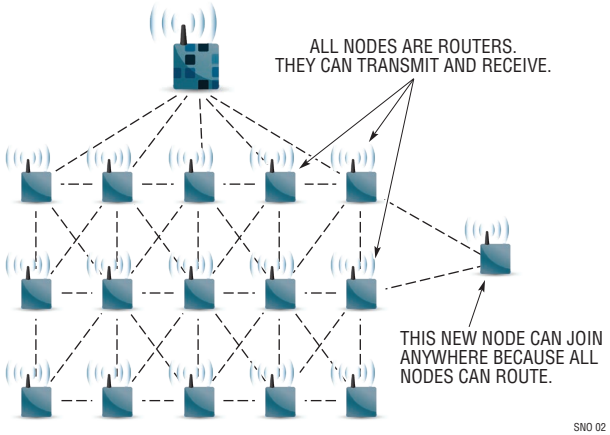
A network begins to form when the network manager instructs its on-board Access Point (AP) radio to begin sending advertisements—packets that contain information that enables a device to synchronize to the network and request to join. This message exchange is part of the security handshake that establishes encrypted communications between the manager or application, and mote. Once motes have joined the network, they maintain synchronization through time corrections when a packet is acknowledged.



An ongoing discovery process ensures that the network continually discovers new paths as the RF conditions change. In addition, each mote in the network tracks performance statistics (e.g. quality of used paths, and lists of potential paths) and periodically sends that information to the network manager in packets called health reports.

The Network Manager uses health reports to continually optimize the network to maintain >99.999% data reliability even in the most challenging RF environments.

The use of TSCH allows SmartMesh devices to sleep in between scheduled communications and draw very little power in this state. Motes are only active in time slots where they are scheduled to transmit or receive, typically resulting in a duty cycle of < 1%. The optimization software in the Network Manager coordinates this schedule automatically. When combined with the Eterna low power radio, every mote in a SmartMesh network—even busy routing ones—can run on batteries for years. By default, all motes in a network are capable of routing traffic from other motes, which simplifies installation by avoiding the complexity of having distinct routers vs non-routing end nodes. Motes may be configured as non-routing to further reduce that particular mote's power consumption and to support a wide variety of network topologies.



At the heart of SmartMesh motes and network managers is the Eterna IEEE 802.15.4e System-on-Chip (SoC), featuring Dust Networks' highly integrated, low power radio design, plus an ARM Cortex-M3 32-bit microprocessor running SmartMesh networking software. The SmartMesh networking software comes fully compiled yet is configurable via a rich set of Application Programming Interfaces (APIs) which allows a host application to interact with the network, e.g. to transfer information to a device, to configure data publishing rates on one or more motes, or to monitor network state or performance metrics. Data publishing can be uniform or different for each device, with motes being able to publish infrequently or faster than once per second as needed.

ABSOLUTE MAXIMUM RATINGS

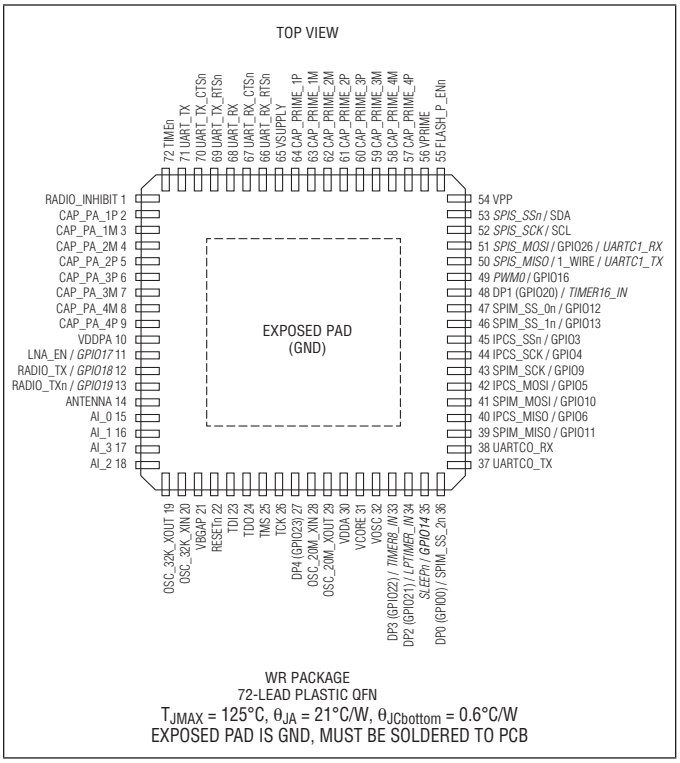
(Note 1)

Supply Voltage on VSUPPLY 4.20V
Input Voltage on AI_0/1/2/3 Inputs 1.80V
Voltage on Any Digital I/O Pin ...–0.3V to V_{SUPPLY} + 0.3V
Input RF Level 10dBm
Storage Temperature Range (Note 3) ..... –55°C to 125°C
Junction Temperature (Note 3) ..... 125°C
Operating Temperature Range
LTC5800I ..... –40°C to 85°C
LTC5800H ..... –55°C to 105°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTC5800-IPM.

PIN CONFIGURATION

Pin functions shown in italics are currently not supported in software.



WR PACKAGE
72-LEAD PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 21°C/W, $\theta_{JCbottom}$ = 0.6°C/W
EXPOSED PAD IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5800IWR-IPMA#PBF	LTC5800IWR-IPMA#PBF	LTC5800WR-IPMA	72-Lead (10mm × 10mm × 0.85mm) Plastic QFN	–40°C to 85°C
LTC5800HWR-IPMA#PBF	LTC5800HWR-IPMA#PBF	LTC5800WR-IPMA	72-Lead (10mm × 10mm × 0.85mm) Plastic QFN	–55°C to 105°C

*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SUPPLY}	Supply Voltage	Including Noise and Load Regulation	●	2.1		3.76	V
	Supply Noise	Requires Recommended RLC Filter, 50Hz to 2MHz	●			250	mV
	Operating Relative Humidity	Non-condensing	●	10		90	% RH
	Temperature Ramp Rate	While Operating in Network	●	–8		+8	°C/min

DC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

OPERATION/STATE	CONDITIONS		MIN	TYP	MAX	UNITS
Reset	After Power-on Reset			1.2		µA
Power-on Reset	During Power-on Reset, Maximum 750µs + VSUPPLY Rise Time from 1V to 1.9V			12		mA
Doze	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Active			1.2		µA
Deep Sleep	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Inactive			0.8		µA
In-Circuit Programming	RESETn and FLASH_P_ENn Asserted, IPCS_SCK @ 8MHz			20		mA
Peak Operating Current +8dBm +0dBm	System Operating at 14.7MHz, Radio Transmitting, During Flash Write. Maximum duration 4.33 ms.			 30 26		 mA mA
Active	ARM Cortex M3, RAM and Flash Operating, Radio and All Other Peripherals Off. Clock Frequency of CPU and Peripherals Set to 7.3728MHz, VCORE = 1.2V			1.3		mA
Flash Write	Single Bank Flash Write			3.7		mA
Flash Erase	Single Bank Page or Mass Erase			2.5		mA
Radio Tx +0dBm (LTC5800I) +0dBm (LTC5800H) +8dBm (LTC5800I) +8dBm (LTC5800H)	Current With Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			 5.4 5.6 9.7 9.9		 mA mA mA mA
Radio Rx LTC5800I LTC5800H	Current With Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			 4.5 4.7		 mA mA

RADIO SPECIFICATIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Band		●	2.4000		2.4835	GHz
Number of Channels		●		15		
Channel Separation		●		5		MHz
Channel Center Frequency	Where k = 11 to 25, as Defined by IEEE.802.15.4	●		2405 + 5•(k-11)		MHz
Raw Data Rate		●		250		kbps
Antenna Pin ESD Protection	HBM Per JEDEC JESD22-A114F			±1000		V
Range (Note 4) Indoor Outdoor Free Space	25°C, 50% RH, +2dBi Omni-Directional Antenna, Antenna 2m Above Ground			 100 300 1200		 m m m

RADIO RECEIVER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Sensitivity	Packet Error Rate (PER) = 1% (Note 5)		–93		dBm
Receiver Sensitivity	PER = 50%		–95		dBm
Saturation	Maximum Input Level the Receiver Will Properly Receive Packets		0		dBm
Adjacent Channel Rejection (High Side)	Desired Signal at -82dBm, Adjacent Modulated Channel 5MHz Above the Desired Signal, PER = 1% (Note 5)		22		dBc
Adjacent Channel Rejection (Low Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Below the Desired Signal, PER = 1% (Note 5)		19		dBc
Alternate Channel Rejection (High Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Above the Desired Signal, PER = 1% (Note 5)		40		dBc
Alternate Channel Rejection (Low Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Below the Desired Signal, PER = 1% (Note 5)		36		dBc
Second Alternate Channel Rejection	Desired Signal at –82dBm, Second Alternate Modulated Channel Either 15MHz Above or Below, PER = 1% (Note 5)		42		dBc
Co-Channel Rejection	Desired Signal at –82dBm, Undesired Signal is an 802.15.4 Modulated Signal at the Same Frequency, PER = 1%		–6		dBc
LO Feed Through			–55		dBm
Frequency Error Tolerance (Note 6)			±50		ppm
Symbol Error Tolerance			±50		ppm
Received Signal Strength Indicator (RSSI) Input Range			–90 to –10		dBm
RSSI Accuracy			±6		dB
RSSI Resolution			1		dB

RADIO TRANSMITTER CHARACTERISTICS

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PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power	Delivered to a 50Ω load				
High Calibrated Setting			8		dBm
Low Calibrated Setting			0		dBm
Spurious Emissions	Conducted Measurement with a 50Ω Single-Ended Load, +8dBm Output Power. All Measurements Made with Max Hold. RF Implementation Per Eterna Reference Design				
30MHz to 1000MHz	R_{BW} = 120kHz, V_{BW} = 100Hz		<–70		dBm
1GHz to 12.75GHz	R_{BW} = 1MHz, V_{BW} = 3MHz		–45		dBm
2.4GHz ISM Upper Band Edge (Peak)	R_{BW} = 1MHz, V_{BW} = 3MHz		–37		dBm
2.4GHz ISM Upper Band Edge (Average)	R_{BW} = 1MHz, V_{BW} = 10Hz		–49		dBm
2.4GHz ISM Lower Band Edge	R_{BW} = 100kHz, V_{BW} = 100kHz		–45		dBc
Harmonic Emissions	Conducted Measurement Delivered to a 50Ω Load, Resolution Bandwidth = 1MHz, Video Bandwidth = 1MHz, RF Implementation Per Eterna Reference Design				
2nd Harmonic			–50		dBm
3rd Harmonic			–45		dBm

DIGITAL I/O CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
V_{IL}	Low Level Input Voltage		●	–0.3		0.6	V
V_{IH}	High Level Input Voltage	(Note 8)	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 1, $I_{OL(MAX)}$ = 1.2mA	●			0.4	V
	Low Level Output Voltage	Type 2, Low Drive, $I_{OL(MAX)}$ = 2.2mA	●			0.4	V
	Low Level Output Voltage	Type 2, High Drive, $I_{OL(MAX)}$ = 4.5mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 1, $I_{OH(MAX)}$ = –0.8mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	High Level Output Voltage	Type 2, Low Drive, $I_{OH(MAX)}$ = –1.6mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	High Level Output Voltage	Type 2, High Drive, $I_{OH(MAX)}$ = –3.2mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	Input Leakage Current	Input Driven to VSUPPLY or GND			50		nA
	Pull-Up/Pull-Down Resistance				50		kΩ

TEMPERATURE SENSOR CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Offset	Temperature Offset Error at 25°C			±0.25		°C
Slope Error				±0.033		°C/°C

ANALOG INPUT CHAIN CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Variable Gain Amplifier						
	Gain			1		8	
	Gain Error					2	%
	Offset-Digital to Analog Converter (DAC)						
	Full-Scale				1.80		V
	Resolution				4		Bits
DNL	Differential Non-Linearity					2.7	mV
	Analog to Digital Converter (ADC)						
	Full-Scale, Signal				1.80		V
	Resolution				1.8		mV
	Offset	Mid-Scale			1.4	12	LSB
DNL	Differential Non-Linearity					1	LSB
INL	Integral Non-Linearity					1	LSB
	Settling Time	10kΩ Source Impedance				10	µs
	Conversion Time					20	µs
	Current Consumption				40		µA
	Analog Inputs (Note 8)						
	Load				20		pF
	Series Input Resistance				1		kΩ

SYSTEM CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Doze to Active State Transition				5		µs
	Doze to Radio Tx or Rx				1.2		ms
Q_{CCA}	Charge to Sample RF Channel RSSI	Charge Consumed Starting from Doze State and Completing an RSSI Measurement			4		µC
Q_{MAX}	Largest Atomic Charge Operation	Flash Erase, 21ms Max Duration	●			200	µC
	RESETn Pulse Width		●	125			µs

UART AC CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Permitted R_X Baud Rate Error	Both Application Programming Interface (API) and Command Line Interface (CLI) UARTs	●	–2		2	%
	Generated T_X Baud Rate Error	Both API and CLI UARTs	●	–1		1	%
$t_{RX\_RTS\ to\ RX\_CTS}$	Assertion of UART_RX_RTSn to Assertion of UART_RX_CTSn, or Negation of UART_RX_RTSn to Negation of UART_RX_CTSn		●	0		2	ms
$t_{RX\_CTS\ to\ RX}$	Assertion of UART_RX_CTSn to Start of Byte		●	0		20	ms
$t_{EOP\ to\ RX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_RX_RTSn		●	0		22	ms
$t_{BEG\_TX\_RTS\ to\ TX\_CTS}$	Assertion of UART_TX_RTSn to Assertion of UART_TX_CTSn		●	0		22	ms
$t_{END\_TX\_RTS\ to\ TX\_CTS}$	Negation of UART_TX_RTSn to Negation of UART_TX_CTSn	Mode 2 Only				22	ms
$t_{END\_TX\_CTS\ to\ TX\_RTS}$	Negation of UART_TX_CTSn to Negation of UART_TX_RTSn	Mode 4 Only		2			Bit Period
$t_{TX\_CTS\ to\ TX}$	Assertion of UART_TX_CTSn to Start of Byte		●	0		2	Bit Period
$t_{EOP\ to\ TX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_TX_RTSn		●	0		1	Bit Period
$t_{RX\_INTERBYTE}$	Receive Inter-Byte Delay		●			100	ms
$t_{RX\_INTERPACKET}$	Receive Inter-Packet Delay		●	20			ms
$t_{TX\_INTERPACKET}$	Transmit Inter-Packet Delay		●	1			Bit Period
$t_{TX\ to\ TX\_CTS}$	Start of Byte to Negation of UART_TX_CTSn		●	0			ns

UART AC CHARACTERISTICS

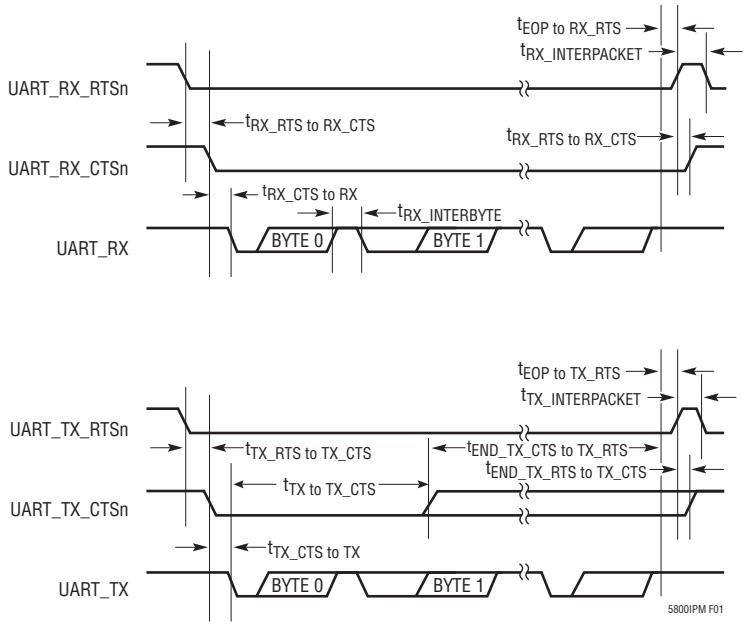


Figure 1. API UART Timing

TIMEn AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{STROBE}	TIMEn Signal Strobe Width		●	125			µs
$t_{RESPONSE}$	Delay from Rising Edge of TIMEn to the Start of Time Packet on API UART		●	0		100	ms
t_{TIME_HOLD}	Delay from End of Time Packet on API UART to Falling Edge of Subsequent TIMEn		●	0			ns
	Timestamp Resolution (Note 10)		●		1		µs
	Network-Wide Time Accuracy (Note 11)		●		±5		µs

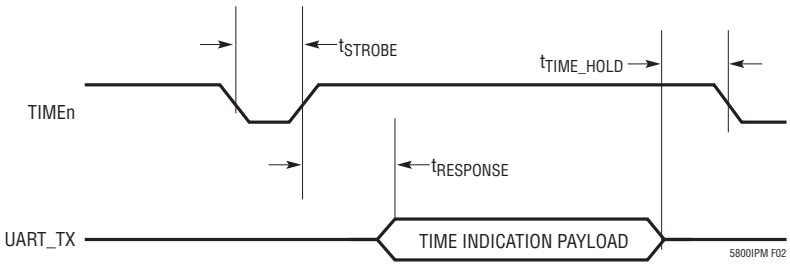


Figure 2. Timestamp Timing

RADIO_INHIBIT AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RADIO_OFF}	Delay from Rising Edge of RADIO_INHIBIT to Radio Disabled		●			20	ms
$t_{RADIO\_INHIBIT\_STROBE}$	Maximum RADIO_INHIBIT Strobe Width		●			2	s

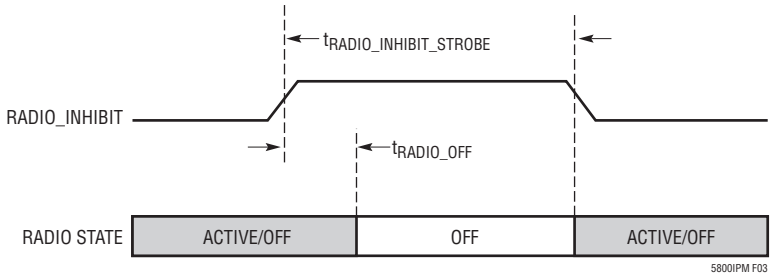


Figure 3. RADIO_INHIBIT Timing

FLASH AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{WRITE}	Time to Write a 32-Bit Word (Note 12)		●			21	µs
t_{PAGE_ERASE}	Time to Erase a 2kB Page (Note 12)		●			21	ms
t_{MASS_ERASE}	Time to Erase 256kB Flash Bank (Note 12)		●			21	ms
	Data Retention	25°C 85°C 105°C		100 20 8			Years Years Years

FLASH SPI SLAVE AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{FP\_EN\_to\_RESET}$	Setup from Assertion of FLASH_P_ENn to Assertion of RESETn		●	0			ns
t_{FP_ENTER}	Delay from the Assertion RESETn to the First Falling Edge of IPCS_SSn		●	125			µs
t_{FP_EXIT}	Delay from the Completion of the Last Flash SPI Slave Transaction to the Negation of RESETn and FLASH_P_ENn (Note 13)		●	10			µs
t_{SSS}	IPCS_SSn Setup to the Leading Edge of IPCS_SCK		●	15			ns
t_{SSH}	IPCS_SSn Hold from Trailing Edge of IPCS_SCK		●	15			ns
t_{CK}	IPCS_SCK Period		●	300			ns
t_{DIS}	IPCS_MOSI Data Setup		●	15			ns
t_{DIH}	IPCS_MOSI Data Hold		●	5			ns
t_{DOV}	IPCS_MISO Data Valid		●	–5		30	ns
t_{OFF}	IPCS_MISO Data Tri-State from Trailing Edge of IPCS_SSn		●	0		30	ns

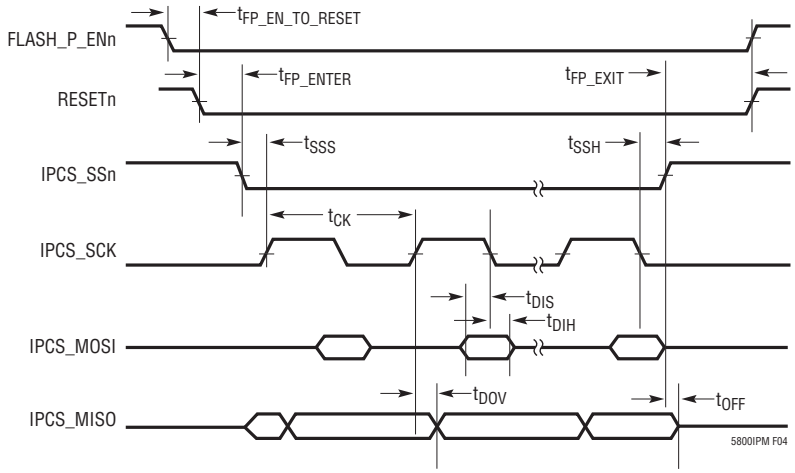


Figure 4. Flash Programming Interface Timing

SPI MASTER AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SSS}	SPIM_SSXn Setup to the Leading Edge of SPIM_SCK		●	t_{CK-30}			ns
t_{SSH}	SPIM_SSXn Hold from Trailing Edge of SPIM_SCK		●	t_{CK-30}			ns
t_{CK}	SPIM_SCK Period		●	268			ns
t_{DIS}	SPIM_MOSI Data Setup		●	30			ns
t_{DIH}	SPIM_MOSI Data Hold		●	5			ns
t_{DOV}	SPIM_MISO Data Valid		●	-5		30	ns
t_{OFF}	SPIM_MISO Data Tri-State from Trailing Edge of SPIM_SSXn		●	0		30	ns

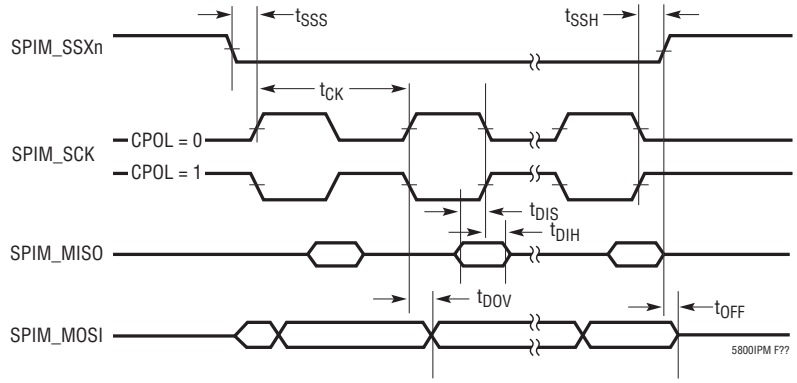


Figure 5. SPI Master Timing - CPHA = 0

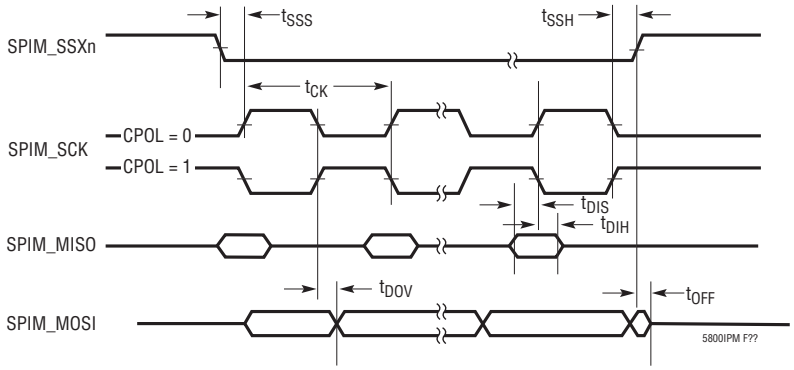


Figure 6. SPI Master Timing - CPHA = 1

I²C AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Frequency	184kHz Operation 92kHz Operation	●		184.3 92.2	188 94	kHz
t_{HD_STA}	Start Hold Time (SCL from SDA)	184kHz Operation 92kHz Operation	●	1 2			µs
t_{SU_STA}	Setup Time for a Repeated Start	184kHz Operation, 750ns SCL Rise Time 92kHz Operation, 1.5µs SCL Rise Time	●	300 600			ns
t_{HD_DAT}	Data Hold Time	184kHz Operation 92kHz Operation	●	1 2			µs
t_{SU_DAT}	Data Setup Time	184kHz Operation 92kHz Operation	●	1 2			µs
t_{SU_STO}	Setup Time for Stop Condition	184kHz Operation 92kHz Operation	●	1 2			µs

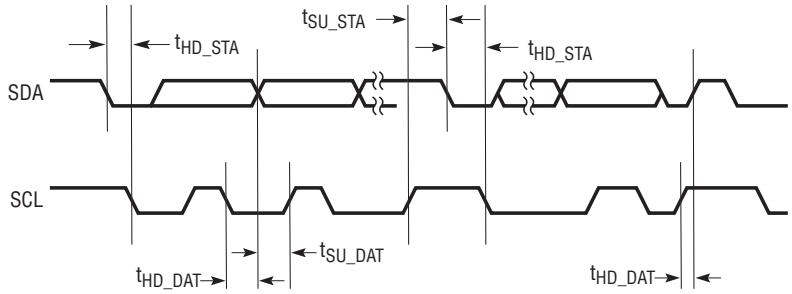


Figure 7. I²C Master Timing

1-WIRE MASTER

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{SUPPLY} = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RSTL}	Reset Low		●	527	556	584	µs
t_{PS}	Presense Sample		●	60.1	69.4	79	µs
t_{BIT_PERIOD}	1_WIRE Data Bit Period		●	82	86.8	92	µs
t_{LOW0}	1_WIRE Write Data 0 Low Width		●	65	69	82	µs
t_{LOW1}	1_WIRE Write Data 1 Low Width		●	8.2	8.7	9.2	µs
t_{LOWR}	1_WIRE Read Data Low Width		●	8.2	8.7	9.2	µs
t_{RS}	Read Sample from 1_WIRE Low		●	13.2	14.6	15.0	µs

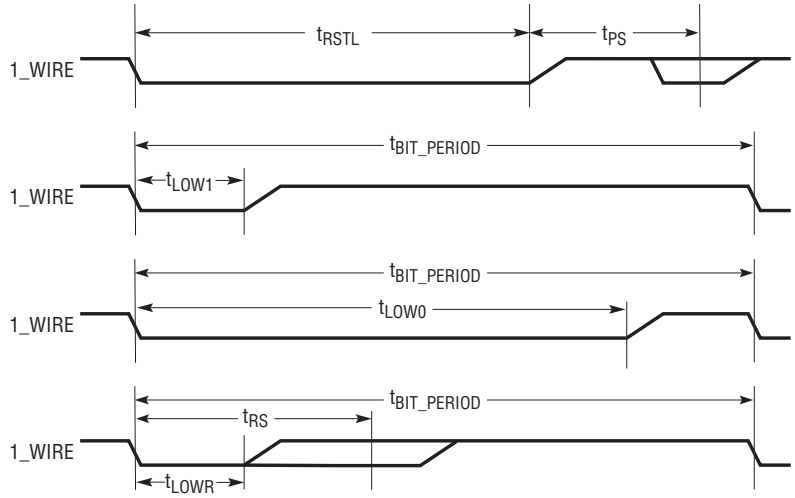


Figure 8. 1-Wire Master Timing

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to Eterna. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: Extended storage at high temperature is discouraged, as this negatively affects the data retention of Eterna's calibration data. See the FLASH Data Retention section for details.

Note 4: Actual RF range is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, range varies.

Note 5: As Specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/findstds/standard/802.15.4-2011.html

Note 6: IEEE Std. 802.15.4-2006 requires transmitters to maintain a frequency tolerance of better than ±40 ppm.

Note 7: Per pin IO types are provided in the Pin Functions section.

Note 8: VIH maximum voltage input must respect the V_{SUPPLY} maximum voltage specification.

Note 9: The analog inputs to the ADC can be modeled as a series resistor to a capacitor. At a minimum the entire circuit, including the source impedance for the signal driving the analog input should be designed to settle to within ¼ LSB within the sampling window to match the performance of the ADC.

Note 10: See the SmartMesh IP Mote API Guide for the timeIndication notification definition.

Note 11: Network time accuracy is a statistical measure and varies over the temperature range, reporting rate and the location of the device relative to the manager in the network. See the Typical Performance Characteristics section for a more detailed description.

Note 12: Code execution from flash banks being written or erased is suspended until completion of the flash operation.

Note 13: Guaranteed by design. Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

Network motes typically route through at least two parents the traffic destined for the manager. The supply current graphs shown in Figure 9 include a parameter called descendants. In these graphs the term descendants is short for traffic-weighted descendants and refers to an amount of activity equivalent to the number of descendants if all of the network traffic directed to the mote in question. Generally the number of descendants of a parent is more, typically 2x or more, than the number of traffic-weighted descendants. For example, with reference to Figure 10 mote P1 has 0.75 traffic-weighted descendants. To obtain this value notice that mote D1 routes half its packets through mote P1 adding 0.5 to the traffic-weighted descendant value; the other half of D1's traffic is routed through its other parent, P2. Mote D2 routes half its packets through mote D1 (the other half going through parent P3), which we know routes half its packets to mote P1, adding another 0.25 to the traffic-weighted descendant value for a total traffic-weighted descendant value of 0.75.

As described in the Application Time Synchronization section, Eterna provides two mechanisms for applications to maintain a time base across a network. The synchronization performance plots that follow were generated using the more precise TIMEn input. Publishing rate is the rate a mote application sends upstream data. Synchronization improves as the publishing rate increases. Baseline synchronization performance is provided for a network operating with a publishing rate of zero. Actual performance for applications in network will improve as publishing rates increase. All synchronization testing was performed with the 1-hop mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the manager and this mote and between this mote and its descendents therefore propagated down through the network. The synchronization of the 3-hop and 5-hop motes to the manager was then affected by the temperature ramps even though they were at room temperature. For 2°C/minute testing the temperature chamber was cycled between –40°C and 85°C at this rate for 24 hours. For 8°C/minute testing, the temperature chamber was rapidly cycled between 85°C and 45°C for 8 hours, followed by rapid cycling between –5°C and 45°C for 8 hours, and lastly, rapid cycling between –40°C and 15°C for 8 hours.

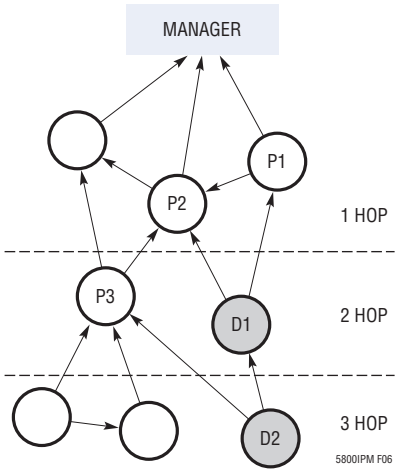


Figure 10. Example Network Graph

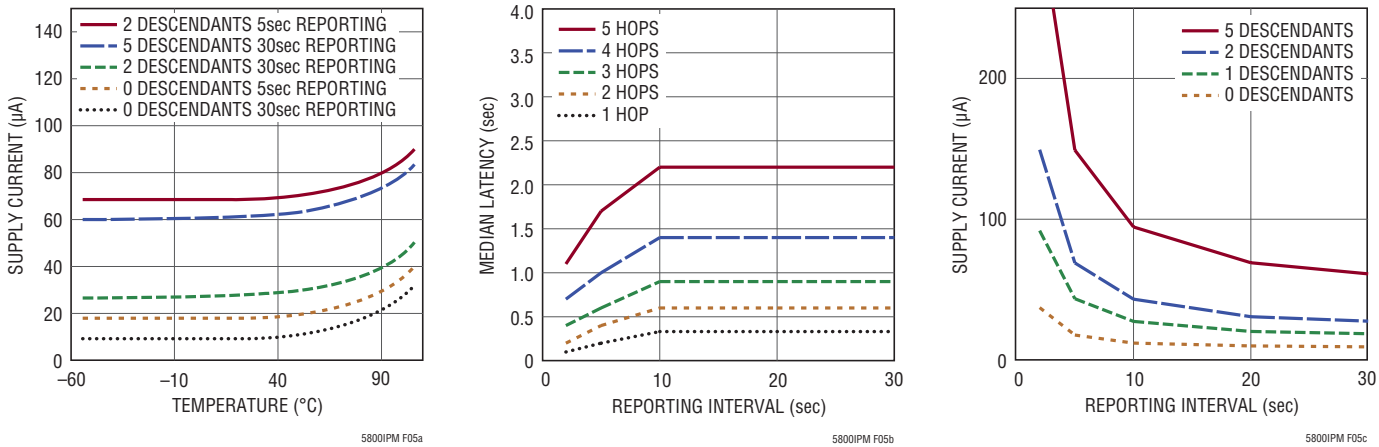
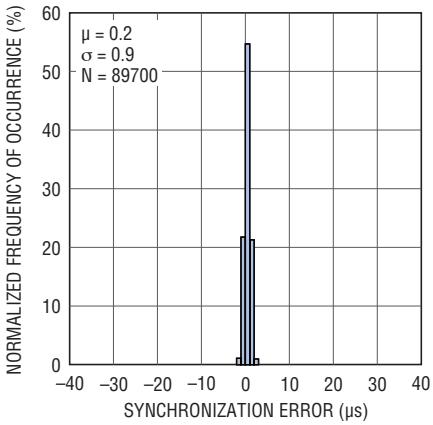


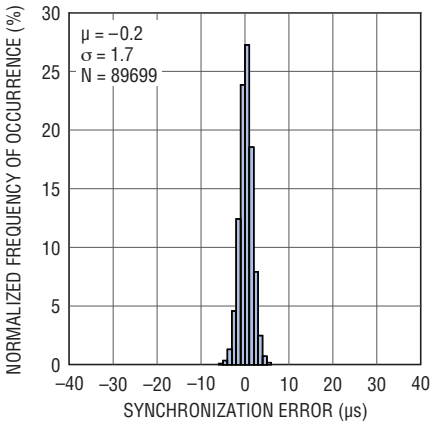
Figure 9

TYPICAL PERFORMANCE CHARACTERISTICS

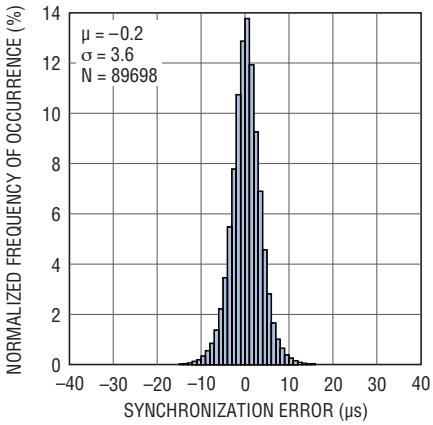
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, Room Temperature



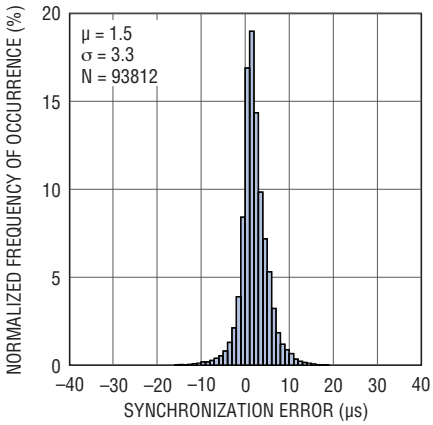
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, Room Temperature



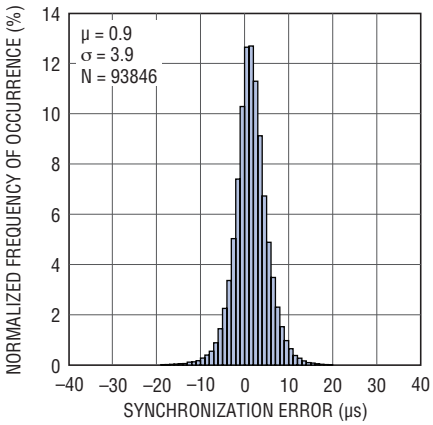
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, Room Temperature



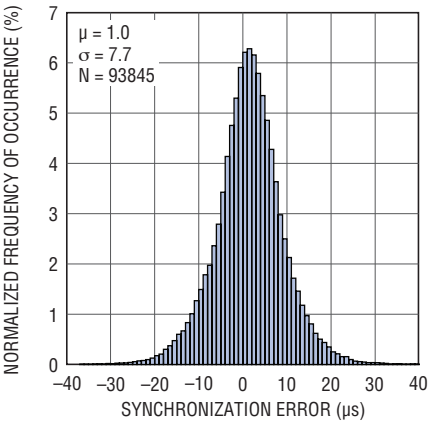
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, 2°C/Min



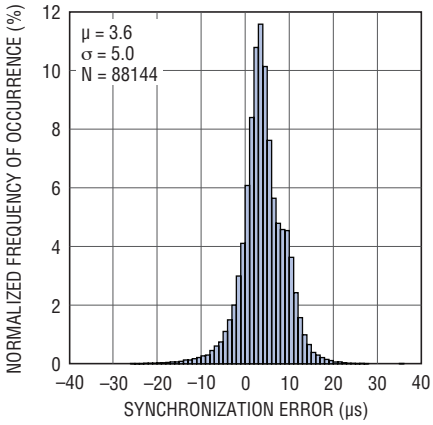
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, 2°C/Min



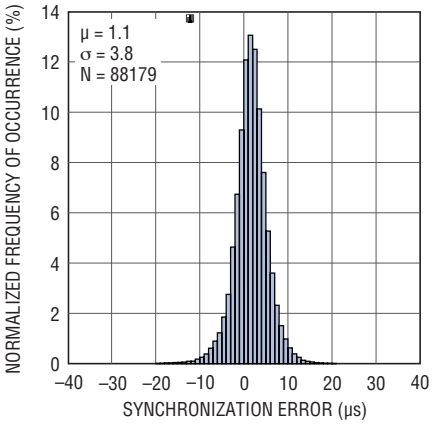
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, 2°C/Min



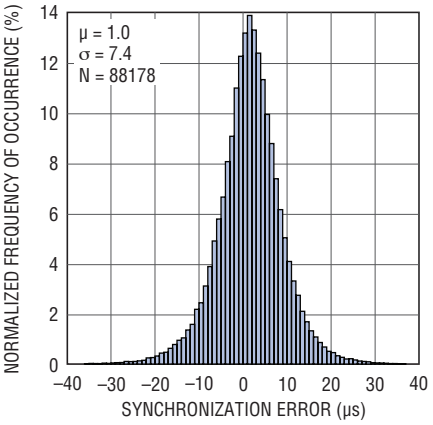
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, 8°C/Min



TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, 8°C/Min

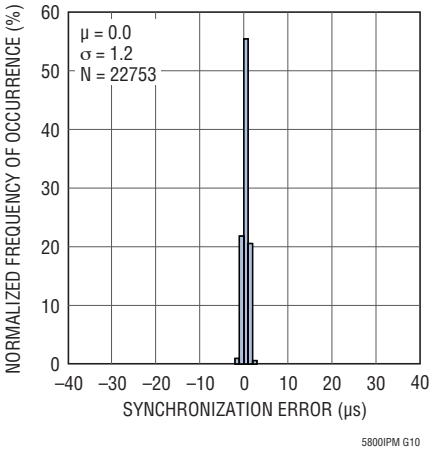


TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, 8°C/Min

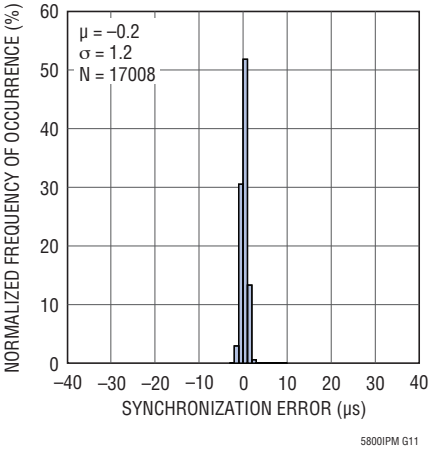


TYPICAL PERFORMANCE CHARACTERISTICS

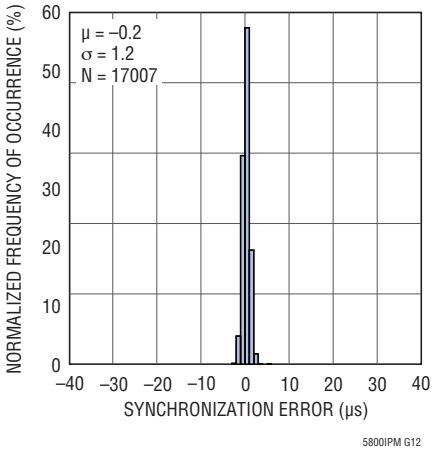
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, Room Temperature



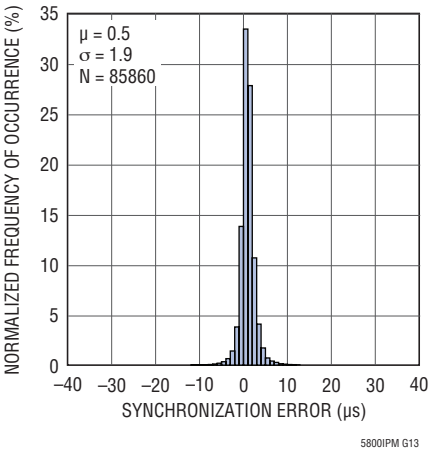
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, Room Temperature



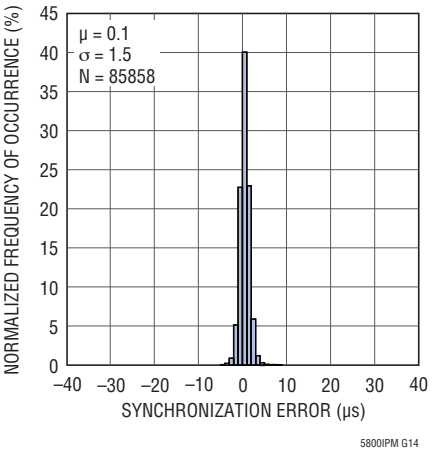
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, Room Temperature



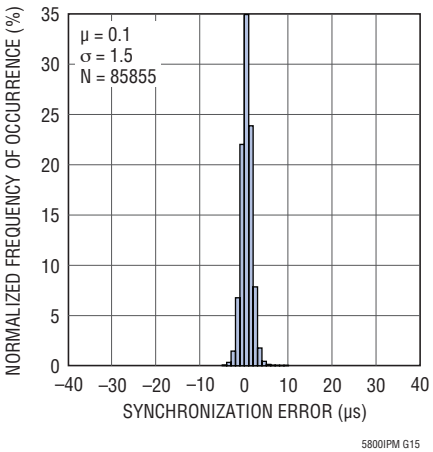
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 2°C/Min



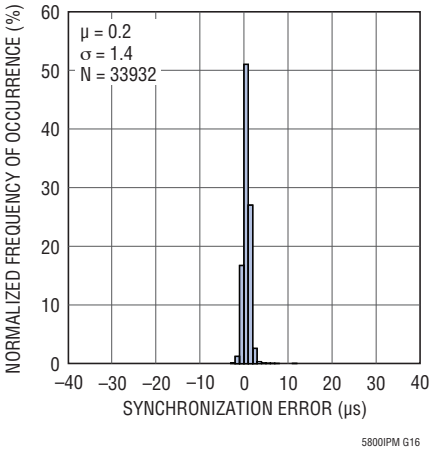
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 2°C/Min



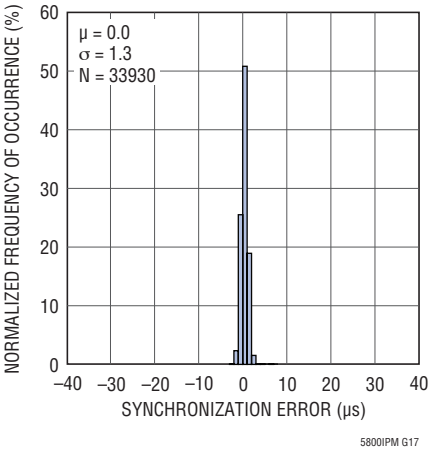
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 2°C/Min



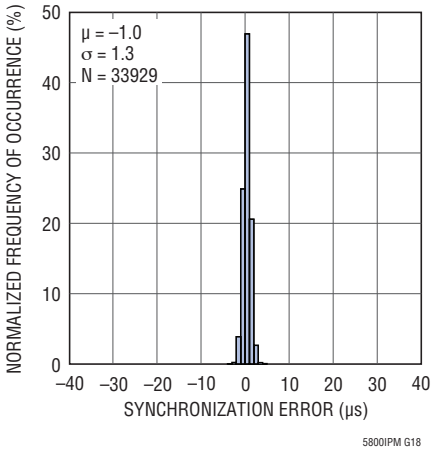
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 8°C/Min



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 8°C/Min



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 8°C/Min



TYPICAL PERFORMANCE CHARACTERISTICS

As described in the SmartMesh Network Overview section, devices in network spend the vast majority of their time inactive in their lowest power state (doze). On a synchronous schedule a mote will wake to communicate with another mote. Regularly occurring sequences which wake, perform a significant function and return to sleep are considered atomic. These operations are considered atomic as the sequence of events can not be separated into smaller events while performing a useful function. For example, transmission of a packet over the radio is an atomic operation. Atomic operations may be characterized in either charge or energy. In a time slot where a mote successfully sends a packet, an atomic transmit includes setup prior to sending the message, sending the message, receiving the acknowledgment and the post processing needed as a result of the message being sent. Similarly in a time slot when a mote successfully receives a packet, an atomic receive includes setup prior to listening, listening until the start of the packet transition, receiving the packet, sending the acknowledgement and post processing required due to the arrival of the packet.

To ensure reliability each mote in the network is provided multiple time slots for each packet it nominally will send and forward. The time slots are assigned to communicate upstream, toward the manager, with at least two different motes. When combined with frequency hopping this provides temporal, spatial and spectral redundancy. Given this approach a mote will often listen for a message that it will never receive, since the time slot is not being used by the transmitting mote. It has already successfully transmitted the packet. Since typically 3 time slots are scheduled for every 1 packet to be sent or forwarded, motes will perform more of these atomic “idle listens” than atomic transmit or atomic receive sequences. Examples of transmit, receive and idle listen atomic operations are shown in Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS

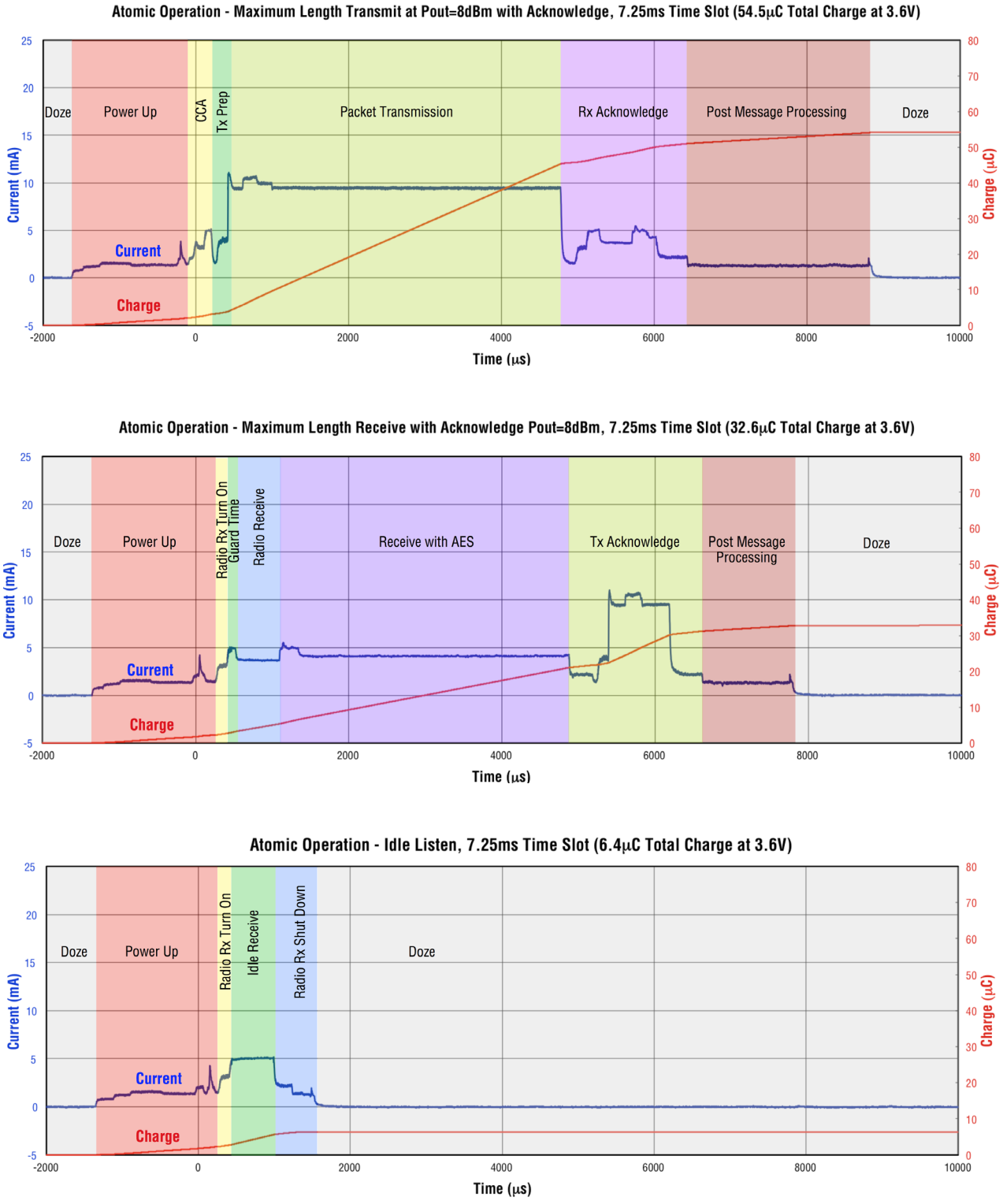


Figure 11

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

The following table organizes the pins by functional groups. For those I/O with multiple functions the alternate functions are shown on the second and third line in their respective row. The **No** column provides the pin number. The second column lists the function. The **Type** column lists the I/O type. The **I/O** column lists the direction of the signal relative to Eterna. The **Pull** column shows which signals have a fixed passive pull-up or pull-down. The **Description** column provides a brief signal description.

NO	POWER SUPPLY	TYPE	I/O	PULL	DESCRIPTION
P	GND	Power	-	-	Ground Connection, P = QFN Paddle
2	CAP_PA_1P	Power	-	-	PA DC/DC Converter Capacitor 1 Plus Terminal
3	CAP_PA_1M	Power	-	-	PA DC/DC Converter Capacitor 1 Minus Terminal
4	CAP_PA_2M	Power	-	-	PA DC/DC Converter Capacitor 2 Minus Terminal
5	CAP_PA_2P	Power	-	-	PA DC/DC Converter Capacitor 2 Plus Terminal
6	CAP_PA_3P	Power	-	-	PA DC/DC Converter Capacitor 3 Plus Terminal
7	CAP_PA_3M	Power	-	-	PA DC/DC Converter Capacitor 3 Minus Terminal
8	CAP_PA_4M	Power	-	-	PA DC/DC Converter Capacitor 4 Minus Terminal
9	CAP_PA_4P	Power	-	-	PA DC/DC Converter Capacitor 4 Plus Terminal
10	VDDPA	Power	-	-	Internal Power Amplifier Power Supply, Bypass
30	VDDA	Power	-	-	Regulated Analog Supply, Bypass
31	VCORE	Power	-	-	Regulated Core Supply, Bypass
32	VOSC	Power	-	-	Regulated Oscillator Supply, Bypass
54	VPP	Test			Internal Regulator Test Port
56	VPRIME	Power	-	-	Internal Primary Power Supply, Bypass
57	CAP_PRIME_4P	Power	-	-	Primary DC/DC Converter Capacitor 4 Plus Terminal
58	CAP_PRIME_4M	Power	-	-	Primary DC/DC Converter Capacitor 4 Minus Terminal
59	CAP_PRIME_3M	Power	-	-	Primary DC/DC Converter Capacitor 3 Minus Terminal
60	CAP_PRIME_3P	Power	-	-	Primary DC/DC Converter Capacitor 3 Plus Terminal
61	CAP_PRIME_2P	Power	-	-	Primary DC/DC Converter Capacitor 2 Plus Terminal
62	CAP_PRIME_2M	Power	-	-	Primary DC/DC Converter Capacitor 2 Minus Terminal
63	CAP_PRIME_1M	Power	-	-	Primary DC/DC Converter Capacitor 1 Minus Terminal
64	CAP_PRIME_1P	Power	-	-	Primary DC/DC Converter Capacitor 1 Plus Terminal
65	VSUPPLY	Power	-	-	Power Supply Input to Eterna

NO	RADIO	TYPE	I/O	PULL	DESCRIPTION
1	RADIO_INHIBIT	1 (Note 14)	I	-	Radio Inhibit
11	LNA_EN *GPIO17*	1	O *I/O*	- -	External LNA Enable *General Purpose Digital I/O*
12	RADIO_TX *GPIO18*	1	O *I/O*	- -	Radio TX Active (External PA Enable/Switch Control) *General Purpose Digital I/O*
13	RADIO_TXn *GPIO19*	1	O *I/O*	- -	Radio TX Active (External PA Enable/Switch Control), Active Low *General Purpose Digital I/O*
14	ANTENNA	-	-	-	Single-Ended Antenna Port, 50Ω

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

NO	ANALOG	TYPE	I/O	PULL	DESCRIPTION
15	AI_0	Analog	I	-	Analog Input 0
16	AI_1	Analog	I	-	Analog Input 1
17	AI_3	Analog	I	-	Analog Input 3
18	AI_2	Analog	I	-	Analog Input 2

NO	CRYSTALS	TYPE	I/O	PULL	DESCRIPTION
19	OSC_32K_XOUT	Crystal	I	-	32 kHz Crystal Xout
20	OSC_32K_XIN	Crystal	I	-	32 kHz Crystal Xin
28	OSC_20M_XIN	Crystal	I	-	20 MHz Crystal Xin
29	OSC_20M_XOUT	Crystal	I	-	20 MHz Crystal Xout

NO	RESET	TYPE	I/O	PULL	DESCRIPTION
22	RESETn	1	I	UP	Reset Input, Active Low

NO	JTAG	TYPE	I/O	PULL	DESCRIPTION
23	TDI	1	I	UP	JTAG Test Data In
24	TDO	1	O	-	JTAG Test Data Out
25	TMS	1	I	UP	JTAG Test Mode Select
26	TCK	1	I	DOWN	JTAG Test Clock

NO	GPIOS (NOTE 14)	TYPE	I/O	PULL	DESCRIPTION
27	DP4 (GPIO23)	1	I/O	-	General Purpose Digital I/O
33	DP3 (GPIO22) *TIMER8_EXT*	1	I/O I	- -	General Purpose Digital I/O *External Input to 8-Bit Timer/Counter*
34	DP2 (GPIO21) *LPTIMER_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to Low Power Timer/Counter*
36	DP0 (GPIO0) SPIM_SS_2n	1	I/O O	- -	General Purpose Digital I/O SPI Master Slave Select 2, Active Low
48	DP1 (GPIO20) *TIMER16_EXT*	1	I/O *I*	- -	General purpose digital I/O *External Input to 16-Bit Timer/Counter*

NO	SPECIAL PURPOSE	TYPE	I/O	PULL	DESCRIPTION
35	*SLEEPn* *GPIO14*	1 (Note 14)	*I* *I/O*	- -	*Deep Sleep, Active Low* *General Purpose Digital I/O*
49	*PWM0* *TIMER16_OUT* GPIO16	2	*O* *O* I/O	- - -	*Pulse Width Modulator 0* *16-Bit Timer/Counter Match Output/PWM Output* General Purpose Digital I/O
72	TIMEn	1 (Note 14)	I	-	Time Capture Request, Active Low

NO	CLI	TYPE	I/O	PULL	DESCRIPTION
37	UARTC0_TX	2	O	-	CLI UART 0 Transmit
38	UARTC0_RX	1	I	UP	CLI UART 0 Receive

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

NO	SPI MASTER	TYPE	I/O	PULL	DESCRIPTION
39	SPIM_MISO GPIO11	1	I I/O	- -	SPI Master (MISO) Master In Slave Out Port General Purpose Digital I/O
41	SPIM_MOSI GPIO10	2	O I/O	- -	SPI Master (MOSI) Master Out Slave In Port General Purpose Digital I/O
43	SPIM_SCK GPIO9	2	O I/O	- -	SPI Master (SCK) Serial Clock Port General Purpose Digital I/O
46	SPIM_SS_1n GPIO13	1	O I/O	- -	SPI Master Slave Select 1, Active Low General Purpose Digital I/O
47	SPIM_SS_0n GPIO12	1	O I/O	- -	SPI Master Slave Select 0, Active Low General Purpose Digital I/O

NO	IPCS SPI/FLASH PROGRAMMING (NOTE 16)	TYPE	I/O	PULL	DESCRIPTION
40	IPCS_MISO *TIMER16_OUT* GPIO6	2	O O I/O	- - -	SPI Flash Emulation (MISO) Master In Slave Out Port *16-Bit Timer/Counter Match Output/PWM Output* General Purpose Digital I/O
42	IPCS_MOSI *TIMER16_EXT* GPIO5	1	I *I* I/O	- - -	SPI Flash Emulation (MOSI) Master Out Slave In Port *External Input to 16-bit Timer/Counter* General Purpose Digital I/O
44	IPCS_SCK *TIMER8_EXT* GPIO4	1	I *I* I/O	- - -	SPI Flash Emulation (SCK) Serial Clock Port *External Input to 8-Bit Timer/Counter* General Purpose Digital I/O
45	IPCS_SSn *LPTIMER_EXT* GPIO3	1	I *I* I/O	- - -	SPI Flash Emulation Slave Select, Active Low *External Input to Low Power Timer/Counter* General Purpose Digital I/O
55	FLASH_P_ENn	1	I	UP	Flash Program Enable, Active Low

NO	I^2C/1-WIRE/SPI SLAVE	TYPE	I/O	PULL	DESCRIPTION
50	*SPIS_MISO* *UARTC1_TX* 1_WIRE	2	*O* *O* I/O	- - -	*SPI Slave (MISO) Master In Slave Out Port* *CLI UART 1 Transmit* 1 Wire Master
51	*SPIS_MOSI* *UARTC1_RX* GPIO26	1	*I* *I* I/O	- - -	*SPI Slave (MOSI) Master Out Slave In Port* *CLI UART 1 Receive* General Purpose Digital I/O
52	*SPIS_SCK* SCL	2	*I* I/O	- -	*SPI Slave (SCK) Serial Clock Port* I2C Serial Clock
53	*SPIS_SSn* SDA	2	*I* I/O	- -	*SPI Slave Select, Active Low* I2C Serial Data

NO	API UART	TYPE	I/O	PULL	DESCRIPTION
66	UART_RX_RTSn	1 (Note 14)	I	-	UART Receive (RTS) Request to Send, Active Low
67	UART_RX_CTSn	1	O	-	UART Receive (CTS) Clear to Send, Active Low
68	UART_RX	1 (Note 14)	I	-	UART Receive
69	UART_TX_RTSn	1	O	-	UART Transmit (RTS) Request to Send, Active Low
70	UART_TX_CTSn	1 (Note 14)	I	-	UART Transmit (CTS) Clear to Send, Active Low
71	UART_TX	2	O	-	UART Transmit

Note 14: These inputs are always enabled and must be driven or pulled to a valid state to avoid leakage.

Note 15: See also pins 40, 42, 44, and 45 for additional GPIO ports.

Note 16: Embedded programming over the IPCS SPI bus is only avaliable when RESETn is asserted.

PIN FUNCTIONS

VSUPPLY: System and I/O Power Supply. Provides power to the chip including the on-chip DC/DC converters. The digital-interface I/O voltages are also set by this voltage. Bypass with 2.2µF and 0.1µF to ensure the DC/DC converters operate properly.

VDDPA: PA-Converter Bypass Pin. A 0.47µF cap should be connected from VDDPA to ground with as short a trace as feasible. Do not connect anything else to this pin.

VDDA: Analog-Regulator Bypass Pin. A 0.1µF cap should be connected from VDDA to ground with as short a trace as feasible. Do not connect anything else to this pin.

VCORE: Core-Regulator Bypass Pin. A 56nF cap should be connected from VCORE to ground with as short a trace as feasible. Do not connect anything else to this pin.

VOSC: Oscillator-Regulator Bypass Pin. A 56nF cap should be connected from VOSC to ground with as short a trace as feasible. Do not connect anything else to this pin.

VPP: Maunufacturing Test port for internal regulator. Do not connect anything to this pin.

VPRIME: Primary-Converter Bypass Pin. A 0.22µF cap should be connected from VPRIME to ground with as short a trace as feasible. Do not connect anything else to this pin.

VBGAP: Bandgap Reference Output. Used for testing and calibration. Do not connect anything to this pin.

CAP_PA_1P, CAP_PA_1M through CAP_PA_4P, CAP_PA_4M: Dedicated Power-Amplifier DC/DC Converter Capacitor Pins. These pins are used when the radio is transmitting to efficiently convert VSUPPLY to the proper voltage for the power amplifier. A 56nF cap should be connected between each P and M pair. Trace length should be as short as feasible.

CAP_PRIME_1P, CAP_PRIME_1M through CAP_PRIME_4P, CAP_PRIME_4M: Primary DC/DC Converter Capacitor Pins. These pins are used when the device is awake to efficiently convert VSUPPLY to the proper voltage for the three on-chip low-dropout regulators. A 56nF cap should be connected between each P and M pair. Trace length should be as short as feasible.

RADIO_INHIBIT: RADIO_INHIBIT provides a mechanism for an external device to temporarily disable radio operation. Failure to observe the timing requirements defined in the Radio_Inhibit AC Characteristics table, may result in unreliable network operation. In designs where the RADIO_INHIBIT function is not needed the input must either be tied, pulled or actively driven low to avoid excess leakage.

LNA_ENABLE, RADIO_TX, RADIO_TXn: Control signals generated by the autonomous MAC supporting the integration of an external LNA/PA. See the Eterna Extended Range Reference Design for implementation details.

ANTENNA: Multiplexed Receiver Input and Transmitter Output Pin. The impedance presented to the antenna pin should be 50Ω, single-ended with respect to paddle ground. To ensure regulatory compliance of the final product please see the Eterna Integration Guide for filtering requirements. The antenna pin should not have a DC path to ground; AC blocking must be included if a DC-grounded antenna is used.

AI_0, AI_1, AI_2, AI_3: Analog Inputs. These pins are multiplexed to the analog input chain. The analog input chain, as shown in Figure 12, is software-configurable and includes a variable-gain amplifier, an offset-DAC for adjusting input range, and a 10b ADC. Valid input range is between 0 to 1.8V. Analog inputs can be sampled as described in the On-Chip Software Development Kit (On-Chip SDK).

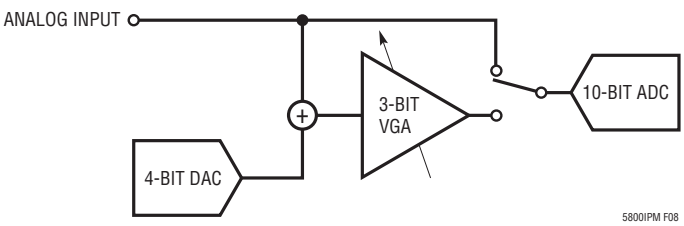


Figure 12. Analog Input Chain

PIN FUNCTIONS

OSC_32K_XOUT: Output Pin for the 32kHz Oscillator. Connect to 32kHz quartz crystal. The OSC_32K_XOUT and OSC_32K_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 13.

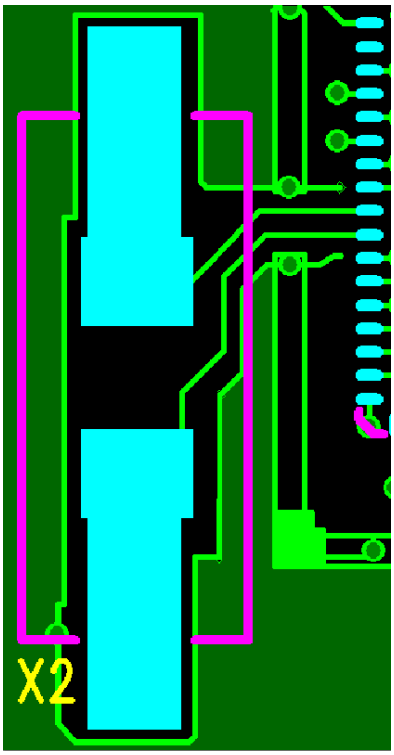


Figure 13. PCB Top Metal Layer Shielding of Crystal Signals

OSC_32K_XIN: Input for the 32kHz Oscillator. Connect to 32kHz quartz crystal.The OSC_32K_XOUT and OSC_32K_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 13.

OSC_20M_XOUT: Output for the 20MHz Oscillator. Connect only to a supported 20MHz quartz crystal. The OSC_20M_XOUT and OSC_20M_XIN traces must be well-shielded from other signals, as shown in Figure 13. See the Eterna Integration Guide for supported crystals.

OSC_20M_XIN: Input for the 20MHz Oscillator. Connect only to a supported 20MHz quartz crystal. The OSC_20M_XOUT and OSC_20M_XIN traces must be well-shielded from other signals, both on the same PCB layer and lower PCB layers, as shown in Figure 13.

RESETn: The asynchronous reset signal is internally pulled up. Resetting Eterna will result in the ARM Cortex M3 rebooting and loss of network connectivity. Use of this signal for resetting Eterna is not recommended except during power-on and in-circuit programming.

TMS, TCK, TDI, TDO: JTAG Port Supporting Software Debug and Boundary Scan. An IEEE Std 1149.1b-1994 compliant Boundary Scan Definition Language (BDSL) file for the WR QFN72 package can be found here.

SLEEPn: The SLEEPn function is not currently supported in software. The SLEEPn input must either be tied, pulled or actively driven high to avoid excess leakage.

UART_RX, UART_RX_RTSn, UART_RX_CTSn, UART_TX, UART_TX_RTSn, UART_TX_CTSn: The API UART interface includes bi-directional wake up and flow control. Unused input signals must be driven or pulled to their inactive state.

TIMEn: Strobing the TIMEn input is the most accurate method to acquire the network time maintained by Eterna. Eterna latches the network timestamp with sub-microsecond resolution on the rising edge of the TIMEn signal and produces a packet on the API serial port containing the timing information.

UARTC0_RX, UARTC0_TX: The CLI UART provides a mechanism for monitoring, configuration and control of Eterna during operation. For a complete description of the supported commands see the SmartMesh IP Mote CLI Guide.

GPIO0, GPIO3 - GPIO6, GPIO9 - GPIO13, GPIO16, GPIO20 - GPIO23, GPIO26: General purpose IO that can be sampled or driven as described in the On-Chip Software Development Kit (On-Chip SDK).

PIN FUNCTIONS

FLASH_P_ENn, IPCS_SSn, IPCS_SCK, IPCS_MISO, IPCS_SSn: The In-circuit Programming Control System (IPCS) bus enables in-circuit programming of Eterna's flash memory. IPCS_SCK is a clock and should be terminated appropriately for the driving source to prevent overshoot and ringing.

SPIM_CLK, SPIM_MISO, SPIM_MOSI, SPIM_SS_0n, SPIM_SS_1n, SPIM_SS_4n: The SPI Master bus with support for up to three SPI slave devices, via the On-Chip Software Development Kit (On-Chip SDK) provides an interface to SPI peripheral slave devices. The SPI interface is syncrhonous to SPIM_CLK, which should be treated as a clock singal and terminated appropriately .

1_WIRE: The 1-Wire master clock/data/power signal. See the On-Chip Software Development Kit (On-Chip SDK) for details on operating the 1-Wire Master controller.

SCL, SDA: The I^2C bus SCL and SDA should be externally pulled to VSUPPLY with a 10kΩ resistor. See the On-Chip Software Development Kit (On-Chip SDK) for details on operating the 1-Wire Master controller.

OPERATION

The LTC5800 is the world's most energy-efficient IEEE 802.15.4 compliant platform, enabling battery and energy harvested applications. With a powerful 32-bit ARM Cortex™-M3, best-in-class radio, flash, RAM and purpose-built peripherals, Eterna provides a flexible, scalable and robust networking solution for applications demanding minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 14, Eterna integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low-power states. Items in the gray shaded region labeled "Analog Core" correspond to the analog/RF components.

POWER SUPPLY

Eterna is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. Eterna's two on-chip DC/DC converters minimize energy consumption while the device is awake. To conserve power the DC/DC converters are disabled when the device is in low-power state. Integrated power supply conditioning, including the two integrated DC/DC converters and three integrated low-dropout regulators, provides excellent rejection of supply noise. Eterna's operating supply voltage range is high enough to support direct connection to lithium-thionyl chloride (Li-$SOCl_2$) sources and wide enough to support battery operation over a broad temperature range.

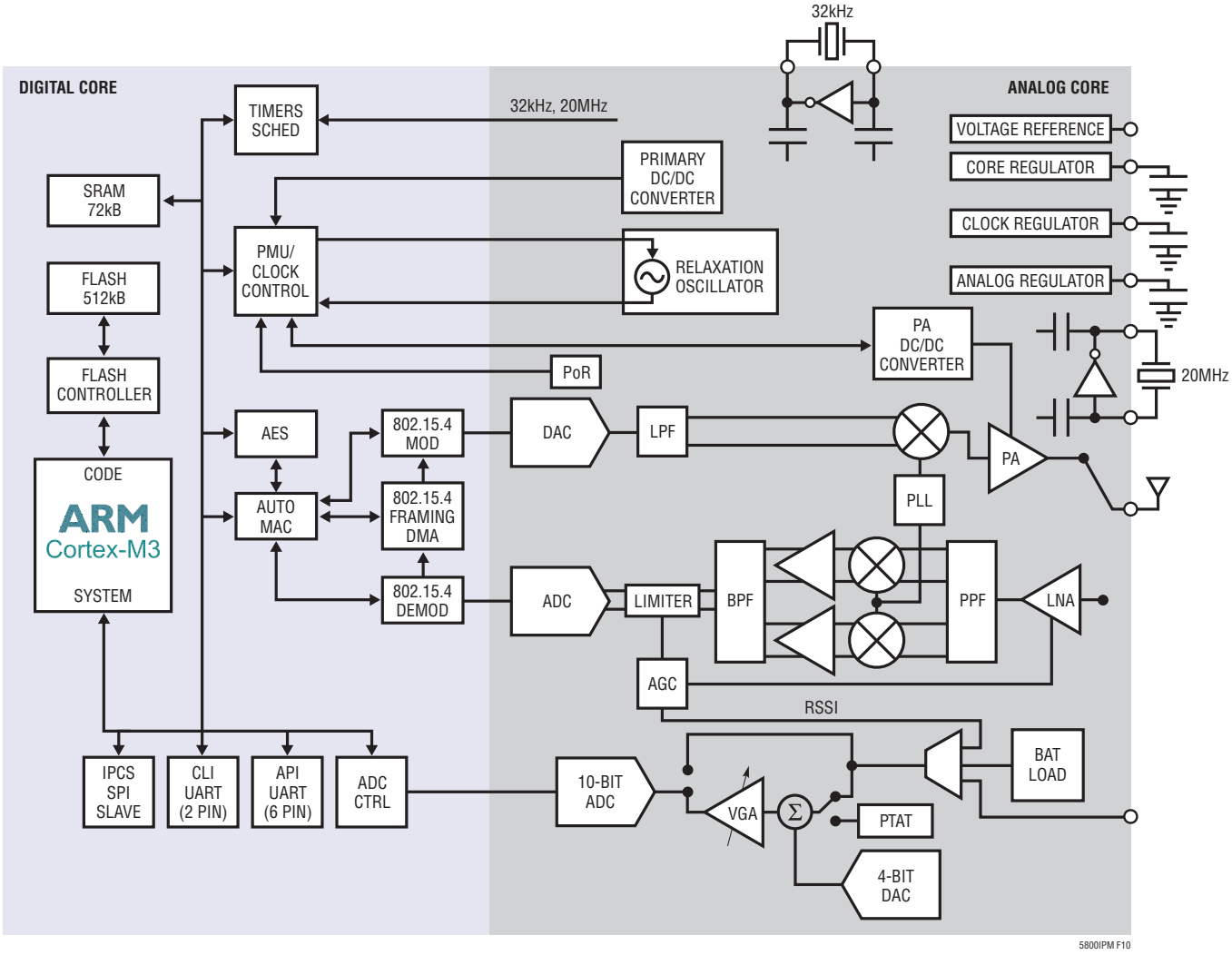


Figure 14. Eterna Block Diagram

OPERATION

SUPPLY MONITORING AND RESET

Eterna integrates a Power-on reset (PoR) circuit. As the RESETn input pin is nominally configured with an internal pull-up resistor, no connection is required. For a graceful shutdown, the software and the networking layers should be cleanly halted via API commands prior to assertion of the RESETn pin. See the SmartMesh IP Mote API Guide for details on the disconnect and reset commands. Eterna includes a soft brown-out monitor that fully protects the flash from corruption in the event that power is removed while writing to flash. Integrated flash supervisory functionality, in conjunction with a fault tolerant file system, yields a robust nonvolatile storage solution.

PRECISION TIMING

Eterna's unique low power dedicated timing hardware and timing algorithms provides a significant improvement over competing 802.15.4 product offerings. This functionality provides timing precision two to three orders of magnitude better than any other low-power solution available at the time of publication. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by SmartMesh networks. Eterna's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating Eterna's reliability when compared with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

APPLICATION TIME SYNCHRONIZATION

In addition to coordinating time slots across the network, which is transparent to the user, Eterna's timing management is used to support two mechanisms to share network time. Having an accurate, shared, network-wide time base enables events to be accurately time stamped or tasks to be performed in a synchronized fashion across a network. Eterna will send a time packet through its serial interface when one of the following occurs:

- Eterna receives an API request to read time
- The TIMEn signal is asserted

The use of TIMEn has the advantage of being more accurate. The value of the timestamp is captured in hardware relative to the rising edge of TIMEn. If an API request is used, due to packet processing, the value of the timestamp may be captured several milliseconds after receipt of the packet. See the TIMEn AC Characteristics section for the TIMEn function's definition and specifications.

TIME REFERENCES

Eterna includes three clock sources: an internal relaxation oscillator, a low power oscillator designed for a 32.768kHz crystal, and the radio reference oscillator designed for a 20MHz crystal.

Relaxation Oscillator

The relaxation oscillator is the primary clock source for Eterna, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator is dynamically calibrated to 7.3728MHz. The internal relaxation oscillator typically starts up in a few µs, providing an expedient, low-energy method for duty cycling between active and low power states. Quick start-up from the doze state, defined in the State Diagram section, allows Eterna to wake up and receive data over the UART and SPI interfaces by simply detecting activity on the appropriate signals.

32.768kHz Crystal

Once Eterna is powered up and the 32.768kHz crystal source has begun oscillating, the 32.768kHz crystal remains operational while in the Active state, and is used as the timing basis when in Doze state. See the State Diagram section, for a description of Eterna's operational states.

20MHz Crystal

The 20MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by Eterna as needed. Eterna requires specific characterized 20MHz crystal references. See the the Eterna Integration Guide for a complete list of the currently supported 20MHz crystals.

OPERATION

RADIO

Eterna includes the lowest-power commercially available 2.4GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to the Radio Specifications section for power consumption numbers.). Eterna's integrated power amplifier is calibrated and temperature-compensated to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, Eterna uniquely includes a hardware-based autonomous MAC that handles precise sequencing of peripherals, including the transmitter, the receiver, and advanced encryption standard (AES) peripherals. The hardware-based autonomous media access controller (MAC) minimizes CPU activity, thereby further decreasing power consumption.

UARTS

The principal network interface is through the application programming interface (API) UART. A command-line interface (CLI) is also provided for support of test and debug functions. Both UARTs sense activity continuously, consuming virtually no power until data is transferred and automatically returning to their lowest power state after the conclusion of a transfer. The definition for packet encoding on the API UART interface can be found in the SmartMesh IP Mote API Guide and the CLI command definitions can be found in the SmartMesh IP Mote CLI Guide.

API UART Protocols

The API UART supports multiple modes with the goal of supporting a wide range of companion multipoint control units (MCUs) while reducing power consumption of the system. As a general rule, higher serial data rates translate into lower energy consumption for both endpoints. The API UART receive protocol includes two additional signals in addition to UART_RX: UART_RX_RTSn and UART_RX_CTSn. The transmit half of the API UART protocol includes two additional signals in addition to UART_TX: UART_TX_RTSn and UART_TX_CTSn. The two supported protocols are referred to as UART Mode 2 and UART Mode 4. Mode setting is controlled via the Fuse Table.

In the Figures accompanying the protocol descriptions, signals driven by the companion processor are drawn in black and signals driven by Eterna are drawn in blue.

UART Mode 2

UART Mode 2 provides the most energy-efficient method for operating Eterna's API UART. UART Mode 2 requires the use of all six UART signals, but does not require adherence to the minimum inter-packet delay as defined in the UART AC Characteristics section. UART Mode 2 incorporates edge-sensitive flow control, at either 9600 or 115200 baud. Packets are HDLC encoded with one stop bit and no parity bit. The flow control signals for Eterna's API receive path are shown in Figure 15. Transfers are initiated by the companion processor asserting UART_RX_RTSn. Eterna then responds by enabling the UART and asserting UART_RX_CTSn. After detecting the assertion of UART_RX_CTSn the companion processor sends the entire packet. Following the transmission of the final byte in the packet, the companion processor negates UART_RX_RTSn and waits until the negation of UART_RX_CTSn before asserting UART_RX_RTSn again.

The flow control signals for Eterna's API transmit path are shown in Figure 16. Transfers are initiated by Eterna asserting UART_TX_RTSn. The companion processor responds by asserting UART_TX_CTSn when ready to receive data. After detecting the falling edge of UART_TX_CTSn Eterna sends the entire packet. Following the transmission of the final byte in the packet Eterna negates UART_TX_RTSn and waits until the negation of UART_TX_CTSn before asserting UART_TX_RTSn again. The companion processor may negate UART_TX_CTSn any time after the first byte is transferred provided the time out from UART_TX_RTSn to UART_TX_CTSn, $t_{END\_TX\_RTS\ to\ TX\_CTS}$, is met.

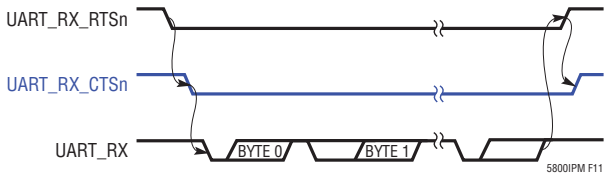


Figure 15. UART Mode 2 Receive Flow Control

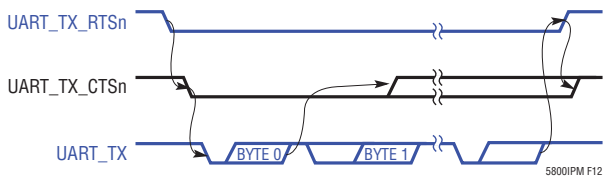


Figure 16. UART Mode 2 Transmit Flow Control

OPERATION

UART Mode 4

UART Mode 4 incorporates level-sensitive flow control on the TX channel and requires no flow control on the RX channel, supporting both 9600 and 115200 baud. The use of level-sensitive flow control signals enables data rates above 9600 baud with the option of using a reduced set of the flow control signals; however, Mode 4 has specific limitations. First, The use of the RX flow control signals (UART_RX_RTSn and UART_RX_CTSn) for Mode 4 are optional provided the use is limited to the industrial temperature range (–40°C to 85°C); otherwise, the flow control is mandatory. If RX flow control signals are not used, UART_RX_RTSn should be tied to VSUPPLY (inactive) and UART_RX_CTSn should be left unconnected. Second, unless the companion processor is always ready to receive a packet, the companion processor must negate UART_TX_CTSn prior to the end of the current packet. Failure to negate UART_TX_CTSn prior to the end of a packet may result in back to back packets. Third, the companion processor must wait at least $t_{RX\_INTERPACKET}$ between transmitting packets on UART_RX. See the UART AC Characteristics section for complete timing specifications. Packets are HDLC encoded with one stop bit and no parity bit. The flow control signals for the TX channel are shown in Figure 17. Transfers are initiated by Eterna asserting UART_TX_RTSn. The UART_TX_CTSn signal may be actively driven by the companion processor when ready to receive a packet or UART_TX_CTSn may be tied low if the companion processor is always ready to receive a packet. After detecting a logic '0' on UART_TX_CTSn Eterna sends the entire packet. Following the transmission of the final byte in the packet Eterna negates UART_TX_RTSn and waits for $t_{TX\_INTERPACKET}$, defined in the UART AC Characteristics section, before asserting UART_TX_RTSn again.

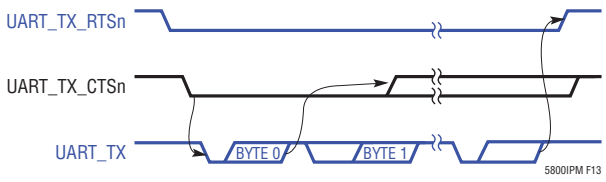


Figure 17. UART Mode 4 Transmit Flow Control

For details on the timing of the UART protocol, see the UART AC Characteristics section.

CLI UART

The command line interface (CLI) UART port is a two wire protocol (TX and RX) that operates at a fixed 9600 baud rate with one stop bit and no parity. The CLI UART interface is intended to support command line instructions and response activity.

AUTONOMOUS MAC

Eterna was designed as a system solution to provide a reliable, ultralow power, and secure network. A reliable network capable of dynamically optimizing operation over changing environments requires solutions that are far too complex to completely support through hardware acceleration alone. As described in the Precision Timing section, proper time management is essential for optimizing a solution that is both low power and reliable. To address these requirements Eterna includes the Autonomous MAC, which incorporates a co-processor for controlling all of the time-critical radio operations. The Autonomous MAC provides two benefits: first, preventing variable software latency from affecting network timing and second, greatly reducing system power consumption by allowing the CPU to remain inactive during the majority of the radio activity. The Autonomous MAC, provides software-independent timing control of the radio and radio-related functions, resulting in superior reliability and exceptionally low power.

SECURITY

Network security is an often overlooked component of a complete network solution. Proper implementation of security protocols is significant in terms of both engineering effort and market value in an OEM product. Eterna system solutions provide a FIPS-140 compliant encryption scheme that includes authentication and encryption at the MAC and network layers with separate keys for each mote. This not only yields end-to-end security, but if a mote is somehow compromised, communication from other motes is still secure. A mechanism for secure key exchange allows keys to be kept fresh. To prevent physical attacks, Eterna includes hardware support for

OPERATION

electronically locking devices, thereby preventing access to Eterna's flash and RAM memory and thus the keys and code stored therein. This lock-out feature also provides a means to securely unlock a device should support of a product require access. For details see the Board Specific Configuration Guide.

TEMPERATURE SENSOR

Eterna includes a calibrated temperature sensor on chip. The temperature readings are available locally through Eterna's serial API, in addition to being available via the network manager. The performance characteristics of the temperature sensor can be found in the Typical Performance Characteristics section.

RADIO INHIBIT

The RADIO_INHIBIT input enables an external controller to temporarily disable the radio software drivers (for example, to take a sensor reading that is susceptible to radio interference). When RADIO_INHIBIT is asserted the software radio drivers will disallow radio operations including clear channel assessment, packet transmits, or packet receipts. If the current timeslot is active when RADIO_INHIBIT is asserted the radio will be diabled after the present operation completes. For details on the timing associated with RADIO_INHIBIT, see the Radio_Inhibit AC Characteristics section.

FLASH PROGRAMMING

This product is provided without software programmed into the device. OEMs will need to program software images during development and manufacturing. Eterna's software images are loaded via the In-Circuit Programming Control System (IPCS) SPI interface. Sequencing of RESETn and FLASH_P_ENn, as described in the Flash SPI Slave AC Characteristics section, places Eterna in a state emulating a serial flash to support in-circuit programming. Hardware and software for supporting development and production programming of devices is described in the Eterna Serial Programmer Guide. The serial protocol, SPI, and timing parameters are described in the Flash SPI Slave AC Characteristics section.

FLASH DATA RETENTION

Eterna contains internal flash (non-volatile memory) to store calibration results, unique ID, configuration settings and software images. Flash retention is specified over the operating temperature range. See the Electrical Characteristics and Absolute Maximum Ratings sections.

Non destructive storage above the operating temperature range of –55°C to 105°C is possible; although, this may result in a degradation of retention characteristics.

The degradation in flash retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 0.6eV

$k = 8.625 \bullet 10^{-5}$eV/°K

T_{USE} = is the specified temperature retention in °C

T_{STRESS} = actual storage temperature in °C

Example: Calculate the effect on retention when storing at a temperature of 125°C.

T_{STRESS} = 125°C

T_{USE} = 85°C

AF = 7.1

So the overall retention of the flash would be degraded by a factor of 7.1, reducing data retention from 20 years at 85°C to 2.8 years at 125°C.

STATE DIAGRAM

In order to provide capabilities and flexibility in addition to ultra low power, Eterna operates in various states, as shown in Figure 18. State transitions shown in red are not recommended.

OPERATION

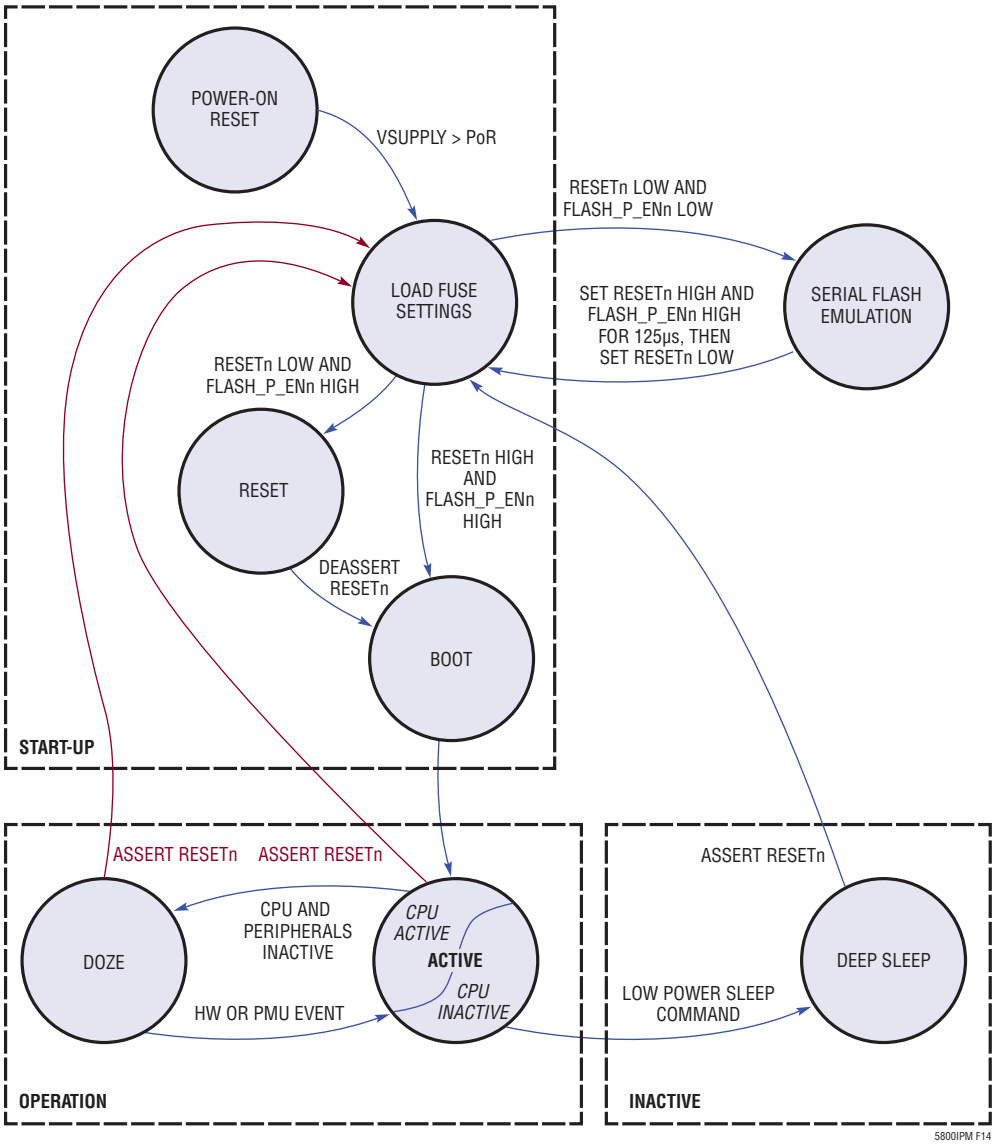


Figure 18. Eterna State Diagram

OPERATION

Fuse Table

Eterna's Fuse Table is a 2kB page in flash that contains two data structures. One structure supports hardware configuration immediately following power-on reset or the assertion of RESETn. The second structure supports configuration of software board support parameters. Fuse Tables are generated via the Fuse Table application described in the Board Specific Configuration Guide. Hardware configuration of I/O immediately following power-on reset provides a method to minimize leakage due to floating nets prior to software configuration. I/O leakage can contribute hundreds of microamperes of leakage per input, potentially stressing current limited supplies. Examples of software board support parameters include setting of UART modes, clock sources and trim values. Fuse Tables are loaded into flash using the same software and in-circuit programmer used to load software images as described in the Eterna Serial Programmer Guide.

Start-Up

Start-up occurs as a result of either crossing the power-on reset threshold or asserting RESETn. After the completion of power-on reset or the falling edge of an internally synchronized RESETn, Eterna loads its Fuse Table which, as described in the previous section, includes configuring I/O direction. In this state, Eterna checks the state of the FLASH_P_ENn and RESETn pins and enters the serial flash emulation mode if both signals are asserted. If the FLASH_P_ENn pin is not asserted but RESETn is asserted, Eterna automatically reduces its energy consumption to a minimum until RESETn is released. Once RESETn is de-asserted, Eterna goes through a boot sequence, and then enters the active state.

Serial Flash Emulation

When both RESETn and FLASH_P_ENn are asserted, Eterna disables normal operation and enters a mode to emulate the operation of a serial flash. In this mode, its flash can be programmed.

Operation

Once Eterna has completed start-up, Eterna transitions to the operational group of states (active/CPU active, active/CPU inactive, and doze). There, Eterna cycles between the various states, automatically selecting the lowest possible power state while fulfilling the demands of network operation.

Active State

In the active state, Eterna's relaxation oscillator is running and peripherals are enabled as needed. The ARM Cortex-M3 cycles between CPU-active and CPU-inactive (referred to in the ARM Cortex-M3 literature as sleep now mode). Eterna's extensive use of DMA and intelligent peripherals that independently move Eterna between active state and doze state minimizes the time the CPU is active, significantly reducing Eterna's energy consumption.

Doze State

The doze state consumes orders of magnitude less current than the active state and is entered when all of the peripherals and the CPU are inactive. In the doze state Eterna's full state is retained, timing is maintained, and Eterna is configured to detect, wake, and rapidly respond to activity on I/Os (such as UART signals and the TIMEn pin). In the doze state the 32.768kHz oscillator and associated timers are active.

SPI MASTER

The Eterna SPI master controller supports all configurations of clock polarity and phase, with a setable shift clock frequencies of 460.8kHz, 921.6kHz, 1.8432MHz, or 3.6864MHz. In addition the SPI master controller can be configured to repetatively issue commands and capture the corresponding output, enabling repetative sampling of signals from a SPI ADC or SPI sensor based upon a clock reference of better than ±50ppm. For implementation details refer to the On-Chip Software Development Kit (On-Chip SDK).

OPERATION

I²C MASTER

The I²C Master enables control of I²C slave devices, including support for clock stretching slaves. I²C Multi-master and bus arbitration protocols are not supported. For implementation details refer to the On-Chip Software Development Kit (On-Chip SDK).

1-WIRE MASTER

The Eterna 1-Wire Master controller supports the reset, pressense detect, read and write 1-Wire protocol operations, incorporating an active pull-up. The active pull-up becomes active when the passive pull-up raises the voltage on the 1_WIRE pin nominally above 1.4V, driving the 1_WIRE signal as specified in Digital I/O Characteristics. For implementation details refer to the On-Chip Software Development Kit (On-Chip SDK).

APPLICATIONS INFORMATION

MODES OF OPERATION

The SmartMesh IP Mote software can be operated in three distinct modes, namely, namely Slave, Master, and On-Chip SDK. Mode selection should be considered during the architecture/design phase of the development process.

Slave Mode

In Slave mode, the Eterna is connected to an external microprocessor through the API UART and is solely used as a networking device. None of the built in I/Os are accessible in this mode. Refer to the SmartMesh IP User's Guide for more detailed information.

Master Mode

In Master mode, no external uProcessor is required and a limited set of functionality is made available with no programming required on the device. The following features are available

- On-Chip Temperature Sensor
- 4 Analog Inputs
- 4 Digital Inputs
- 3 Digital Outputs

Refer to the SmartMesh IP User's Guide for more detailed information.

On-Chip SDK (OCSDK)

The SmartMesh IP On-Chip Software Development Kit (On-Chip SDK) enables development of C-code applications for execution on the LTC5800-IPM, running Micrium's µCOS-II real-time operating system. With the On-Chip SDK, users may quickly and easily develop application code without the need for an external microprocessor.

Applications written within the On-Chip SDK may send and receive wireless messages through the mesh network; process data, such as statistical analysis; execute local decision-making and control; and manage the following peripherals:

- General Purpose Input-Output (GPIO) pins
- Analog-to-Digital Converter (ADC)
- Universal Asynchronous Receiver/Transmitter (UART)
- Serial Peripheral Interface (SPI) Master
- Inter-Integrated Circuit (I2C) Master
- 1-Wire Master

Network connectivity and quality of service is handled by the SmartMesh IP protocol stack. The SmartMesh IP stack comes as a pre-compiled library and delivers >99.999% data reliability while providing ultra low power operation.

APPLICATIONS INFORMATION

REGULATORY AND STANDARDS COMPLIANCE

Radio Certification

Eterna is suitable for systems targeting compliance with worldwide radio frequency regulations: ETSI EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan). Application Programming Interfaces (APIs) supporting regulatory testing are provided on both the API and CLI UART interfaces. The Eterna Certification User Guide provides:

- Reference information required for certification
- Test plans for common regulatory test cases
- Example CLI API calls
- Sample manual language and example label

Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium (Cr^{+6}), mercury (Hg), Polybrominated Biphenyl (PBB), and Polybrominated Diphenyl Ethers (PBDE). Linear Technology is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS-compliant materials and to eliminate or reduce the use of restricted materials to comply with 2002/95/EC.

The RoHS-compliant design features include:

- RoHS-compliant solder for solder joints
- RoHS-compliant base metal alloys
- RoHS-compliant precious metal plating
- RoHS-compliant cable assemblies and connector choices
- Lead-free QFN package
- Halogen-free mold compound
- RoHS-compliant and 245°C re-flow compatible

Note: Customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2002/95/EC. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

SOLDERING INFORMATION

Eterna is suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260°C. A more detailed description of layout recommendations, assembly procedures and design considerations is included in the Eterna Integration Guide.

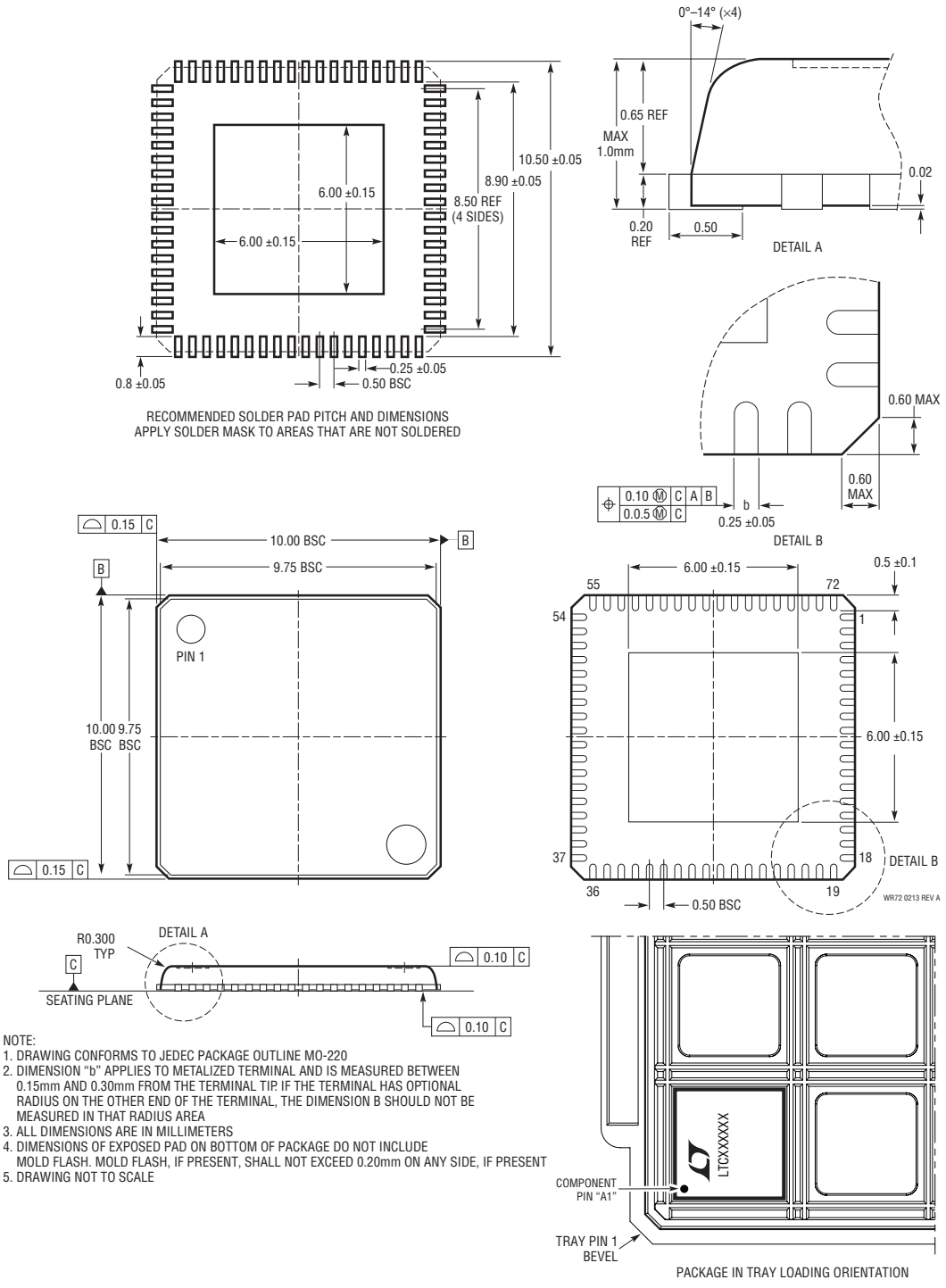
RELATED DOCUMENTATION

TITLE	LOCATION	DESCRIPTION
SmartMesh IP User's Guide	http://www.linear.com/docs/41880	User's guide for Smartmesh IP networks, managers and motes.
SmartMesh IP Mote API Guide	http://www.linear.com/docs/41886	Definitions of the applications interface commands available over the API UART
SmartMesh IP Mote CLI Guide	http://www.linear.com/docs/41885	Definitions of the command line interface commands available over the CLI UART
Eterna Integration Guide	http://www.linear.com/docs/41874	Recommended practices for designing with the LTC5800-IPM
Eterna Serial Programmer Guide	http://www.linear.com/docs/41876	User's guide for the Eterna Serial programmer used for in circuit programming of the LTC5800-IPM
Board Specific Configuration Guide	http://www.linear.com/docs/41875	User's guide for the Eterna Board Specific Configuration application, used to configure the board specific parameters
Eterna Certification User Guide	http://www.linear.com/docs/42918	The essential documentation necessary to complete radio certifications, including examples for common test cases
SmartMesh IP Tools Guide	http://www.linear.com/docs/42453	The user's guide for all IP related tools, and specifically the definition for the On-chip Application Protocol (OAP)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC5800-IPM#packaging for the most recent package drawings.

WR Package
72-Lead QFN (10mm × 10mm)
(Reference LTC DWG # 05-08-1930 Rev A)



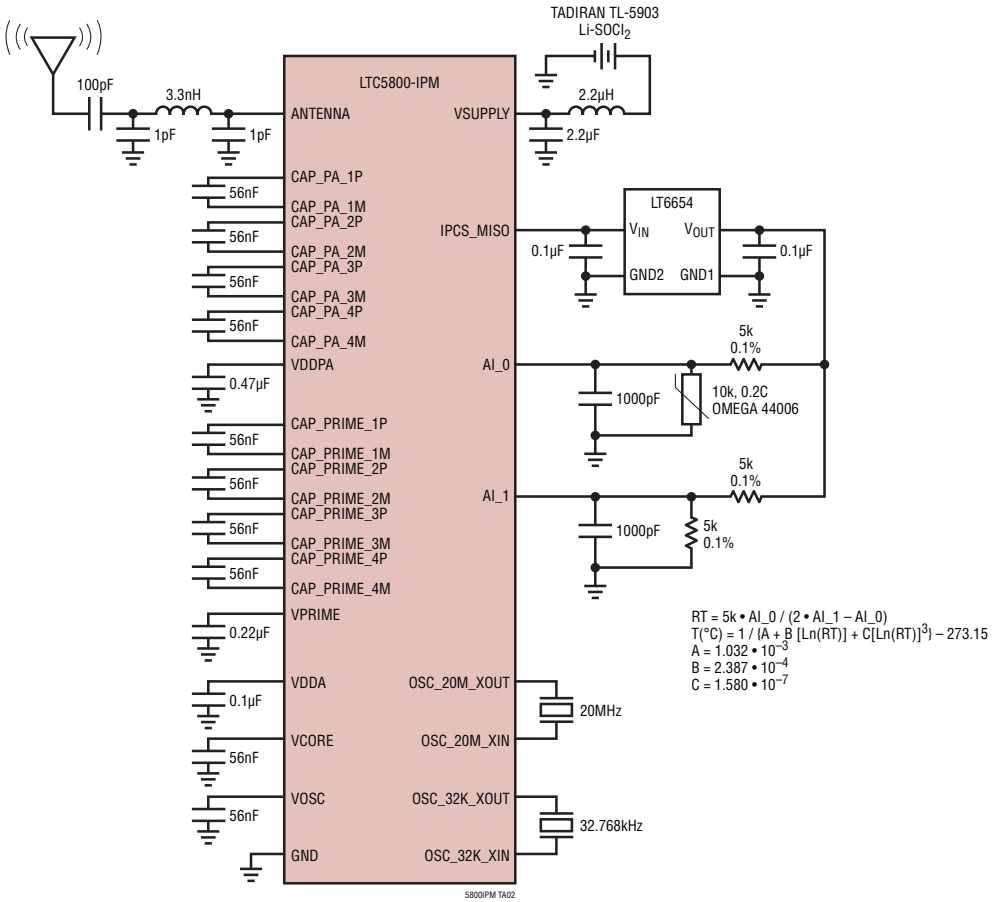
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220
2. DIMENSION "b" APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. DRAWING NOT TO SCALE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Added H-Grade Ordering Information and Product Specifications	4, 5, 29
		Added SPI Master AC Characteristics	12
		Added I^2C Master AC Characteristics	13
		Added 1-Wire Master section	14
		Added Overviews of On-Chip SDK Operation, SPI Master, I^2C Master and 1-Wire Master Ports	32-33

TYPICAL APPLICATION

Mesh Network Thermistor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC5800-IPRA	IP Wireless Mesh 32 Mote Manager	Manages Networks of Up to 32 SmartMesh IP Nodes.
LTC5800-IPRB	IP Wireless Mesh 100 Mote Manager	Manages Networks of Up to 100 SmartMesh IP Nodes.
LTP5901-IPMA	IP Wireless Mesh Mote PCB Module with Chip Antenna	Includes Modular Radio Certification in the United States, Canada, Europe, Japan, South Korea, Taiwan, India, Australia and New Zealand
LTP5902-IPMA	IP Wireless Mesh Mote PCB Module with MMCX Antenna Connector	Includes Modular Radio Certification in the United States, Canada, Europe, Japan, South Korea, Taiwan, India, Australia and New Zealand
LT6654	Precision High Output Drive Low Noise Reference	1.6ppm Peak-to-Peak Noise (0.1Hz to 10Hz), Sink/Source ±10mA, 5ppm/°C Max Drift
LTC2379-18	18-Bit,1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC
LTC3388-1/ LTC3388-3	20V High Efficiency Nanopower Step-Down Regulator	860nA I_Q in Sleep, 2.7V to 20V Input, V_{OUT} = 1.2V to 5.0V, Enable and Standby Pins
LTC3588-1	Piezoelectric Energy Generator with Integrated High Efficiency Buck Converter	V_{IN} = 2.7V to 20V, $V_{OUT(MIN)}$ = Fixed to 1.8V/2.5V/3.3V/3.6V, I_Q = 0.95µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LTC3108-1	Ultralow Voltage Step-Up Converter and Power Manager	V_{IN} = 0.02V to 1V, V_{OUT} = 2.5V/3V/3.7V/4.5V Fixed, I_Q = 6µA, 3mm × 4mm DFN-12 and SSOP-16 Packages
LTC3459	Micropower Synchronous Boost Converter	V_{IN} = 1.5V to 5.5V, $V_{OUT(MAX)}$ = 10V, I_Q = 10µA, 2mm × 2mm DFN, 2mm × 3mm DFN or SOT-23 Package

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