ANALOG DEVICES

180MHz, 1mA Power Efficient Rail-to-Rail I/O Op Amps

FEATURES

- **Gain Bandwidth Product: 180MHz**
- **–3dB Frequency (A_V = 1): 120MHz**
- **Low Quiescent Current: 1mA Max**
- **High Slew Rate: 90V/µs**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- Low Broadband Voltage Noise: 4.2nV/$\sqrt{Hz}$
- Power-Down Mode: 42µA
- Fast Output Recovery
- Supply Voltage Range: 2.5V to 5.25V
- Input Offset Voltage: 0.5mV Max
- Input Bias Current: 100nA
- Large Output Current: 50mA
- CMRR: 110dB
- Open Loop Gain: 45V/mV
- Operating Temperature Range: –40°C to 125°C
- Single in 6-Lead TSOT-23
- Dual in MS8, 2mm × 2mm DFN,TSOT-23, MS10
- Quad in MS16

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Amplifiers
- Fast Current Sensing Amplifiers
- Battery Powered Equipment

DESCRIPTION

The LTC®6246/LTC6247/LTC6248 are single/dual/quad low power, high speed unity gain stable rail-to-rail input/output operational amplifiers. On only 1mA of supply current they feature an impressive 180MHz gain-bandwidth product, 90V/µs slew rate and a low 4.2nV/$\sqrt{Hz}$ of input-referred noise. The combination of high bandwidth, high slew rate, low power consumption and low broadband noise makes these amplifiers unique among rail-to-rail input/output op amps with similar supply currents. They are ideal for lower supply voltage high speed signal conditioning systems.

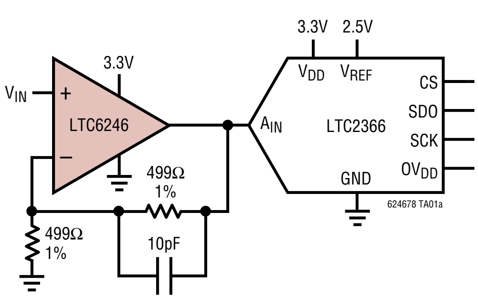
The LTC6246 family maintains high efficiency performance from supply voltage levels of 2.5V to 5.25V and is fully specified at supplies of 2.7V and 5.0V.

For applications that require power-down, the LTC6246 and the LTC6247 in MS10 offer a shutdown pin which disables the amplifier and reduces current consumption to 42µA.

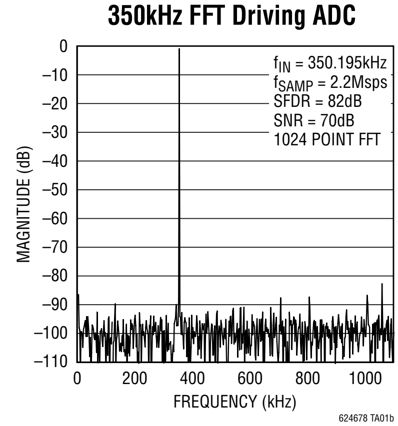
The LTC6246 family can be used as a plug-in replacement for many commercially available op amps to reduce power or to improve input/output range and performance.

TYPICAL APPLICATION

Low Noise Low Distortion Gain = 2 ADC Driver



350kHz FFT Driving ADC



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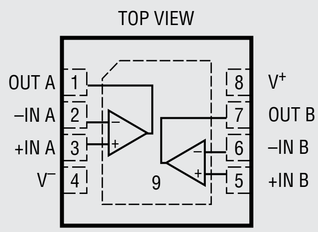
ABSOLUTE MAXIMUM RATINGS (Note 1)

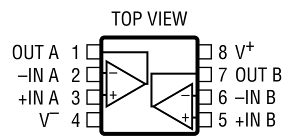
Total Supply Voltage (V^+ to V^-) 5.5V
Input Current (+IN, –IN, $\overline{\text{SHDN}}$) (Note 2) .... ±10mA
Output Current (Note 3) .... ±100mA
Operating Temperature Range (Note 4).. –40°C to 125°C
Specified Temperature Range (Note 5) .. –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Junction Temperature .... 150°C
Lead Temperature (Soldering, 10 sec)
(MSOP, TSOT Packages Only)............................... 300°C

PIN CONFIGURATION

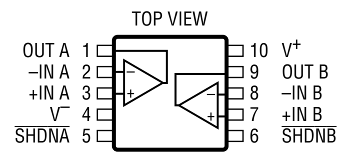


KC PACKAGE
8-LEAD PLASTIC UTDFN (2mm × 2mm × 0.6mm)
T_{JMAX} = 125°C, θ_{JA} = 102°C/W (NOTE 9)
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB

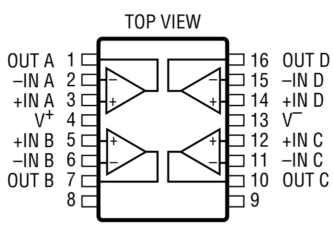
OBSOLETE PACKAGE



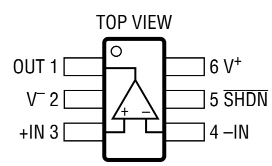
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W (NOTE 9)



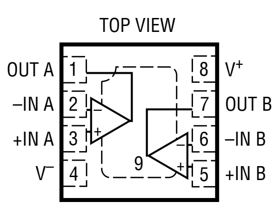
MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 160°C/W (NOTE 9)



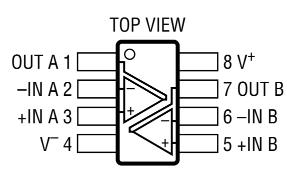
MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 125°C/W (NOTE 9)



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 192°C/W (NOTE 9)



DC PACKAGE
8-LEAD (2mm × 2mm × 0.8mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 102°C/W (NOTE 9)
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 195°C/W (NOTE 9)

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ORDER INFORMATION http://www.linear.com/product/LTC6246#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6246CS6#TRMPBF	LTC6246CS6#TRPBF	LTDWF	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6246IS6#TRMPBF	LTC6246IS6#TRPBF	LTDWF	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6246HS6#TRMPBF	LTC6246HS6#TRPBF	LTDWF	6-Lead Plastic TSOT-23	–40°C to 125°C
		OBSOLETE		
LTC6247CKC#TRMPBF	LTC6247CKC#TRPBF	DWJT	8-Lead (2mm × 2mm × 0.6mm) UTDFN	0°C to 70°C
LTC6247IKC#TRMPBF	LTC6247IKC#TRPBF	DWJT	8-Lead (2mm × 2mm × 0.6mm) UTDFN	–40°C to 85°C
LTC6247CMS8#PBF	LTC6247CMS8#TRPBF	LTDWH	8-Lead Plastic MSOP	0°C to 70°C
LTC6247IMS8#PBF	LTC6247IMS8#TRPBF	LTDWH	8-Lead Plastic MSOP	–40°C to 85°C
LTC6247CTS8#TRMPBF	LTC6247CTS8#TRPBF	LTDWK	8-Lead Plastic TSOT-23	0°C to 70°C
LTC6247ITS8#TRMPBF	LTC6247ITS8#TRPBF	LTDWK	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC6247HTS8#TRMPBF	LTC6247HTS8#TRPBF	LTDWK	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC6247CMS#PBF	LTC6247CMS#TRPBF	LTDWM	10-Lead Plastic MSOP	0°C to 70°C
LTC6247IMS#PBF	LTC6247IMS#TRPBF	LTDWM	10-Lead Plastic MSOP	–40°C to 85°C
LTC6247CDC#TRMPBF	LTC6247CDC#TRPBF	LGVN	8-Lead (2mm × 2mm × 0.8mm) DFN	0°C to 70°C
LTC6247IDC#TRMPBF	LTC6247IDC#TRPBF	LGVN	8-Lead (2mm × 2mm × 0.8mm) DFN	–40°C to 85°C
LTC6248CMS#PBF	LTC6248CMS#TRPBF	6248	16-Lead Plastic MSOP	0°C to 70°C
LTC6248IMS#PBF	LTC6248IMS#TRPBF	6248	16-Lead Plastic MSOP	–40°C to 85°C
LTC6248HMS#PBF	LTC6248HMS#TRPBF	6248	16-Lead Plastic MSOP	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult ADI Marketing for parts specified with wider operating temperature ranges.
Consult ADI Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (V_S = 5V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply	 ●	–500 –1000	50	500 1000	µV µV
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–2.5 –3	0.1	2.5 3	mV mV
ΔV_{OS}	Input Offset Voltage Match (Channel-to-Channel) (Note 8)	V_{CM} = Half Supply	 ●	–600 –1000	50	600 1000	µV µV
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–3.5 –4	0.1	3.5 4	mV mV
V_{OS} T_C	Input Offset Voltage Drift		●		–2		µV/°C
I_B	Input Bias Current (Note 7)	V_{CM} = Half Supply	 ●	–350 –550	–30	350 550	nA nA
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	100 0	400	1000 1500	nA nA

ELECTRICAL CHARACTERISTICS (V_S = 5V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current	V_{CM} = Half Supply		–250	–10	250	nA
			●	–400		400	nA
		V_{CM} = V^+ – 0.5V, NPN Mode		–250	–10	250	nA
			●	–400		400	nA
e_n	Input Noise Voltage Density	f = 100kHz			4.2		nV/√Hz
	Input 1/f Noise Voltage	f = 0.1Hz to 10Hz			1.6		μV_{P-P}
i_n	Input Noise Current Density	f = 100kHz			2.0		pA/√Hz
C_{IN}	Input Capacitance	Differential Mode			2		pF
		Common Mode			0.8		pF
R_{IN}	Input Resistance	Differential Mode			32		kΩ
		Common Mode			14		MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1k to Half Supply (Note 10)		30	45		V/mV
			●	14			V/mV
		R_L = 100Ω to Half Supply (Note 10)		5	15		V/mV
			●	2.5			V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V		78	110		dB
			●	76			dB
I_{CMR}	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.25V		69	73		dB
		V_{CM} = 1V	●	65			dB
	Supply Voltage Range (Note 6)		●	2.5		5.25	V
V_{OL}	Output Swing Low (V_{OUT} – $V^–$)	No Load			25	40	mV
			●			55	mV
		I_{SINK} = 5mA			70	110	mV
			●			160	mV
		I_{SINK} = 25mA			160	250	mV
			●			450	mV
V_{OH}	Output Swing High (V^+ – V_{OUT})	No Load			70	100	mV
			●			150	mV
		I_{SOURCE} = 5mA			130	175	mV
			●			225	mV
		I_{SOURCE} = 25mA			300	500	mV
			●			750	mV
I_{SC}	Output Short-Circuit Current	Sourcing			–80	–35	mA
			●			–30	mA
		Sinking		60	100		mA
			●	40			mA
I_S	Supply Current per Amplifier	V_{CM} = Half Supply			0.95	1	mA
			●			1.4	mA
		V_{CM} = V^+ – 0.5V			1.25	1.4	mA
			●			1.8	mA
I_{SD}	Disable Supply Current per Amplifier	$V_{\overline{SHDN}}$ = 0.8V			42	75	µA
			●			200	µA
$I_{\overline{SHDN}L}$	$\overline{SHDN}$ Pin Current Low	$V_{\overline{SHDN}}$ = 0.8V		–3	–1.6	0	µA
			●	–4		0	µA

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ELECTRICAL CHARACTERISTICS (V_S = 5V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{\overline{SHDN}H}$	$\overline{SHDN}$ Pin Current High	$V_{\overline{SHDN}}$ = 2V	 ●	–300 –350	35	300 350	nA nA
V_L	$\overline{SHDN}$ Pin Input Voltage Low		●			0.8	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		●	2			V
I_{OSD}	Output Leakage Current Magnitude in Shutdown	$V_{\overline{SHDN}}$ = 0.8V, Output Shorted to Either Supply			100		nA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.8V to 2V			5		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 2V to 0.8V			2		µs
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1k to Half Supply			120		MHz
GBW	Gain-Bandwidth Product	f = 2MHz, R_L = 1k to Half Supply	 ●	100 70	180		MHz MHz
t_S, 0.1%	Settling Time to 0.1%	A_V = –1, V_O = 2V Step R_L = 1k			74		ns
t_S, 0.01%	Settling Time to 0.01%	A_V = –1, V_O = 2V Step R_L = 1k			202		ns
SR	Slew Rate	A_V = –3.33, 4.6V Step (Note 11)	 ●	60 50	90		V/µs V/µs
FPBW	Full Power Bandwidth	V_{OUT} = $4V_{P-P}$ (Note 13)			4		MHz
HD2/HD3	Harmonic Distortion R_L = 1k to Half Supply	f_C = 100kHz, V_O = $2V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2MHz, V_O = $2V_{P-P}$			110/90 88/80 78/62		dBc dBc dBc
	R_L = 100Ω to Half Supply	f_C = 100kHz, V_O = $2V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2MHz, V_O = $2V_{P-P}$			90/79 66/60 59/51		
ΔG	Differential Gain (Note 14)	A_V = 1, R_L = 1k, V_S = ±2.5V			0.2		%
Δθ	Differential Phase (Note 14)	A_V = 1, R_L = 1k, V_S = ±2.5V			0.08		Deg
	Crosstalk	A_V = –1, R_L = 1k to Half Supply, V_{OUT} = $2V_{P-P}$, f = 1MHz			–90		dB

ELECTRICAL CHARACTERISTICS (V_S = 2.7V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 1.35V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply	 ●	–100 –300	500	1000 1400	µV µV
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–1.75 –2.25	0.75	3.25 3.75	mV mV
ΔV_{OS}	Input Offset Voltage Match (Channel-to-Channel) (Note 8)	V_{CM} = Half Supply	 ●	–700 –1000	–20	700 1000	µV µV
		V_{CM} = V^+ – 0.5V, NPN Mode	 ●	–3.5 –4	0.1	3.5 4	mV mV
V_{OS} T_C	Input Offset Voltage Drift		●		2		µV/°C

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ELECTRICAL CHARACTERISTICS (V_S = 2.7V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 1.35V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_B	Input Bias Current (Note 7)	V_{CM} = Half Supply		–450	–100	450	nA
			●	–600		600	nA
		V_{CM} = V^+ – 0.5V, NPN Mode		50	350	1000	nA
			●	0		1500	nA
I_{OS}	Input Offset Current	V_{CM} = Half Supply		–250	–10	250	nA
			●	–350		350	nA
		V_{CM} = V^+ – 0.5V, NPN Mode		–250	–10	250	nA
			●	–350		350	nA
e_n	Input Noise Voltage Density	f = 100kHz			4.6		$nV/\sqrt{Hz}$
	Input 1/f Noise Voltage	f = 0.1Hz to 10Hz			1.7		μV_{P-P}
i_n	Input Noise Current Density	f = 100kHz			1.8		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	Differential Mode			2		pF
		Common Mode			0.8		pF
R_{IN}	Input Resistance	Differential Mode			32		kΩ
		Common Mode			12		MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1k to Half Supply		15	25		V/mV
		(Note 12)	●	7.5			V/mV
		R_L = 100Ω to Half Supply		2	7.5		V/mV
		(Note 12)	●	1.3			V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 1.2V		80	100		dB
			●	78			dB
I_{CMR}	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.25V		69	73		dB
		V_{CM} = 1V	●	65			dB
	Supply Voltage Range (Note 6)		●	2.5		5.25	V
V_{OL}	Output Swing Low (V_{OUT} – V^-)	No Load			20	40	mV
			●			55	mV
		I_{SINK} = 5mA			80	125	mV
			●			160	mV
		I_{SINK} = 10mA			110	175	mV
			●			225	mV
V_{OH}	Output Swing High (V^+ – V_{OUT})	No Load			60	85	mV
			●			100	mV
		I_{SOURCE} = 5mA			135	190	mV
			●			225	mV
		I_{SOURCE} = 10mA			180	275	mV
			●			400	mV
I_{SC}	Short Circuit Current	Sourcing			–35	–20	mA
			●			–15	mA
		Sinking		25	50		mA
			●	20			mA
I_S	Supply Current per Amplifier	V_{CM} = Half Supply			0.89	1	mA
			●			1.3	mA
		V_{CM} = V^+ – 0.5V			1	1.3	mA
			●			1.7	mA

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ELECTRICAL CHARACTERISTICS (V_S = 2.7V)

The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at T_A = 25°C. For each amplifier V_S = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; V_{CM} = V_{OUT} = 1.35V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SD}	Disable Supply Current per Amplifier	$V_{\overline{SHDN}}$ = 0.8V			22	50	µA
			●			90	µA
$I_{\overline{SHDN}L}$	$\overline{SHDN}$ Pin Current Low	$V_{\overline{SHDN}}$ = 0.8V		–1	–0.5	0	µA
			●	–1.5		0	µA
$I_{\overline{SHDN}H}$	$\overline{SHDN}$ Pin Current High	$V_{\overline{SHDN}}$ = 2V		–300	45	300	nA
			●	–350		350	nA
V_L	$\overline{SHDN}$ Pin Input Voltage		●			0.8	V
V_H	$\overline{SHDN}$ Pin Input Voltage		●	2.0			V
I_{OSD}	Output Leakage Current Magnitude in Shutdown	$V_{\overline{SHDN}}$ = 0.8V, Output Shorted to Either Supply			100		nA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.8V to 2V			5		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 2V to 0.8V			2		µs
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1k to Half Supply			100		MHz
GBW	Gain-Bandwidth Product	f = 2MHz, R_L = 1k to Half Supply		80	150		MHz
			●	50			
t_S, 0.1	Settling Time to 0.1%	A_V = –1, V_O = 2V Step R_L = 1k			119		ns
t_S, 0.01	Settling Time to 0.01%	A_V = –1, V_O = 2V Step R_L = 1k			170		ns
SR	Slew Rate	A_V = –1, 2V Step			55		V/µs
FPBW	Full Power Bandwidth	V_{OUT} = $2V_{P-P}$ (Note 13)			3.3		MHz
	Crosstalk	A_V = –1, R_L = 1k to Half Supply, V_{OUT} = $2V_{P-P}$, f = 1MHz			–90		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If any of the input or shutdown pins goes 300mV beyond either supply or the differential input voltage exceeds 1.4V the input current should be limited to less than 10mA. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output current is high.

Note 4: The LTC6246C/LTC6247C/LTC6248C and LTC6246I/LTC6247I/LTC6248I are guaranteed functional over the temperature range of –40°C to 85°C. The LTC6246H/LTC6247H/LTC6248H are guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LTC6246C/LTC6247C/LTC6248C are guaranteed to meet specified performance from 0°C to 70°C. The LTC6246C/LTC6247C/LTC6248C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6246I/LTC6247I/LTC6248I are guaranteed to meet specified performance from –40°C to 85°C. The LTC6246H/LTC6247H/LTC6248H are guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: The input bias current is the average of the average of the currents through the positive and negative input pins.

Note 8: Matching parameters are the difference between amplifiers A and D and between B and C on the LTC6248; between the two amplifiers on the LTC6247.

Note 9: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are with short traces connected to the leads with minimal metal area.

Note 10: The output voltage is varied from 0.5V to 4.5V during measurement.

Note 11: Middle 80% of the output waveform is observed. R_L = 1k at half supply.

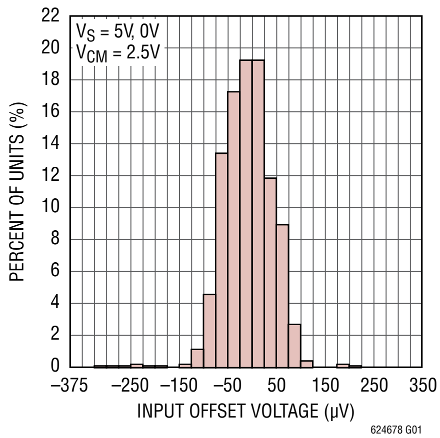
Note 12: The output voltage is varied from 0.5V to 2.2V during measurement.

Note 13: FPBW is determined from distortion performance in a gain of +2 configuration with HD2, HD3 < –40dBc as the criteria for a valid output.

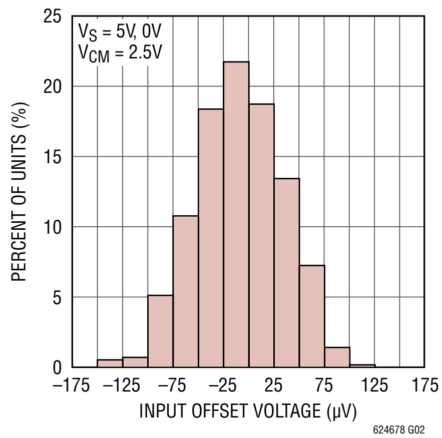
Note 14: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set.

TYPICAL PERFORMANCE CHARACTERISTICS

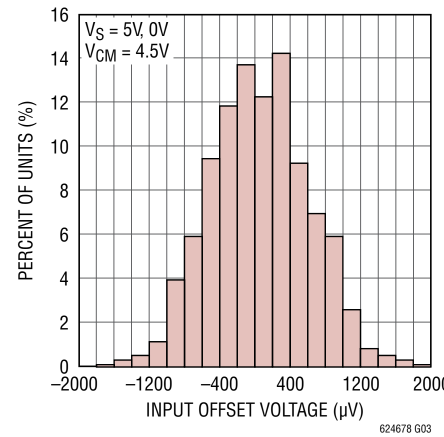
V_{OS} Distribution, V_{CM} = V_S/2 (MS, PNP Stage)



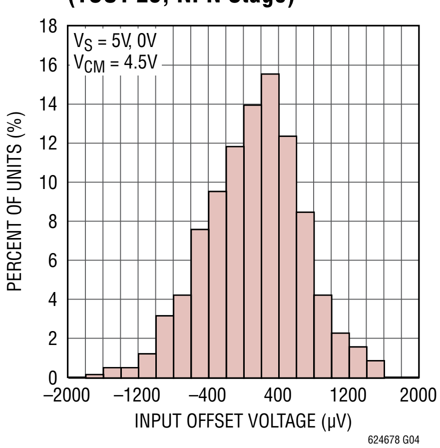
V_{OS} Distribution, V_{CM} = V_S/2 (TSOT-23, PNP Stage)



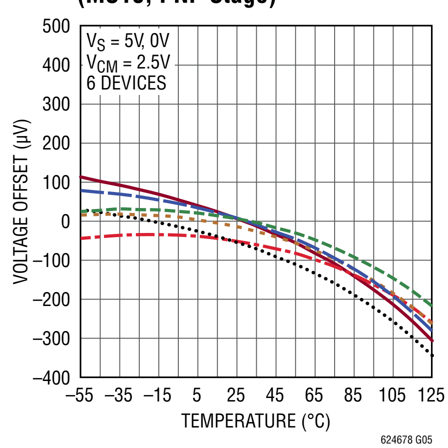
V_{OS} Distribution, V_{CM} = V^+ – 0.5V (MS, NPN Stage)



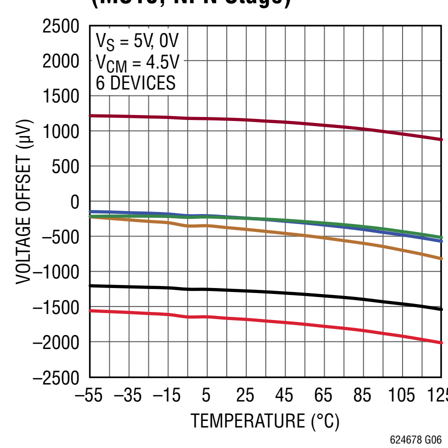
V_{OS} Distribution, V_{CM} = V^+ – 0.5V (TSOT-23, NPN Stage)



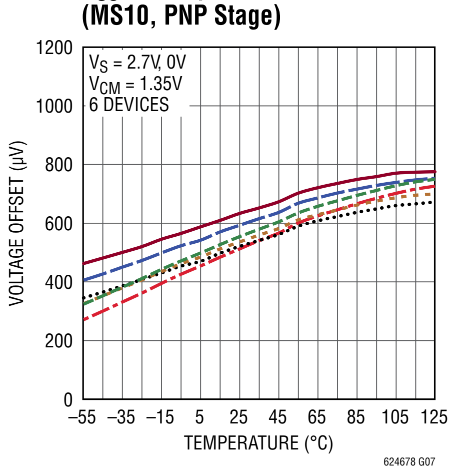
V_{OS} vs Temperature (MS10, PNP Stage)



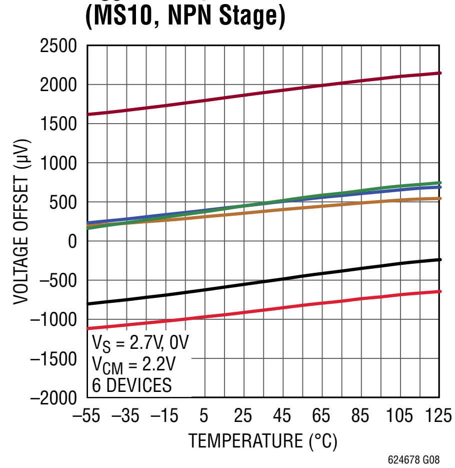
V_{OS} vs Temperature (MS10, NPN Stage)



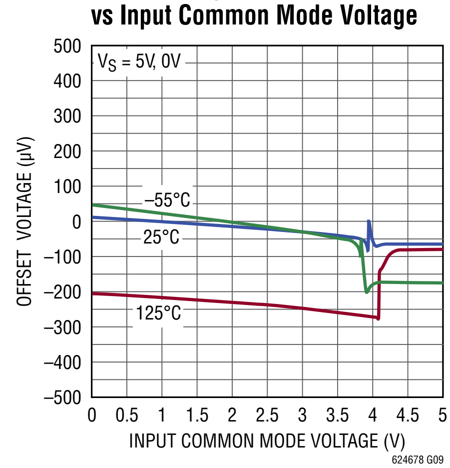
V_{OS} vs Temperature (MS10, PNP Stage)



V_{OS} vs Temperature (MS10, NPN Stage)



Offset Voltage vs Input Common Mode Voltage



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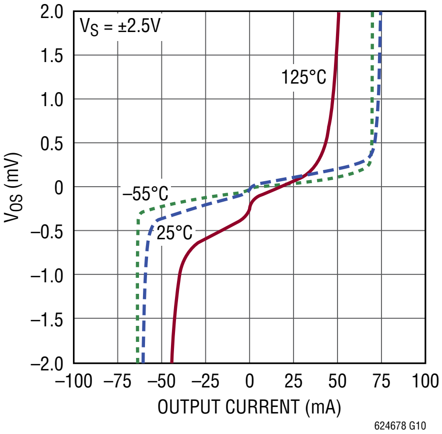
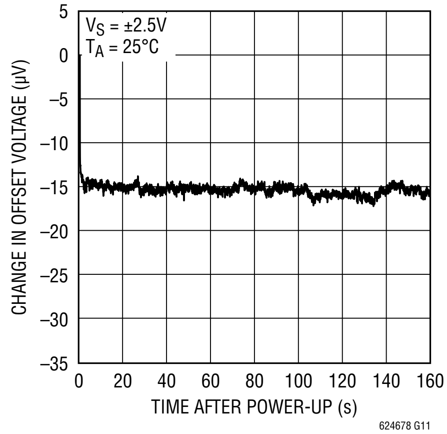
TYPICAL PERFORMANCE CHARACTERISTICS

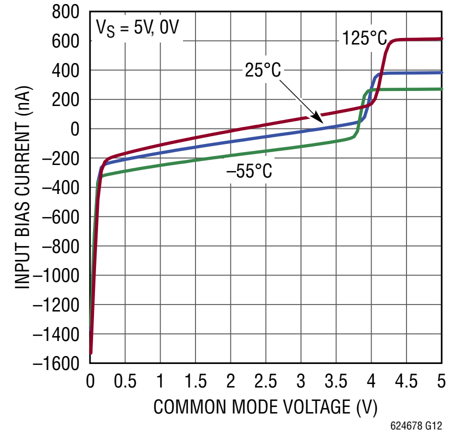
Offset Voltage vs Output Current



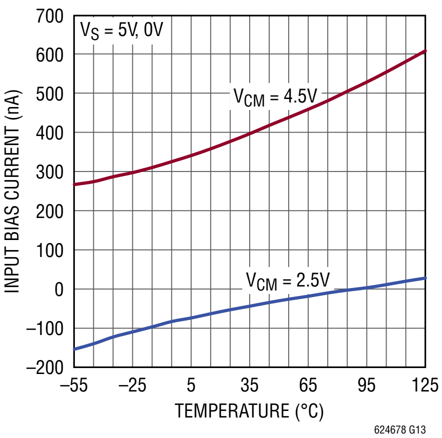
Warm-Up Drift vs Time



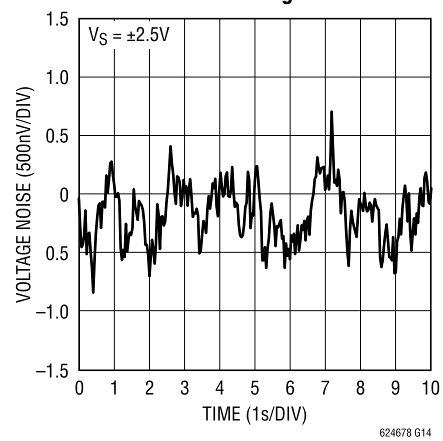
Input Bias Current vs Common Mode Voltage



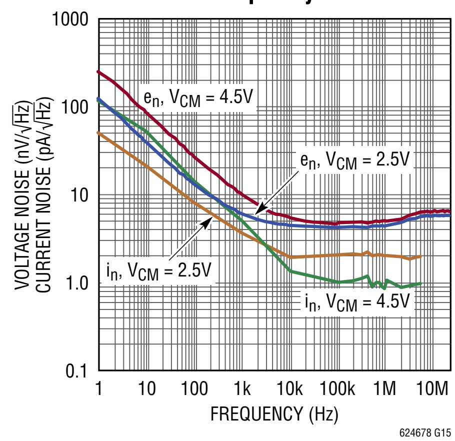
Input Bias Current vs Temperature



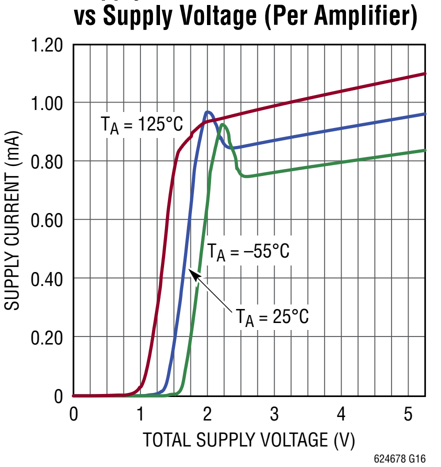
0.1Hz to 10Hz Voltage Noise



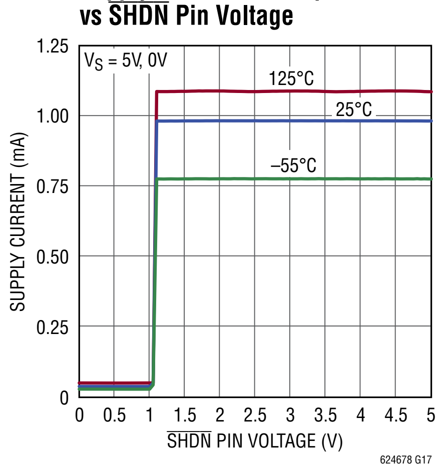
Input Noise Voltage and Noise Current vs Frequency



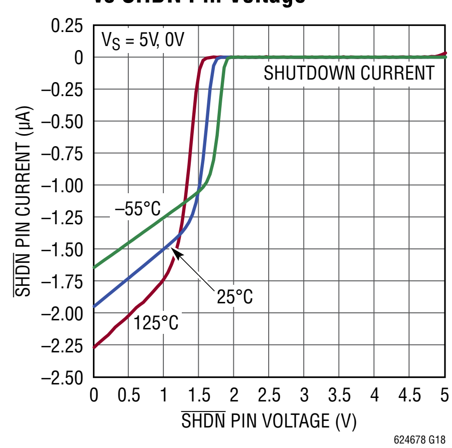
Supply Current vs Supply Voltage (Per Amplifier)



Supply Current Per Amplifier vs SHDN Pin Voltage



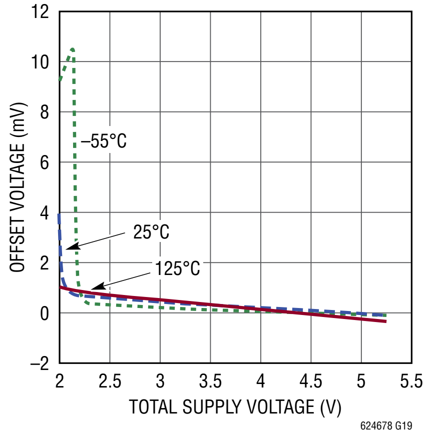
SHDN Pin Current vs SHDN Pin Voltage



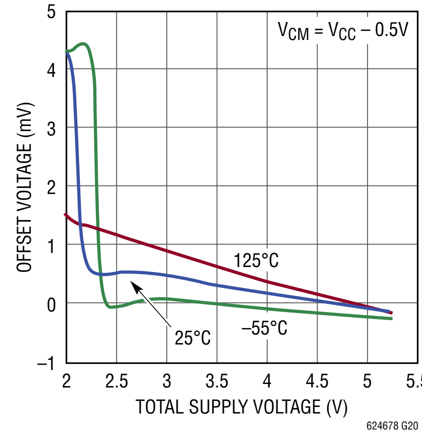
Rev C

TYPICAL PERFORMANCE CHARACTERISTICS

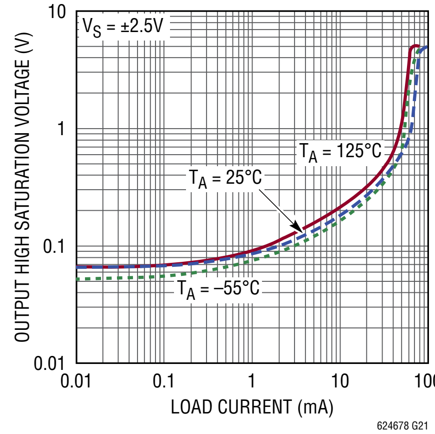
Minimum Supply Voltage, $V_{CM} = V_S/2$ (PNP Operation)



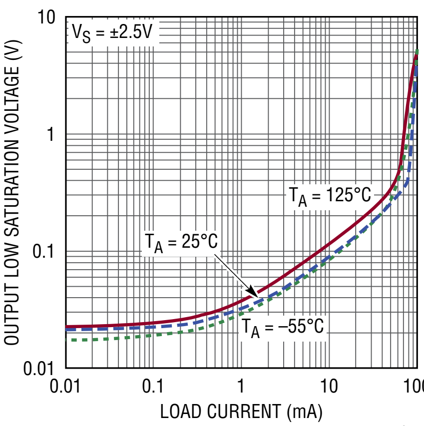
Minimum Supply Voltage, $V_{CM} = V^+ – 0.5V$ (NPN Operation)



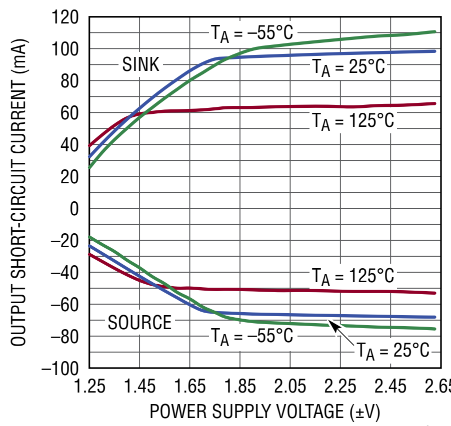
Output Saturation Voltage vs Load Current (Output High)



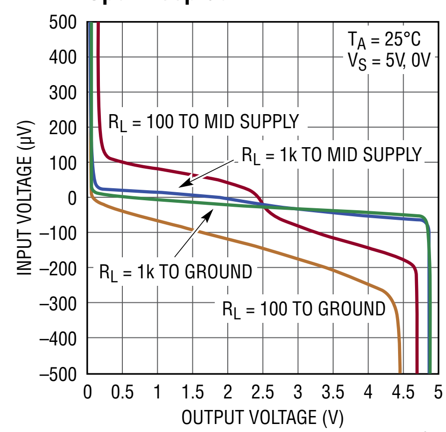
Output Saturation Voltage vs Load Current (Output Low)



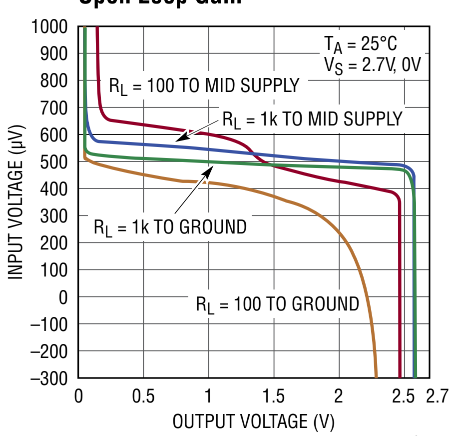
Output Short-Circuit Current vs Power Supply Voltage



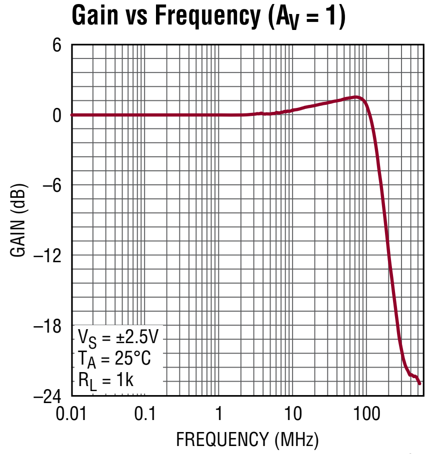
Open Loop Gain



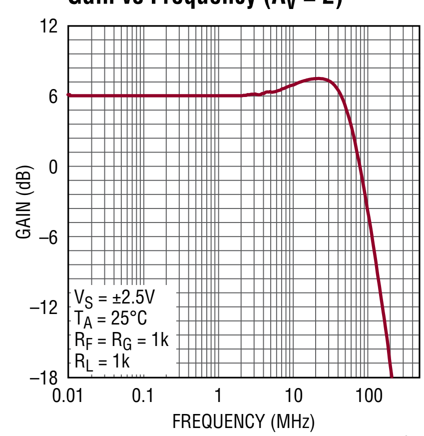
Open Loop Gain



Gain vs Frequency ($A_V = 1$)



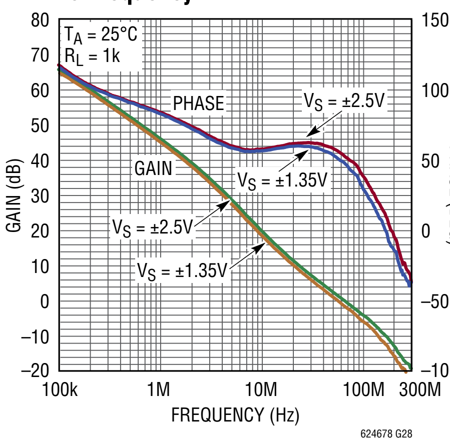
Gain vs Frequency ($A_V = 2$)



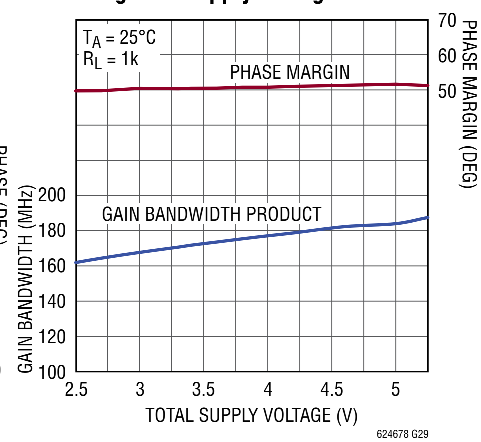
Rev C

TYPICAL PERFORMANCE CHARACTERISTICS

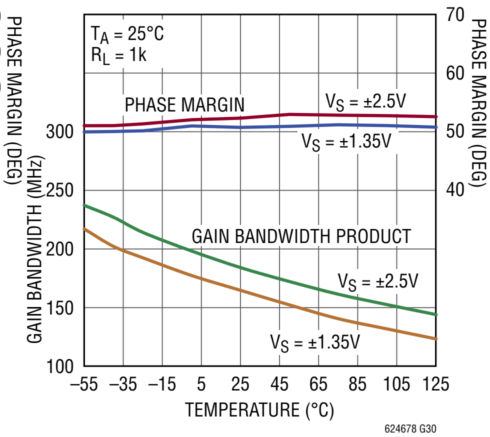
Open Loop Gain and Phase vs Frequency



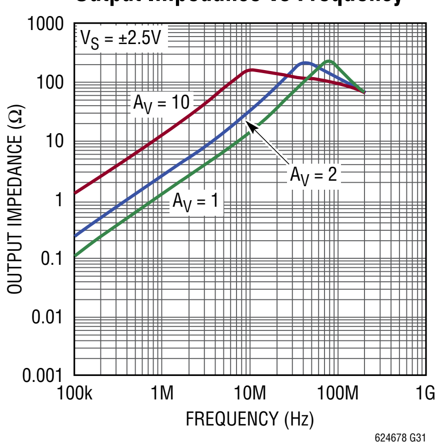
Gain Bandwidth and Phase Margin vs Supply Voltage



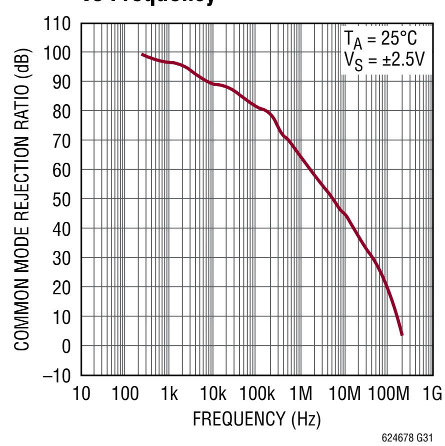
Gain Bandwidth and Phase Margin vs Temperature



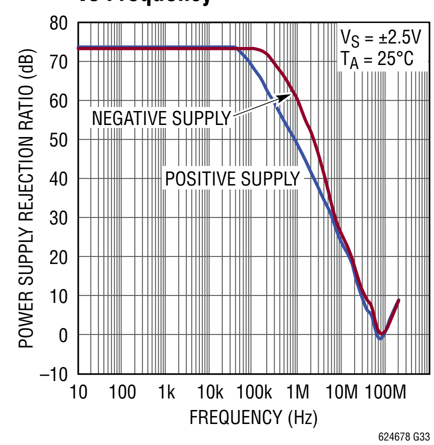
Output Impedance vs Frequency



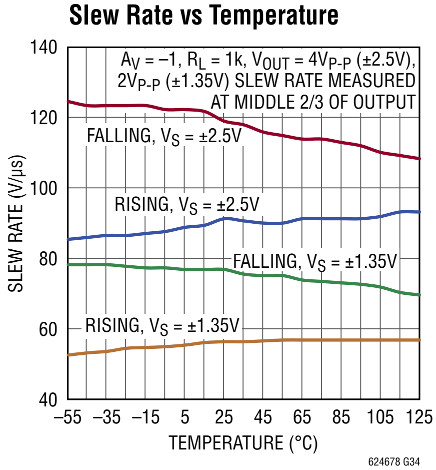
Common Mode Rejection Ratio vs Frequency



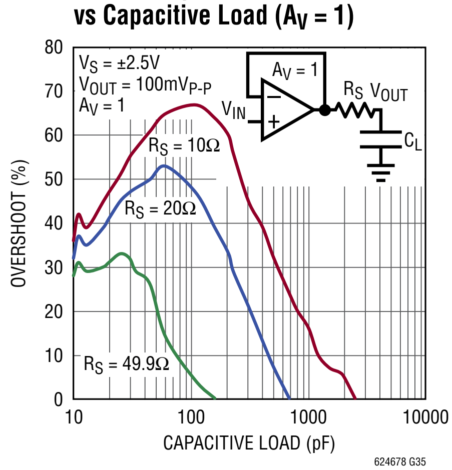
Power Supply Rejection Ratio vs Frequency



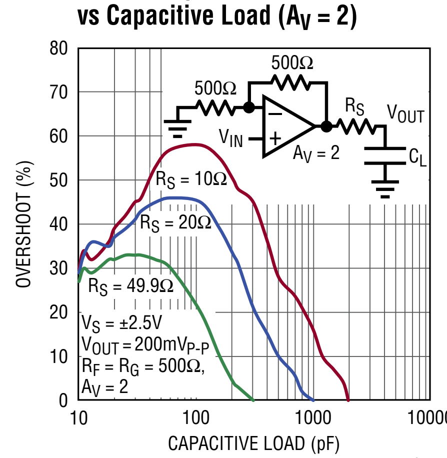
Slew Rate vs Temperature



Series Output Resistor vs Capacitive Load (A_V = 1)

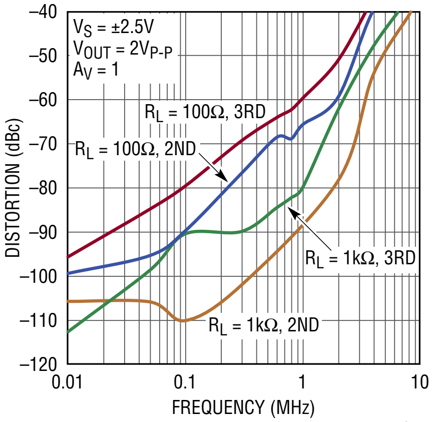


Series Output Resistor vs Capacitive Load (A_V = 2)

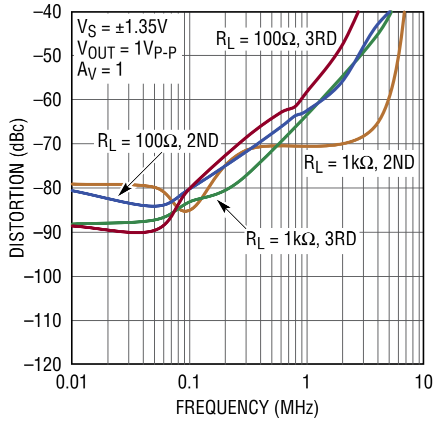


TYPICAL PERFORMANCE CHARACTERISTICS

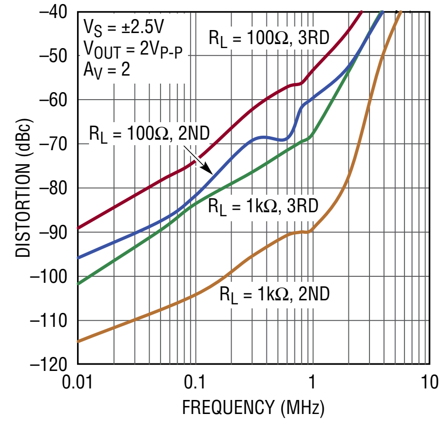
Distortion vs Frequency (A_V = 1, 5V)



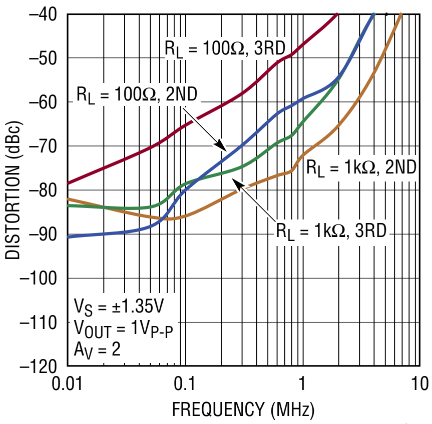
Distortion vs Frequency (A_V = 1, 2.7V)



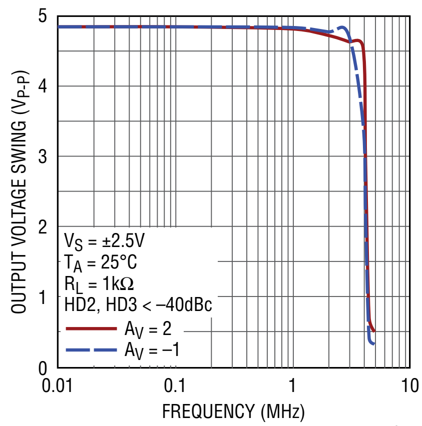
Distortion vs Frequency (A_V = 2, 5V)



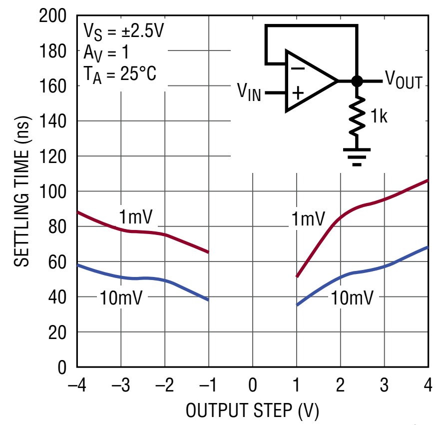
Distortion vs Frequency A_V = 2, 2.7V)



Maximum Undistorted Output Signal vs Frequency

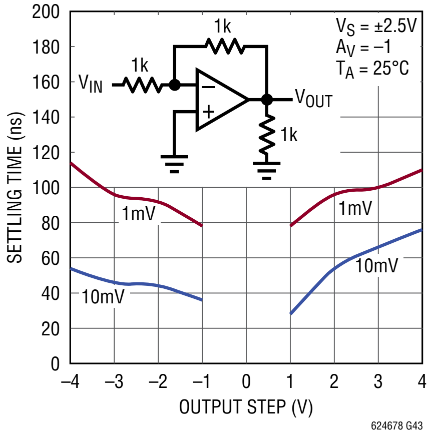


Settling Time vs Output Step (Noninverting)

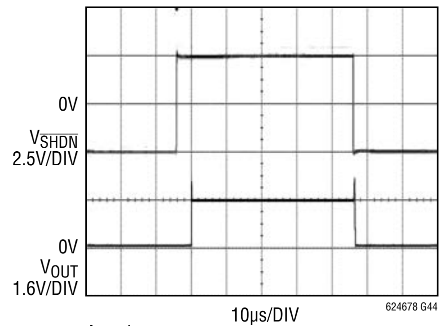


TYPICAL PERFORMANCE CHARACTERISTICS

Settling Time vs Output Step (Inverting)

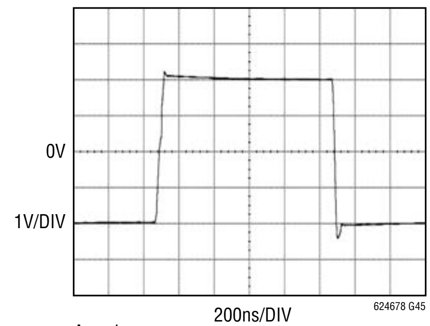


$\overline{SHDN}$ Pin Response Time



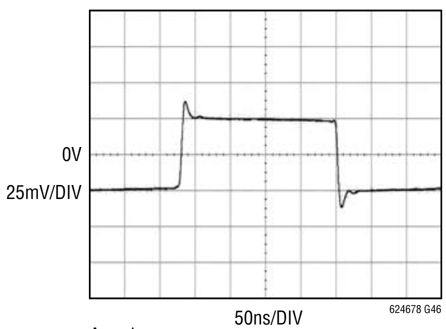
A_V = 1
V_S = ±2.5V
R_L = 1k
V_{IN} = 1.6V

Large Signal Response



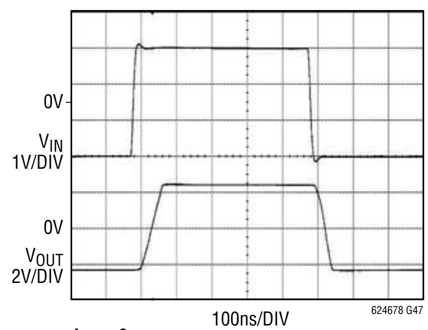
A_V = 1
V_S = ±2.5V
R_L = 1k

Small Signal Response



A_V = 1
V_S = ±2.5V
R_L = 1k

Output Overdriven Recovery



A_V = ±2
V_S = ±2.5V
R_L = 1k
V_{IN} = $3V_{P-P}$

PIN FUNCTIONS

–IN: Inverting Input of Amplifier. Valid input range from V^- to V^+.

+IN: Non-Inverting Input of Amplifier. Valid input range from V^- to V^+.

V⁺ : Positive Supply Voltage. Allowed applied voltage ranges from 2.5V to 5.25V when $V^- = 0V$.

V⁻ : Negative Supply Voltage. Typically 0V. This can be made a negative voltage as long as $2.5V \le (V^+ – V^-) \le 5.25V$.

$\overline{\text{SHDN}}$: Active Low Shutdown. Threshold is typically 1.1V referenced to V^-. Floating this pin will turn the part on.

OUT: Amplifier Output. Swings rail-to-rail and can typically source/sink over 50mA of current at a total supply of 5V.

APPLICATIONS INFORMATION

Circuit Description

The LTC6246/LTC6247/LTC6248 have an input and output signal range that extends from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage, Q1/Q2, and an NPN stage, Q3/Q4 that are active over different common mode input voltages. The PNP stage is active between the negative supply to nominally 1.2V below the positive supply. As the input voltage approaches the positive supply, the transistor Q5 will steer the tail current, I_1, to the current mirror, Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the remaining input common mode range. Also, at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1/Q2 are active, the current in Q16 is controlled to be the same as the current in Q1 and Q2. Thus, the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17 to Q19 to cancel the base current of the input devices Q1/Q2. A pair of complementary common emitter stages, Q14/Q15, enable the output to swing from rail-to-rail.

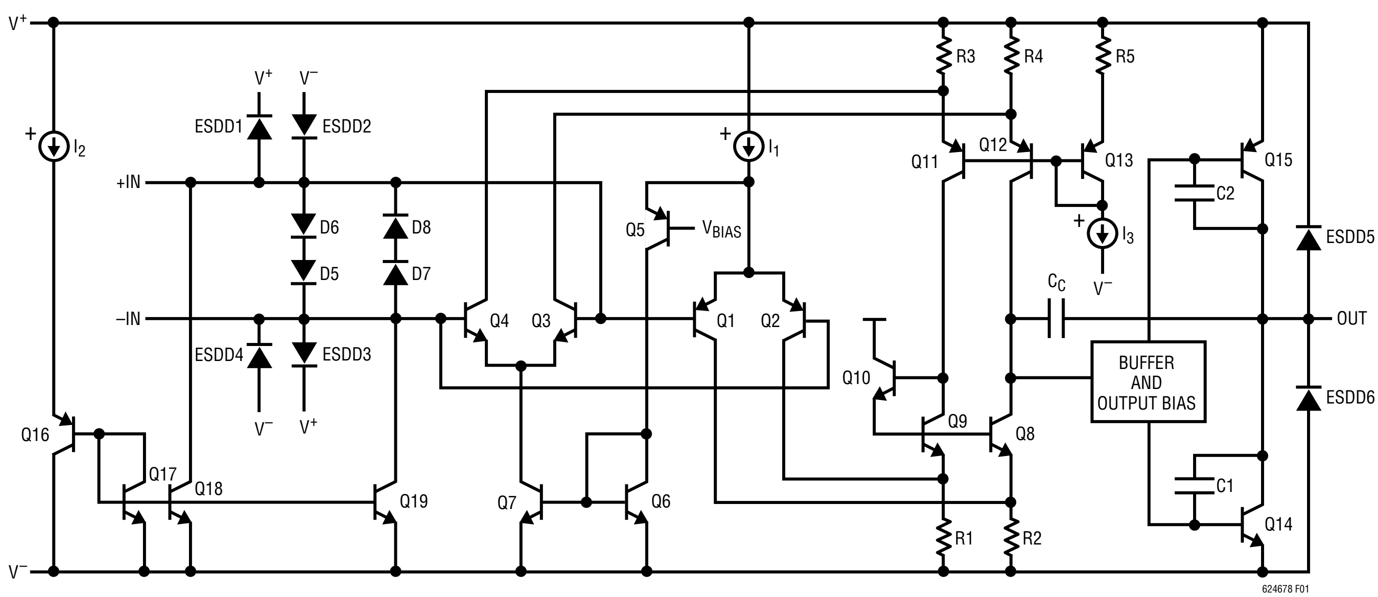


Figure 1. LTC6246/LTC6247/LTC6248 Simplified Schematic Diagram

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APPLICATIONS INFORMATION

Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to approximately 1.2V below the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail with the PNP stage inactive. The offset voltage magnitude for the PNP input stage is trimmed to less than 500µV with 5V total supply at room temperature, and is typically less than 150µV. The offset voltage for the NPN input stage is typically less than 1.7mV with 5V total supply at room temperature.

Input Bias Current

The LTC6246 family uses a bias current cancellation circuit to compensate for the base current of the PNP input pair. When the input common mode voltage is less than 200mV, the bias cancellation circuit is no longer effective and the input bias current magnitude can reach a value above 1µA. For common mode voltages ranging from 0.2V above the negative supply to 1.2V below the positive supply, the low input bias current of the LTC6246 family allows the amplifiers to be used in applications with high source resistances where errors due to voltage drops must be minimized.

Output

The LTC6246 family has excellent output drive capability. The amplifiers can typically deliver over 50mA of output drive current at a total supply of 5V. The maximum output current is a function of the total supply voltage. As the supply voltage to the amplifier decreases, the output current capability also decreases. Attention must be paid to keep the junction temperature of the IC below 150°C (refer to the Power Dissipation section) when the output is in continuous short circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, extremely high current will flow through these diodes which can result in damage to the device. Forcing the output to even 1V beyond either supply could result in several hundred milliamps of current through either diode.

Input Protection

The input stages are protected against a large differential input voltage of 1.4V or higher by 2 pairs of back-to-back diodes to prevent the emitter-base breakdown of the input transistors. In addition, the input and shutdown pins have reverse biased diodes connected to the supplies. The current in these diodes must be limited to less than 10mA. The amplifiers should not be used as comparators or in other open loop applications.

ESD

The LTC6246 family has reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1.

There is an additional clamp between the positive and negative supplies that further protects the device during ESD strikes. Hot plugging of the device into a powered socket must be avoided since this can trigger the clamp resulting in larger currents flowing between the supply pins.

Capacitive Loads

The LTC6246/LTC6247/LTC6248 are optimized for high bandwidth and low power applications. Consequently they have not been designed to directly drive large capacitive loads. Increased capacitance at the output creates an additional pole in the open loop frequency response, worsening the phase margin. When driving capacitive loads, a resistor of 10Ω to 100Ω should be connected between the amplifier output and the capacitive load to avoid ringing or oscillation. The feedback should be taken directly from the amplifier output. Higher voltage gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin. The graphs titled Series Output Resistor vs Capacitive Load demonstrate the transient response of the amplifier when driving capacitive loads with various series resistors.

APPLICATIONS INFORMATION

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example if the amplifier is set up in a gain of +2 configuration with gain and feedback resistors of 5k, a parasitic capacitance of 5pF (device + PC board) at the amplifier's inverting input will cause the part to oscillate, due to a pole formed at 12.7MHz. An additional capacitor of 5pF across the feedback resistor as shown in Figure 2 will eliminate any ringing or oscillation. In general, if the resistive feedback network results in a pole whose frequency lies within the closed loop bandwidth of the amplifier, a capacitor can be added in parallel with the feedback resistor to introduce a zero whose frequency is close to the frequency of the pole, improving stability.

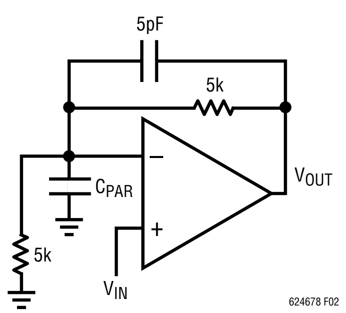


Figure 2. 5pF Feedback Cancels Parasitic Pole

Shutdown

The LTC6246 and LTC6247MS have $\overline{SHDN}$ pins that can shut down the amplifier to 42µA typical supply current. The $\overline{SHDN}$ pin needs to be taken below 0.8V above the negative supply for the amplifier to shut down. When left floating, the $\overline{SHDN}$ pin is internally pulled up to the positive supply and the amplifier remains on.

Power Dissipation

The LTC6246 and LTC6247 contain one and two amplifiers respectively. Hence the maximum on-chip power dissipation for them will be less than the maximum on-chip power dissipation for the LTC6248, which contains four amplifiers.

The LTC6248 is housed in a small 16-lead MS package and typically has a thermal resistance (θ_{JA}) of 125°C/W. It is necessary to ensure that the die's junction temperature does not exceed 150°C. The junction temperature, T_J, is calculated from the ambient temperature, T_A, power dissipation, PD, and thermal resistance, θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is a function of the supply voltage, output voltage and load resistance. For a given supply voltage with output connected to ground or supply, the worst-case power dissipation $P_{D(MAX)}$ occurs when the supply current is maximum and the output voltage at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is approximately (since I_S actually changes with output load current) given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + \left(\frac{V_S}{2}\right)^2 / R_L$$

Example: For an LTC6248 in a 16-lead MS package operating on ±2.5V supplies and driving a 100Ω load to ground, the worst-case power dissipation is approximately given by

$$P_{D(MAX)}/Amp = (5 \bullet 1.3mA) + (1.25)^2/100 = 22mW$$

If all four amplifiers are loaded simultaneously then the total power dissipation is 88mW.

At the Absolute Maximum ambient operating temperature, the junction temperature under these conditions will be:

$$T_J = T_A + P_D \bullet 125°C/W$$
$$= 125 + (0.088W \bullet 125°C/W) = 136°C$$

which is less than the absolute maximum junction temperature for the LTC6248 (150°C).

Refer to the Pin Configuration section for thermal resistances of various packages.

Rev C

TYPICAL APPLICATIONS

12-Bit ADC Driver

Figure 3 shows the LTC6246 driving an LTC2366 12-bit A/D converter. The low wideband noise of the LTC6246 maintains a 70dB SNR even without the use of an intermediate antialiasing RC filter. On a single 3.3V supply with a 2.5V reference, a full –1dBFS output can be obtained without the amplifier transitioning between input regions, thus minimizing crossover distortion. Figure 4 shows an FFT obtained with a sampling rate of 2.2Msps and a 350kHz input waveform. Spurious free dynamic range is a quite handsome 82dB.

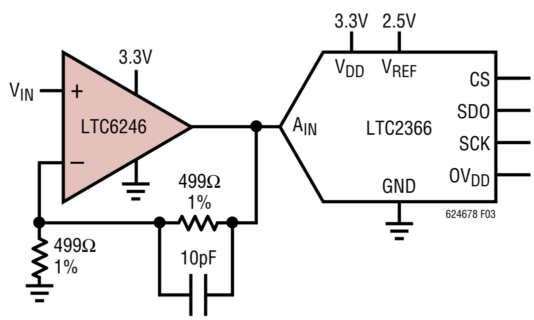


Figure 3. Single Supply 12-Bit ADC Driver

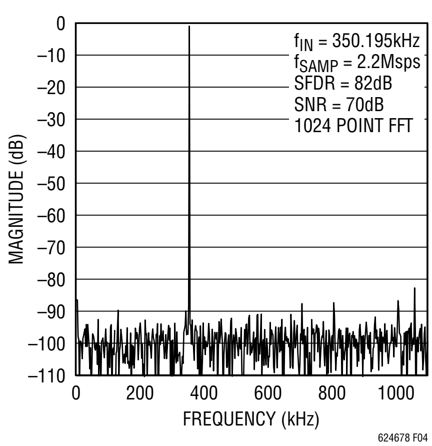


Figure 4. 350kHz FFT Showing 82dB SFDR

Low Noise Low Power DC-Accurate Single Supply Photodiode Amplifier

Figure 5 shows the LTC6246 applied as a low power high performance transimpedance amplifier for a photodiode. A low noise JFET Q1 acts as a current buffer, with R2 and R3 imposing a low frequency gain of approximately 1. Transimpedance gain is set by feedback resistor R1 to 1MΩ. R4 and R5 set the LTC6246 inputs at 1V below the 3V rail, with C3 reducing their noise contribution. By feedback this 1V also appears across R2, setting the JFET quiescent current at 1mA completely independent of its pinchoff voltage and I_{DSS} characteristics. It does this by placing the JFETs 1mA V_{GS} at the gate referenced to the source, which is sitting 1V above ground. For this JFET, that will typically be about 500mV, and this voltage is imposed as a reverse voltage on the photodiode PD1. At zero I_{PD} photocurrent, the output sits at the same voltage and rises as photocurrent increases. As mentioned before, R2 and R3 set the JFET gain to 1 at low frequency.

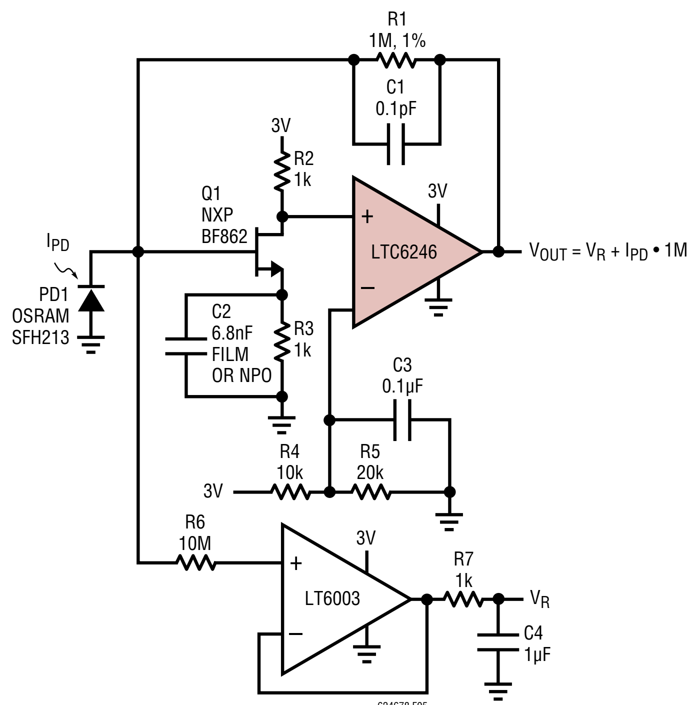


Figure 5. Low Noise Low Power DC Accurate Single Supply Photodiode Amplifier

Rev C

TYPICAL APPLICATIONS

This is not the lowest noise configuration for a transistor, as downstream noise sources appear at the input completely unattenuated. At low frequency, this is not a concern for a transimpedance amplifier because the noise gain is 1 and the output noise is dominated by the $130nV/\sqrt{Hz}$ of the 1MΩ R1. However, at increasing frequencies the capacitance of the photodiode comes into play and the circuit noise gain rises as the 1MΩ feedback looks back into lower and lower impedance. But capacitor C2 comes to the rescue. In addition to the obvious quenching of noise source R3, capacitor C2 increases the JFET gain to about 30 at high frequency effectively attenuating the downstream noise contributions of R2 and the op amp input noise. Thus the circuit achieves low input voltage noise at high frequency where it is most needed. Amplifier LT6003 is used to buffer the output voltage of the photodiode and R7 and C4 are used to filter out the voltage noise of the LT6003. Bandwidth to 700kHz was achieved with this circuit, with integrated output noise being $160\mu V_{RMS}$ up to 1MHz. Total supply current was a very low 2.2mA.

60dB 5.5MHz Gain Block

Figure 6 shows the LTC6247 configured as a low power high gain high bandwidth block. Two amplifiers each configured with a gain of 31V/V, are cascaded in series. A 660nF capacitor is used to limit the DC gain of the block to around 30dB to minimize output offset voltage. Figure 7 shows the frequency response of the block. Mid-band voltage gain is approximately 60dB with a –3dB frequency of 5.5MHz, thus resulting in a gain-bandwidth product of 5.5GHz with only 1.9mA of quiescent supply current.

Single 2.7V Supply 4MHz 4th Order Butterworth Filter

Benefitting from low voltage operation and rail-to-rail output, a low power filter that is suitable for antialiasing can be built as shown in Figure 8. On a 2.7V supply the filter has a passband of approximately 4MHz with $2V_{P-P}$ input signal and a stopband attenuation that is greater than –75dB at 43MHz as shown in Figure 9. The resistor and capacitor values can be scaled to reduce noise at the cost of large signal power consumption and distortion.

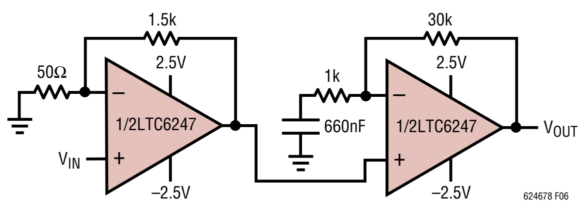


Figure 6. 60dB 5.5MHz Gain Block

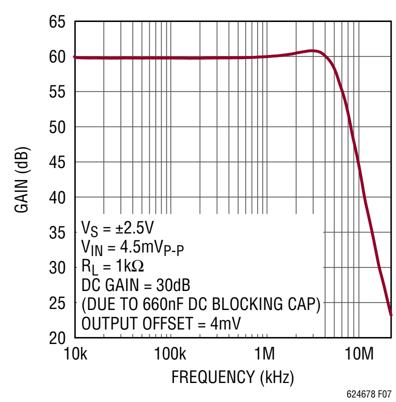


Figure 7

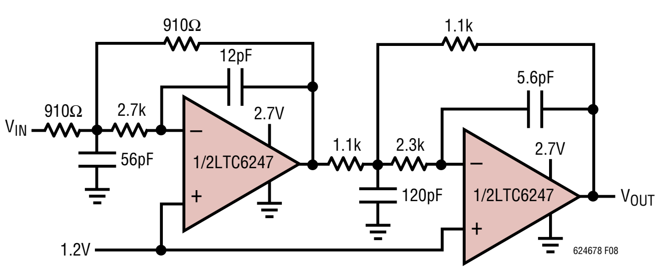


Figure 8. Single 2.7V Supply 4MHz 4th Order Butterworth Filter

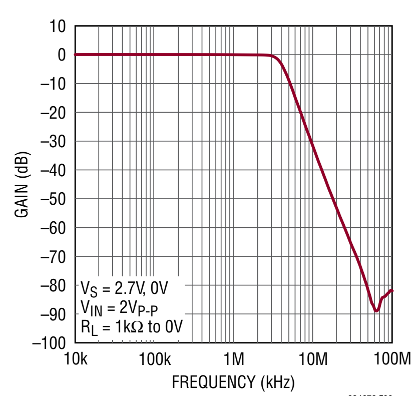


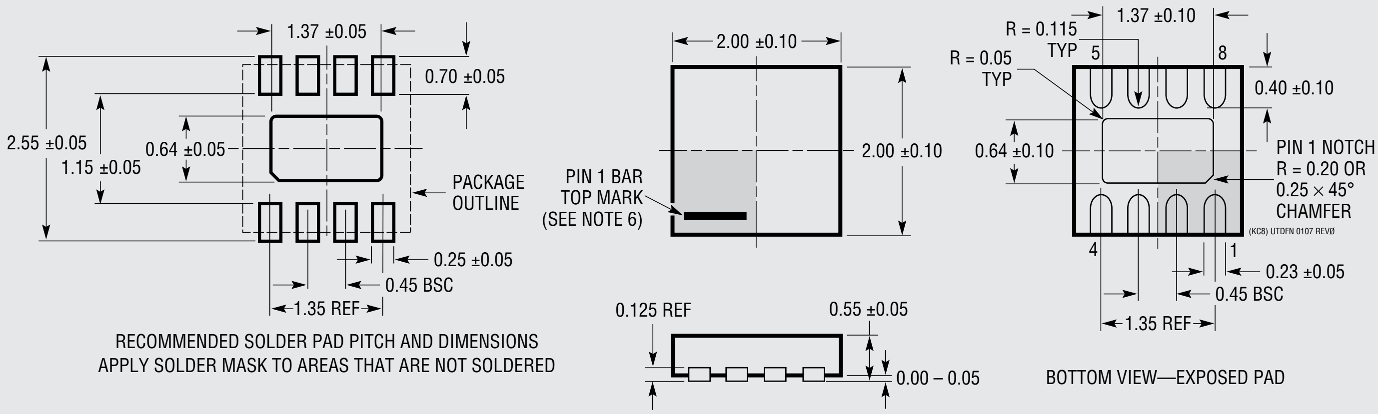
Figure 9

Rev C

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6246#packaging for the most recent package drawings.

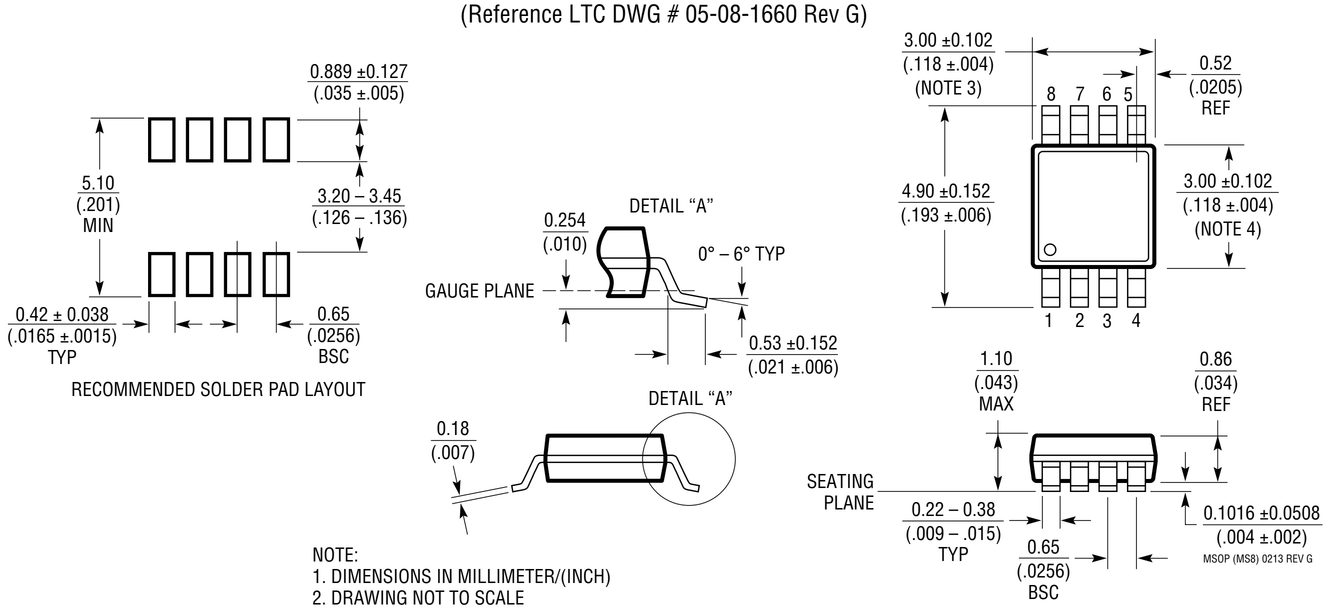
KC Package
8-Lead Plastic UTDFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1749 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

OBSOLETE PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



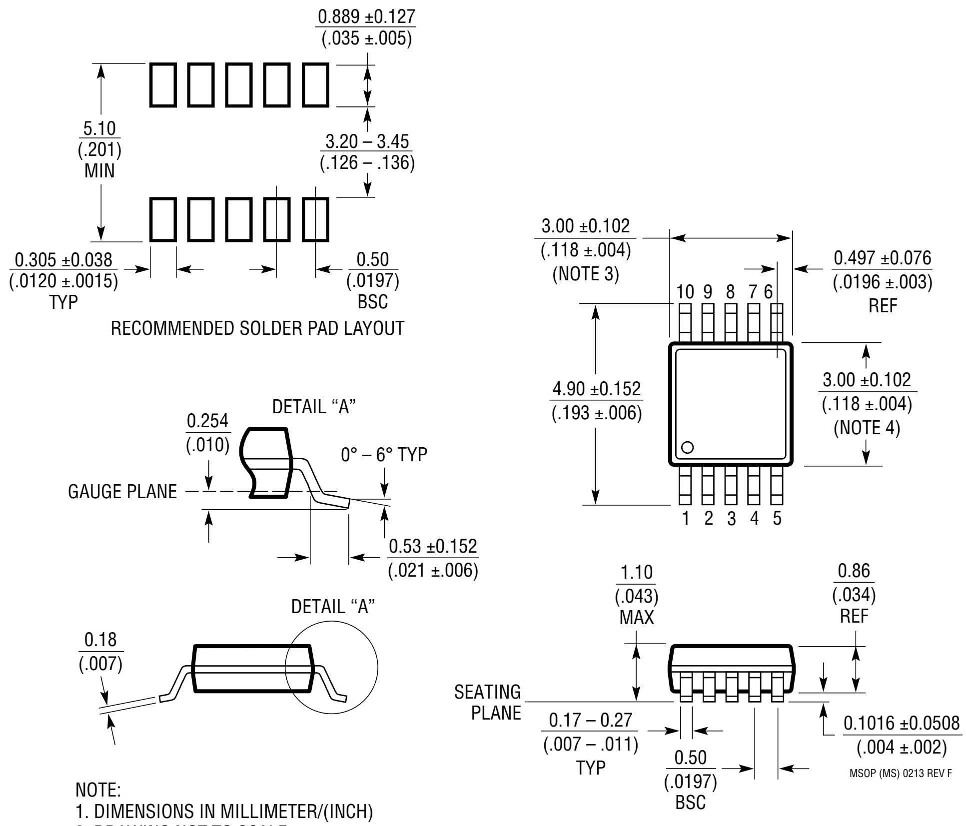
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Rev C

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6246#packaging for the most recent package drawings.

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)

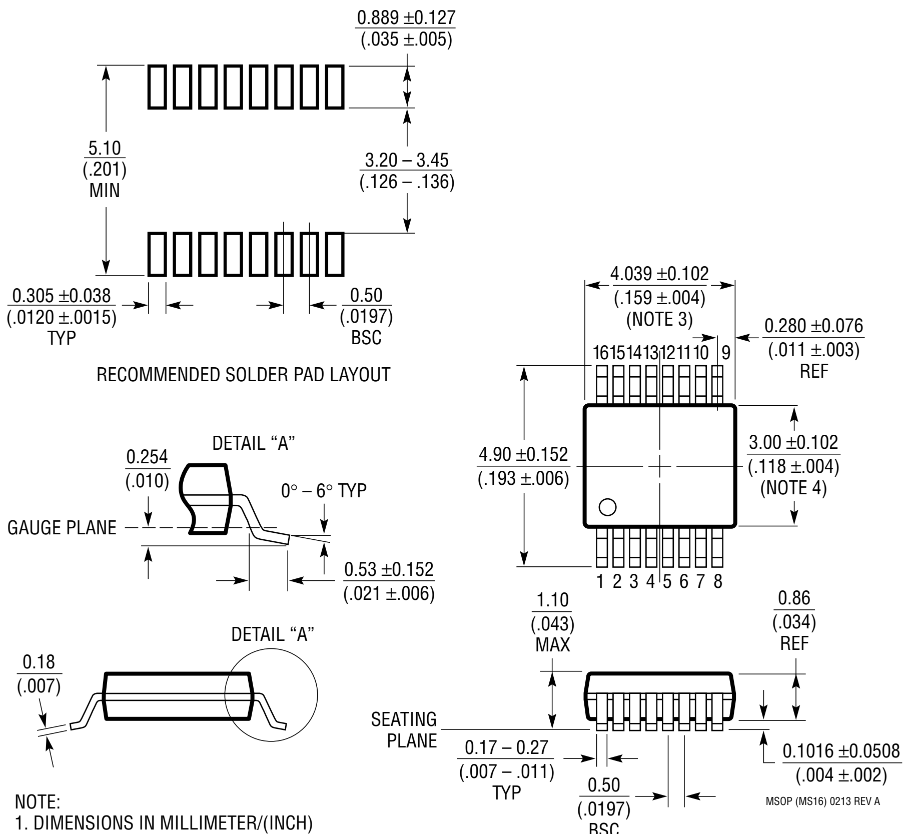


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6246#packaging for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)

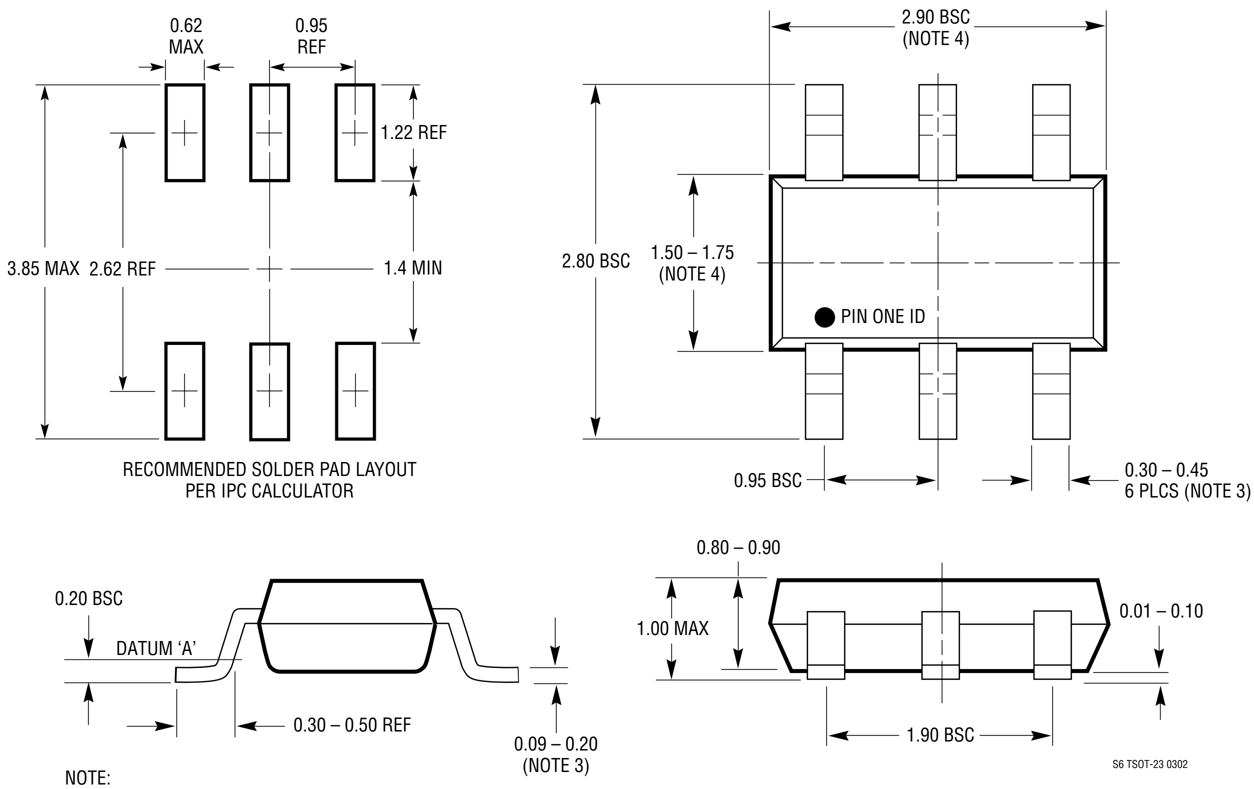


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6246#packaging for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

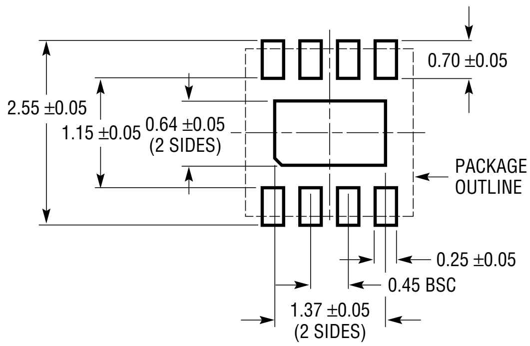


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

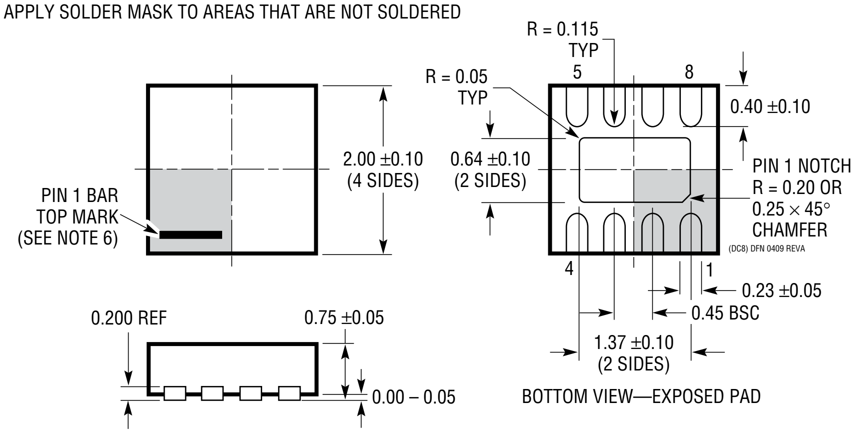
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6246#packaging for the most recent package drawings.

DC8 Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

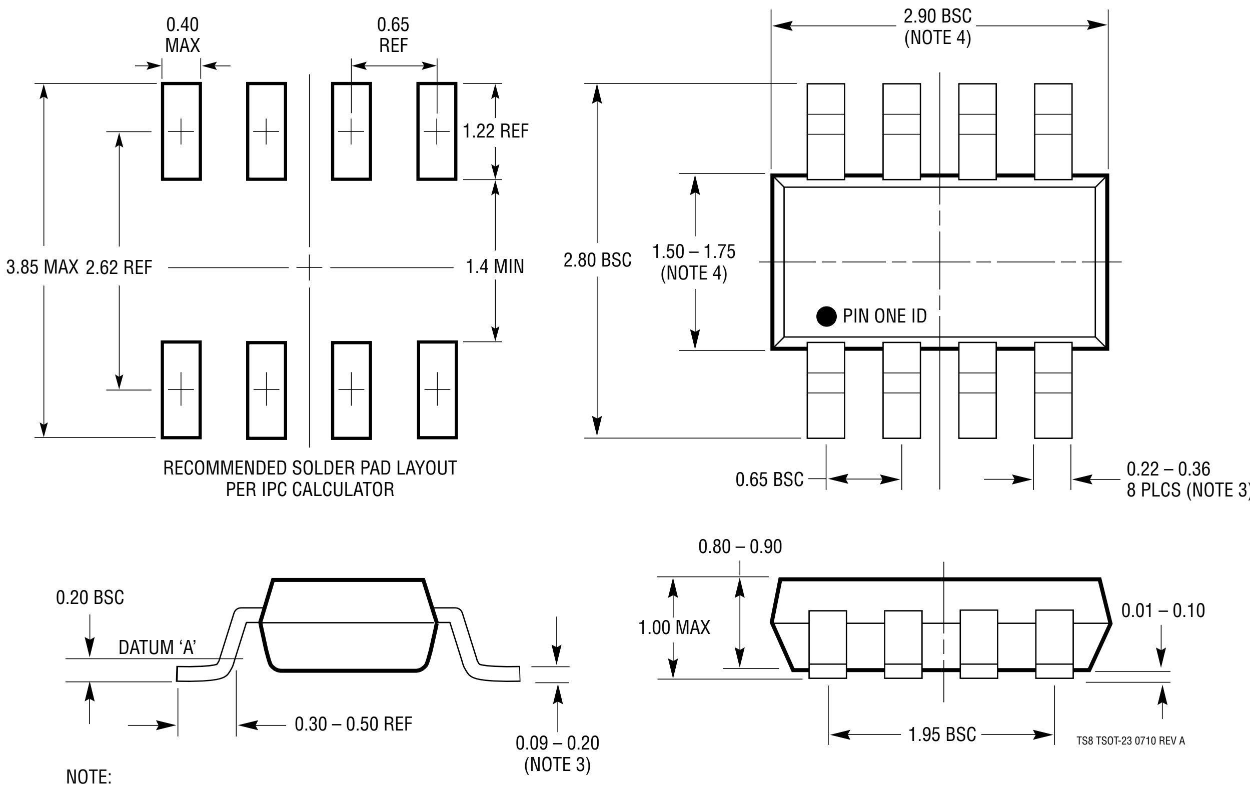


NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6246#packaging for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



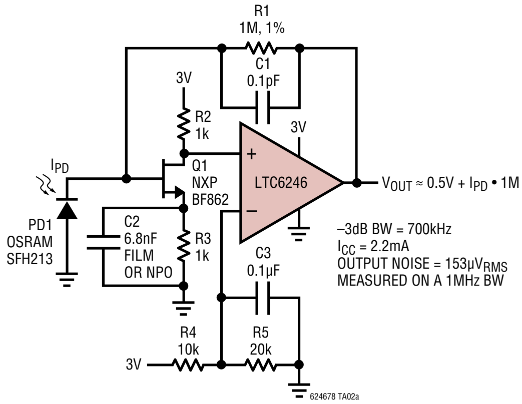
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

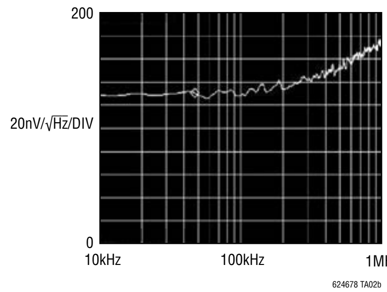
REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/10	Changes to Graph G15.	9
B	7/15	Added 2mm × 2mm × 0.8mm DFN package.	2, 3, 23
C	5/18	Obsoleted KC package option	2, 3, 19 to 24

TYPICAL APPLICATION

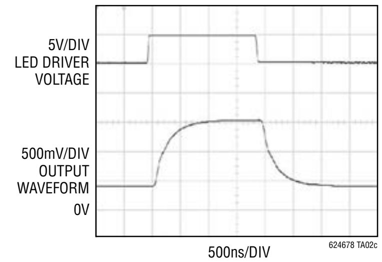
700kHz, 1MΩ Single Supply Photodiode Amplifier



Output Noise Spectrum



Transient Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Operational Amplifiers		
LT1818/LT1819	Single/Dual Wide Bandwidth, High Slew Rate Low Noise and Distortion Op Amps	400MHz, 9mA, 6nV/√Hz, 2500V/µs, 1.5mV –85dBc at 5MHz
LT1806/LT1807	Single/Dual Low Noise Rail-to-Rail Input and Output Op Amps	325MHz, 13mA, 3.5nV/√Hz, 140V/µs, 550µV, 85mA Output Drive
LT6230/LT6231/ LT6232	Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps	215MHz, 3.5mA, 1.1nV/√Hz, 70V/µs, 350µV
LT6200/LT6201	Single/Dual Ultralow Noise Rail-to-Rail Input/Output Op Amps	165MHz, 20mA, 0.95nV/√Hz, 44V/µs, 1mV
LT6202/LT6203/ LT6204	Single/Dual/Quad Ultralow Noise Rail-to-Rail Op Amp	100MHz, 3mA, 1.9nV/√Hz, 25V/µs, 0.5mV
LT1468	16-Bit Accurate Precision High Speed Op Amp	90MHz, 3.9mA, 5nV/√Hz, 22V/µs, 175µV, –96.5dB THD at $10V_{P-P}$, 100kHz
LT1803/LT1804/ LT1805	Single/Dual/Quad Low Power High Speed Rail-to-Rail Input and Output Op Amps	85MHz, 3mA, 21nV√Hz, 100V/µs, 2mV
LT1801/LT1802	Dual/Quad Low Power High Speed Rail-to-Rail Input and Output Op Amps	80MHz, 2mA, 8.5nV√Hz, 25V/µs, 350µV
LT6552	Single Supply Rail-to-Rail Output Video Difference Amplifier	75MHz (–3dB), 13.5mA, 55.5nV/√Hz, 350V/µs, 20mV
LT1028	Ultralow Noise, Precision High Speed Op Amps	75MHz, 9.5mA, 0.85nV/√Hz, 11V/µs, 40µV
LT6233/LT6234/ LT6235	Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps	60MHz, 1.2mA, 1.2nV/√Hz, 15V/µs, 0.5mV
LT6220/LT6221/ LT6222	Single/Dual/Quad Low Power High Speed Rail-to-Rail Input and Output Op Amps	60MHz, 1mA, 10nV/√Hz, 20V/µs, 350µV
LTC6244	Dual High Speed CMOS Op Amp	50MHz, 7.4mA, 8nV/√Hz, 35V/µs, 100µV, Input Bias Current = 1pA
LT1632/LT1633	Dual/Quad Rail-to-Rail Input and Output Precision Op Amps	45MHz, 4.3mA, 12nV/√Hz, 45V/µs, 1.35mV
LT1630/LT1631	Dual/Quad Rail-to-Rail Input and Output Op Amps	30MHz, 3.5mA, 6nV/√Hz, 10V/µs, 525µV
LT1358/LT1359	Dual/Quad Low Power High Speed Op Amps	25MHz, 2.5mA, 8nV/√Hz, 600V/µs, 800µV, Drives All Capacitive Loads
ADC's		
LTC2366	3Msps, 12-Bit ADC Serial I/O	72dB SNR, 7.8mW No Data Latency TSOT-23 Package
LTC2365	1Msps, 12-Bit ADC Serial I/O	73dB SNR, 7.8mW No Data Latency TSOT-23 Package
LTC1417	Low Power 14-Bit 400ksps ADC Parallel I/O	Single 5V or ±5V Supplies, 0V to 4.096V or ±2.048V Input Range
LTC1274	Low Power 12-Bit 400ksps ADC Parallel I/O	10mW Single 5V or ±5V Supplies, 0V to 4.096V or ±2.048V Input Range

Rev C

D16949-0-5/18(C)

ANALOG DEVICES

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