LTC6955

Ultralow Jitter, 7.5GHz, 11 Output Fanout Buffer Family

FEATURES

- **LTC6955: 11 Output Buffer**
- **LTC6955-1: 10 Buffered Outputs and One ÷2 Output**
- **Additive Output Jitter ~45fs RMS (ADC SNR Method)**
- **Additive Output Jitter < 5fs RMS (Integration BW = 12kHz to 20MHz, f = 7.5GHz)**
- Eleven Ultralow Noise CML Outputs
- Parallel Control for Multiple Output Configurations
- –40°C to 125°C Operating Junction Temperature Range

APPLICATIONS

- High Performance Data Converter Clocking
- SONET, Fibre Channel, GigE Clock Distribution
- Low Skew and Jitter Clock and Data Fanout
- Wireless and Wired Communications
- Single-Ended to Differential Conversion

DESCRIPTION

The LTC®6955 is a high performance, ultralow jitter, fanout clock buffer with eleven outputs. Its 4-pin parallel control port allows for multiple output setups, enabling any number between three and eleven outputs, as well as a complete shutdown. The parallel port also provides the ability to invert the output polarity of alternating outputs, simplifying designs with top and bottom board routing. Each of the CML outputs can run from DC to 7.5GHz. The LTC6955-1 replaces one output buffer with a divide-by-2 frequency divider, allowing it to drive Analog Devices' LTC6952 or LTC6953 to generate JESD204B subclass 1 SYSREF signals. These SYSREFs can pair with ultralow jitter device clocks from the LTC6955-1, which can run at frequencies up to 7.5GHz.
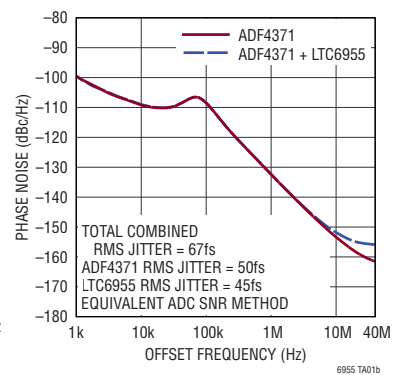
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TYPICAL APPLICATION

Generation of Multiple Low Jitter 7GHz Clocks
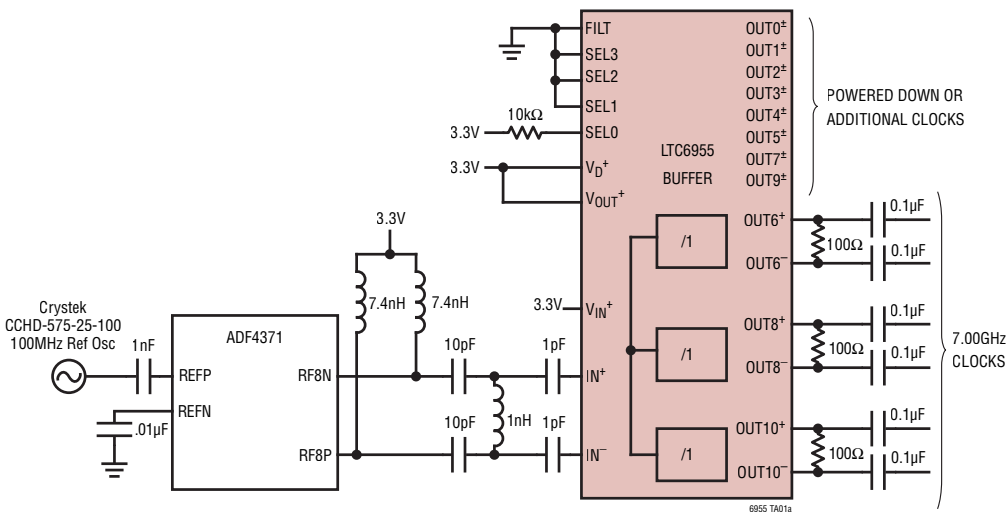
7GHz Cumulative Phase Noise ADF4371 Driving LTC6955

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V^+ (V_{IN}^+, V_D^+, V_{OUT}^+) to GND 3.6V

Voltage on All Pins....................GND − 0.3V to V^+ + 0.3V

Current into OUTx$^+$, OUTx$^-$, (x = 0 to 10) ....±25mA

Operating Junction Temperature Range, T_J (Note 2)

LTC6955I and LTC6955I-1 .... −40°C to 125°C

Junction Temperature, T_{JMAX}...............................130°C

Storage Temperature Range ....−65°C to 150°C

PIN CONFIGURATION

TOP VIEW

Pin	Name
52	SEL2
51	SEL1
50	SEL0
49	TEMP
48	NC
47	NC
46	NC
45	NC
44	NC
43	NC
42	NC
41	GND

Pin	Name
1	SEL3
2	V_D^+
3	OUT10$^-$
4	OUT10$^+$
5	V_{OUT}^+
6	OUT9$^-$
7	OUT9$^+$
8	V_{OUT}^+
9	OUT8$^-$
10	OUT8$^+$
11	V_{OUT}^+
12	OUT7$^-$
13	OUT7$^+$
14	V_{OUT}^+

53 (GND)

Pin	Name
40	FILT
39	V_{IN}^+
38	IN$^-$
37	IN$^+$
36	NC
35	V_{OUT}^+
34	OUT0$^+$
33	OUT0$^-$
32	V_{OUT}^+
31	OUT1$^+$
30	OUT1$^-$
29	V_{OUT}^+
28	OUT2$^+$
27	OUT2$^-$

Pin	Name
15	OUT6$^-$
16	OUT6$^+$
17	V_{OUT}^+
18	OUT5$^-$
19	OUT5$^+$
20	V_{OUT}^+
21	OUT4$^-$
22	OUT4$^+$
23	V_{OUT}^+
24	OUT3$^-$
25	OUT3$^+$
26	V_{OUT}^+

UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC QFN

T_{JMAX} = 130°C, θ_{JC} = 2°C/W, θ_{JA} = 31°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6955IUKG#PBF	LTC6955IUKG#TRPBF	LTC6955UKG	52-Lead (7mm × 8mm) Plastic QFN	−40°C to 125°C
LTC6955IUKG-1#PBF	LTC6955IUKG-1#TRPBF	LTC6955UKG-1	52-Lead (7mm × 8mm) Plastic QFN	−40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_D^+ = V_{IN}^+ = V_{OUT}^+ = 3.3V unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input (IN⁺, IN⁻)							
f_{IN}	Frequency Range		●			7500	MHz
	Input Power Level	R_Z = 50Ω, Single-Ended	●	0.25	0.8	1.6	V_{P-P}
			●	−8	2	8	dBm
	Self-Bias Voltage				2.05		V
	Input Common Mode Voltage	800 mV_{P-P} Differential Input	●	1.6		2.7	V
	Input Duty Cycle				50		%
	Minimum Input Slew Rate				100		V/µs
	Input Resistance	Differential			250		Ω
	Input Capacitance	Differential			1.0		pF
Digital Pin Specifications							
V_{IH}	High-Level Input Voltage	SEL3, SEL2, SEL1, SEL0, FILT	●	1.55			V
V_{IL}	Low-Level Input Voltage	SEL3, SEL2, SEL1, SEL0, FILT	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	SEL3, SEL2, SEL1, SEL0, FILT			250		mV
	Input Current	SEL3, SEL2, SEL1, SEL0, FILT	●			±1	µA
Clock Outputs (OUT0⁺, OUT0⁻, OUT1⁺, OUT1⁻, OUT2⁺, OUT2⁻, …, OUT10⁺, OUT10⁻)							
f_{OUT}	LTC6955 Output Frequency	Differential Termination = 100Ω, All Outputs	●	0		7500	MHz
	LTC6955-1 Output Frequency	Differential Termination = 100Ω, All Outputs Except OUT10	●	0		7500	MHz
		Differential Termination = 100Ω, OUT10 Only	●	0		3750	MHz
V_{OD}	Output Differential Voltage	Differential Termination = 100Ω	●	320	420	550	mV_{P-P}
	Output Resistance	Differential			100		Ω
	Output Common Mode Voltage	Differential Termination = 100Ω			V_{OUT}^+ − 1.0		V
t_R	Output Rise Time, 20% to 80%	Differential Termination = 100Ω			50		ps
t_F	Output Fall Time, 80% to 20%	Differential Termination = 100Ω			50		ps
DC	Output Duty Cycle	Differential Termination = 100Ω	●	45	50	55	%
t_{PD}	LTC6955 Propagation Delay, All Outputs	$V_{FILT} < V_{IL}$, T_A = 25°C			220		ps
		$V_{FILT} > V_{IH}$, T_A = 25°C			230		ps
	LTC6955-1 Propagation Delay, All Outputs Except OUT10	$V_{FILT} < V_{IL}$, T_A = 25°C			220		ps
		$V_{FILT} > V_{IH}$, T_A = 25°C			230		ps
	LTC6955-1 Propagation Delay, OUT10 Only	$V_{FILT} < V_{IL}$, T_A = 25°C			280		ps
		$V_{FILT} > V_{IH}$, T_A = 25°C			290		ps
	Propagation Delay, Temperature Variation				0.23		ps/°C
t_{SKEW}	LTC6955 Skew, All Outputs Except OUT0 (Note 4)	Same Part	●		±10	±25	ps
		Across Multiple Parts	●		±20	±50	ps
	LTC6955-1 Skew, All Outputs Except OUT0 and OUT10 (Note 4)	Same Part	●		±10	±25	ps
		Across Multiple Parts	●		±20	±50	ps

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_D^+ = V_{IN}^+ = V_{OUT}^+ = 3.3V unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Voltages							
	V_{OUT}^+ Supply Range		●	3.15	3.3	3.45	V
	V_D^+ Supply Range		●	3.15	3.3	3.45	V
	V_{IN}^+ Supply Range		●	3.15	3.3	3.45	V
Power Supply Currents							
I_{DDOUT}	LTC6955 V_{OUT}^+ Supply Current (Note 3)	SEL = 14, All Outputs Active	●		350	420	mA
		SEL = 1, Three Outputs Active			105		mA
		SEL = 0 or 15, All Outputs Off			90		µA
	LTC6955-1 V_{OUT}^+ Supply Current (Note 3)	SEL = 14, All Outputs Active	●		358	430	mA
		SEL = 1, Three Outputs Active			108		mA
		SEL = 0 or 15, All Outputs Off			90		µA
$I_{DD – 3.3V}$	LTC6955 or LTC6955-1 Sum V_D^+, V_{IN}^+ Supply Currents (Note 3)	SEL = 14, All Outputs Active	●		85	110	mA
		SEL = 1, Three Outputs Active			67		mA
		SEL = 0, All Outputs Off, Temp Diode Off			20		µA
		SEL = 15, All Outputs Off, Temp Diode On			360		µA
Additive Phase Noise, Jitter and Spurious (Note 5)							
	Output Noise/Jitter, f_{IN} = 7.5GHz	Phase Noise Floor			−155.2		dBc/Hz
		RMS Jitter, 12kHz to 20MHz Integration BW			5		fs_{RMS}
		RMS Jitter, ADC SNR Method (Note 6)			45		fs_{RMS}
	Output Noise/Jitter, f_{IN} = 1.0GHz	Phase Noise Floor			−164		dBc/Hz
		RMS Jitter, 12kHz to 20MHz Integration BW			7		fs_{RMS}
		RMS Jitter, ADC SNR Method (Note 6)			45		fs_{RMS}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6955 is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 125°C.

Note 3: The SEL code (SEL) programs the state of each output as described in Table 2. SEL's value is determined by the voltage state of the SELx pins. If V_{SELx} > V_{IH}, its digital value (SELx) is "1". If V_{SELx} < V_{IL}, its digital value (SELx) is "0". The SEL code is equal to 8•SEL3 + 4•SEL2 + 2•SEL1 + SEL0.

Note 4: For LTC6955, skew is defined as the difference between the zero-crossing time of a given output and the average zero-crossing time of all outputs. For LTC6955-1, skew is defined as the difference between the zero-crossing time of a given output and the average zero-crossing time of outputs 0 to 9.

Note 5: Additive phase noise and jitter from LTC6955 only. Incoming clock phase noise is not included.

Note 6: Additive RMS jitter (ADC SNR method) is calculated by integrating the distribution section's measured additive phase noise floor out to f_{CLK}. Actual ADC SNR measurements show good agreement with this method.

Note 7: The LTC6955 is driven from a VCO (CVCO55CC-4000-4000) through a splitter. The other side of the splitter drives the input of a LTC6952 to lock the VCO in a PLL. The reference for the LTC6952 PLL is a Pascal OCXO-E, f_{REF} = 100MHz, P_{REF} = 6dBm.

Note 8: Measured using DC2611.

Note 9: Cable loss is de-embeded in this plot, but board and connector losses are not. Output board traces are approximately 5cm long.

Note 10: Data for outputs 0 to 9 was taken on 1304 total parts from four assembly lots (two LTC6955 and two LTC6955-1). Data for LTC6955 OUT10 was taken on 710 parts from two assembly lots. Data for LTC6955-1 OUT10 was taken on 594 parts from two assembly lots.
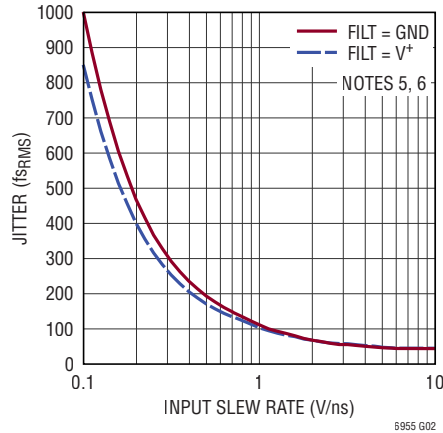
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$. $V_D^+ = V_{IN}^+ = V_{OUT}^+ = 3.3V$, unless otherwise noted.
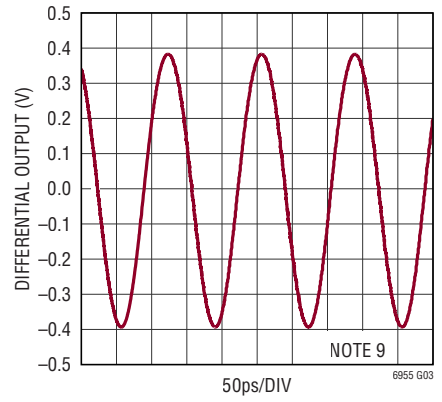
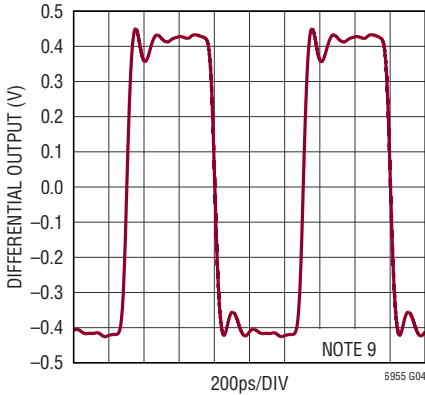**Total Phase Noise, Driven from VCO in a Locked PLL, f_{IN} = 4000MHz, FILT = GND**
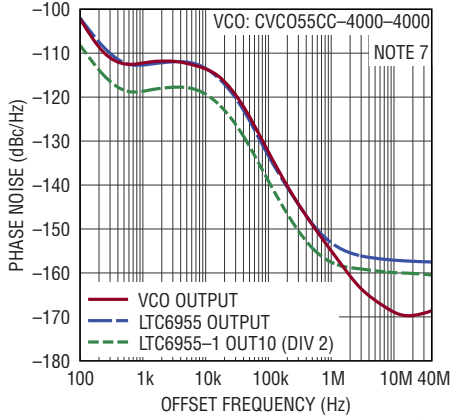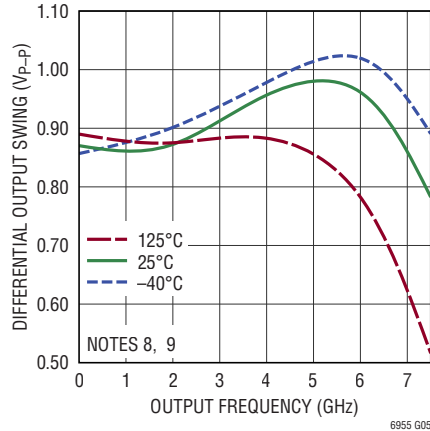
Additive Jitter vs Input Slew Rate, ADC SNR Method
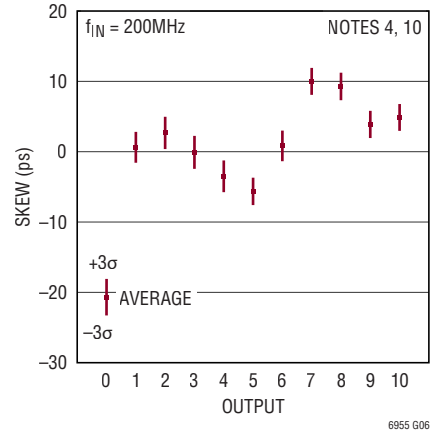
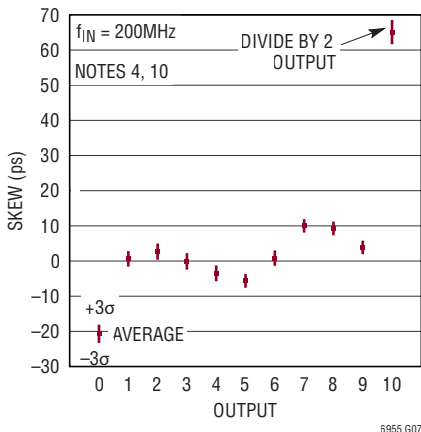**CML Differential Output at 7.5GHz**

CML Differential Output at 1GHz

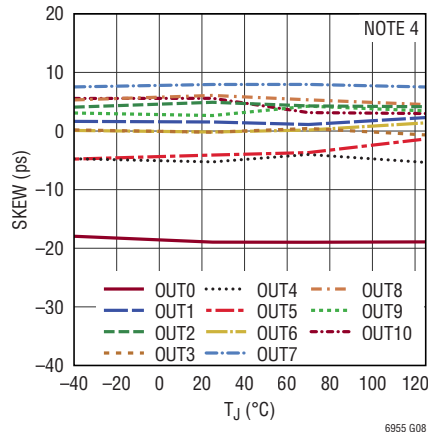**Differential Output Swing vs Frequency, Junction Temperature**
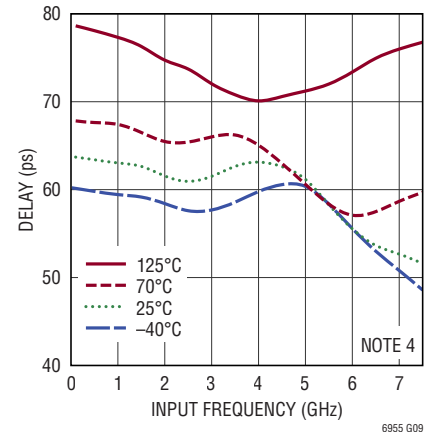
Expected Skew Variation for a Single LTC6955

Expected Skew Variation for a Single LTC6955-1

Skew Variation with Junction Temperature for a Single Typical LTC6955

LTC6955-1 OUT10 Skew vs Frequency, Junction Temperature
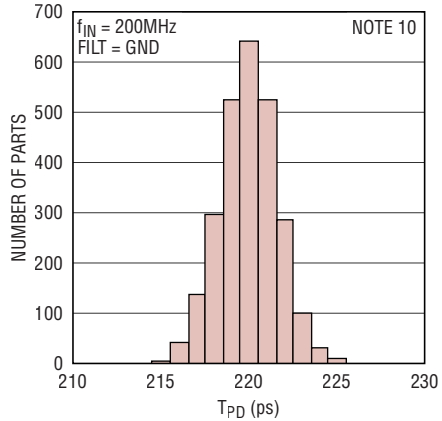
Rev. 0

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TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_D{}^+$ = $V_{IN}{}^+$ = $V_{OUT}{}^+$ = 3.3V, unless otherwise noted.

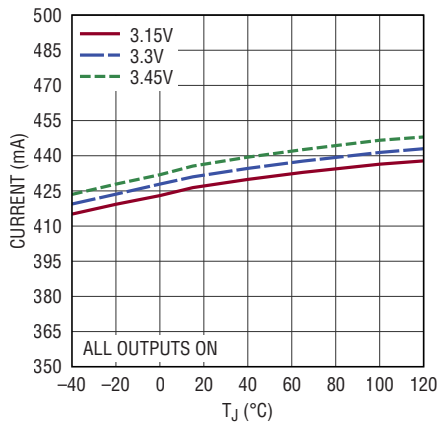**Propagation Delay vs Frequency, Junction Temperature**
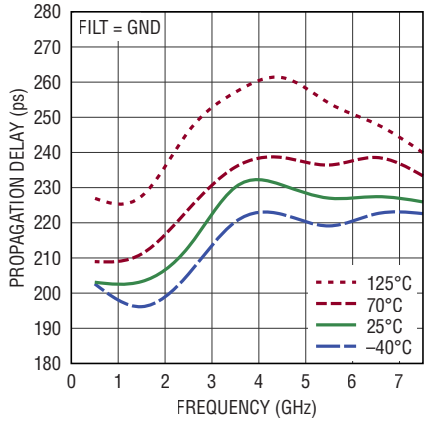
6955 G10

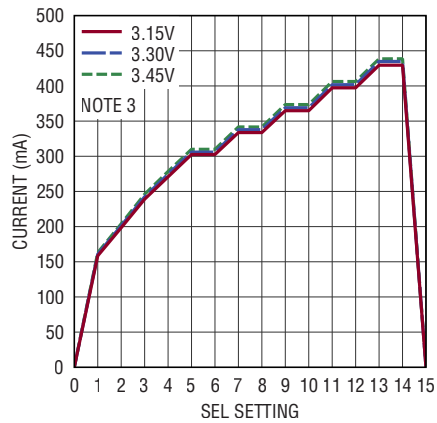**LTC6955 and LTC6955-1 Propagation Delay Variation, Input to OUT5**

6955 G11

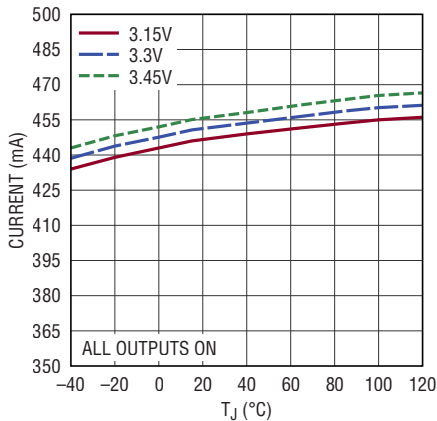**LTC6955 Supply Current vs Junctiion Temperature and Voltage**

6955 G12
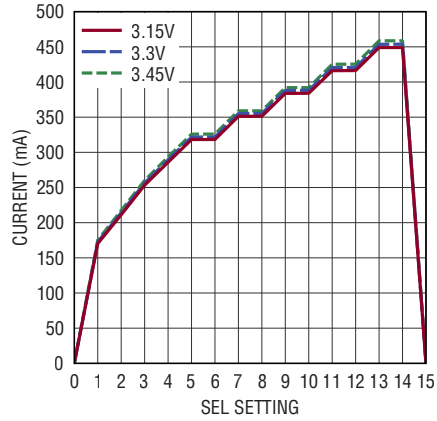
LTC6955 Supply Current vs Voltage and SEL Setting

6955 G13

LTC6955-1 Supply Current vs Junction Temperature and Voltage

6955 G14

LTC6955-1 Supply Current vs Voltage and SEL Setting

6955 G15

Rev. 0

PIN FUNCTIONS

SEL3, SEL2, SEL1, SEL0 (Pins 1, 52, 51, 50): Parallel Port Control Bits. These CMOS inputs control the output configuration. See the Operation section for more details.

V_D^+ (Pin 2): 3.15 to 3.45V Positive Supply Pins for Parallel Port. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

V_{OUT}^+ (Pins 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35): 3.15 to 3.45V Positive Supply Pins for Outputs. Each pin should be separately bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

OUT10$^+$, OUT10$^-$ (Pins 3, 4): Output Signals. The output is buffered and presented differentially on these pins. The outputs have 50Ω (typical) output resistance per side (100Ω differential). The far end of the transmission line is typically terminated with 100Ω connected across the outputs. For the LTC6955, this output is an undivided version of the input, identical to the other outputs. For the LTC6955-1, only this output is a frequency divided by two version of the input signal. See the Operation and Applications Information section for more details.

OUT9$^+$, OUT9$^-$ (Pins 6, 7): Output Signals. The output is buffered and presented differentially on these pins. The outputs have 50Ω (typical) output resistance per side (100Ω differential). The far end of the transmission line is typically terminated with 100Ω connected across the outputs. This output is an undivided version of the input.

OUT8$^+$, OUT8$^-$ (Pins 9, 10): Same as OUT9.

OUT7$^+$, OUT7$^-$ (Pins 12, 13): Same as OUT9.

OUT6$^+$, OUT6$^-$ (Pins 15, 16): Same as OUT9.

OUT5$^+$, OUT5$^-$ (Pins 18, 19): Same as OUT9.

OUT4$^+$, OUT4$^-$ (Pins 21, 22): Same as OUT9.

OUT3$^+$, OUT3$^-$ (Pins 24, 25): Same as OUT9.

OUT2$^+$, OUT2$^-$ (Pins 27, 28): Same as OUT9.

OUT1$^+$, OUT1$^-$ (Pins 30, 31): Same as OUT9.

OUT0$^+$, OUT0$^-$ (Pins 33, 34): Same as OUT9.

NC (Pin 36): Not Connected Internally. It is recommended that this pin be connected to the ground pad (Pin 53).

IN$^+$, IN$^-$ (Pins 37, 38): Input Signals. The differential signal placed on these pins is buffered with a low noise amplifier and fed to the internal distribution path and outputs. These self-biased inputs present a differential 250Ω (typical) resistance to aid impedance matching. They may be driven single-ended by using the matching circuit in the Applications Information section.

V_{IN}^+ (Pins 39): 3.15 to 3.45V Positive Supply Pin for Input Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

FILT (Pin 40): Input Filter Control Pin. When tied to GND, the input is not filtered. When tied to V$^+$, the input is filtered to improved noise performance of low slew rate input signals. See the Operation section for details.

GND (Pin 41): Negative Power Supply (Ground). This pin should be tied directly to the ground plane with multiple vias.

NC (Pins 42, 43, 44, 45, 46, 47, 48): No Connect. These pins should be left open or connected to GND.

TEMP (Pin 49): Temperature Measurement Pin. When enabled, this outputs a temperature measurement diode voltage. See the Operation section for details.

GND (Exposed Pad Pin 53): Negative Power Supply (Ground). The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.
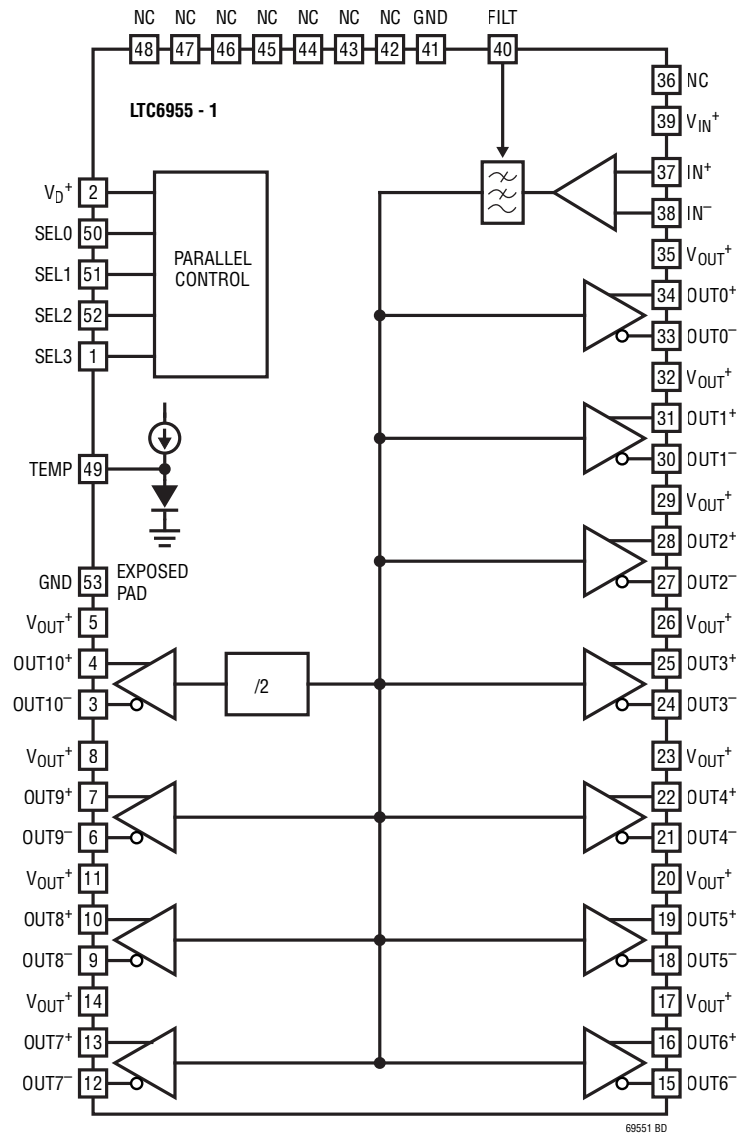
7
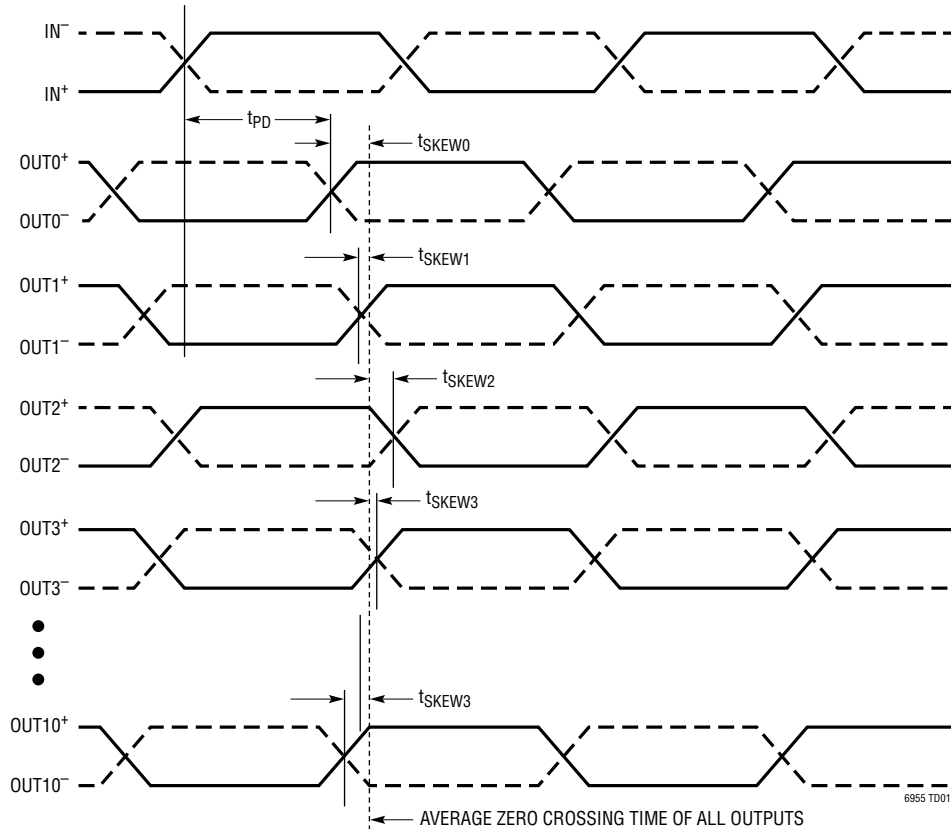
BLOCK DIAGRAM

LTC6955 Block Diagram

6955 BD
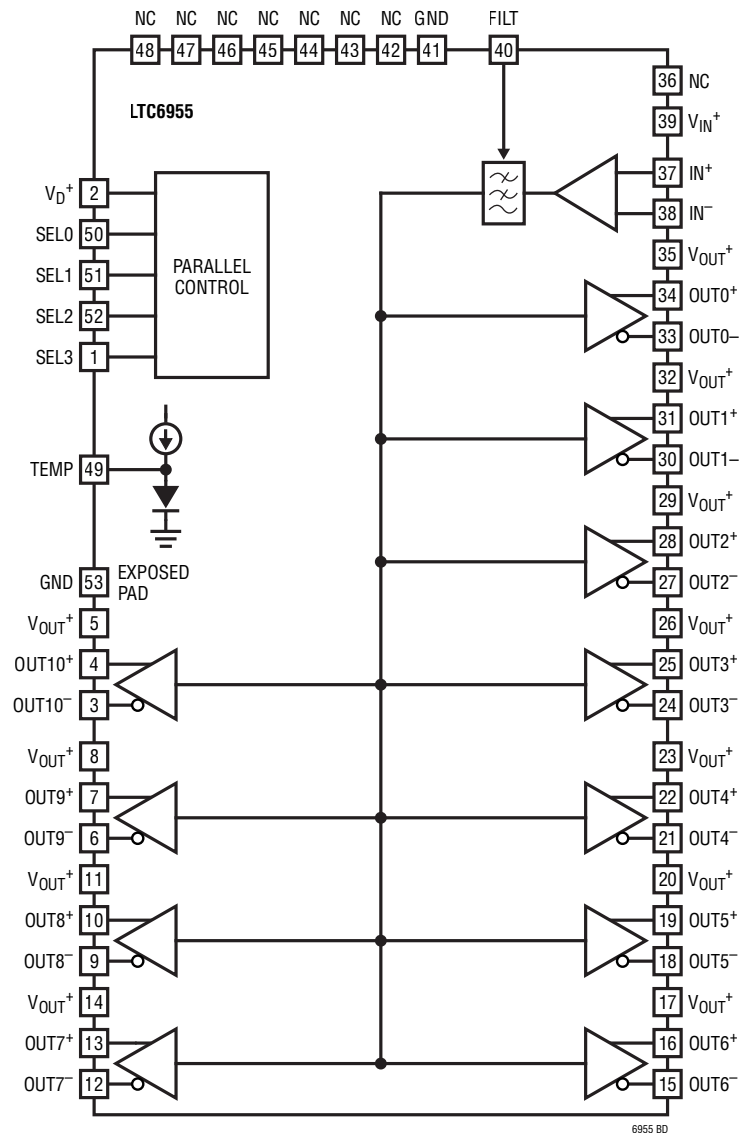
BLOCK DIAGRAM

LTC6955-1 Block Diagram
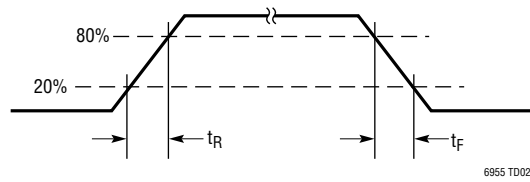

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69551 BD

TIMING DIAGRAMS

Propagation Delay and Output Skew

6955 TD01

AVERAGE ZERO CROSSING TIME OF ALL OUTPUTS

Differential CML Rise/Fall Times

6955 TD02

Rev. 0

For more information www.analog.com

OPERATION

The LTC6955 is a high-performance multi-output clock buffer that operates up to 7.5GHz. The device is able to achieve superior integrated jitter performance by way of its excellent output noise floor.

Input Buffer

The LTC6955's input buffer provides a flexible interface to either differential or single-ended frequency sources. The inputs are self-biased, and AC-coupling is recommended for applications using external VCO/VCXO/VCSOs. However, the input can also be driven DC-coupled by LVPECL, CML, or any other driver type within the input's specified common mode range. See the Applications Information section for more information on common input interface configurations, noting that the LTC6955's input buffer has an internal differential resistance of 250Ω as shown in Figure 1.
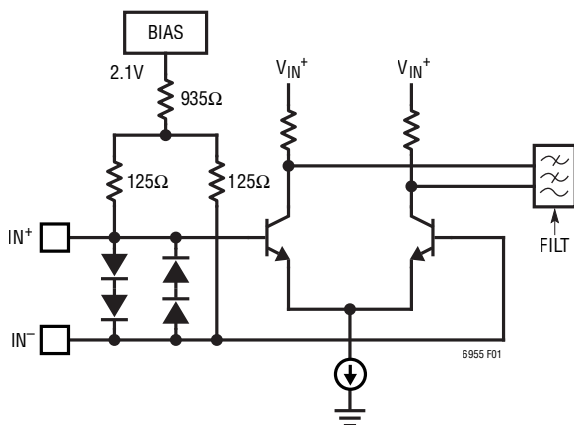

Figure 1. Simplified Input Interface Schematic

The maximum frequency for the input buffer is 7.5GHz, and the maximum amplitude is 1.6V_{P-P}. It is also important that the input signal be low noise and have a slew rate of at least 100V/µs, although better performance will be achieved with a higher slew rate. For applications with an input slew rate less than 2V/ns, better phase noise performance will be achieved by enabling the internal broadband noise filtering circuit within the input buffer. This is accomplished by setting the FILT pin (pin 40) to V^+. Note that setting FILT = V^+ when the slew rate of the input is greater than 2V/ns will degrade the overall phase noise performance. See Table 1 for recommended settings of FILT.

Table 1. FILT Control Voltage

FILTV	Slew Rate of Input
V^+	< 2V/ns
GND	≥ 2V/ns

CML Output Buffers (OUT0 to OUT10)

All of the outputs are ultralow noise, low skew 2.5V CML buffers. Each output can be AC or DC coupled and terminated with 100Ω differential. If a single-ended output is desired, each side of the CML output can be individually AC coupled and terminated with 50Ω. See Figure 2 for circuit details.
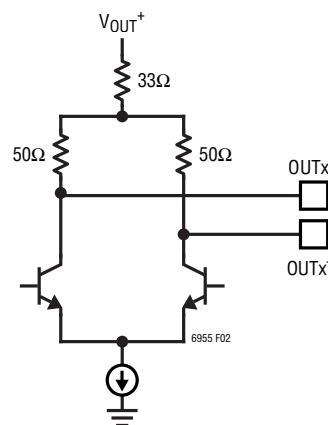

Figure 2. Simplified CML Interface Schematic (All OUTx)

OPERATION

Output Programming

The LTC6955's eleven outputs can be configured by setting the state of the four SELx pins. Three to eleven outputs can be enabled at one time, and odd outputs have the additional ability to be enabled with their output inverted. See Table 2 for full programming details, where OFF means the output is disabled, ON means the output is enabled and not inverted from the input, and INV means the output is enabled and inverted from the input.

TEMP Pin

The TEMP pin outputs a temperature measurement diode voltage when enabled. For an approximate die temperature, a calibration point is required. Measure the TEMP pin voltage (V_{TEMPC}) with the LTC6955 powered down (SEL3 = SEL2 = SEL1 = SEL0 = 1) at a known temperature (t_{CAL}). Then calculate the operating temperature in a desired application by measuring the TEMP voltage again (V_{TEMP}) and using the following equation:

$$t = 665 \cdot (V_{TEMPC} - V_{TEMP}) + t_{CAL}$$

where t and t_{CAL} are in °C, and V_{TEMPC} and V_{TEMP} are in V.

The TEMP diode is enabled in all modes except a full shutdown (SEL3 = SEL2 = SEL1 = SEL0 = 0) as shown in Table 2.

Table 2. Output Programming with SELx Pins (Note 3)

| SEL CODE	SEL3	SEL2	SEL1	SEL0	# OF ACTIVE OUTPUTS	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8	OUT9	OUT10	TEMP
0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	0	1	3	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	ON
2	0	0	1	0	4	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON
3	0	0	1	1	5	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON
4	0	1	0	0	6	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	ON	ON
5	0	1	0	1	7	OFF	OFF	ON	OFF	ON	OFF	ON	INV	ON	INV	ON	ON
6	0	1	1	0	7	OFF	OFF	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON
7	0	1	1	1	8	OFF	OFF	ON	OFF	ON	INV	ON	INV	ON	INV	ON	ON
8	1	0	0	0	8	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
9	1	0	0	1	9	OFF	OFF	ON	INV	ON	INV	ON	INV	ON	INV	ON	ON
10	1	0	1	0	9	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
11	1	0	1	1	10	OFF	INV	ON	INV	ON	INV	ON	INV	ON	INV	ON	ON
12	1	1	0	0	10	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
13	1	1	0	1	11	ON	INV	ON	INV	ON	INV	ON	INV	ON	INV	ON	ON
14	1	1	1	0	11	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
15	1	1	1	1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

# APPLICATIONS INFORMATION

Introduction

The LTC6955 can be used in any application where multiple outputs of the same clock frequency are needed. It is especially effective for data converter clocking, where ultralow jitter is often necessary to prevent negative impact on the data converter's noise performance.
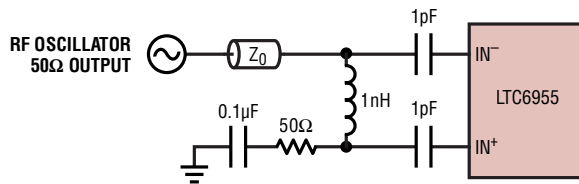
Input

The LTC6955's input buffer, shown in Figure 1, has a frequency range of DC to 7.5GHz. The buffer has a partial on-chip differential input termination of 250Ω, allowing some flexibility for an external matching network if desired. Figure 3 shows recommended interfaces for different input signal types.
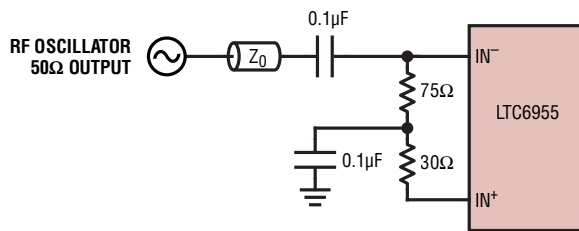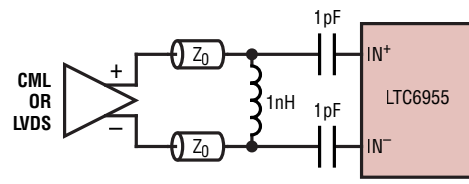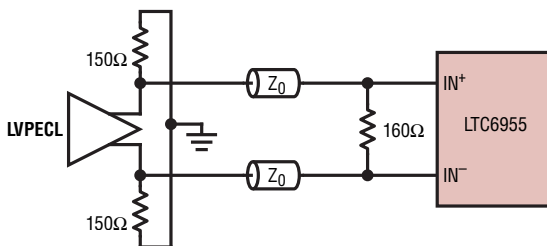

AC-Coupled RF Sine Wave Oscillator (f_{IN} < 5GHz)
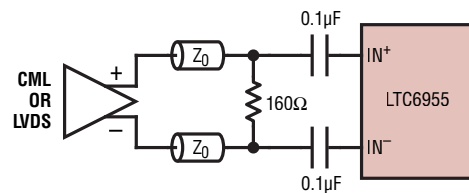
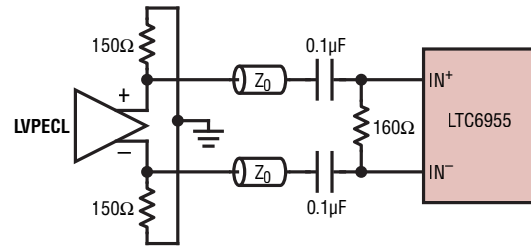**AC-Coupled Differential CML or LVDS (f_{IN} < 5GHz)**

AC-Coupled RF Sine Wave Oscillator ($f_{IN} \geq$ 5GHz)
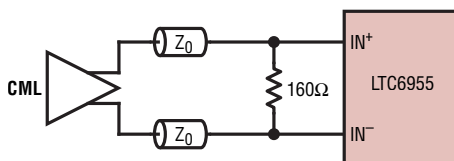

AC-Coupled Differential CML or LVDS ($f_{IN} \geq$ 5GHz)

DC-Coupled Differential LVPECL*

AC-Coupled Differential LVPECL

DC-Coupled Differential CML*

* DC coupled CML and LVPECL input common mode level must be within the min and max levels specified in the Electrical Characteristics. All LTC6951, LTC6952, LTC6953, and LTC6955 CML output levels are acceptable.

6955 F03

Figure 3. Common Input Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines

APPLICATIONS INFORMATION

LTC6955 Design Example with Eight ADCs

This design example consists of a system of eight analog-to-digital converters (ADCs) being driven from a single LTC6955. Assume PCB layout constraints require four ADCs on the top of the circuit board and four on the bottom. This means the LTC6955 should ideally provide four non-inverted clocks for the topside ADCs and four inverted clocks for the bottom side ADCs. Referring to Table 2, SEL code 9 provides the closest number and polarity of active outputs, even though one spare output will be active. Figure 4 shows a block diagram of the proposed system. Note that any active output should be terminated with 100Ω, even if it is not used.

For this example, assume the input is being driven single-ended by a 500MHz sine wave oscillator with output swing of 1.6V_{P-P}. The incoming slew rate (SR) can be determined from the following equation:

$$SR = V_{AMP} \cdot 2\pi \cdot f_{IN}$$

where V_{AMP} is the input amplitude (in V_P) and f_{IN} is the input frequency (in Hz). In this example:

$$SR = 0.8V_P \cdot 2\pi \cdot 500MHz = 2.5V/ns$$

Referring to Table 1, set the FILT pin to GND since 2.5V/ns is greater than 2V/ns.
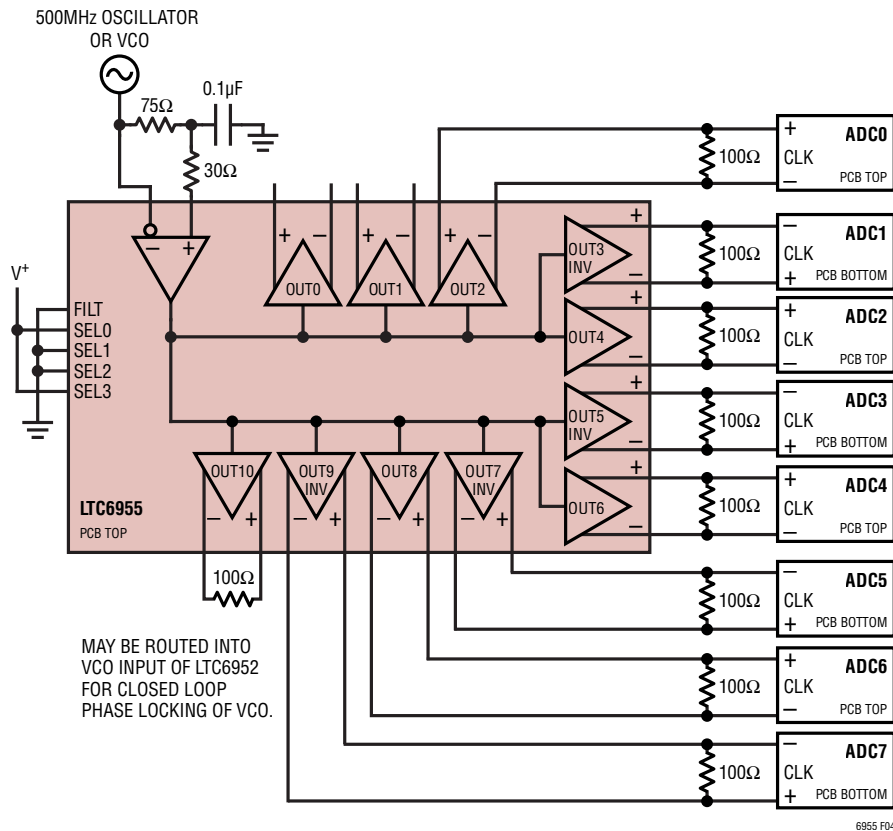

Figure 4. Block Diagram for LTC6955 Design Example
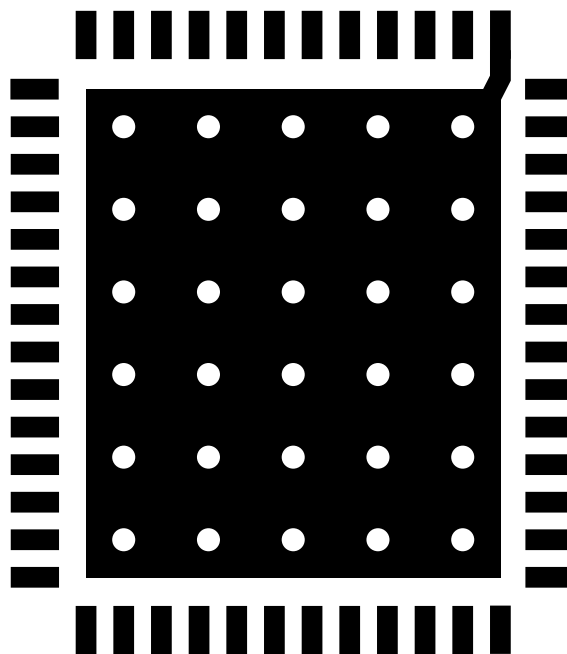
APPLICATIONS INFORMATION

Supply Bypassing and PCB Layout Guidelines

Care must be taken when creating a PCB layout to minimize power supply decoupling and ground inductances. All power supply V$^+$ pins should be bypassed directly to the ground plane using either a 0.01µF or a 0.1µF ceramic capacitor as called out in the Pin Functions section as close to the pin as possible. Multiple vias to the ground plane should be used for all ground connections, including to the power supply decoupling capacitors.

The presence of the divide-by-2 output on the LTC6955-1 causes a spur to appear on the other buffered outputs of the part. This spur can be improved by adding a ferrite bead in series with the V$_{OUT}^+$ supply pin for OUT10 (Pin 6). See the Typical Application Generation of 7.25GHz, 52fs ADC SNR Jitter Clocks Using LTC6952 and LTC6955-1 for an example.

The package's exposed pad is a ground connection, and must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance (see Figure 5 for an example). An example of grounding for electrical and thermal performance can be found on the DC2611 layout.

6955 F05

Figure 5. PCB Top Metal Layer Pin and Exposed Ground Pad Design. Pin 41 Is Signal Ground and Connected Directly to the Exposed Pad Metal

APPLICATIONS INFORMATION

ADC Clocking and Jitter Requirements

Adding noise directly to a clean signal clearly reduces its signal to noise ratio (SNR). In data acquisition applications, digitizing a clean signal with a noisy clock signal also degrades the SNR. This issue is best explained in the time domain using jitter instead of phase noise. For this discussion, assume that the jitter is white (flat with frequency) and of Gaussian distribution.

Figure 6 shows a sine wave signal entering a typical data acquisition circuit composed of an ADC, an input signal amplifier and a sampling clock. Also shown are three signal sampling scenarios for sampling the sine wave at its zero crossing.

In the first scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. Without any added noise or sampling clock jitter, the ADC's digitized output value is very clearly determined and perfectly repeatable from cycle to cycle.

In the second scenario, a perfect sine wave input is buffered by a noisy amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. The added noise results in an uncertainty in the digitized value, causing an error term which degrades the SNR. The degraded SNR in this scenario, from adding noise to the signal, is expected.
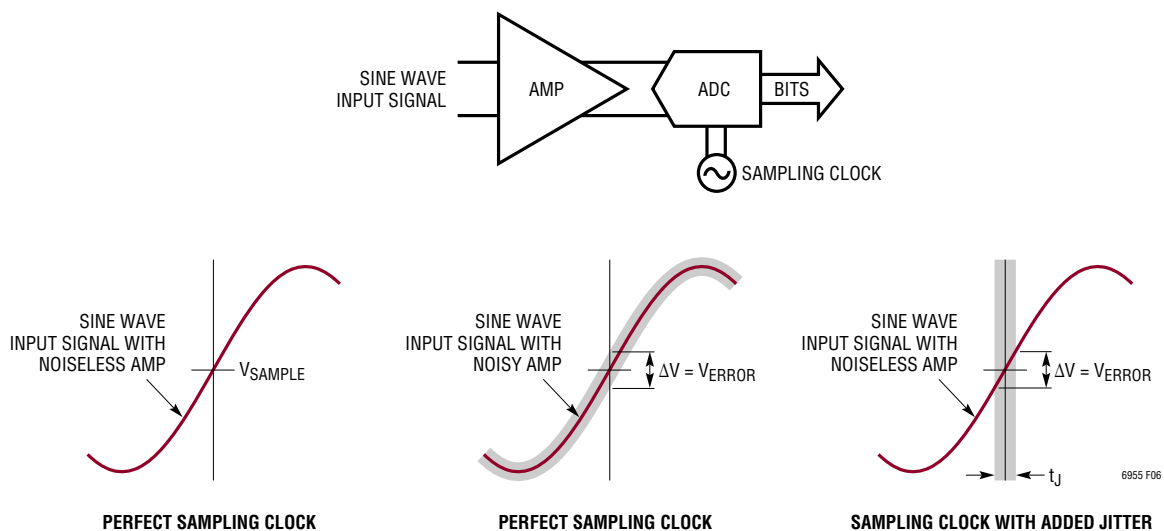

Figure 6. A Typical Data Acquisition Circuit Showing the Sampling Error Effects of a Noisy Amplifier and a Jittery Sampling Clock

APPLICATIONS INFORMATION

In the third scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a clock signal with added jitter. Note that as the signal is slewing, the jitter of the clock signal leads to an uncertainty in the digitized value and an error term just as in the previous scenario. Again, this error term degrades the SNR.

A real-world system will have both additive amplifier noise and sample clock jitter. Once the signal is digitized, determining the root cause of any SNR degradation – amplifier noise or sampling clock jitter – is difficult.

Degradation of the SNR due to sample clock jitter only occurs if the analog input signal is slewing. If the analog input signal is stationary (DC) then it does not matter when in time the sampling occurs. Additionally, a faster slewing input signal yields a greater error (more noise) than a slower slewing input signal.

Figure 7 demonstrates this effect. Note how much larger the error term is with the fast slewing signal than with the slow slewing signal. To maintain the data converter's SNR performance, digitization of high input frequency signals requires a clock with much less jitter than applications with lower frequency input signals.
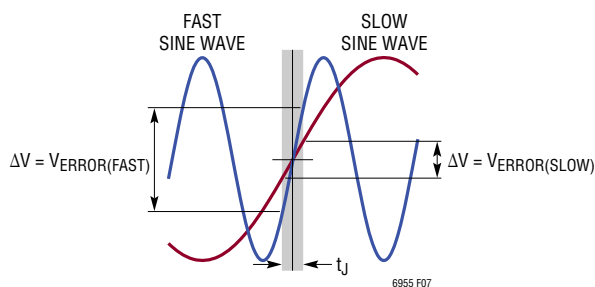

Figure 7. Fast and Slow Sine Wave Signals Sampled with a Jittery Clock

It is important to note that the frequency of the analog input signal determines the sample clock's jitter requirement. The actual sample clock frequency does not matter. Many ADC applications that under-sample high frequency signals have especially challenging sample clock jitter requirements.

The previous discussion was useful for gaining an intuitive feel for the SNR degradation due to sampling clock jitter.

Quantitatively, the actual sample clock jitter requirement for a given application is calculated as follows:

$$t_{J(TOTAL)} = \frac{10^{\frac{-SNR_{dB}}{20}}}{2 \cdot \pi \cdot f_{SIG}} \tag{1}$$

Where f_{SIG} is the highest frequency signal to be digitized expressed in Hz, SNRdB is the SNR requirement in decibels and $t_{J(TOTAL)}$ is the total RMS jitter in seconds. The total jitter is the RMS sum of the ADC's aperture jitter and the sample clock jitter calculated as follows:

$$t_{J(TOTAL)} = \sqrt{t_{J(CLK)}^2 + t_{J(ADC)}^2} \tag{2}$$

Alternatively, for a given total jitter, the attainable SNR is calculated as follows:

$$SNR_{dB} = -20 \log_{10}\left(2 \cdot \pi \cdot f_{SIG} \cdot t_{J(TOTAL)}\right) \tag{3}$$

These calculations assume a full-scale sine wave input signal. If the input signal is a complex, modulated signal with a moderate crest factor, the peak slew rate of the signal may be lower and the sample clock jitter requirement may be relaxed.

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APPLICATIONS INFORMATION

These calculations are also theoretical. They assume a noiseless ADC with infinite resolution. All realistic ADCs have both added noise and a resolution limit. The limitations of the ADC must be accounted for to prevent over-specifying the sampling clock.

Figure 8 plots the previous equations and provides a simple, quick way to estimate the sampling clock jitter requirement for a given input signal or the expected SNR performance for a given sample clock jitter.
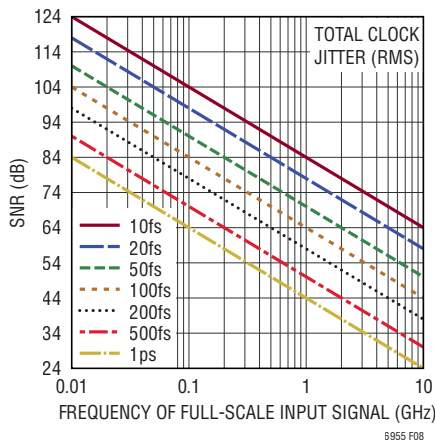

Figure 8. SNR vs Input Signal Frequency vs Sample Clock Jitter

Measuring Clock Jitter Indirectly Using ADC SNR

For some applications, integrating a clock generator's phase noise within a defined offset frequency range (i.e. 12kHz to 20MHz) is sufficient to calculate the clock's impact on the overall system performance. In these situations, the RMS jitter can be calculated from a phase noise measurement.

However, other applications require knowledge of the clock's phase noise at frequency offsets that exceed the capabilities of today's phase noise analyzers. This limitation makes it difficult to calculate jitter from a phase noise measurement.

The RMS jitter of an ADC clock source can be indirectly measured by comparing a jitter dominated SNR measurement to a non-jitter dominated SNR measurement. A jitter dominated SNR measurement (SNRjitter) is created by applying a low jitter, high frequency full-scale sine wave to the ADC analog input. A non-jitter dominated SNR measurement (SNRbase) is created by applying a very low amplitude (or low frequency) sine wave to the ADC analog input. The total clock jitter ($t_{J(TOTAL)}$) can be calculated using Equation 4.

$$t_{J(TOTAL)} = \frac{10^{\left[\frac{1}{2}\log 10\left(10^{-\left(\frac{SNR_{jitter}}{10}\right)} - 10^{-\left(\frac{SNR_{base}}{10}\right)}\right)\right]}}{2\pi f_{IN}} \tag{4}$$

Assuming the inherent aperture jitter of the ADC ($t_{J(ADC)}$) is known, the jitter of the clock generator ($t_{J(CLK)}$) is obtained using Equation 2.

ADC Sample Clock Input Drive Requirements

Modern high speed, high resolution ADCs are incredibly sensitive components able to match or exceed laboratory instrument performance in many regards. Noise or interfering signals on the analog signal input, the voltage reference or the sampling clock input can easily appear in the digitized data. To deliver the full performance of any ADC, the sampling clock input must be driven with a clean, low jitter signal.

Figure 9 shows a simplified version of a typical ADC sample clock input. In this case the input pins are labeled ENC± for Encode while some ADCs label the inputs CLK± for Clock. The input is composed of a differential limiting amplifier stage followed by a buffer that directly controls the ADC's track and hold stage.

The sample clock input amplifier also benefits from a fast slewing input signal as the amplifier has noise of its own. By slewing through the crossover region quickly, the amplifier noise creates less jitter than if the transition were slow.
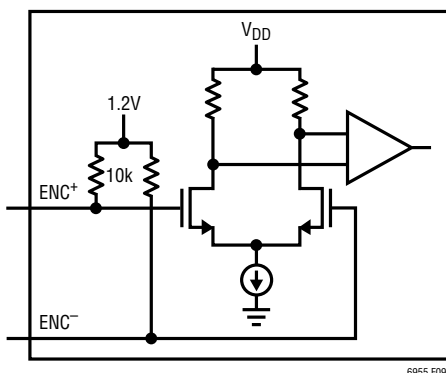
18

APPLICATIONS INFORMATION

Figure 9. Simplified Sample Clock Input Circuit

As shown in Figure 9, the ADC's sample clock input is typically differential, with a differential sampling clock delivering the best performance. Figure 9 also shows the sample clock input having a different common mode input voltage than the LTC6955's CML outputs. Most ADC applications will require AC coupling to convert between the two common mode voltages.

Transmission Lines and Termination

Interconnection of high speed signaling with fast rise and fall times requires the use of transmission lines with properly matched termination. The transmission lines may be stripline, microstrip or any other design topology. A detailed discussion of transmission line design is beyond the scope of this data sheet. Any mismatch between the transmission line's characteristic impedance and the terminating impedance results in a portion of the signal reflecting back toward the other end of the transmission line. In the extreme case of an open or short circuit termination, all of the signal is reflected back. This signal reflection leads to overshoot and ringing on the waveform. Figure 10 shows the preferred method of far-end termination of the transmission line.
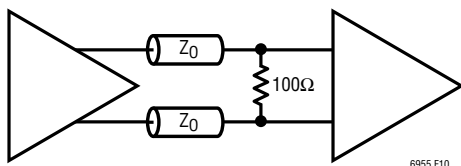
Figure 10. Far-End Transmission Line Termination ($Z_0 = 50\Omega$)

Using the LTC6955 to Drive ADC Sample Clock Inputs

The LTC6955's CML outputs are designed to interface with standard CML or LVPECL devices while driving transmission lines with far-end termination. Figure 11 shows DC coupled and AC coupled output configurations for the CML outputs.
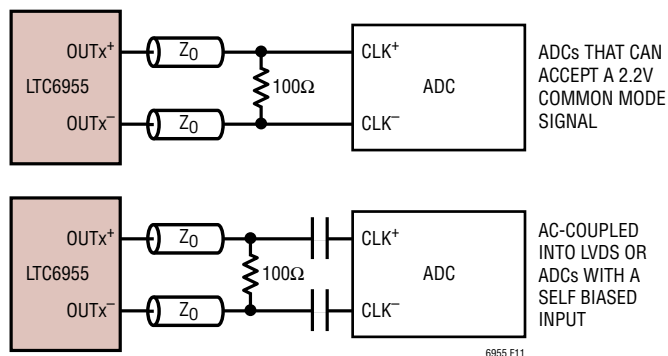
Figure 11. OUTx CML Connections to ADC Sample Clock Inputs ($Z_0 = 50\Omega$)

Rev. 0

TYPICAL APPLICATIONS

Generation of 7.25GHz, 52fs ADC SNR Jitter Clocks Using LTC6952 and LTC6955-1

6955 TA02a

LTC6955-1 and LTC6952
Phase Noise f_{VCO} = 7.25GHz

6955 TA02b

7.25GHz JESD204B
CLK to SYSREF Alignment
Calibration Over Temperature

6955 TA02c
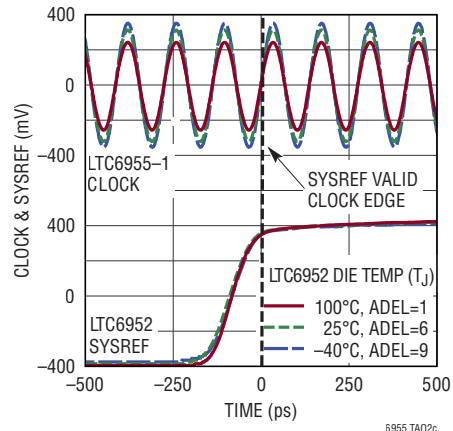
Rev. 0

PACKAGE DESCRIPTION

UKG Package
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)
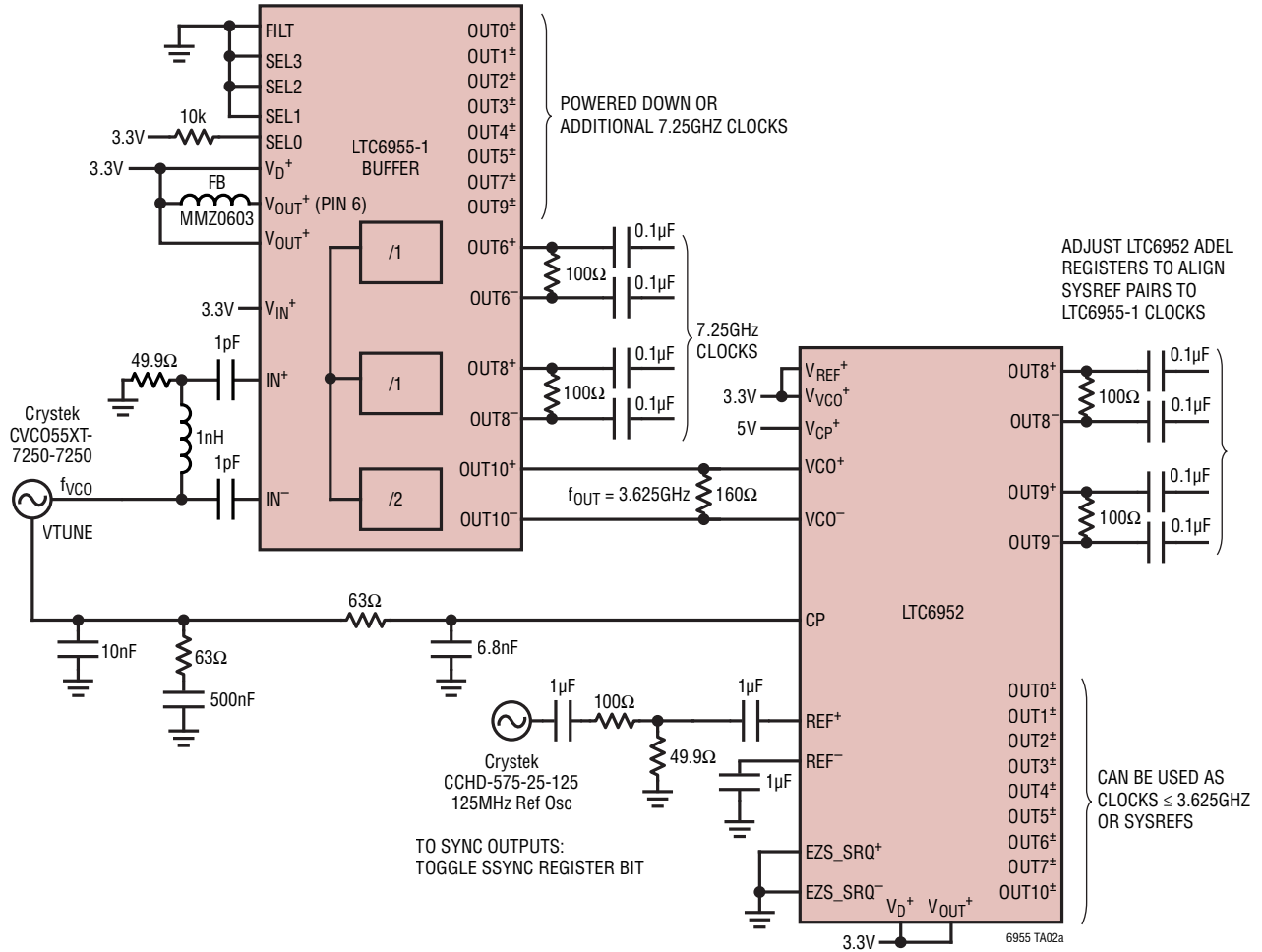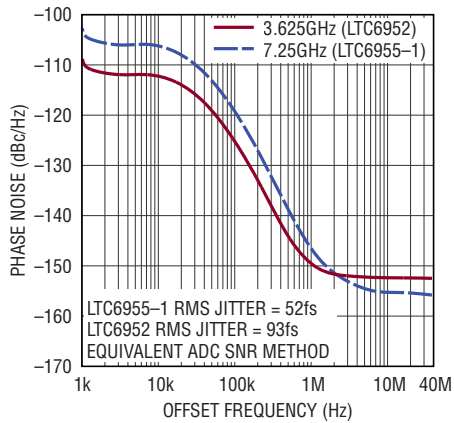
7.50 ±0.05

6.10 ±0.05

5.50 REF
(2 SIDES)

0.70 ±0.05

6.45 ±0.05

6.50 REF
(2 SIDES)

7.10 ±0.05   8.50 ±0.05

5.41 ±0.05

PACKAGE OUTLINE

0.25 ±0.05

0.50 BSC

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

7.00 ±0.10
(2 SIDES)

0.75 ±0.05

0.00 – 0.05

5.50 REF
(2 SIDES)

R = 0.115
TYP

51   52

0.40 ±0.10

1

2

PIN 1 TOP MARK
(SEE NOTE 6)

PIN 1 NOTCH
R = 0.30 TYP OR
0.35 × 45°C
CHAMFER

8.00 ±0.10
(2 SIDES)

6.50 REF
(2 SIDES)

6.45 ±0.10

5.41 ±0.10

R = 0.10
TYP

0.25 ±0.05

0.50 BSC

(UKG52) QFN REV Ø 0306

TOP VIEW

BOTTOM VIEW—EXPOSED PAD

0.75 ±0.05

0.200 REF
0.00 – 0.05

SIDE VIEW

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Rev. 0

TYPICAL APPLICATION

Generation of 4GHz, 52fs ADC SNR Jitter Clocks Using LTC6952 and LTC6955

LTC6955 vs LTC6952 4GHz Phase Noise

LTC6955 RMS JITTER = 52fs
LTC6952 RMS JITTER = 78fs
EQUIVALENT ADC SNR METHOD

PHASE NOISE (dBc/Hz)

LTC6952 (6 OUTPUTS ON)
LTC6955 (ALL OUTPUT ON)

OFFSET FREQUENCY (Hz)

6955 TA03b

FILT
SEL3
SEL2
SEL1
SEL0

10kΩ
3.3V

LTC6955 BUFFER

V_D^+
V_{OUT}^+

3.3V

OUT0±
OUT1±
OUT2±
OUT3±
OUT4±
OUT5±
OUT7±
OUT9±

POWERED DOWN OR ADDITIONAL 4GHZ CLOCKS

/1

OUT6+
OUT6−

100Ω

0.1µF
0.1µF

4GHz CLOCKS

3.3V V_{IN}^+

/1

OUT8+
OUT8−

100Ω

0.1µF
0.1µF

Crystek
CVCO55CC-4000-4000

0.1µF

30Ω

f_{VCO}

0.1µF 75Ω

VTUNE

IN+
IN−

/1

OUT10+
OUT10−

f_{OUT} = 4GHz

160Ω

VCO+
VCO−

3.3V

V_{VCO}^+ V_{REF}^+

OUT0+
OUT0−

100Ω

0.1µF
0.1µF

SYSREF PAIRS TO LTC6955 CLOCKS

48.7Ω

33nF 48.7Ω

1.2µF 0.47µF

22nF

5V

V_{CP}^+
CP

LTC6952

OUT2±

OUT2−

100Ω

0.1µF
0.1µF

1µF 100Ω 1µF

Crystek
CCHD-575-25-100
100MHz Ref Osc

REF+

REF−

49.9Ω

1µF

OUT1±
OUT3±
OUT4±
OUT5±
OUT6±
OUT7±
OUT8±
OUT9±
OUT10±

CAN BE USED AS CLOCKS ≤ 4GHz OR SYSREFS

LTC6952Wizard REGISTER VALUES:
FILE: LTC6952_LTC6955_4GHz

TO SYNC OUTPUTS:
TOGGLE SSYNC REGISTER BIT

EZS_SRQ+

EZS_SRQ−

V_D^+ V_{OUT}^+

3.3V

6955 TA03a

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6952	Ultralow Jitter, 4.5GHz PPL with 11 Outputs and JESD204B Support	PLL with Eleven Independent CML Outputs with Dividers and Delays, 65fs Additive ADC SNR Jitter
LTC6953	Ultralow Jitter, 4.5GHz Clock Distributor with 11 Outputs and JESD204B Support	Eleven Independent CML Outputs with Dividers and Delays, 65fs Additive ADC SNR Jitter
LTC6945/ LTC6946	Ultralow Noise and Spurious Integer-N Synthesizers	370MHz to 6.39GHz, −226dBc/Hz Normalized In-Band Phase Noise Floor, −157dBc/Hz Wideband Output Phase Noise Floor
LTC6947/ LTC6948	Ultralow Noise and Spurious Frac-N Synthesizers	350MHz to 6.39GHz, −226dBc/Hz Normalized In-Band Phase Noise Floor, −157dBc/Hz Wideband Output Phase Noise Floor
LTC6950	1.4GHz Low Phase Noise, Low Jitter PLL with Clock Distribution	Four Independent LVPECL Outputs with 18fsRMS Additive Jitter (12kHz to 20MHz)
LTC6951	Ultralow Jitter Multioutput Clock Synthesizer with Integrated VCO	Four Independent CML Outputs and One LVDS Output, Integrated VCO, 110fs ADC SNR Jitter
LTC6954	Low Phase Noise, Triple Output Clock Distribution Divider/Driver	LVPECL, LVDS and CMOS Outputs with <20fsRMS Additive Jitter (12kHz to 20MHz)

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