

16-Channel μ Module PMBus Power System Manager

FEATURES

- Sequence, Trim, Margin and Supervise 16 Power Supplies
- Manage Faults, Monitor Telemetry and Create Fault Logs
- PMBus™ Compliant Command Set
- Supported by LTpowerPlay® GUI
- Margin or Trim Supplies to Within 0.25% of Target
- Fast OV/UV Supervisors Per Channel
- Coordinate Sequencing and Fault Management Across Multiple LTC PSM Devices
- Automatic Fault Logging to Internal EEPROM
- Operate Autonomously without Additional Software
- Internal Temperature and Input Voltage Supervisors
- Accurate Monitoring of 16 Output Voltages, Two Input Voltages and Internal Die Temperature
- I²C/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Programmable Watchdog Timer
- Available in 144-Pin 15mm × 15mm BGA Package

APPLICATIONS

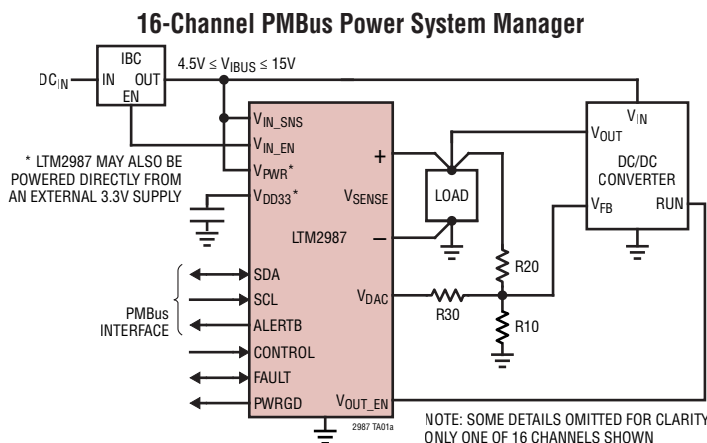
- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

DESCRIPTION

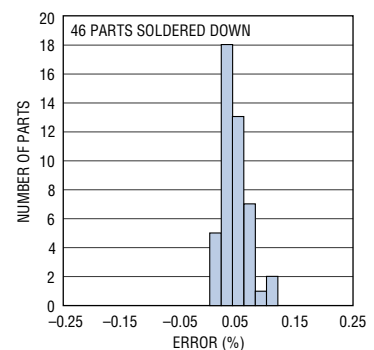
The LTM[®]2987 is a 16-channel μ Module[®] (micromodule) Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include overvoltage and undervoltage threshold limits for sixteen power supply output channels and two power supply input channels, as well as over and under temperature limits. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors sixteen output voltages, two input voltages, and die temperature. In addition, odd numbered channels can be configured to measure the voltage across a current sense resistor. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

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TYPICAL APPLICATION



Power Supply Accuracy



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

Supply Voltages:

| | |
|---------------------|----------------|
| V_{PWR} | -0.3V to 15V |
| V_{IN_SNS} | -0.3V to 15V |
| V_{DD33} | -0.3V to 3.6V |
| V_{DD25} | -0.3V to 2.75V |

Digital Input/Output Voltages:

| | |
|--|----------------------------|
| ALERTB, SDA, SCL, CONTROL0, CONTROL1..... | -0.3V to 5.5V |
| PWRGD, SHARE_CLK, WDI/RESETB, WP..... | -0.3V to $V_{DD33} + 0.3V$ |
| FAULTB00, FAULTB01, FAULTB10, FAULTB11..... | -0.3V to $V_{DD33} + 0.3V$ |
| ASELO, ASEL1..... | -0.3V to $V_{DD33} + 0.3V$ |

Analog Voltages:

| | |
|---|----------------|
| REFP..... | -0.3V to 1.35V |
| REFM..... | -0.3V to 0.3V |
| $V_{SENSE}[7:0]$ | -0.3V to 6V |
| $V_{SENSEM}[7:0]$ | -0.3V to 6V |
| $V_{OUT_EN}[3:0]$, V_{IN_EN} | -0.3V to 15V |
| $V_{OUT_EN}[7:4]$ | -0.3V to 6V |
| $V_{DACP}[7:0]$ | -0.3V to 6V |
| $V_{DACM}[7:0]$ | -0.3V to 0.3V |

Pull-Up Resistors:

| | |
|---|---------------|
| V_{PU} | -0.3V to 5.5V |
| R_{PU1} , R_{PU2} , R_{PU3} , R_{PU4} | -0.3V to 5.5V |

Operating Junction Temperature Range:

| | |
|---------------|----------------|
| LTM2987C..... | 0°C to 70°C |
| LTM2987I..... | -40°C to 105°C |

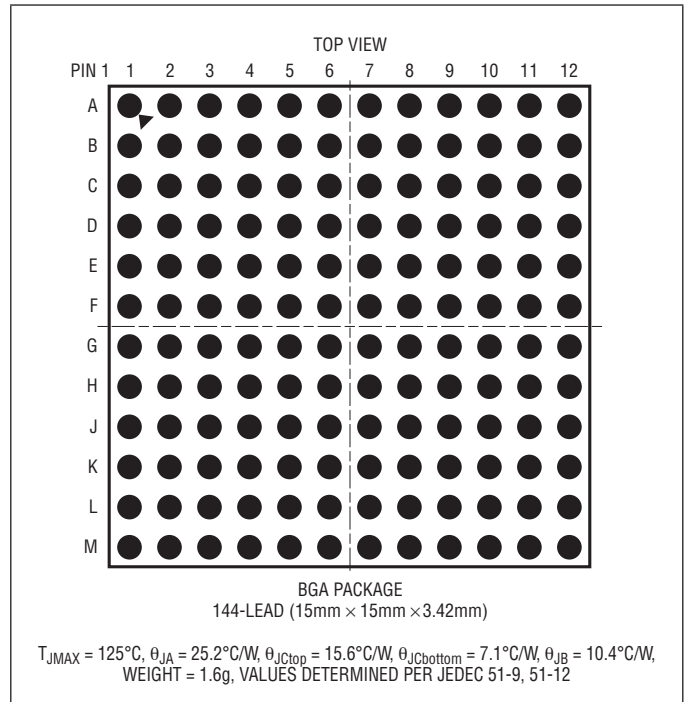
Storage Temperature Range..... -55°C to 125°C*

Maximum Junction Temperature..... 125°C*

Maximum Solder Temperature..... 250°C

*See OPERATION section of the LTC2977 data sheet for detailed EEPROM derating information for junction temperatures in excess of 105°C.

PIN CONFIGURATION



ORDER INFORMATION <http://www.linear.com/product/LTM2987#orderinfo>

| PART NUMBER | PAD OR BALL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | OPERATING JUNCTION TEMPERATURE RANGE |
|---------------|--------------------|---------------|-------------|--------------|------------|--------------------------------------|
| | | DEVICE | FINISH CODE | | | |
| LTM2987CY#PBF | SAC305 (RoHS) | LTM2987Y | e1 | BGA | 3 | 0°C to 70°C |
| LTM2987IY#PBF | SAC305 (RoHS) | LTM2987Y | e1 | BGA | 3 | -40°C to 105°C |

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

• Terminal Finish Part Marking:
www.linear.com/leadfree

• Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:

www.linear.com/umodule/pcbassembly

• LGA and BGA Package and Tray Drawings:
www.linear.com/packaging

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25^\circ\text{C}$. $V_{PWR} = V_{IN_SNS} = 12\text{V}$, V_{DD33} , REFP and REFM pins floating, unless otherwise indicated. (Notes 2, 3)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|--|--|-------|---------------------------------------|------------|--|----|
| Power Supply Characteristics | | | | | | | |
| V_{PWR} | V_{PWR} Supply Input Operating Range | | ● 4.5 | | 15 | V | |
| I_{PWR} | V_{PWR} Supply Current | $4.5\text{V} \leq V_{PWR} \leq 15\text{V}$, V_{DD33} Floating | ● | 10 | 13 | mA | |
| I_{VDD33} | V_{DD33} Supply Current | $3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$, $V_{PWR} = V_{DD33}$ | ● | 10 | 13 | mA | |
| V_{UVLO_VDD33} | V_{DD33} Undervoltage Lockout | V_{DD33} Ramping Up, $V_{PWR} = V_{DD33}$ | ● | 2.35 | 2.55 | 2.8 | V |
| | V_{DD33} Undervoltage Lockout Hysteresis | | | 120 | | | mV |
| V_{DD33} | Supply Input Operating Range | $V_{PWR} = V_{DD33}$ | ● | 3.13 | | 3.47 | V |
| | Regulator Output Voltage | $4.5\text{V} \leq V_{PWR} \leq 15\text{V}$ | ● | 3.13 | 3.26 | 3.47 | V |
| | Regulator Output Short-Circuit Current | $V_{PWR} = 4.5\text{V}$, $V_{DD33} = 0\text{V}$ | ● | 75 | 90 | 140 | mA |
| V_{DD25} | Regulator Output Voltage | $3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$ | ● | 2.35 | 2.5 | 2.6 | V |
| | Regulator Output Short-Circuit Current | $V_{PWR} = V_{DD33} = 3.47\text{V}$, $V_{DD25} = 0\text{V}$ | ● | 30 | 55 | 80 | mA |
| t_{INIT} | Initialization Time | Time from V_{IN} Applied Until the TON_DELAY Timer Starts | | 30 | | ms | |
| Voltage Reference Characteristics | | | | | | | |
| V_{REF} | Output Voltage | (Note 4) | | 1.232 | | V | |
| | Temperature Coefficient | | | 3 | | ppm/ $^\circ\text{C}$ | |
| | Hysteresis | (Note 5) | | 100 | | ppm | |
| ADC Characteristics | | | | | | | |
| V_{IN_ADC} | Voltage Sense Input Range | Differential Voltage: $V_{IN_ADC} = (V_{SENSEPN} - V_{SENSEMN})$ | ● | 0 | 6 | V | |
| | | Single-Ended Voltage: $V_{SENSEMN}$ | ● | -0.1 | 0.1 | V | |
| | Current Sense Input Range (Odd Numbered Channels Only) | Single-Ended Voltage: $V_{SENSEPN}$, $V_{SENSEMN}$ | ● | -0.1 | 6 | V | |
| | | Differential Voltage: V_{IN_ADC} | ● | -170 | 170 | mV | |
| N_{ADC} | Voltage Sense Resolution (Uses L16 Format) | $0\text{V} \leq V_{IN_ADC} \leq 6\text{V}$ Mfr_config_adc_hires = 0 | | 122 | | $\mu\text{V}/\text{LSB}$ | |
| | Current Sense Resolution (Odd Numbered Channels Only) | $0\text{mV} \leq V_{IN_ADC} < 16\text{mV}$ (Note 6) $16\text{mV} \leq V_{IN_ADC} < 32\text{mV}$ $32\text{mV} \leq V_{IN_ADC} < 63.9\text{mV}$ $63.9\text{mV} \leq V_{IN_ADC} < 127.9\text{mV}$ $127.9\text{mV} \leq V_{IN_ADC} $ Mfr_config_adc_hires = 1 | | 15.625 31.25 62.5 125 250 | | $\mu\text{V}/\text{LSB}$ $\mu\text{V}/\text{LSB}$ $\mu\text{V}/\text{LSB}$ $\mu\text{V}/\text{LSB}$ $\mu\text{V}/\text{LSB}$ | |
| $TUE_ADC_VOLT_SNS$ | Total Unadjusted Error (Note 4) | Voltage Sense Mode $V_{IN_ADC} \geq 1\text{V}$ | ● | | ± 0.25 | % of Reading | |
| | | Voltage Sense Mode $0 \leq V_{IN_ADC} \leq 1\text{V}$ | ● | | ± 2.5 | mV | |
| $TUE_ADC_CURR_SNS$ | Total Unadjusted Error (Note 4) | Current Sense Mode, Odd Numbered Channels Only, $20\text{mV} \leq V_{IN_ADC} \leq 170\text{mV}$ | ● | | ± 0.7 | % of Reading | |
| | | Current Sense Mode, Odd Numbered Channels Only, $V_{IN_ADC} \leq 20\text{mV}$ | ● | | ± 140 | μV | |
| V_{OS_ADC} | Offset Error | Current Sense Mode, Odd Numbered Channels Only | ● | | ± 35 | μV | |
| t_{CONV_ADC} | Conversion Time | Voltage Sense Mode (Note 7) | | 6.15 | | ms | |
| | | Current Sense Mode (Note 7) | | 24.6 | | ms | |
| | | Temperature Input (Note 7) | | 24.6 | | ms | |

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25^\circ\text{C}$. $V_{PWR} = V_{IN_SNS} = 12\text{V}$, V_{DD33} , REFP and REFM pins floating, unless otherwise indicated. (Notes 2, 3)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------|----------------------------|---|-----|------|-----------|---------------|
| t_{UPDATE_ADC} | Update Time | Odd Numbered Channels in Current Sense Mode (Note 7) | | 160 | | ms |
| C_{IN_ADC} | Input Sampling Capacitance | | | 1 | | pF |
| f_{IN_ADC} | Input Sampling Frequency | | | 62.5 | | kHz |
| I_{IN_ADC} | Input Leakage Current | $V_{IN_ADC} = 0\text{V}$, $0\text{V} \leq V_{COMMONMODE} \leq 6\text{V}$, Current Sense Mode | ● | | ± 0.5 | μA |
| | Differential Input Current | $V_{IN_ADC} = 0.17\text{V}$, Current Sense Mode | ● | 80 | 250 | nA |
| | | $V_{IN_ADC} = 6\text{V}$, Voltage Sense Mode | ● | 10 | 15 | μA |

DAC Output Characteristics

| | | | | | | | | |
|----------------------------|---|---|-----------------------|-----|-----|---------------|--------|---|
| N_{VDACP} | Resolution | | | 10 | | Bits | | |
| V_{FS_VDACP} | Full-Scale Output Voltage (Programmable) | DAC Code = 0x3FF | Buffer Gain Setting_0 | ● | 1.3 | 1.38 | 1.44 | V |
| | | DAC Polarity = 1 | Buffer Gain Setting_1 | ● | 2.5 | 2.65 | 2.77 | V |
| INL_VDACP | Integral Nonlinearity | (Note 8) | ● | | | ± 2 | LSB | |
| DNL_VDACP | Differential Nonlinearity | (Note 8) | ● | | | ± 2.4 | LSB | |
| V_{OS_VDACP} | Offset Voltage | (Note 8) | ● | | | ± 10 | mV | |
| V_{DACP} | Load Regulation ($V_{DACPn} - V_{DACMn}$) | $V_{DACPn} = 2.65\text{V}$, I_{VDACPn} Sourcing = 2mA | | | 100 | | ppm/mA | |
| | | $V_{DACPn} = 0.1\text{V}$, I_{VDACPn} Sinking = 2mA | | | 100 | | ppm/mA | |
| | PSRR ($V_{DACPn} - V_{DACMn}$) | DC: $3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$, $V_{PWR} = V_{DD33}$ | | | 60 | | dB | |
| | | 100mV Step in 20ns with 50pF Load | | | 40 | | dB | |
| | DC CMRR ($V_{DACPn} - V_{DACMn}$) | $-0.1\text{V} \leq V_{DACMn} \leq 0.1\text{V}$ | | | 60 | | dB | |
| | Leakage Current | V_{DACPn} Hi-Z, $0\text{V} \leq V_{DACPn} \leq 6\text{V}$ | ● | | | ± 100 | nA | |
| | Short-Circuit Current Low | V_{DACPn} Shorted to GND | ● | -10 | | -4 | mA | |
| Short-Circuit Current High | V_{DACPn} Shorted to V_{DD33} | ● | 4 | | 10 | mA | | |
| C_{OUT} | Output Capacitance | V_{DACPn} Hi-Z | | 10 | | pF | | |
| t_{S_VDACP} | DAC Output Update Rate | Fast Servo Mode | | 500 | | μs | | |

DAC Soft-Connect Comparator Characteristics

| | | | | | | |
|---------------|----------------|----------------------------|---|---------|----------|----|
| V_{OS_CMP} | Offset Voltage | $V_{DACPn} = 0.2\text{V}$ | ● | ± 1 | ± 18 | mV |
| | | $V_{DACPn} = 1.3\text{V}$ | ● | ± 2 | ± 26 | mV |
| | | $V_{DACPn} = 2.65\text{V}$ | ● | ± 3 | ± 52 | mV |

Voltage Supervisor Characteristics

| | | | | | | | |
|--------------|------------------------------------|---|----------------------|-------|-----|---------------|--------------|
| V_{IN_VS} | Input Voltage Range (Programmable) | $V_{IN_VS} = (V_{SENSEn} - V_{SENSEMn})$ | Low Resolution Mode | ● | 0 | 6 | V |
| | | | High Resolution Mode | ● | 0 | 3.8 | V |
| | | Single-Ended Voltage: $V_{SENSEMn}$ | ● | -0.1 | 0.1 | V | |
| N_VS | Voltage Sensing Resolution | 0V to 3.8V Range: High Resolution Mode | | | 4 | | mV/LSB |
| | | 0V to 6V Range: Low Resolution Mode | | | 8 | | mV/LSB |
| TUE_VS | Total Unadjusted Error | $2\text{V} \leq V_{IN_VS} \leq 6\text{V}$, Low Resolution Mode | ● | | | ± 1.25 | % of Reading |
| | | $1.5\text{V} < V_{IN_VS} \leq 3.8\text{V}$, High Resolution Mode | ● | | | ± 1.0 | % of Reading |
| | | $0.8\text{V} \leq V_{IN_VS} \leq 1.5\text{V}$, High Resolution Mode | ● | | | ± 1.5 | % of Reading |
| t_{S_VS} | Update Period | | | 12.21 | | μs | |

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25^\circ\text{C}$. $V_{PWR} = V_{IN_SNS} = 12\text{V}$, V_{DD33} , REFP and REFM pins floating, unless otherwise indicated. (Notes 2, 3)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--|---|---|--------|---------|-----------|------------------|
| V_{IN_SNS} Input Characteristics | | | | | | | |
| V_{IN_SNS} | V_{IN_SNS} Input Voltage Range | | ● | 0 | | 15 | V |
| R_{VIN_SNS} | V_{IN_SNS} Input Resistance | | ● | 70 | 90 | 110 | k Ω |
| TUE_{VIN_SNS} | VIN_ON, VIN_OFF Threshold Total Unadjusted Error | $3\text{V} \leq V_{VIN_SNS} \leq 8\text{V}$ | ● | | | ± 2.0 | % of Reading |
| | | $V_{VIN_SNS} > 8\text{V}$ | ● | | | ± 1.0 | % of Reading |
| | READ_VIN Total Unadjusted Error | $3\text{V} \leq V_{VIN_SNS} \leq 8\text{V}$ | ● | | | ± 1.5 | % of Reading |
| | | $V_{VIN_SNS} > 8\text{V}$ | ● | | | ± 1.0 | % of Reading |
| Temperature Sensor Characteristics | | | | | | | |
| TUE_{TS} | Total Unadjusted Error | | | | ± 1 | | $^\circ\text{C}$ |
| V_{OUT_EN} Output (V_{OUT_EN} [3:0]) Characteristics | | | | | | | |
| V_{VOUT_ENn} | Output High Voltage (Note 9) | $I_{VOUT_ENn} = -5\mu\text{A}$, $V_{DD33} = 3.3\text{V}$ | ● | 10 | 12.5 | 14.7 | V |
| I_{VOUT_ENn} | Output Sourcing Current | V_{VOUT_ENn} Pull-Up Enabled, $V_{VOUT_ENn} = 1\text{V}$ | ● | -5 | -6 | -8 | μA |
| | Output Sinking Current | Strong Pull-Down Enabled, $V_{VOUT_ENn} = 0.4\text{V}$ | ● | 3 | 5 | 8 | mA |
| | | Weak Pull-Down Enabled, $V_{VOUT_ENn} = 0.4\text{V}$ | ● | 33 | 50 | 60 | μA |
| | Output Leakage Current | Internal Pull-Up Disabled, $0\text{V} \leq V_{VOUT_ENn} \leq 15\text{V}$ | ● | | | ± 1 | μA |
| V_{OUT_EN} Output (V_{OUT_EN} [7:4]) Characteristics | | | | | | | |
| I_{VOUT_ENn} | Output Sinking Current | Strong Pull-Down Enabled, $V_{OUT_ENn} = 0.1\text{V}$ | ● | 3 | 6 | 9 | mA |
| | Output Leakage Current | $0\text{V} \leq V_{VOUT_ENn} \leq 6\text{V}$ | ● | | | ± 1 | μA |
| V_{IN_EN} Enable Output (V_{IN_EN}) Characteristics | | | | | | | |
| V_{VIN_EN} | Output High Voltage | $I_{VIN_EN} = -5\mu\text{A}$, $V_{DD33} = 3.3\text{V}$ | ● | 10 | 12.5 | 14.7 | V |
| I_{VIN_EN} | Output Sourcing Current | V_{IN_EN} Pull-Up Enabled, $V_{VIN_EN} = 1\text{V}$ | ● | -5 | -6 | -8 | μA |
| | Output Sinking Current | $V_{VIN_EN} = 0.4\text{V}$ | ● | 3 | 5 | 8 | mA |
| | Leakage Current | Internal Pull-Up Disabled, $0\text{V} \leq V_{VIN_EN} \leq 15\text{V}$ | ● | | | ± 1 | μA |
| EEPROM Characteristics | | | | | | | |
| Endurance | (Notes 10, 11) | $0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations | ● | 10,000 | | | Cycles |
| Retention | (Notes 10, 11) | $T_J < 105^\circ\text{C}$ | ● | 20 | | | Years |
| t_{MASS_WRITE} | Mass Write Operation Time (Note 12) | STORE_USER_ALL, $0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations | ● | | 440 | 4100 | ms |
| General Purpose Pull-Up Resistors | | | | | | | |
| R_{PU} | Pull-Up Resistance | | | | 10 | | k Ω |
| Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP | | | | | | | |
| V_{IH} | High Level Input Voltage | | ● | 2.1 | | | V |
| V_{IL} | Low Level Input Voltage | | ● | | | 1.5 | V |
| V_{HYST} | Input Hysteresis | | | | 20 | | mV |

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25^\circ\text{C}$. $V_{PWR} = V_{IN_SNS} = 12\text{V}$, V_{DD33} , REFP and REFM pins floating, unless otherwise indicated. (Notes 2, 3)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------|---|---|-----|-----|-----|-------|
| I_{LEAK} | Input Leakage Current | $0\text{V} \leq V_{PIN} \leq 5.5\text{V}$, SDA, SCL, CONTROL n Pins Only | ● | | ±2 | μA |
| | | $0\text{V} \leq V_{PIN} \leq V_{DD33} + 0.3\text{V}$, FAULTBzn, WDI/RESETB, WP Pins Only | ● | | ±2 | μA |
| t_{SP} | Pulse Width of Spike Suppressed | FAULTBzn, CONTROL n Pins Only | | 10 | | μs |
| | | SDA, SCL Pins Only | | 98 | | ns |
| t_{FAULT_MIN} | Minimum Low Pulse Width for Externally Generated Faults | | 110 | | | ms |
| t_{RESETB} | Pulse Width to Assert Reset | $V_{WDI/RESETB} \leq 1.5\text{V}$ | ● | 300 | | μs |
| t_{WDI} | Pulse Width to Reset Watchdog Timer | $V_{WDI/RESETB} \leq 1.5\text{V}$ | ● | 0.3 | 200 | μs |
| f_{WDI} | Watchdog Interrupt Input Frequency | | ● | | 1 | MHz |
| C_{IN} | Digital Input Capacitance | | | 10 | | pF |

Digital Input SHARE_CLK

| | | | | | | |
|----------------------|---------------------------------|--|---|-------|-----|-----|
| V_{IH} | High Level Input Voltage | | ● | 1.6 | | V |
| V_{IL} | Low Level Input Voltage | | ● | | 0.8 | V |
| $f_{SHARE_CLK_IN}$ | Input Frequency Operating Range | | ● | 90 | 110 | kHz |
| t_{LOW} | Assertion Low Time | $V_{SHARE_CLK} < 0.8\text{V}$ | ● | 0.825 | 1.1 | μs |
| t_{RISE} | Rise Time | $V_{SHARE_CLK} < 0.8\text{V}$ to $V_{SHARE_CLK} > 1.6\text{V}$ | ● | | 450 | ns |
| I_{LEAK} | Input Leakage Current | $0\text{V} \leq V_{SHARE_CLK} \leq V_{DD33} + 0.3\text{V}$ | ● | | ±1 | μA |
| C_{IN} | Input Capacitance | | | 10 | | pF |

Digital Outputs SDA, ALERTB, PWRGD, SHARE_CLK, FAULTB00, FAULTB01, FAULTB10, FAULTB11

| | | | | | | | |
|-----------------------|----------------------------------|------------------------------|---|----|-----|-----|-----|
| V_{OL} | Digital Output Low Voltage | $I_{SINK} = 3\text{mA}$ | ● | | 0.4 | V | |
| $f_{SHARE_CLK_OUT}$ | Output Frequency Operating Range | 5.49kΩ Pull-Up to V_{DD33} | ● | 90 | 100 | 110 | kHz |

Digital Inputs ASELO,ASEL1

| | | | | | | |
|------------------|------------------------------|---------------------------|---|------------------|-----|----|
| V_{IH} | Input High Threshold Voltage | | ● | $V_{DD33} - 0.5$ | | V |
| V_{IL} | Input Low Threshold Voltage | | ● | | 0.5 | V |
| I_{IH}, I_{IL} | High, Low Input Current | $ASEL[1:0] = 0, V_{DD33}$ | ● | | ±95 | μA |
| I_{HIZ} | Hi-Z Input Current | | ● | | ±24 | μA |
| C_{IN} | Input Capacitance | | | 10 | | pF |

Serial Bus Timing Characteristics

| | | | | | | |
|---------------|--|--|---|-----|-----|-----|
| f_{SCL} | Serial Clock Frequency (Note 13) | | ● | 10 | 400 | kHz |
| t_{LOW} | Serial Clock Low Period (Note 13) | | ● | 1.3 | | μs |
| t_{HIGH} | Serial Clock High Period (Note 13) | | ● | 0.6 | | μs |
| t_{BUF} | Bus Free Time Between Stop and Start (Note 13) | | ● | 1.3 | | μs |
| t_{HD_STA} | Start Condition Hold Time (Note 13) | | ● | 600 | | ns |
| t_{SU_STA} | Start Condition Setup Time (Note 13) | | ● | 600 | | ns |
| t_{SU_STO} | Stop Condition Setup Time (Note 13) | | ● | 600 | | ns |
| t_{HD_DAT} | Data Hold Time (LTM2987 Receiving Data) (Note 13) | | ● | 0 | | ns |
| | Data Hold Time (LTM2987 Transmitting Data) (Note 13) | | ● | 300 | 900 | ns |

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25^\circ\text{C}$. $V_{\text{PWR}} = V_{\text{IN_SNS}} = 12\text{V}$, V_{DD33} , REFP and REFM pins floating, unless otherwise indicated. (Notes 2, 3)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|---|---|-------|-----|-----|-------|
| $t_{\text{SU,DAT}}$ | Data Setup Time (Note 13) | | ● 100 | | | ns |
| t_{SP} | Pulse Width of Spike Suppressed (Note 13) | | | 98 | | ns |
| $t_{\text{TIMEOUT_BUS}}$ | Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated | Mfr_config_all_longer_pmbus_timeout = 0 | ● | 25 | 35 | ms |
| | | Mfr_config_all_longer_pmbus_timeout = 1 | ● | 200 | 280 | ms |

Additional Digital Timing Characteristics

| | | | | | | |
|-----------------------|----------------------------------|--|--|-----|--|----|
| $t_{\text{OFF_MIN}}$ | Minimum Off Time for Any Channel | | | 100 | | ms |
|-----------------------|----------------------------------|--|--|-----|--|----|

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: The LTM2987 electrical characteristics apply to each half of the device, unless otherwise noted. The specifications and functions are the same for both Device A pins and Device B pins.

Note 4: The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage (V_{REF}) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high-resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

Note 5: Hysteresis in the output voltage is created by package stress that differs depending on whether the module was previously at a higher or lower temperature. Output voltage is always measured at 25°C , but the module is cycled to 105°C or -40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 6: The current sense resolution is determined by the L11 format and the mV units of the returned value. For example a full scale value of 170mV returns a L11 value of $0x\text{F2A8} = 680 \cdot 2^{-2} = 170$. This is the lowest range

that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is $2^{-2} \text{ mV} = 250\mu\text{V}$. Each successively lower range improves resolution by cutting the LSB size in half.

Note 7: The time between successive ADC conversions (latency of the ADC) for any given channel is given as: $36.9\text{ms} + (6.15\text{ms} \cdot \text{number of ADC channels configured in Low Resolution mode}) + (24.6\text{ms} \cdot \text{number of ADC channels configured in High Resolution mode})$.

Note 8: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 9: Output enable pins are charge pumped from V_{DD33} .

Note 10: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 11: EEPROM endurance and retention will be degraded when $T_J > 105^\circ\text{C}$.

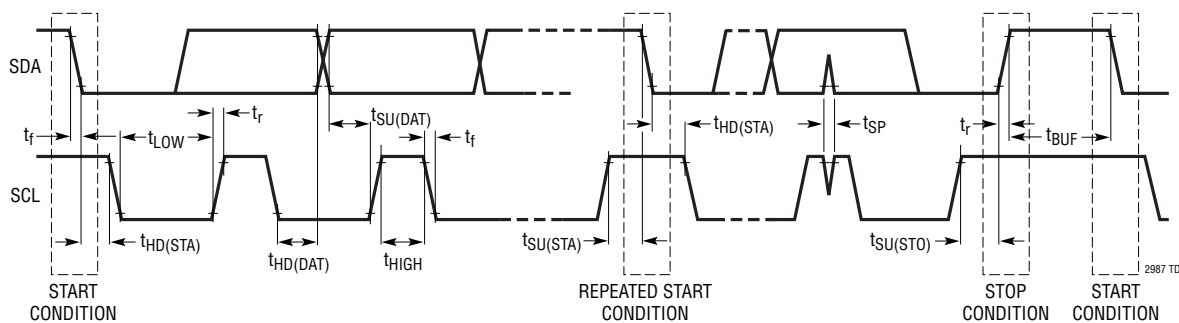
Note 12: The LTM2987 will not acknowledge any PMBus commands while a mass write operation is being executed. This includes the STORE_USER_ALL and MFR_FAULT_LOG_STORE commands or a fault log store initiated by a channel faulting off.

Note 13: Maximum capacitive load, C_B , for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are:

$$(20 + 0.1 \cdot C_B) \text{ (ns)} < t_r < 300\text{ns} \text{ and } (20 + 0.1 \cdot C_B) \text{ (ns)} < t_f < 300\text{ns}.$$

C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO} , is $3.13\text{V} < V_{\text{IO}} < 5.5\text{V}$.

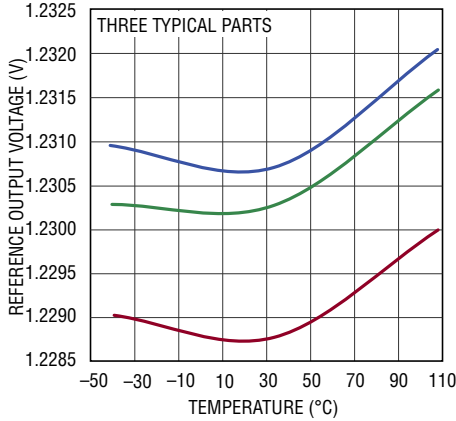
PMBUS TIMING DIAGRAM



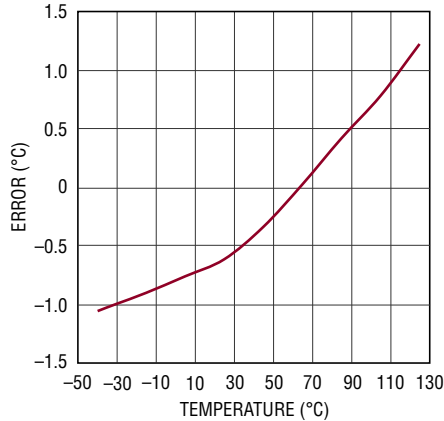
2987fa

TYPICAL PERFORMANCE CHARACTERISTICS

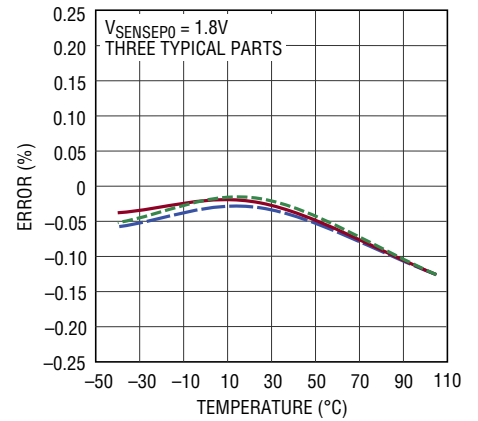
Reference Voltage vs Temperature



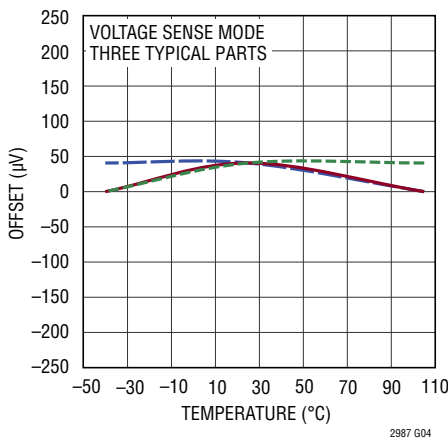
Temperature Sensor Error vs Temperature



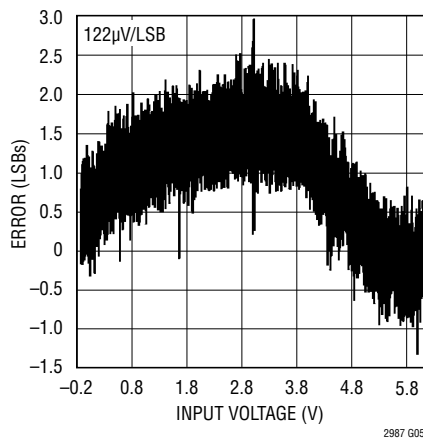
ADC Total Unadjusted Error vs Temperature



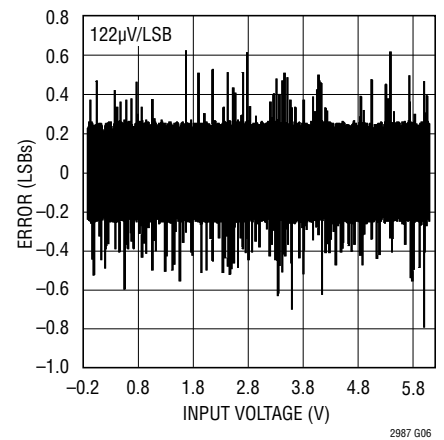
ADC Zero Code Center Offset Voltage vs Temperature



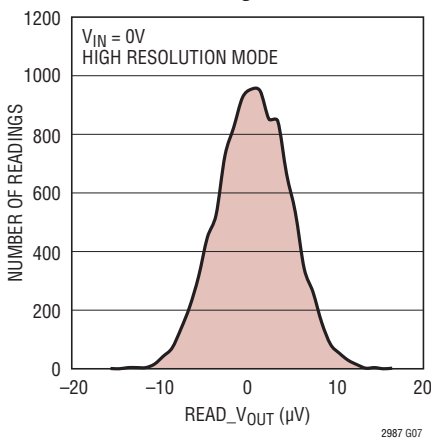
ADC INL



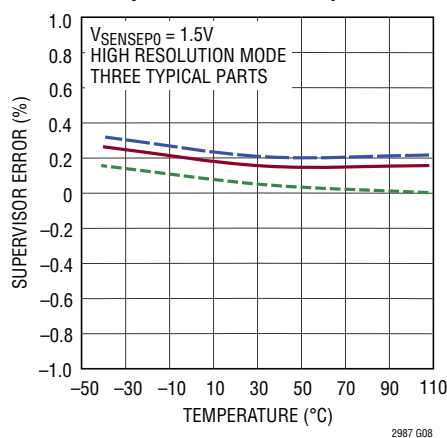
ADC DNL



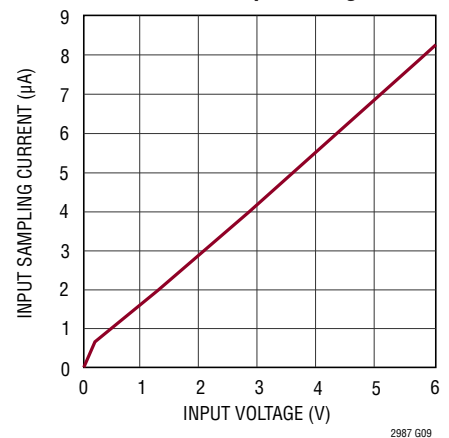
ADC Noise Histogram



Voltage Supervisor Total Unadjusted Error vs Temperature

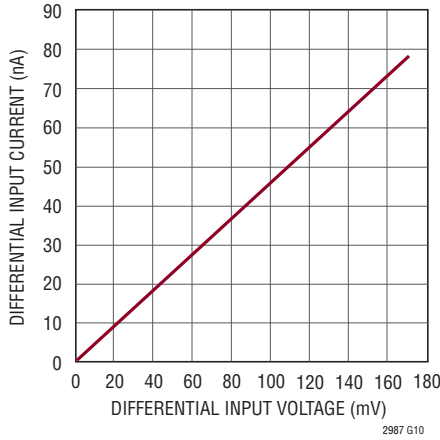


Input Sampling Current vs Differential Input Voltage

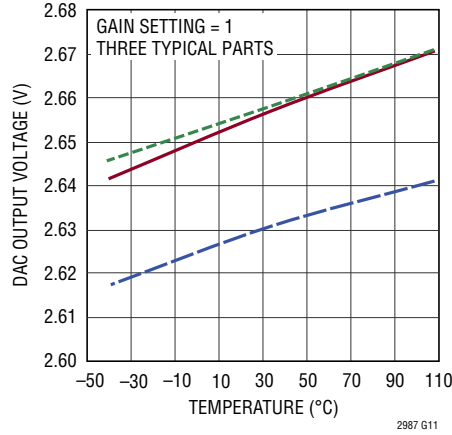


TYPICAL PERFORMANCE CHARACTERISTICS

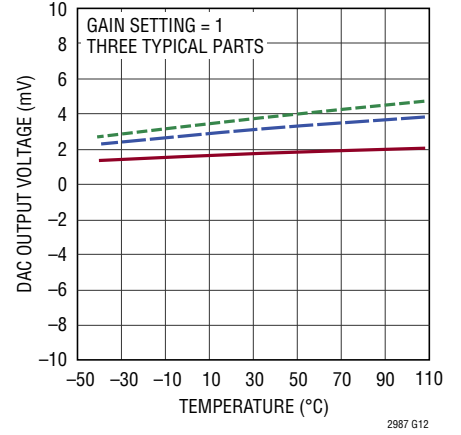
**ADC High Resolution Mode
Differential Input Current**



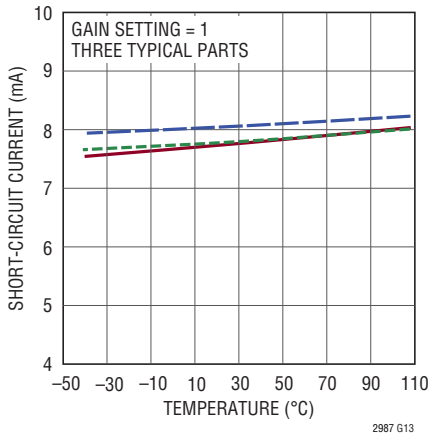
**DAC Full-Scale Output Voltage vs
Temperature**



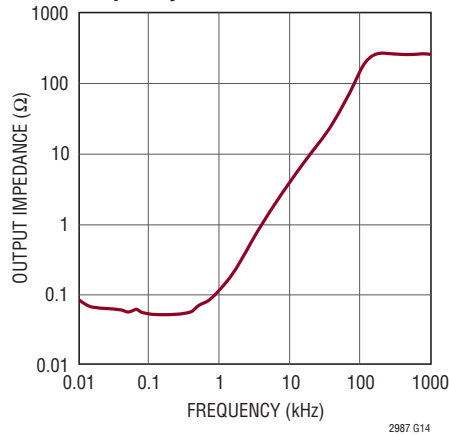
**DAC Offset Voltage vs
Temperature**



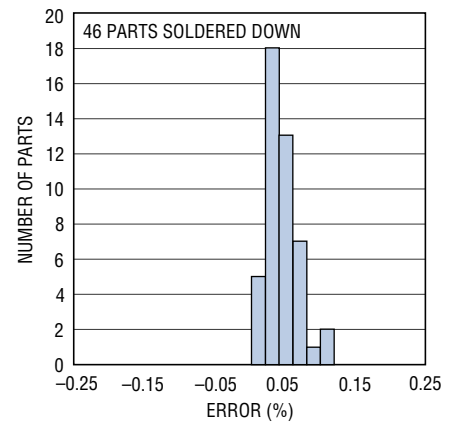
**DAC Short-Circuit Current vs
Temperature**



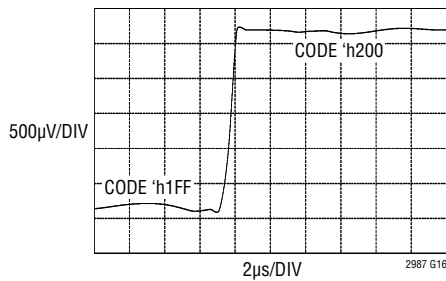
**DAC Output Impedance vs
Frequency**



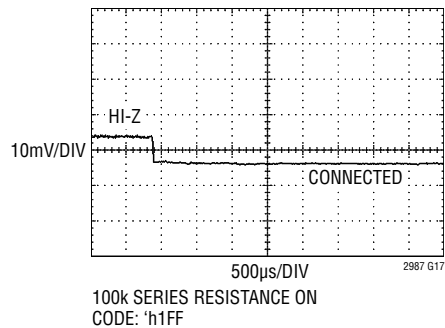
Closed-Loop Servo Error



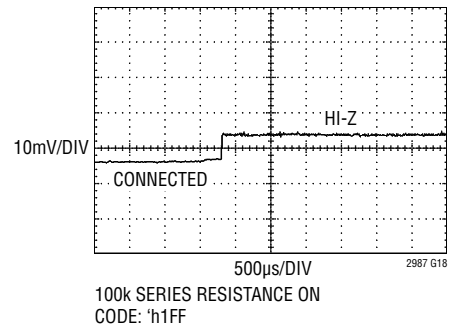
**DAC Transient Response to 1LSB
DAC Code Change**



**DAC Soft-Connect Transient
Response When Transitioning
from Hi-Z State to ON State**

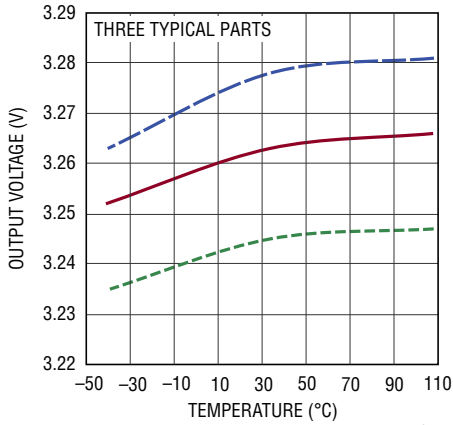


**DAC Soft-Connect Transient
Response When Transitioning
from ON State to Hi-Z State**

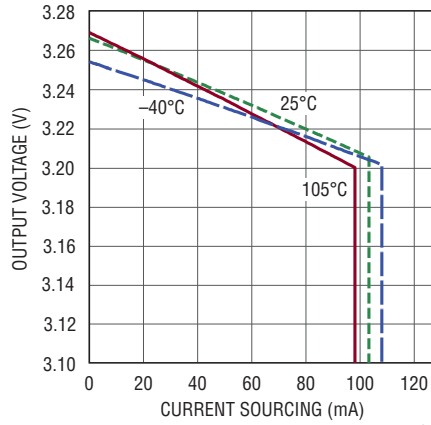


TYPICAL PERFORMANCE CHARACTERISTICS

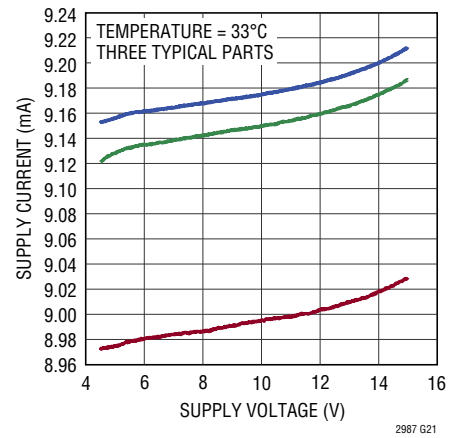
V_{DD33} Regulator Output Voltage vs Temperature



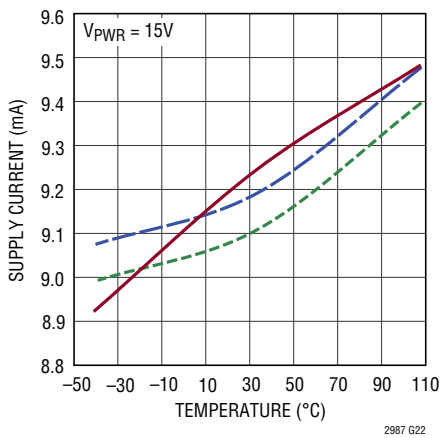
V_{DD33} Regulator Load Regulation



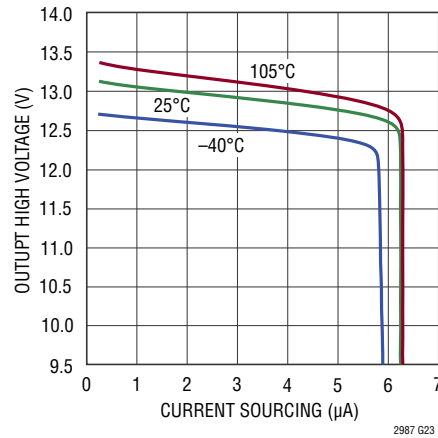
Supply Current vs Supply Voltage (1/2 LTM2987)



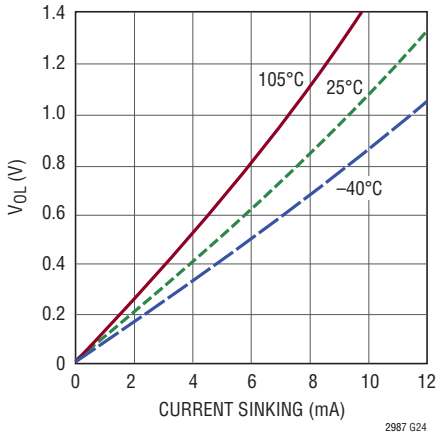
Supply Current vs Temperature (1/2 LTM2987)



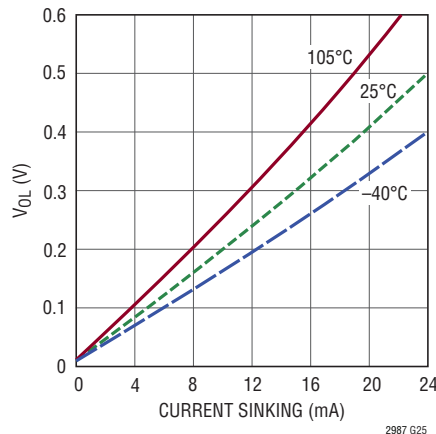
V_{OUT_EN[3:0]} and V_{IN_EN} Output High Voltage vs Current



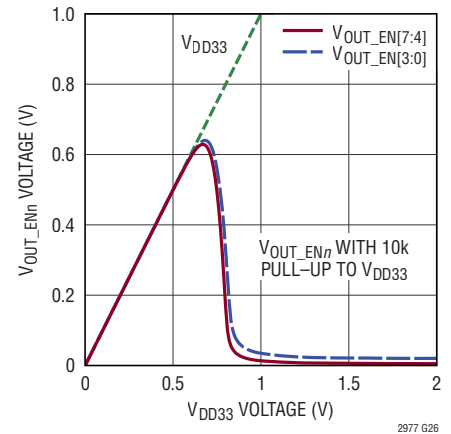
V_{OUT_EN[3:0]} and V_{IN_EN} Output V_{OL} vs Current



V_{OUT_EN[7:4]} V_{OL} vs Current



V_{OUT_EN[7:0]} Output Voltage vs V_{DD33}



PIN FUNCTIONS

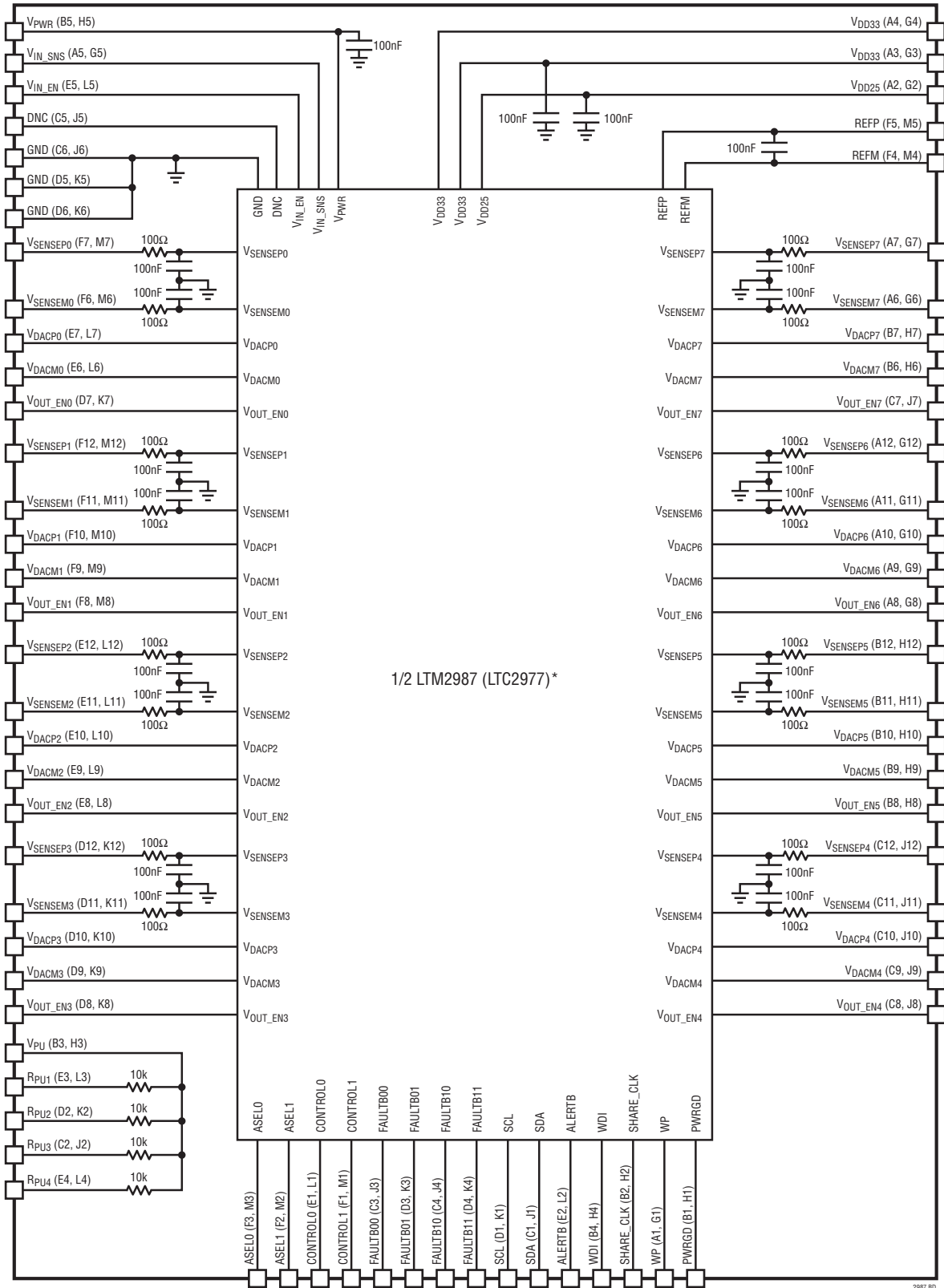
| PIN NAME | PIN | | PIN TYPE | DESCRIPTION |
|-----------------------|----------|----------|----------|---|
| | Device A | Device B | | |
| V _{SENSE} P0 | F7* | M7* | In | DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin |
| V _{SENSE} M0 | F6* | M6* | In | DC/DC Converter Differential (-) Output Voltage-0 Sensing Pin |
| V _{SENSE} P1 | F12* | M12* | In | DC/DC Converter Differential (+) Output Voltage or Current-1 Sensing Pins. |
| V _{SENSE} M1 | F11* | M11* | In | DC/DC Converter Differential (-) Output Voltage or Current-1 Sensing Pins. |
| V _{SENSE} P2 | E12* | L12* | In | DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin |
| V _{SENSE} M2 | E11* | L11* | In | DC/DC Converter Differential (-) Output Voltage-2 Sensing Pin |
| V _{SENSE} P3 | D12* | K12* | In | DC/DC Converter Differential (+) Output Voltage or Current-3 Sensing Pins. |
| V _{SENSE} M3 | D11* | K11* | In | DC/DC Converter Differential (-) Output Voltage or Current-3 Sensing Pins. |
| V _{SENSE} P4 | C12* | J12* | In | DC/DC Converter Differential (+) Output Voltage-4 Sensing Pin |
| V _{SENSE} M4 | C11* | J11* | In | DC/DC Converter Differential (-) Output Voltage-4 Sensing Pin |
| V _{SENSE} P5 | B12* | H12* | In | DC/DC Converter Differential (+) Output Voltage or Current-5 Sensing Pins. |
| V _{SENSE} M5 | B11* | H11* | In | DC/DC Converter Differential (-) Output Voltage or Current-5 Sensing Pins. |
| V _{SENSE} P6 | A12* | G12* | In | DC/DC Converter Differential (+) Output Voltage-6 Sensing Pin |
| V _{SENSE} M6 | A11* | G11* | In | DC/DC Converter Differential (-) Output Voltage-6 Sensing Pin |
| V _{SENSE} P7 | A7* | G7* | In | DC/DC Converter Differential (+) Output Voltage or Current-7 Sensing Pin |
| V _{SENSE} M7 | A6* | G6* | In | DC/DC Converter Differential (-) Output Voltage or Current-7 Sensing Pin |
| V _{OUT_EN} 0 | D7 | K7 | Out | DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled Up to 12V by 5 μ A |
| V _{OUT_EN} 1 | F8 | M8 | Out | DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled Up to 12V by 5 μ A |
| V _{OUT_EN} 2 | E8 | L8 | Out | DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled Up to 12V by 5 μ A |
| V _{OUT_EN} 3 | D8 | K8 | Out | DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled Up to 12V by 5 μ A |
| V _{OUT_EN} 4 | C8 | J8 | Out | DC/DC Converter Enable-4 Pin. Open-Drain Pull-Down Output. |
| V _{OUT_EN} 5 | B8 | H8 | Out | DC/DC Converter Enable-5 Pin. Open-Drain Pull-Down Output. |
| V _{OUT_EN} 6 | A8 | G8 | Out | DC/DC Converter Enable-6 Pin. Open-Drain Pull-Down Output. |
| V _{OUT_EN} 7 | C7 | J7 | Out | DC/DC Converter Enable-7 Pin. Open-Drain Pull-Down Output. |
| V _{IN_EN} | E5 | L5 | Out | DC/DC Converter V _{IN} ENABLE Pin. Output High Voltage Optionally Pulled Up to 12V by 5 μ A |
| V _{IN_SNS} | A5 | G5 | In | V _{IN} SENSE Input. This Voltage is Compared Against the V _{IN} On and Off Voltage Thresholds in Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters |
| V _{PWR} | B5 | H5 | In | V _{PWR} Serves as the Unregulated Power Supply Input to the Chip (4.5V to 15V). If a 4.5V to 15V Supply Voltage is Unavailable, Short V _{PWR} to V _{DD33} and Power the Chip Directly from a 3.3V Supply |
| V _{DD33} | A4 | G4 | In/Out | If Shorted to V _{PWR} , it Serves as 3.13V to 3.47V Supply Input Pin. Otherwise it is a 3.3V Internally Regulated Voltage Output. If using the internal regulator to provide V _{DD33} , do not connect to V _{DD33} pins of any other devices |
| V _{DD33} | A3 | G3 | In | Input for Internal 2.5V Sub-Regulator. Short Pin A3 to Pin A4 and Pin G3 to Pin G4. If using the internal regulator to provide V _{DD33} , do not connect to V _{DD33} pins of any other devices |
| V _{DD25} | A2 | G2 | In/Out | 2.5V Internally Regulated Voltage Output. Do not connect to V _{DD25} pins of any other devices |
| WP | A1 | G1 | In | Digital Input. Write-Protect Input Pin, Active High |
| PWRGD | B1 | H1 | Out | Power Good Open-Drain Output. Indicates When Outputs are Power Good. Can be Used as System Power-On Reset. The Latency of This Signal May Be as Long as the ADC Latency. See Note 6 |
| SHARE_CLK | B2 | H2 | In/Out | Bidirectional Clock Sharing Pin. Connect a 5.49k Pull-Up Resistor to V _{DD33} . Connect to all other SHARE_CLK pins in the system |
| WDI/RESETB | B4 | H4 | In | Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k Pull-Up Resistor to V _{DD33} . Rising Edge Resets Watchdog Counter. Holding This Pin Low for More Than t _{RESETB} Resets the Chip |
| FAULTB00 | C3 | J3 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-00. Connect a 10k Pull-Up Resistor to V _{DD33} |
| FAULTB01 | D3 | K3 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-01. Connect a 10k Pull-Up Resistor to V _{DD33} |

PIN FUNCTIONS

| PIN NAME | PIN | | PIN TYPE | DESCRIPTION |
|-------------|------------|------------|----------------|--|
| | Device A | Device B | | |
| FAULTB10 | C4 | J4 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-10. Connect a 10k Pull-Up Resistor to V_{DD33} |
| FAULTB11 | D4 | K4 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-11. Connect a 10k Pull-Up Resistor to V_{DD33} |
| SDA | C1 | J1 | In/Out | PMBus Bidirectional Serial Data Pin |
| SCL | D1 | K1 | In | PMBus Serial Clock Input Pin (400kHz Maximum) |
| ALERTB | E2 | L2 | Out | Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation |
| CONTROL0 | E1 | L1 | In | Control Pin 0 Input |
| CONTROL1 | F1 | M1 | In | Control Pin 1 Input |
| ASEL0 | F3 | M3 | In | Ternary Address Select Pin 0 Input. Connect to V_{DD33} , GND or Float to Encode 1 of 3 Logic States |
| ASEL1 | F2 | M2 | In | Ternary Address Select Pin 1 Input. Connect to V_{DD33} , GND or Float to Encode 1 of 3 Logic States |
| REFP | F5 | M5 | Out | Reference Voltage Output |
| REFM | F4 | M4 | Out | Reference Return Pin |
| V_{DACP0} | E7 | L7 | Out | DAC0 Output |
| V_{DACM0} | E6* | L6* | Out | DAC0 Return. Connect to Channel 0 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP1} | F10 | M10 | Out | DAC1 Output |
| V_{DACM1} | F9* | M9* | Out | DAC1 Return. Connect to Channel 1 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP2} | E10 | L10 | Out | DAC2 Output |
| V_{DACM2} | E9* | L9* | Out | DAC2 Return. Connect to Channel 2 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP3} | D10 | K10 | Out | DAC3 Output |
| V_{DACM3} | D9* | K9* | Out | DAC3 Return. Connect to Channel 3 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP4} | C10 | J10 | Out | DAC4 Output |
| V_{DACM4} | C9* | J9* | Out | DAC4 Return. Connect to Channel 4 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP5} | B10 | H10 | Out | DAC5 Output |
| V_{DACM5} | B9* | H9* | Out | DAC5 Return. Connect to Channel 5 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP6} | A10 | G10 | Out | DAC6 Output |
| V_{DACM6} | A9* | G9* | Out | DAC6 Return. Connect to Channel 6 DC/DC Converter's GND Sense or Return to GND |
| V_{DACP7} | B7 | H7 | Out | DAC7 Output |
| V_{DACM7} | B6* | H6* | Out | DAC7 Return. Connect to Channel 7 DC/DC Converter's GND Sense or Return to GND |
| V_{PU} | B3 | H3 | In | Common Connection for Internal Pull-Up Resistors |
| R_{PU1} | E3 | L3 | Out | General Purpose 10k Pull-Up Resistor 1 |
| R_{PU2} | D2 | K2 | Out | General Purpose 10k Pull-Up Resistor 2 |
| R_{PU3} | C2 | J2 | Out | General Purpose 10k Pull-Up Resistor 3 |
| R_{PU4} | E4 | L4 | Out | General Purpose 10k Pull-Up Resistor 4 |
| GND | C6, D5, D6 | J6, K5, K6 | Ground | Device A Ground Pins are Isolated from the Device B Ground Pins |
| DNC | C5 | J5 | Do Not Connect | Do Not Connect to This Pin |

*Any unused V_{SENSEn} or $V_{SENSEMn}$ or V_{DACMn} pins must be tied to GND.

BLOCK DIAGRAM



- *NOTES: 1. ONLY 1/2 OF THE LTM2987 MODULE SHOWN
 2. THE TWO 8-CHANNEL LTC2977 HALVES ARE IDENTICAL AND COMPLETELY ISOLATED
 3. PIN NAMES REFER TO (DEVICE A, DEVICE B)

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OPERATION

Overview

The LTM2987 contains two independent LTC2977 devices and most of the passive components required to make a complete 16-channel power system manager. The LTM2987 simplifies power system design by integrating the required passive components, reducing the bill-of-materials and improving PC board routing efficiency.

Each half of the LTM2987 behaves the same as a stand-alone LTC2977 including independent power supply and ground pins. This feature can be used to increase redundancy in a system while keeping the overall solution size small.

Refer to the LTC2977 data sheet for a detailed description of the device operation, the PMBus command set, and applications information.

Device Address

Since the LTM2987 consists of two independent LTC2977 devices, each half of the LTM2987 must be configured for a unique address. The I²C/SMBus addresses of the LTM2987 are configured in the same manner as for individual LTC2977 devices. The LTM2987 also responds to the LTC2977 global address and the SMBus Alert Response address, regardless of the state of the ASEL pins and the MFR_I2C_BASE_ADDRESS register. Please refer to the Device Address section in the LTC2977 data sheet for more details.

MFR_SPECIAL_ID

The LTM2987 contains unique MFR_SPECIAL_ID values to differentiate it from the LTC2977. Table 1 lists the MFR_SPECIAL_ID values for the LTM2987.

Table 1. LTM2987 MFR_SPECIAL_ID Values

| LTM2987 DEVICE | MFR_SPECIAL_ID |
|----------------|----------------|
| Device A | 0x8011 |
| Device B | 0x8021 |

APPLICATIONS INFORMATION

OVERVIEW

The LTM2987 is a Power System Manager that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, providing fault management, and voltage readback for sixteen DC/DC converters. Input voltage and LTM2987 junction temperature readback are also available. Odd numbered channels can be configured to read back current sense resistor voltages. Multiple LTM2987s can be synchronized to operate in unison using the SHARE_CLK, FAULTB and CONTROL pins. The LTM2987 utilizes a PMBus compliant interface and command set.

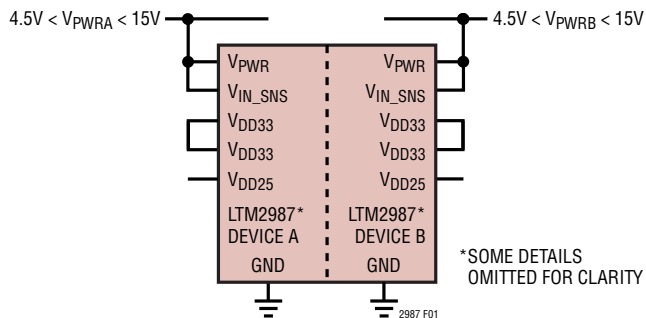


Figure 1. Powering LTM2987 Directly from an Intermediate Bus

POWERING THE LTM2987

The LTM2987 can be powered two ways. The first method requires that a voltage between 4.5V and 15V be applied to the V_{PWR} pin. See Figure 1. Internal linear regulators convert V_{PWR} down to 3.3V which drives all of the internal circuitry in each device. Do not tie the $V_{DD33(A)}$ and $V_{DD33(B)}$ pins together since each half of the LTM2987 has independent voltage regulators.

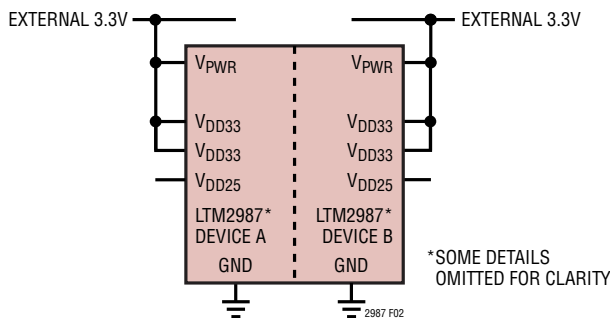


Figure 2. Powering LTM2987 from External 3.3V Supply

Alternatively, power from an external 3.3V supply may be applied directly to the V_{DD33} pins using a voltage between 3.13V and 3.47V. Tie V_{PWR} to the V_{DD33} pins. See Figure 2. In this case, $V_{DD33(A)}$ and $V_{DD33(B)}$ may be tied together. All functionality is available when using this alternate power method. The higher voltages needed for the $V_{OUT_EN[0:3]}$ pins and bias for the V_{SENSE} pins are charge pumped from V_{DD33} .

The method used to power each device in the LTM2987 is independent of the other device. Either method may be used in any combination.

APPLICATION CIRCUITS

Undedicated Pull-Up Resistors

Each half of the LTM2987 module has four undedicated 10k pull-up resistors as shown in Figure 3. The common pull-up voltage is applied to the V_{PU} pin, and the individual pull-up resistors are on R_{PU1} , R_{PU2} , R_{PU3} and R_{PU4} . These pull-up resistors can be used for the open-drain pins such as SDA, SCL, ALERTB or FAULTB $_zn$ in which case the common pull-up voltage V_{PU} should be connected to a 3.3V supply. To simplify the layout, the pin V_{PU} is adjacent to the V_{DD33} pin.

Anti-Aliasing Filter Considerations

Since most of the passive components required for operation are integrated into the LTM2987, no external filter components are required.

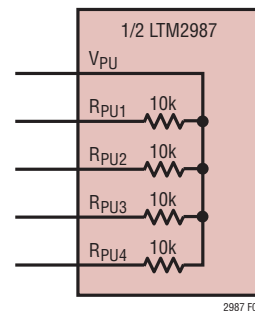


Figure 3. Undedicated Pull-Up Resistors

APPLICATIONS INFORMATION

V_{IN} Sense

Voltages other than V_{IN} can be monitored and supervised using the V_{IN_SNS} pins. Each V_{IN_SNS} pin has a calibrated internal divider allowing it to directly sense voltages up to 15V.

Unused ADC Sense Inputs

Connect all unused ADC sense inputs ($V_{SENSEPN}$ or $V_{SENSEMN}$) to GND. In a system where the inputs are connected to removable cards and may be left floating in certain situations, connect the inputs to GND using 100k resistors, as shown in Figure 4.

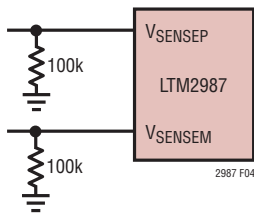


Figure 4. Connecting Unused Inputs to GND

PCB ASSEMBLY AND LAYOUT SUGGESTIONS

Bypass Capacitor Placement

All required bypass capacitors are integrated into the LTM2987. No additional bypass capacitance is required. The PCB layout should adhere to good layout guidelines. A multilayer PCB that dedicates a layer to power and ground is recommended. Low resistance and low inductance power and ground connections are important to minimize power supply noise and ensure proper device operation.

DESIGN CHECKLIST

I²C

- Each half of the LTM2987 must be configured for a unique address. Unique hardware $ASEL_n$ values are recommended for simplest in system programming.
- The address select pins ($ASEL_n$) are tri-level; Check Table 1 of the LTC2977 data sheet.
- Check addresses for collision with other devices on the bus and any global addresses.

Output Enables

- Use appropriate pull-up resistors on all V_{OUT_ENn} pins.
- Verify that the absolute maximum ratings of the V_{OUT_ENn} pins are not exceeded.

V_{IN} Sense

- No external resistive divider is required to sense V_{IN} ; V_{IN_SNS} already has an internal calibrated divider.

Logic Signals

- Verify the absolute maximum ratings of the digital pins (SCL, SDA, ALERTB, FAULTB zn , CONTROL n , SHARE_CLK, WDI, ASEL n , PWRGD) are not exceeded.
- Connect all SHARE_CLK pins in the system together and pull up to 3.3V with a 5.49k resistor.
- Do not leave CONTROL n pins floating. Pull up to 3.3V with a 10k resistor.
- Tie WDI/RESETB to V_{DD33} with a 10k resistor. Do not connect a capacitor to the WDI/RESETB pin.
- Tie WP to either V_{DD33} or GND. Do not leave floating.

Unused Inputs

- Connect all unused $V_{SENSEPN}$, $V_{SENSEMn}$ and DACM n pins to GND. Do not float unused inputs. Refer to Unused ADC Sense Inputs in the Applications Information section of the LTC2977 data sheet.

DAC Outputs

- Select appropriate resistor for desired margin range. Refer to the resistor selection tool in LTpowerPlay for assistance.

Power Supplies

- If powered from VPWR, do not connect the $V_{DD33(A)}$ and $V_{DD33(B)}$ pins together. Each V_{DD33} pin has an independent, internal regulator.

For a more complete list of design considerations and a schematic checklist, see the Design Checklist on the LTM2987 product page: www.linear.com/LTM2987.

PACKAGE DESCRIPTION

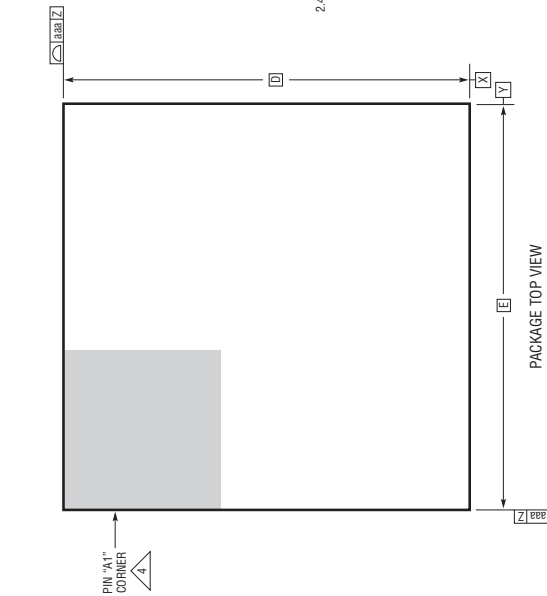
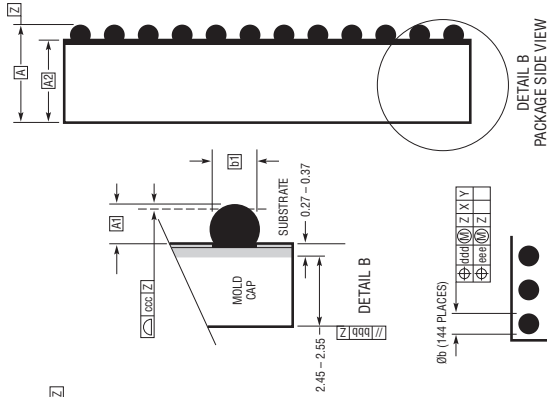
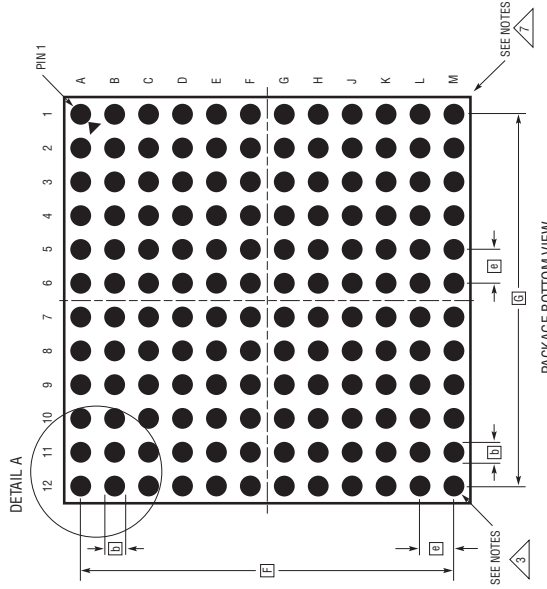
LTM2987 Component BGA Pinout (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|-----------------|----------|----------|-------------------|-------------------|-------------------|---------------------|----------------------|----------------------|----------------------|--------------------|--------------------|----------------------|----------------------|
| Device A | A | WP | V _{DD25} | V _{DD33} | V _{DD33} | V _{IN_SNS} | V _{SENSEM7} | V _{SENSEP7} | V _{OUT_EN6} | V _{DACM6} | V _{DACP6} | V _{SENSEM6} | V _{SENSEP6} |
| | B | PWRGD | SHARE_CLK | V _{PU} | WDI | V _{PWR} | V _{DACM7} | V _{DACP7} | V _{OUT_EN5} | V _{DACM5} | V _{DACP5} | V _{SENSEM5} | V _{SENSEP5} |
| | C | SDA | R _{PU3} | FAULTB00 | FAULTB10 | DNC | GND | V _{OUT_EN7} | V _{OUT_EN4} | V _{DACM4} | V _{DACP4} | V _{SENSEM4} | V _{SENSEP4} |
| | D | SCL | R _{PU2} | FAULTB01 | FAULTB11 | GND | GND | V _{OUT_EN0} | V _{OUT_EN3} | V _{DACM3} | V _{DACP3} | V _{SENSEM3} | V _{SENSEP3} |
| | E | CONTROL0 | ALERTB | R _{PU1} | R _{PU4} | V _{IN_EN} | V _{DACM0} | V _{DACP0} | V _{OUT_EN2} | V _{DACM2} | V _{DACP2} | V _{SENSEM2} | V _{SENSEP2} |
| | F | CONTROL1 | ASEL1 | ASEL0 | REFM | REFP | V _{SENSEM0} | V _{SENSEP0} | V _{OUT_EN1} | V _{DACM1} | V _{DACP1} | V _{SENSEM1} | V _{SENSEP1} |
| Device B | G | WP | V _{DD25} | V _{DD33} | V _{DD33} | V _{IN_SNS} | V _{SENSEM7} | V _{SENSEP7} | V _{OUT_EN6} | V _{DACM6} | V _{DACP6} | V _{SENSEM6} | V _{SENSEP6} |
| | H | PWRGD | SHARE_CLK | V _{PU} | WDI | V _{PWR} | V _{DACM7} | V _{DACP7} | V _{OUT_EN5} | V _{DACM5} | V _{DACP5} | V _{SENSEM5} | V _{SENSEP5} |
| | J | SDA | R _{PU3} | FAULTB00 | FAULTB10 | DNC | GND | V _{OUT_EN7} | V _{OUT_EN4} | V _{DACM4} | V _{DACP4} | V _{SENSEM4} | V _{SENSEP4} |
| | K | SCL | R _{PU2} | FAULTB01 | FAULTB11 | GND | GND | V _{OUT_EN0} | V _{OUT_EN3} | V _{DACM3} | V _{DACP3} | V _{SENSEM3} | V _{SENSEP3} |
| | L | CONTROL0 | ALERTB | R _{PU1} | R _{PU4} | V _{IN_EN} | V _{DACM0} | V _{DACP0} | V _{OUT_EN2} | V _{DACM2} | V _{DACP2} | V _{SENSEM2} | V _{SENSEP2} |
| | M | CONTROL1 | ASEL1 | ASEL0 | REFM | REFP | V _{SENSEM0} | V _{SENSEP0} | V _{OUT_EN1} | V _{DACM1} | V _{DACP1} | V _{SENSEM1} | V _{SENSEP1} |

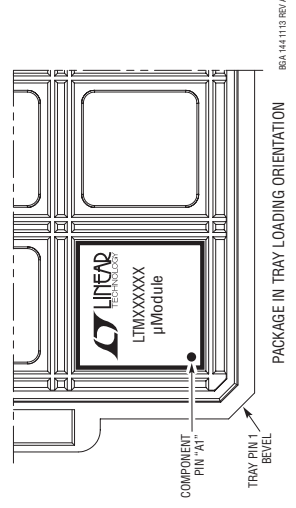
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTM2987#packaging> for the most recent package drawings.

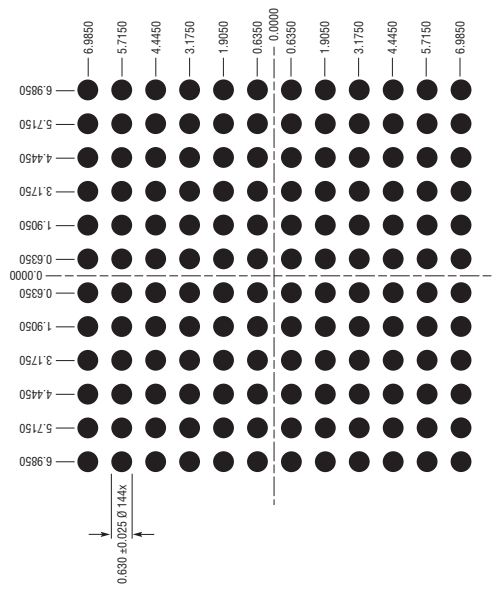
BGA Package
144-Lead (15mm × 15mm × 3.42mm)
 (Reference LTC DWG # 05-08-1946 Rev A)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
 4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
 5. PRIMARY DATUM - Z - IS SEATING PLANE
 6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
 7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG μ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



| SYMBOL | DIMENSIONS | | NOTES |
|----------------------------|------------|------|-------|
| | MIN | NOM | |
| A | 3.22 | 3.42 | 3.62 |
| A1 | 0.50 | 0.60 | 0.70 |
| A2 | 2.72 | 2.82 | 2.92 |
| b | 0.60 | 0.75 | 0.90 |
| b1 | 0.60 | 0.63 | 0.66 |
| D | 15.0 | | |
| E | 15.0 | | |
| e | 1.27 | | |
| F | 13.97 | | |
| G | 13.97 | | |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.20 | | |
| ddd | 0.30 | | |
| eee | 0.15 | | |
| TOTAL NUMBER OF BALLS: 144 | | | |



REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|---|-------------|
| A | 08/16 | Added EEPROM ECC information and updated Typical Application | 1 |
| | | Increased Maximum Solder Temperature from 245°C to 250°C | 2 |
| | | Updated DAC Output Update Rate (t_{S_VDACP}) to 500 μ s from 250 μ s | 4 |
| | | Added Note 4 | 7 |
| | | Added graph: $V_{OUT_EN[7:0]}$ Output Voltage vs V_{DD33} | 10 |
| | | Updated V_{DD33} and SHARE_CLK pin functions | 11 |
| | | Changed MFR_SPECIAL_ID in Table 1 | 14 |

TYPICAL APPLICATION

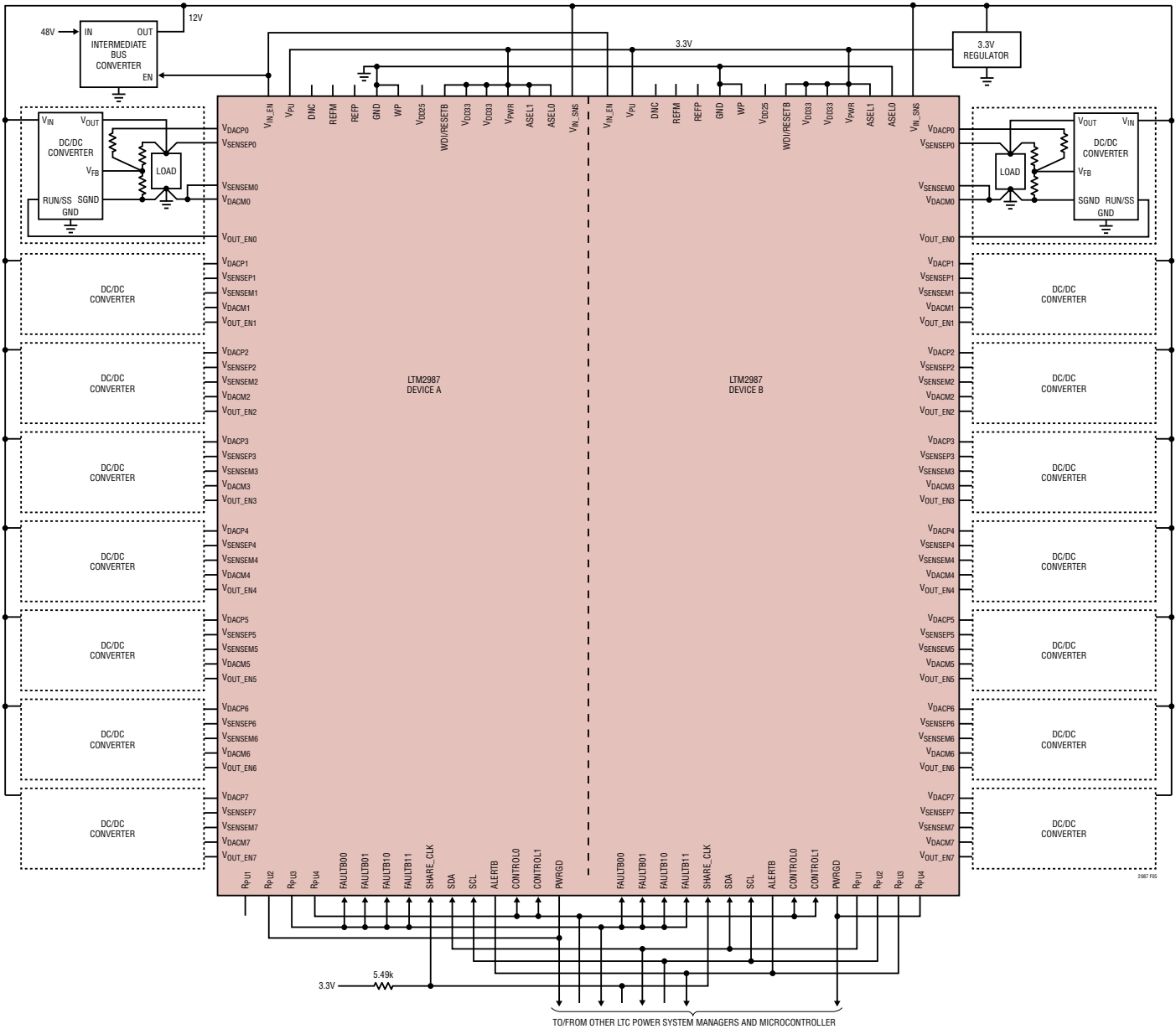


Figure 5. LTM2987 16-Channel Application Circuit with External 3.3V Chip Power

RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|-------------------------|---|---|
| LTC2970 | Dual I ² C Power Supply Monitor and Margining Controller | 5V to 15V, 0.5% TUE 14-Bit ADC, 8-Bit DAC, Temperature Sensor |
| LTC2974 | 4-Channel PMBus Power System Manager | 0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring/Supervision |
| LTC2975 | 4-Channel PMBus Power System Manager | LTC2974 Plus Input Current, Power and Energy Accumulator |
| LTC2977 | 8-Channel PMBus Power System Manager | 0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision |
| LTC2980 | 16-Channel PMBus Power System Manager | Dual LTC2977 |
| LTC3880 | Dual Output PolyPhase Step-Down DC/DC Controller | 0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision |
| LTC3883 | Single Output PolyPhase Step-Down DC/DC Controller | 0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision |

2987fa

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[LTC2970HUFD#PBF](#) [LTM2987CY#PBF](#) [ZXCT1080QE5TA](#) [ZXCT1081QE5TA](#) [NCP4353ASNT1G](#) [MAX1864TEEE+T](#) [PAC1931T-](#)
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[DS1842N+](#) [STPMS1BPQR](#) [STPM33TR](#) [ISL28023FR60Z](#) [ZXCT1023DFGTA](#) [MAX17523ATE+](#) [MAX14626ETTT](#)