Triple Output, Low Voltage DC/DC µModule Regulator

FEATURES

- **Dual 4A Output Power Supply with 1.5A VLDO™**
- Short-Circuit and Overtemperature Protection
- Power Good Indicators

Switching Regulators Section—Current Mode Control

- **Input Voltage Range: 2.375V to 5.5V**
- **4A DC Typical, 5A Peak Output Current Each**
- **0.8V Up to 5V Output Each, Parallelable**
- **±2% Total DC Output Error**
- **Output Voltage Tracking**
- Up to 95% Efficiency
- Programmable Soft-Start

VLDO Section

- **VLDO, 1.14V to 3.5V Input Range**
- **VLDO, 0.4V to 2.6V, 1.5A Output**
- **VLDO, 40dB Supply Rejection at f_{SW}**
- **±1% Total DC Output Error**
- Small and Very Low Profile Package: 15mm × 15mm × 2.82mm

APPLICATIONS

- Telecom and Networking Equipment
- Industrial Power Systems
- Low Noise Applications
- FPGA, SERDES Power

DESCRIPTION

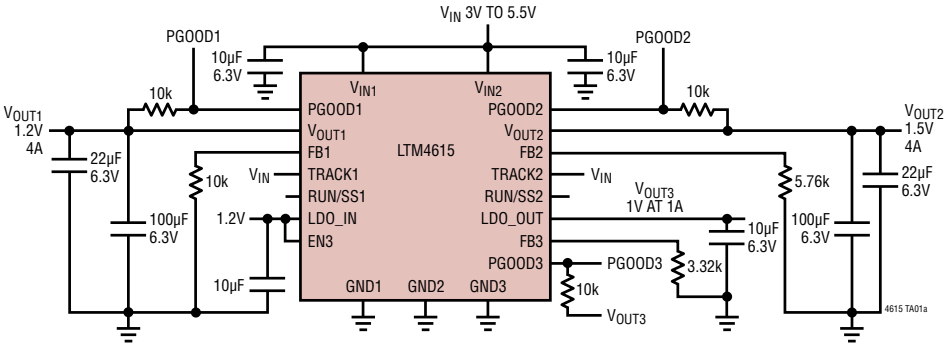
The LTM®4615 is a complete 4A dual output switching mode DC/DC power supply plus an additional 1.5A VLDO (very low dropout) linear regulator. Included in the package are the switching controllers, power FETs, inductors, a 1.5A regulator and all support components. The dual 4A DC/DC converters operate over an input voltage range of 2.375V to 5.5V, and the VLDO operates from a 1.14V to 3.5V input. The LTM4615 supports output voltages ranging from 0.8V to 5V for the DC/DC converters, and 0.4V to 2.6V for the VLDO. The three regulator output voltages are set by a single resistor for each output. Only bulk input and output capacitors are needed to complete the design.

The low profile package (2.82mm) enables utilization of unused space on the bottom of PC boards for high density point of load regulation. High switching frequency and a current mode architecture enables a very fast transient response to line and load changes without sacrificing stability. The device supports output voltage tracking for supply rail sequencing.

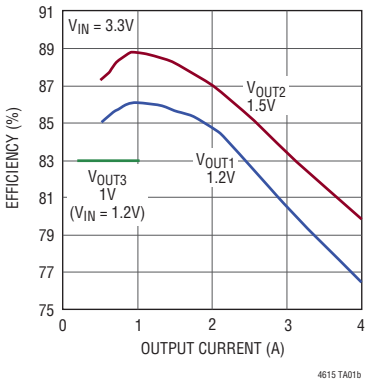
Additional features include overvoltage protection, overcurrent protection, thermal shutdown and programmable soft-start. The power module is offered in a space saving and thermally enhanced 15mm × 15mm × 2.82mm LGA package. The LTM4615 is RoHS compliant with Pb-free finish.

TYPICAL APPLICATION

1.2V at 4A, 1.5V at 4A and 1V at 1A DC/DC µModule® Regulator



Efficiency vs Output Current



ABSOLUTE MAXIMUM RATINGS

(Note 1)

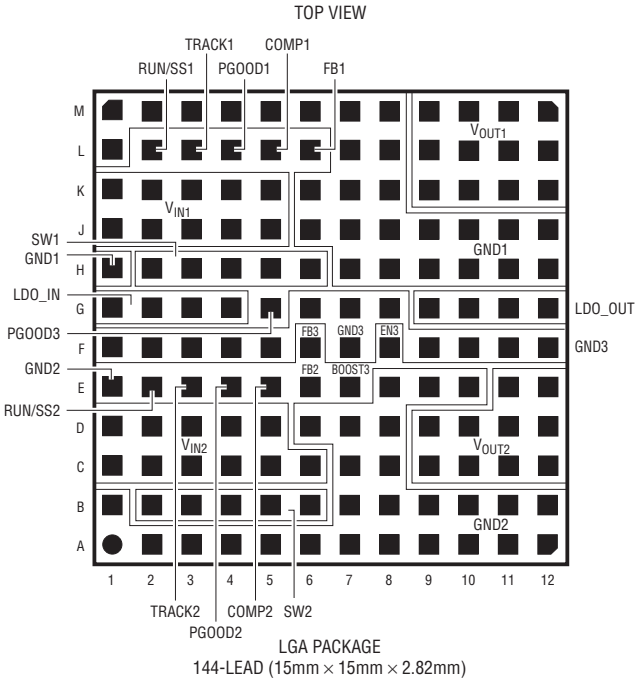
Switching Regulators

V_{IN1}, V_{IN2}, PGOOD1, PGOOD2..... –0.3V to 6V
COMP1, COMP2, RUN/SS1, RUN/SS2
V_{FB1}, V_{FB2},TRACK1, TRACK2 ..... –0.3V to V_{IN}
SW, V_{OUT} ..... –0.3V to (V_{IN} + 0.3V)

Very Low Dropout Regulator

LDO_IN, PGOOD3, EN3..... –0.3V to 6V
LDO_OUT.....–0.3 to 4V
FB3 ..... –0.3V to (LDO_IN + 0.3V)
LDO_OUT Short-Circuit..... Indefinite
Internal Operating Temperature Range
(Notes 2, 5)..... –40°C to 125°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
144-LEAD (15mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, $\theta_{JCbottom}$ = 2-3°C/W, θ_{JA} = 15°C/W, θ_{JCtop} = 25°C/W,
θ VALUES DETERMINED FROM 4 LAYER 76mm × 95mm PCB
WEIGHT = 1.6g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE†
LTM4615EV#PBF	LTM4615EV#PBF	LTM4615V	144-Lead (15mm × 15mm × 2.82mm) LGA	–40°C to 125°C
LTM4615IV#PBF	LTM4615IV#PBF	LTM4615V	144-Lead (15mm × 15mm × 2.82mm) LGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

† See Note 2.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 5V, LDO_IN = 1.2V unless otherwise noted. Per Typical Application Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel							
$V_{IN(DC)}$	Input DC Voltage Range		●	2.375		5.5	V
$V_{OUT(DC)}$	Output DC Voltage Range		●	0.8		5.0	V
$V_{OUT(DC)}$	Output Voltage	C_{IN} = 22µF, C_{OUT} = 100µF, R_{FB} = 5.76k, V_{IN} = 2.375V to 5.5V, I_{OUT} = 0A to 4A (Note 6) 0°C ≤ T_J ≤ 125°C	 ●	1.460 1.45	1.49 1.49	1.512 1.512	V V
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A		1.6	2	2.3	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 22µF, C_{OUT} = 100µF, V_{OUT} = 1.5V, V_{IN} = 5.5V			0.35		A
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 2.375V, V_{OUT} = 1.5V, Switching Continuous V_{IN} = 5.5V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 5V			28 45 7	 12	mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 2.375V, V_{OUT} = 1.5V, I_{OUT} = 4A V_{IN} = 5.5V, V_{OUT} = 1.5V, I_{OUT} = 4A			3.2 1.48		A A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 5.5V, V_{OUT} = 1.5V (Note 6)		0		4	A
$\frac{\Delta V_{OUT(LOAD + LINE)}}{V_{OUT}}$	Load and Line Regulation Accuracy	V_{OUT} = 1.5V, 0A to 4A (Note 6) V_{IN} = 2.375V to 5.5V	 ●		±1.0 ±1.3	±1.30 ±1.6	% %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF V_{IN} = 5V, V_{OUT} = 1.5V			12		mV_{P-P}
f_S	Output Ripple Voltage Frequency	I_{OUT} = 4A, V_{IN} = 5V, V_{OUT} = 1.5V			1.25		MHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF, V_{OUT} = 1.5V, RUN/SS = 10nF, I_{OUT} = 0A V_{IN} = 3.3V V_{IN} = 5V			 20 20		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 100µF, V_{OUT} = 1.5V, I_{OUT} = 1A Resistive Load, TRACK = V_{IN} and RUN/SS = Float V_{IN} = 5V			0.5		ms
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF, V_{IN} = 5V, V_{OUT} = 1.5V			25		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 5V, V_{OUT} = 1.5V			10		µs
$I_{OUT(PK)}$	Output Current Limit	C_{OUT} = 100µF, V_{IN} = 5V, V_{OUT} = 1.5V			8		A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	 ●	0.790 0.786	0.8 0.8	0.807 0.809	V V
I_{FB}					0.2		µA
V_{RUN}	RUN Pin On/Off Threshold			0.6	0.75	0.9	V
I_{TRACK}	TRACK Pin Current				0.2		µA
$V_{TRACK(OFFSET)}$	Offset Voltage	TRACK = 0.4V			30		mV
$V_{TRACK(RANGE)}$	Tracking Input Range			0		0.8	V
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			4.96	4.99	5.02	kΩ
ΔV_{PGOOD}	PGOOD Range				±7.5		%
R_{PGOOD}	PGOOD Resistance	Open-Drain Pull-Down			90	150	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 5V, LDO_IN = 1.2V unless otherwise noted. Per Typical Application Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VLDO Section							
V_{LDO_IN}	Operating Voltage	(Note 3)	●	1.14		3.5	V
$I_{IN(LDO\_IN)}$	Operating Current	I_{OUT} = 0mA, V_{OUT} = 1V, EN3 = 1.2V			1		mA
$I_{IN(SHDN)}$	Shutdown Current	EN3 = 0V, LDO_IN = 1.5V			0.6	20	µA
V_{BOOST3}	BOOST3 Output Voltage	EN3 = 1.2V		4.8	5	5.2	V
$V_{BOOST3(UVLO)}$	Undervoltage Lockout				4.3		V
V_{FB3}	FB3 Internal Reference Voltage	1mA ≤ I_{OUT} ≤ 1.5A, 1.14V ≤ V_{LDO_IN} ≤ 3.5V, BOOST3 = 5V, 1V ≤ V_{OUT} ≤ 2.59V	 ●	0.397 0.395	0.4 0.4	0.404 0.405	V V
V_{LDO_OUT}	Output Voltage Range			0.4		2.6	V
V_{DO}	Dropout Voltage	V_{LDO_IN} = 1.5V, V_{FB3} = 0.38V, I_{OUT} = 1.5A (Note 4)			100	250	mV
LDO_RHI	LDO Top Feedback Resistor			4.96	4.99	5.02	kΩ
I_{OUT}	Output Current	V_{EN3} = 1.2V	●	1.5			A
I_{LIM}	Output Current Limit	(Note 5)			2.5		A
e_n	Output Voltage Noise	Frequency = 10Hz to 1MHz, I_{LOAD} = 1A			300		µRMS
V_{IH_EN3}	EN3 Input High Voltage	1.14V ≤ V_{LDO_IN} ≤ 3.5V	●	1			V
V_{IL_EN3}	EN3 Input Low Voltage	1.14V ≤ V_{LDO_IN} ≤ 3.5V				0.4	V
I_{IN_EN3}	EN3 Input Current			–1		1	µA
V_{OL_PGOOD3}	PGOOD Low Voltage	I_{PGOOD3} = 2mA			0.1	0.4	V
PGOOD Threshold	Output Threshold Relative to V_{FB3}	PGOOD3 High to Low PGOOD3 Low to High		–14 –4	–12 –3	–10 –2	% %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4615 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4615E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4615I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: Minimum operating voltage required for regulation is:

$V_{IN} \geq V_{OUT(MIN)} + V_{DROPOUT}$

Note 4: Dropout voltage is the minimum input to output differential needed to maintain regulation at a specified output current. In dropout the output voltage will be equal to $V_{IN} – V_{DROPOUT}$.

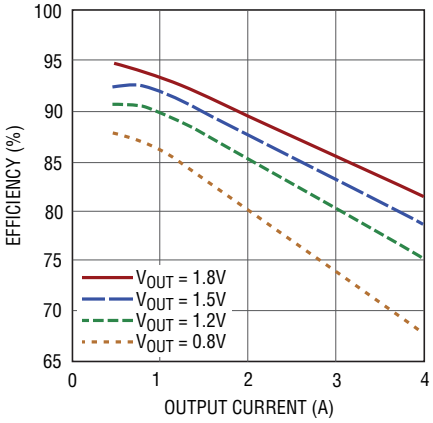
Note 5: The LTM4615 has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature is activated. Continuous overtemperature activation can impair long-term reliability.

Note 6: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

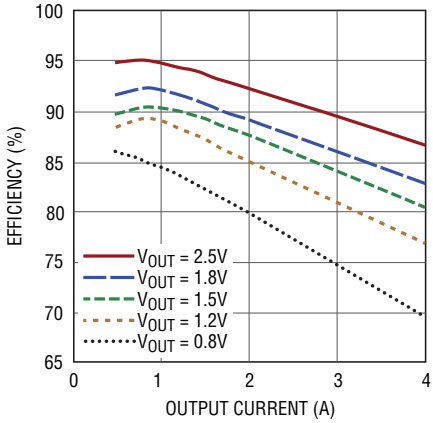
TYPICAL PERFORMANCE CHARACTERISTICS

Switching Regulators

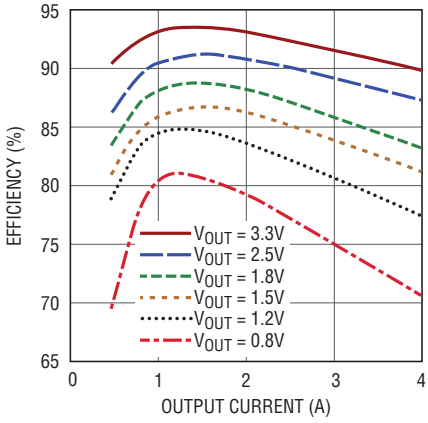
Efficiency vs Output Current
V_{IN} = 2.5V



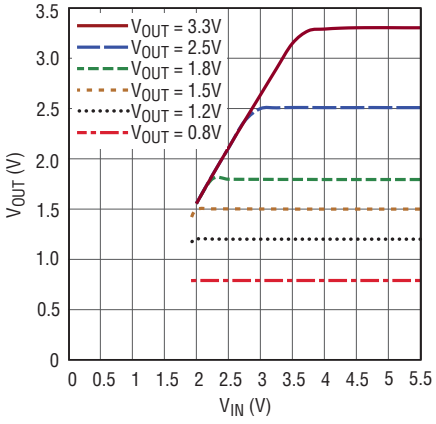
Efficiency vs Output Current
V_{IN} = 3.3V



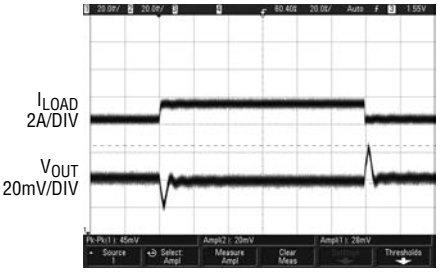
Efficiency vs Output Current
V_{IN} = 5V



Minimum Input Voltage at 4A Load

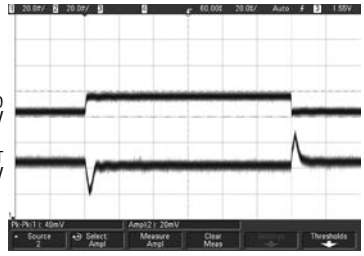


Load Transient Response



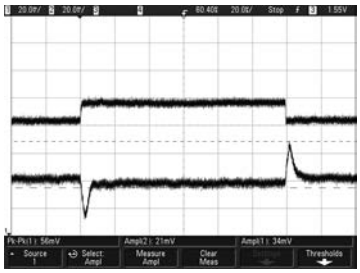
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.2V
C_{OUT} = 100µF, 6.3V CERAMICS

Load Transient Response



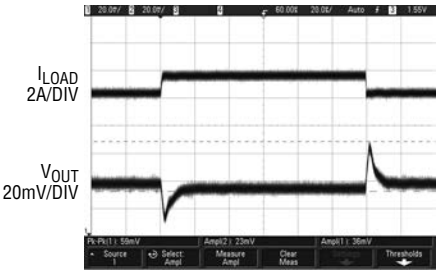
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 100µF, 6.3V CERAMICS

Load Transient Response



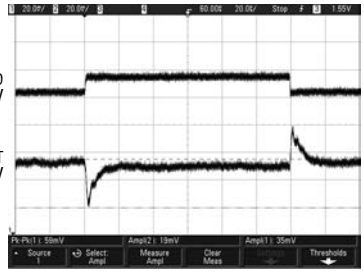
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.8V
C_{OUT} = 100µF, 6.3V CERAMICS

Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 100µF, 6.3V CERAMICS

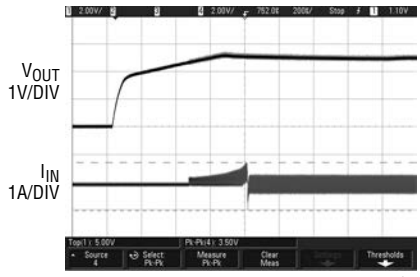
Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 3.3V
C_{OUT} = 100µF, 6.3V CERAMICS

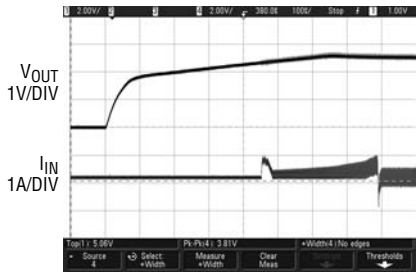
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up



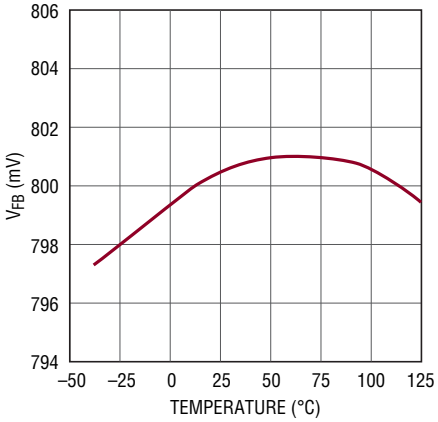
V_{IN} = 5V 200µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 100µF
NO LOAD
(0.01µF SOFT-START CAPACITOR)

Start-Up

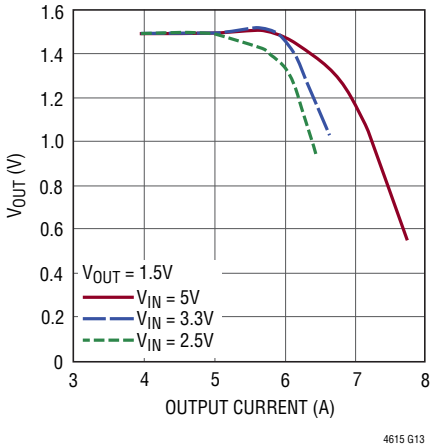


V_{IN} = 5V 200µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 100µF
4A LOAD
(0.01µF SOFT-START CAPACITOR)

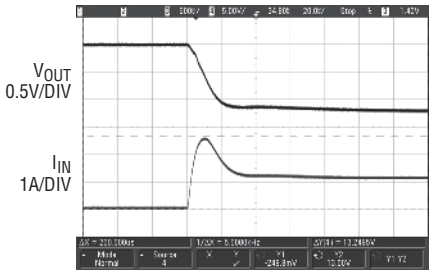
V_{FB} vs Temperature



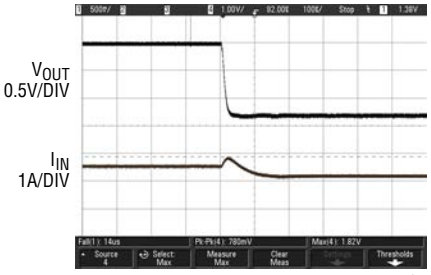
Current Limit



Short-Circuit Protection 1.5V Short, No Load

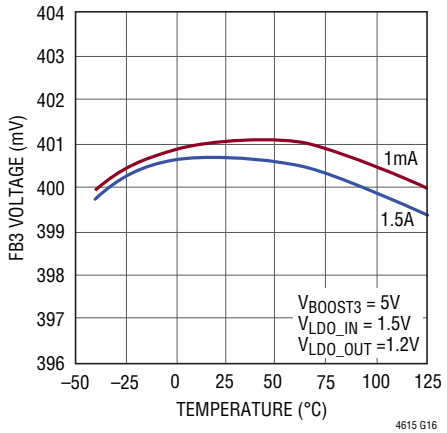


Short-Circuit Protection 1.5V Short, 4A Load

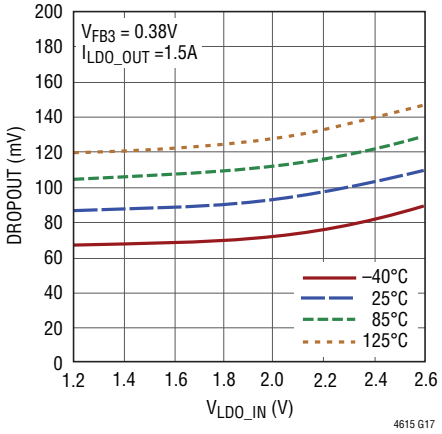


VLDO

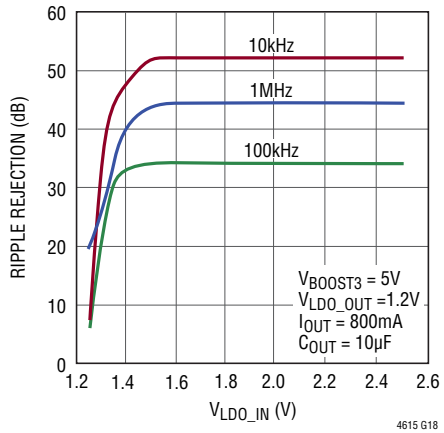
V_{FB3} vs Temperature



Dropout Voltage vs Input Voltage

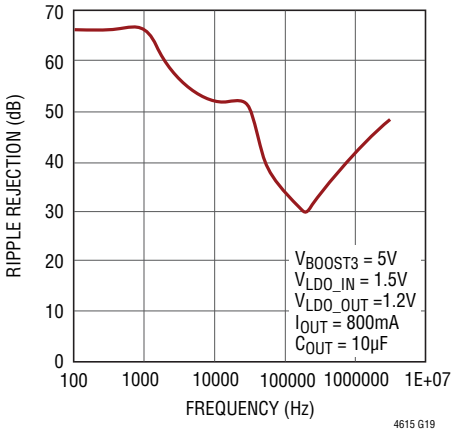


Ripple Rejection

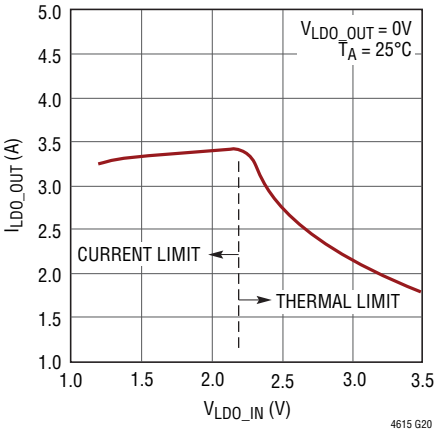


TYPICAL PERFORMANCE CHARACTERISTICS

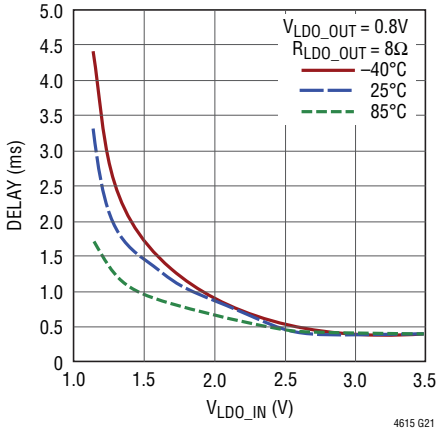
Ripple Rejection



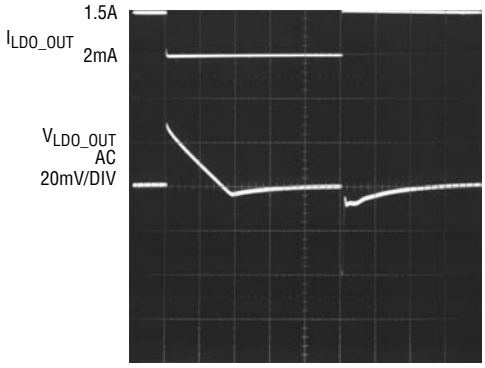
Output Current Limit



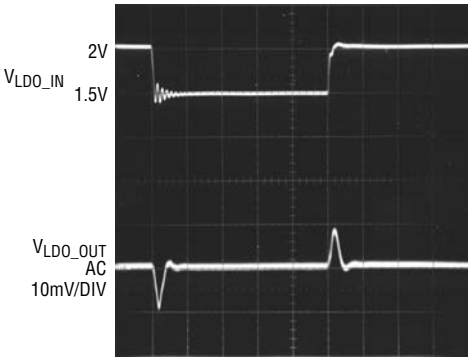
Delay from Enable to Power Good



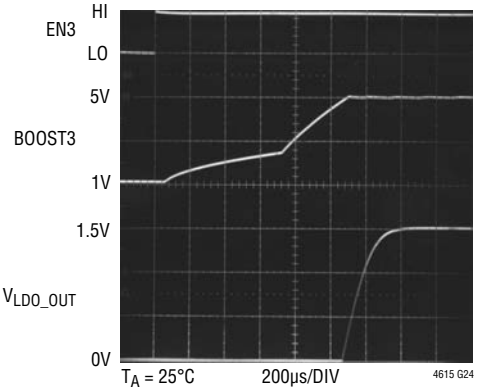
Output Load Transient Response



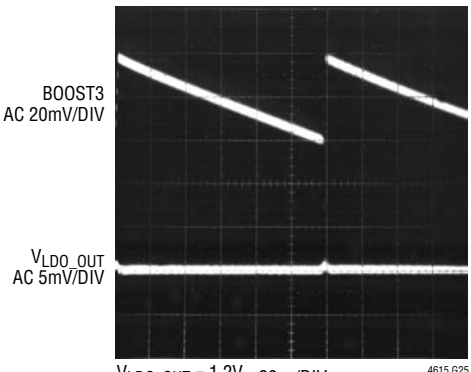
IN Supply Transient Response



BOOST3/OUT Start-Up



BOOST3 Ripple and Feedthrough to V_{LDO_OUT}



PIN FUNCTIONS

V_{IN1}, V_{IN2} (J1-J5, K1-K5); (C1-C6, D1-D5): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT1}, V_{OUT2} (K9-K12, L9-L12, M9-M12); (C9-C12, D9-D12, E11-E12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

GND1, GND2, (H1, H7-H12, J6-J12, K6-K8 L1, L7-L8, M1-M8); (A1-A12, B1, B7-B12, C7-C8, D6-D8, E1, E8-E10): Power Ground Pins for Both Input and Output Returns.

TRACK1, TRACK2 (L3, E3): Output Voltage Tracking Pins. When the module is configured as a master output, then a soft-start capacitor is placed on the RUN/SS pin to ground to control the master ramp rate, or an external ramp can be applied to the master regulator's track pin to control it. Slave operation is performed by putting a resistor divider from the master output to ground, and connecting the center point of the divider to this pin on the slave regulator. If tracking is not desired, then connect the TRACK pin to V_{IN}. Load current must be present for tracking. See the Applications Information section.

FB1, FB2 (L6, E6): The Negative Input of the Switching Regulators' Error Amplifier. Internally, these pins are connected to V_{OUT} with a 4.99k precision resistor. Different output voltages can be programmed with an additional resistor between the FB and GND pins. Two power modules can current share when this pin is connected in parallel with the adjacent module's FB pin. See the Applications Information section.

FB3 (F6): The Negative Input of the LDO Error Amplifier. Internally the pin is connected to LDO_OUT with a 4.99k resistor. Different output voltages can be programmed with an additional resistor between the FB3 and GND pins. See the Applications Information section.

COMP1, COMP2 (L5, E5): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Two power modules can current share when this pin is connected in parallel with the adjacent module's COMP pin. Each channel has been internally compensated. See the Applications Information section.

PGOOD1, PGOOD2 (L4, E4): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

RUN/SS1, RUN/SS2 (L2, E2): Run Control and Soft-Start Pin. A voltage above 0.8V will turn on the module, and below 0.5V will turn off the module. This pin has a 1M resistor to V_{IN} and a 1000pF capacitor to GND. See the Applications Information section for soft-start information.

SW1, SW2 (H2-H6, B2-B6): The switching node of the circuit is used for testing purposes. This can be connected to copper on the board for improved thermal performance. SW1 and SW2 must be floating on separate copper planes.

LDO_IN (G1-G4): VLDO Input Power Pins. Place input capacitor close to these pins.

LDO_OUT (G9-G12): VLDO Output Power Pins. Place output capacitor close to these pins. Minimum 1mA load is necessary for proper output voltage accuracy.

BOOST3 (E7): Boost Supply for Driving the Internal VLDO NMOS Into Full Enhancement. The pin is use for testing the internal boost converter. The output is typically 5V.

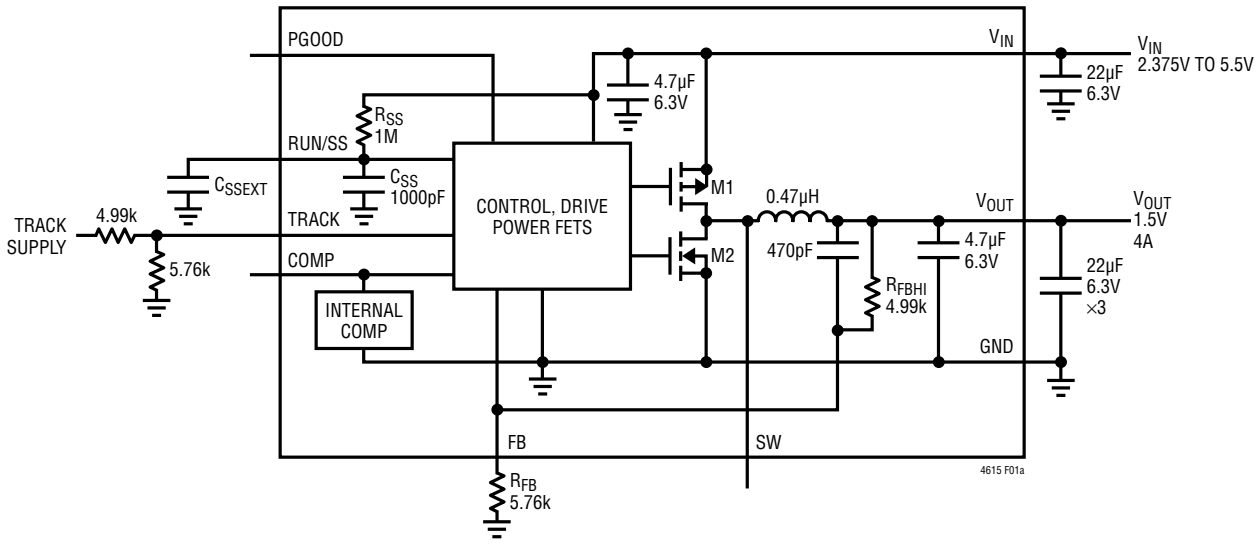
GND3 (F1-F5, F7, F9-F12, G6-G8): The power ground pins for both input and output returns for the internal VLDO.

PGOOD3 (G5): VLDO Power Good Pin.

EN3 (F8): VLDO Enable Pin.

SIMPLIFIED BLOCK DIAGRAM

Switching Regulator Block Diagram



VLDO Block Diagram

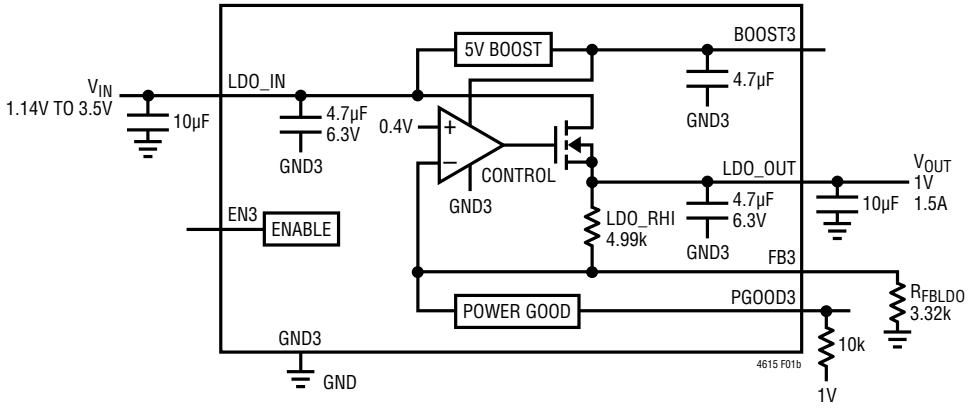


Figure 1. Simplified LTM4615 Block Diagram of Each Switching Regulator Channel and the VLDO

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration for each channel.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 2.375V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 4A	22			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 2.375V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 4A	66	100		µF
LDO_IN	LDO Input Capacitance	I_{OUT} = 1A	4.7	10		µF
LDO_OUT	LDO Output Capacitance	I_{OUT} = 1A	10			µF

OPERATION

LTM4615 POWER MODULE DESCRIPTION

Dual Switching Regulator Section

The LTM4615 is a standalone dual nonisolated switching mode DC/DC power supply with an additional onboard 1.5A VLDO. It can deliver up to 4A of DC output current for each channel with few external input and output capacitors. This module provides two precisely regulated output voltages programmable via one external resistor for each channel from 0.8V DC to 5V DC over a 2.375V to 5.5V input voltage range. The VLDO is an independent 1.5A linear regulator that can be powered from either switching converter. The typical application schematic is shown in Figure 12.

The LTM4615 has two integrated constant frequency current mode regulators, with built-in power MOSFETs with fast switching speed. The typical switching frequency is 1.25MHz. With current mode control and internal feedback loop compensation, these switching regulators have sufficient stability margins and good transient performance under a wide range of operating conditions, and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. Besides, current limiting is provided in an overcurrent condition with thermal shutdown. In addition, internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the particular output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET, M1, is turned off and bottom FET, M2, is turned on and held on until the overvoltage condition clears, or current limit is exceeded.

Pulling each specific RUN/SS pin below 0.8V forces the specific regulator controller into its shutdown state, turning off both M1 and M2 for each power stage. At low load current, each regulator works in continuous current mode by default to achieve minimum output voltage ripple.

The TRACK pins are used for power supply tracking for each specific regulator. See the Applications Information section.

The LTM4615 is internally compensated to be stable over the operating conditions. Table 4 provides a guideline for input and output capacitance for several operating conditions. The LTpowerCAD™ Design Tool is provided for transient and stability analysis.

The FB pins are used to program the specific output voltage with a single resistor to ground.

VLDO Section

The VLDO (very low dropout) linear regulator operates from a 1.14V to 3.5V input. The VLDO uses an internal NMOS transistor as the pass device in a source-follower configuration. The BOOST3 pin is the output of an internal boost converter that supplies the higher supply drive to the pass device for low dropout enhancement. The internal boost converter operates on very low current, thus optimizing high efficiency for the VLDO in close to dropout operation.

An undervoltage lockout comparator on the LDO ensures that the boost voltage is greater than 4.2V before enabling the LDO, otherwise the LDO is disabled.

The LDO provides a high accuracy output capable of supply 1.5A of output current with a typical drop out of 100mV. A single ceramic 10µF capacitor is all that is required for output capacitor bypassing. A low reference voltage allows the VLDO to have lower output voltages than the commonly available LDO.

The device also includes current limit and thermal overload protection. The NMOS follower architecture has fast transient response without the traditional high drive currents in dropout. The VLDO includes a soft-start feature to prevent excessive current on the input during start-up. When the VLDO is enabled, the soft-start circuitry gradually increases the reference voltage from 0V to 0.4V over a period of approximately 200µs.

APPLICATIONS INFORMATION

Dual Switching Regulator

The typical LTM4615 application circuit is shown in Figure 12. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage on the two switching regulators. The LTM4615 is 100% duty cycle, but the V_{IN} to V_{OUT} minimum dropout will be a function the load current. A typical 0.5V minimum is sufficient.

Output Voltage Programming

Each regulator channel has an internal 0.8V reference voltage. As shown in the block diagram, a 4.99k internal feedback resistor connects the V_{OUT} and FB pins together. The output voltage will default to 0.8V with no feedback resistor. Adding a resistor R_{FB} from the FB pin to GND programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{4.99k + R_{FB}}{R_{FB}}$$

or equivalently,

$$R_{FB} = \frac{4.99k}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1. FB Resistor Table vs Various Output Voltages

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
FB	Open	10k	5.76k	3.92k	2.37k	1.62k

Input Capacitors

The LTM4615 module should be connected to a low AC impedance DC source. One 4.7µF ceramic capacitor is included inside the module for each regulator channel. Additional input capacitors are needed if a large load step is required, up to the full 4A level, and for RMS ripple current requirements. A 47µF bulk capacitor can be used for more input capacitance. This 47µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces. The bulk capacitor can be a switcher-rated aluminum electrolytic OS-CON capacitor.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. If a low inductance plane is used to power the device, then no input capacitance is required. The internal 4.7µF ceramics on each channel input are typically rated for 1A of RMS ripple current up to 85°C operation. The worse-case ripple current for the 4A maximum current is 2A or less. An additional 10µF or 22µF ceramic capacitor can be used to supplement the internal capacitor with an additional 1A to 2A ripple current rating.

Output Capacitors

The LTM4615 switchers are designed for low output voltage ripple on each channel. The bulk output capacitors are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. The output capacitors can be a low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range is 66µF to 100µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

APPLICATIONS INFORMATION

Fault Conditions: Current Limit and Overtemperature Protection

The LTM4615 has current mode control, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

Along with current limiting in the event of an overload condition, the LTM4615 has overtemperature shutdown protection that inhibits switching operation around 150°C for each channel.

Run Enable and Soft-Start

The RUN/SS pins provide a dual function of enable and soft-start control for each channel. The RUN/SS pins are used to control turn on of the LTM4615. While each enable pin is below 0.5V, the LTM4615 will be in a low quiescent current state. At least a 0.8V level applied to the enable pins will turn on the LTM4615 regulators. This pin can be used to sequence the regulator channels. The soft-start control is provided by a 1M pull-up resistor (R_{SS}) and a 1000pF capacitor (C_{SS}) as drawn in the block diagram for each channel. An external capacitor can be applied to the RUN/SS pin to increase the soft-start time. A typical value is 0.01µF. The approximate equation for soft-start:

$$t_{SOFTSTART} = \ln\left(\frac{V_{IN}}{V_{IN}-1.8V}\right) \bullet R_{SS} \bullet C_{SS}$$

where R_{SS} and C_{SS} are shown in the block diagram of Figure 1, and the 1.8V is soft-start upper range. The soft-start function can also be used to control the output ramp-up time, so that another regulator can be easily tracked to it.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. Either output can be tracked up or down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4615 uses a very accurate 4.99k resistor for the internal top feedback resistor. Figure 2 shows an example of coincident tracking.

Equations:

$$TRACK1 = \left(\frac{R_{FB1}}{4.99k + R_{FB1}}\right) \bullet Master$$

$$Slave = \left(1 + \frac{4.99k}{R_{FB1}}\right) \bullet TRACK1$$

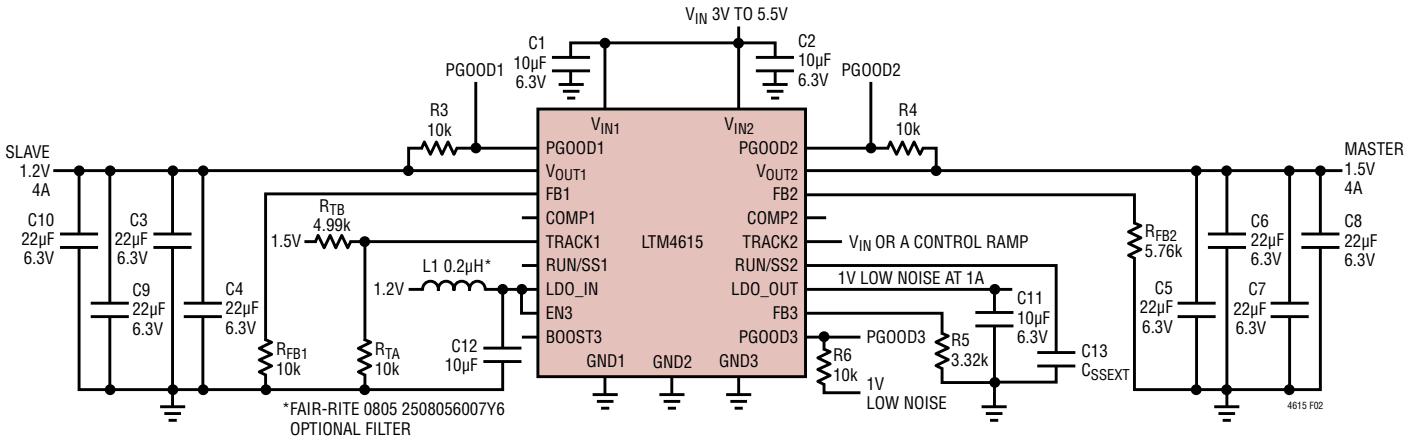


Figure 2. Dual Outputs (1.5V and 1.2V) with Tracking

APPLICATIONS INFORMATION

TRACK1 is the track ramp applied to the slave's track pin. TRACK1 applies the track reference for the slave output up to the point of the programmed value at which TRACK1 proceeds beyond the 0.8V reference value. The TRACK1 pin must go beyond the 0.8V to ensure the slave output has reached its final value.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK pin. As mentioned above, the TRACK pin has a control range from 0V to 0.8V. The control ramp slew rate applied to the master's TRACK pin is directly equal to the master's output slew rate in Volts/Time.

The equation:

$$\frac{MR}{SR} \bullet 4.99k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 4.99k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.8V}{\frac{V_{FB}}{4.99k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.8V. Since R_{TB} is equal to the 4.99k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 4.99k and R_{TA} = 10k in Figure 2.

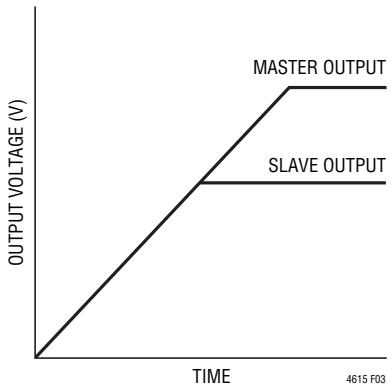


Figure 3. Output Voltage Coincident Tracking

Figure 3 shows the output voltage tracking waveform for coincident tracking.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

For example, MR = 2.5V/ms and SR = 1.8V/1ms. Then R_{TB} = 6.98k. Solve for R_{TA} to equal to 3.24k. The master output must be greater than the slave output for the tracking to work. Output load current must be present for tracking to operate properly during power-down.

Power Good

PGOOD1 and PGOOD2 are open-drain pins that can be used to monitor valid output voltage regulation. These pins monitor a ±7.5% window around the regulation point. If the output is disabled, the respective pin will go low.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for all output voltages. Table 4 is provided for most application requirements. The LTpowerCAD Design Tool is provided for other control loop optimization. The COMP pins must be tied together in parallel operation.

Parallel Switching Regulator Operation

The LTM4615 switching regulators are inherently current mode control. Paralleling will have very good current sharing. This will balance the thermals on the design. Figure 13 shows a schematic of a parallel design. The voltage feedback equation changes with the variable N as channels are paralleled.

The equation:

$$V_{OUT} = 0.8V \bullet \frac{\frac{4.99k}{N} + R_{FB}}{R_{FB}}$$

N is the number of paralleled channels.

APPLICATIONS INFORMATION

VLDO SECTION

Adjustable Output Voltage

The output voltage is set by the ratio of two resistors. A 4.99k resistor is built onboard the module from LDO_OUT to FB3. An additional resistor (R_{FBLDO}) is required from FB3 to GND3 to set the output voltage over a range of 0.4V to 2.6V. Minimum output current of 1mA is required for full output voltage range.

The equation:

$$V_{LDO\_OUT} = 0.4V \bullet \frac{4.99k + R_{FBLDO}}{R_{FBLDO}}$$

or equivalently,

$$R_{FBLDO} = \frac{4.99k}{\frac{V_{LDO\_OUT}}{0.4V} - 1}$$

Power Good Operation

The VLDO includes an open-drain power good (PGOOD3) pin with hysteresis. If the VLDO is in shutdown or under UVLO conditions (BOOST3 < 4.2V), then PGOOD3 is low impedance to ground. PGOOD3 becomes high impedance when the VLDO output voltage rises to 93% of its regulated voltage. PGOOD3 stays high impedance until the output voltage falls to 91% of its regulated voltage. A pull-up resistor can be inserted between the PGOOD3 pin and a positive logic supply such as the VLDO output or V_{IN}. LDO_IN should be at least 1.14V or greater for power good to operate properly.

Output Capacitance and Transient Response

The VLDO is designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitors affects stability, especially smaller value capacitors. An output capacitor of 10µF or greater with an ESR of 0.05Ω or less is recommended to ensure stability. Larger value capacitors can be used to reduce the transient deviations under load changes. Bypass capacitors that are used at the load device can also increase the effective output capacitance. High ESR tantalum or electrolytic bulk capacitance can be used, but a ceramic capacitor must be used in parallel at the output.

Extra consideration should be given to the use of ceramic capacitors related to dielectrics, temperature and DC bias effects on the capacitor. The VLDO requires a minimum 10µF value. The X7R and X5R dielectrics are more stable with DC bias and temperature, thus more preferred.

Short-Circuit/Thermal Protection

The VLDO has built-in short-circuit current limiting of ~3A as well as overtemperature protection. During short-circuit conditions the device is in control to 3A, and as the internal temperature rises to approximately 150°C, then the internal boost and LDO are shut down until the internal temperature drops back to 140°C. The device will cycle in and out of this mode with no latchup or damage. Long term over stress in this condition can degrade the device over time.

Reverse Current Protection

The VLDO features reverse current protection to limit current draw from any supplementary power source at the output. Figure 4 shows the reverse input current limit versus input voltage for a nominal V_{LDO_OUT} setpoint of 1.5V. Note: Positive input current represents current flowing into the LDO_IN pin. With LDO_OUT held at or below the output regulation voltage and LDO_IN varied, input current flow will follow the Figure 4 curve. Input reverse current ramps up to 16µA as LDO_IN approaches LDO_OUT.

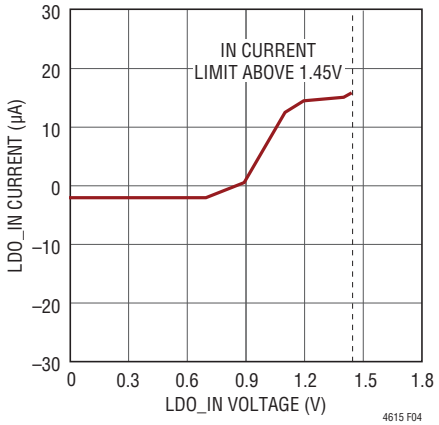


Figure 4. Reverse Current Limit for VLDO

APPLICATIONS INFORMATION

Reverse input current will spike up as LDO_IN gets to within about 30mV of LDO_OUT as reverse current protection circuitry is disabled and normal operation resumes. As LDO_IN transitions above LDO_OUT the reverse current transitions into short circuit current as long as LDO_OUT is held below the regulation voltage.

Thermal Considerations and Output Current Derating

The power loss curves in Figures 5 and 6 can be used in coordination with the load current derating curves in Figures 7 to 10 for calculating an approximate θ_{JA} thermal resistance for the LTM4615 with various heat sinking and airflow conditions. Both of the LTM4615 outputs are at full 4A load current, and the power loss curves in Figures 5 and 6 are combined power losses plotted for both output voltages up to 4A each. The VLDO regulator is set to have a power dissipation of 0.5W since it is generally used with dropout voltages of 0.5V or less. For example: 1.2V to 1V, 1.5V to 1V, 1.5V to 1.2V and 1.8V to 1.5V. Other dropout voltages can be supported at VLDO maximum load, but further thermal analysis will be required for the VLDO. The 4A output voltages are 1.2V and 3.3V. These voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The junctions are maintained at ~120°C while lowering output current or power with increasing ambient temperature. The 120°C value is chosen to allow for a 5°C margin window relative to the maximum 125°C limit. The decreased output current will decrease the internal module loss as ambient temperature is increased. The power loss curves in Figures 5 and 6 show this amount of power loss as a function of load current that is specified for both channels. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 7 the load current is derated to 3A for each channel with 0LFM at ~90°C and the power loss for both channels at 5V to 1.2V at 3A output is ~1.4W. Add the VDLO power loss of 0.5W to equal 1.9W. If the 90°C ambient temperature is subtracted from the 120°C maximum junction temperature, then the difference of 30°C divided by 1.9W equals a 15.7°C/W thermal resistance. Table 2 specifies a 15°C/W value which is very close. Table 2 and Table 3 provide equivalent thermal resistances for 1.2V and 3.3V outputs with and without air flow and heat sinking. The combined power loss for the two 4A outputs plus the VLDO power loss can be summed together and multiplied by the thermal resistance values in Tables 2 and 3 for module temperature rise under the specified conditions. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and 1 ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed below Table 3. The data sheet lists the θ_{JC} (Junction to Case) thermal resistances under the Pin Configuration diagram.

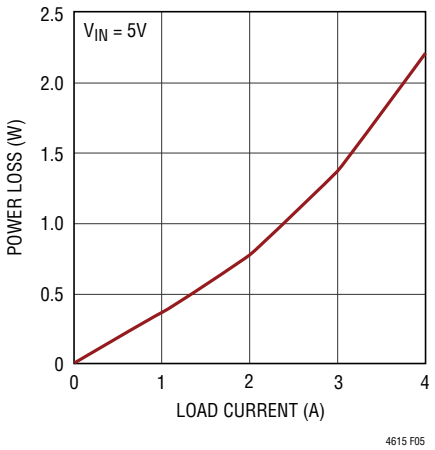


Figure 5. 1.2V Power Loss

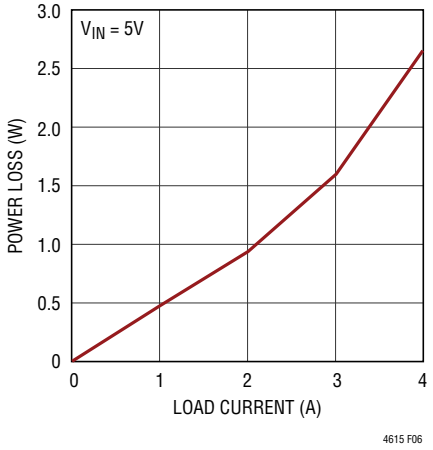


Figure 6. 3.3V Power Loss

APPLICATIONS INFORMATION

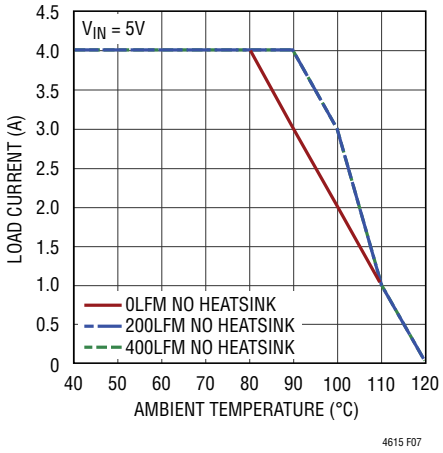


Figure 7. 1.2V No Heat Sink

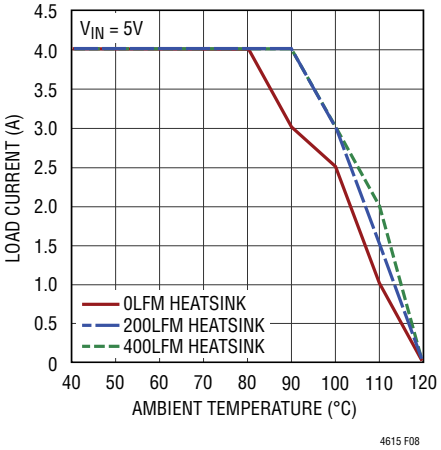


Figure 8. 1.2V Heat Sink

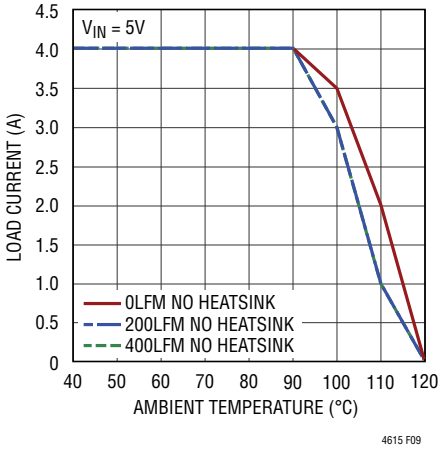


Figure 9. 3.3V No Heat Sink

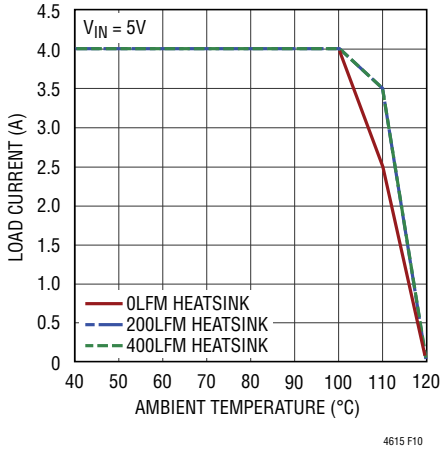


Figure 10. 3.3V Heat Sink

APPLICATIONS INFORMATION

Table 2. 1.2V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 7	5	Figure 5	0	None	15
Figure 7	5	Figure 5	200	None	12
Figure 7	5	Figure 5	400	None	10
Figure 8	5	Figure 5	0	BGA Heat Sink	14
Figure 8	5	Figure 5	200	BGA Heat Sink	9
Figure 8	5	Figure 5	400	BGA Heat Sink	8

Table 3. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9	5	Figure 6	0	None	15
Figure 9	5	Figure 6	200	None	12
Figure 9	5	Figure 6	400	None	10
Figure 10	5	Figure 6	0	BGA Heat Sink	14
Figure 10	5	Figure 6	200	BGA Heat Sink	9
Figure 10	5	Figure 6	400	BGA Heat Sink	8

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid	375424B00034G	www.aavid.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

APPLICATIONS INFORMATION

Safety Considerations

The LTM4615 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4615 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
- Do not put via directly on pads unless the via is capped.

Figure 11 gives a good example of the recommended layout.

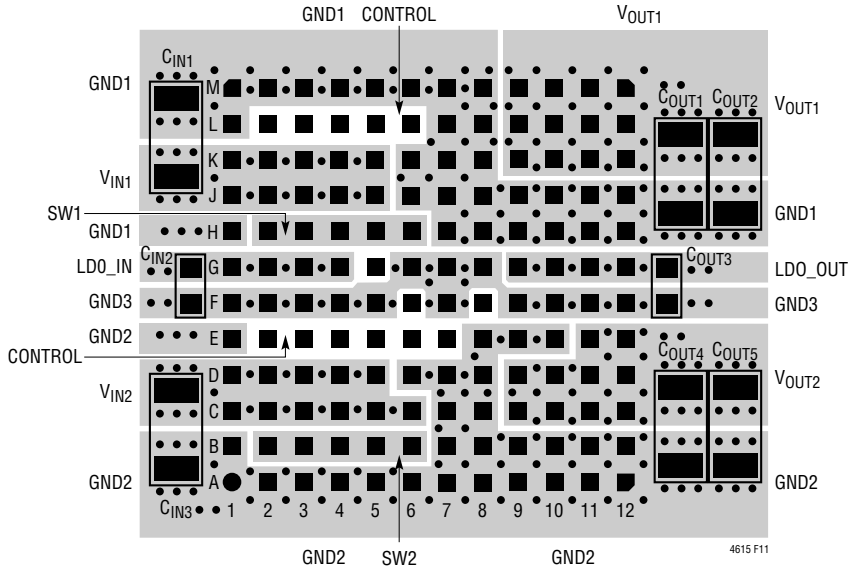


Figure 11. Recommended PCB Layout

APPLICATIONS INFORMATION

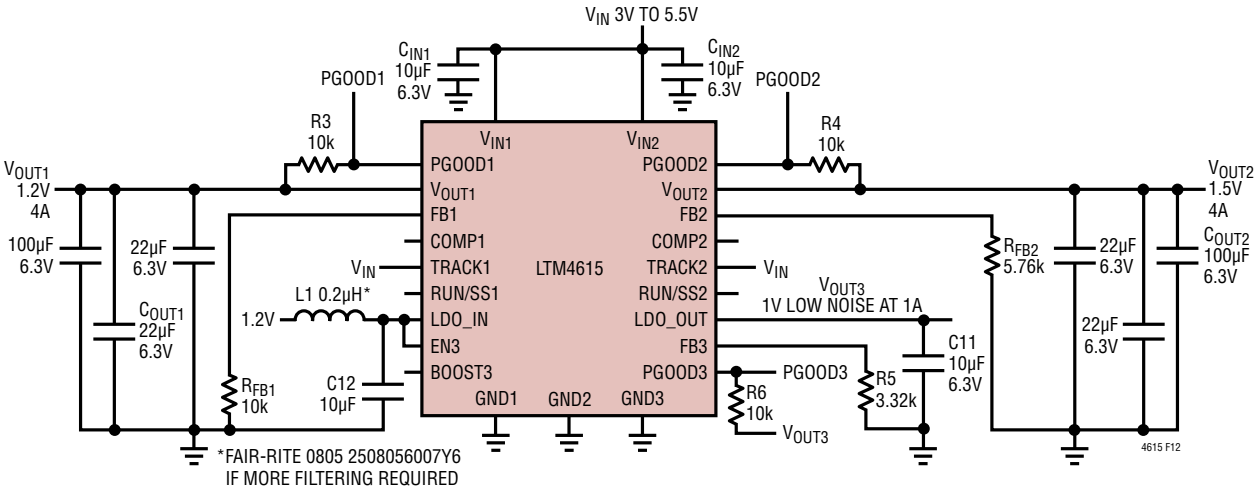


Figure 12. Typical 3V to 5.5V_{IN}, 1.5V and 1.2V at 4A and 1V at 1A Design

Table 4. Output Voltage Response vs Component Matrix (Refer to Figure 12) 0A to 2.5A Load Step Typical Measured Values

C_{OUT1} AND C_{OUT2} CERAMIC VENDORS	VALUE	PART NUMBER	C_{OUT1} AND C_{OUT2} BULK VENDORS	VALUE	PART NUMBER
TDK	22µF 6.3V	C3216X7SOJ226M	Sanyo POSCAP	150µF 10V	10TPD150M
Murata	22µF 16V	GRM31CR61C226KE15L	Sanyo POSCAP	220µF 4V	4TPE220MF
TDK	100µF 6.3V	C4532X5R0J107MZ	**C_{IN} BULK VENDORS**	**VALUE**	**PART NUMBER**
Murata	100µF 6.3V	GRM32ER60J107M	Sanyo POSCAP	100µF 10V	10CE100FH

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)*	C_{OUT1} AND C_{OUT2} (CER) EACH	C_{OUT1} AND C_{OUT2} (POSCAP) EACH	I_{TH}	V_{IN} (V)	DROOP (mV)	PEAK-TO-PEAK DEVIATION	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)
1.2	10µF ×2	100µF	100µF, 22µF ×2	None	None	5	33	68	11	2.5	10
1.2	10µF ×2	100µF	22µF ×1	220µF	None	5	25	50	9	2.5	10
1.2	10µF ×2	100µF	100µF, 22µF ×2	None	None	3.3	33	68	8	2.5	10
1.2	10µF ×2	100µF	22µF ×1	220µF	None	3.3	25	50	10	2.5	10
1.5	10µF ×2	100µF	100µF, 22µF ×2	None	None	5	30	60	11	2.5	5.76
1.5	10µF ×2	100µF	22µF ×1	220µF	None	5	28	60	11	2.5	5.76
1.5	10µF ×2	100µF	100µF, 22µF ×2	None	None	3.3	30	60	10	2.5	5.76
1.5	10µF ×2	100µF	22µF ×1	220µF	None	3.3	27	56	10	2.5	5.76
1.8	10µF ×2	100µF	100µF, 22µF ×2	None	None	5	34	68	12	2.5	3.92
1.8	10µF ×2	100µF	22µF ×1	220µF	None	5	30	60	12	2.5	3.92
1.8	10µF ×2	100µF	22µF ×1	220µF	None	3.3	30	60	12	2.5	3.92
2.5	10µF ×2	None	22µF ×1	None	None	5	50	90	10	2.5	2.37
2.5	10µF ×2	100µF	22µF ×1	150µF	None	5	33	60	10	2.5	2.37
2.5	10µF ×2	100µF	22µF ×1	150µF	None	3.3	50	95	12	2.5	2.37
3.3	10µF ×2	100µF	22µF ×1	150µF	None	5	50	90	12	2.5	1.62

*Bulk capacitance is optional if V_{IN} has very low input impedance.

APPLICATIONS INFORMATION

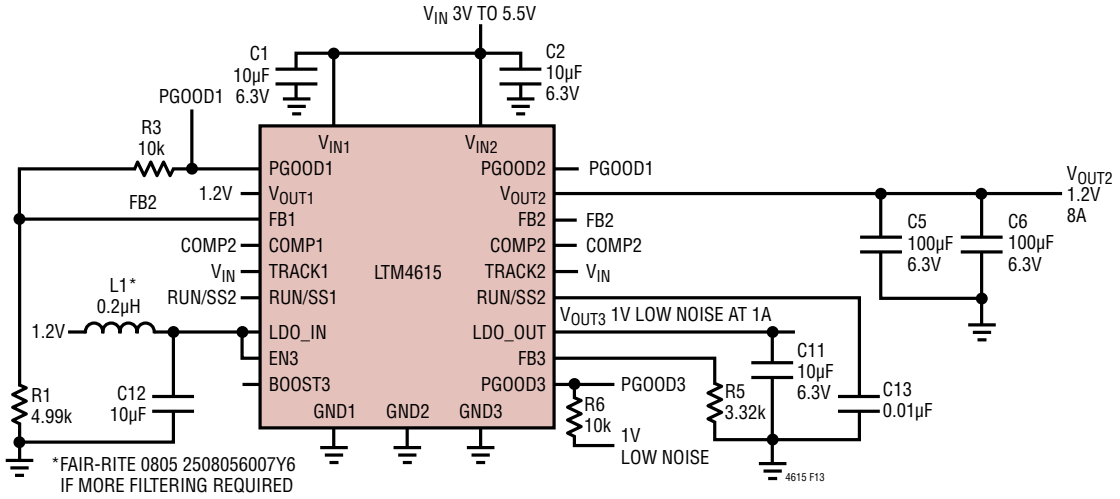


Figure 13. LTM4615 Parallel 1.2V at 8A Design, 1V at 1A Design

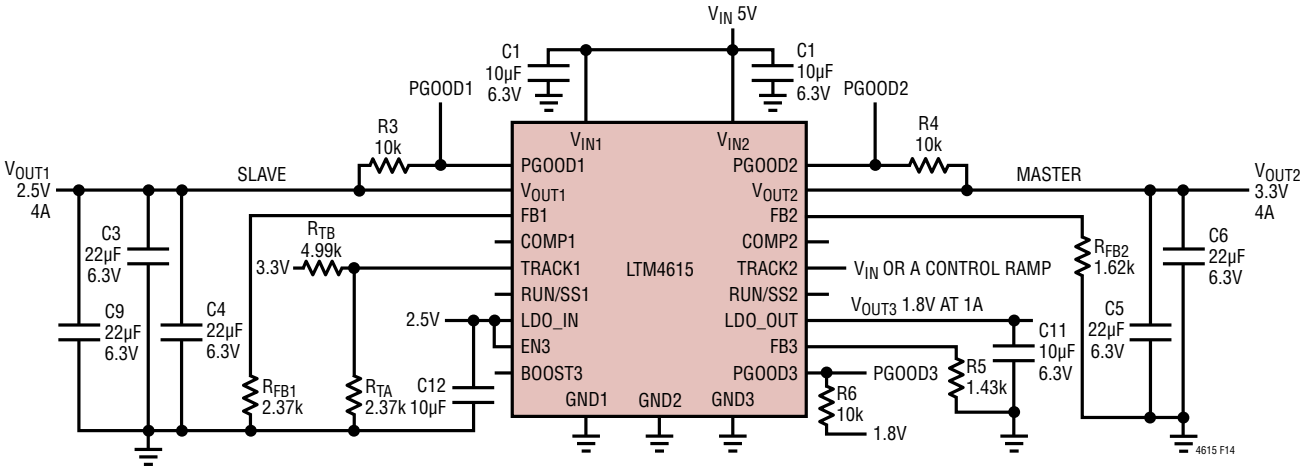
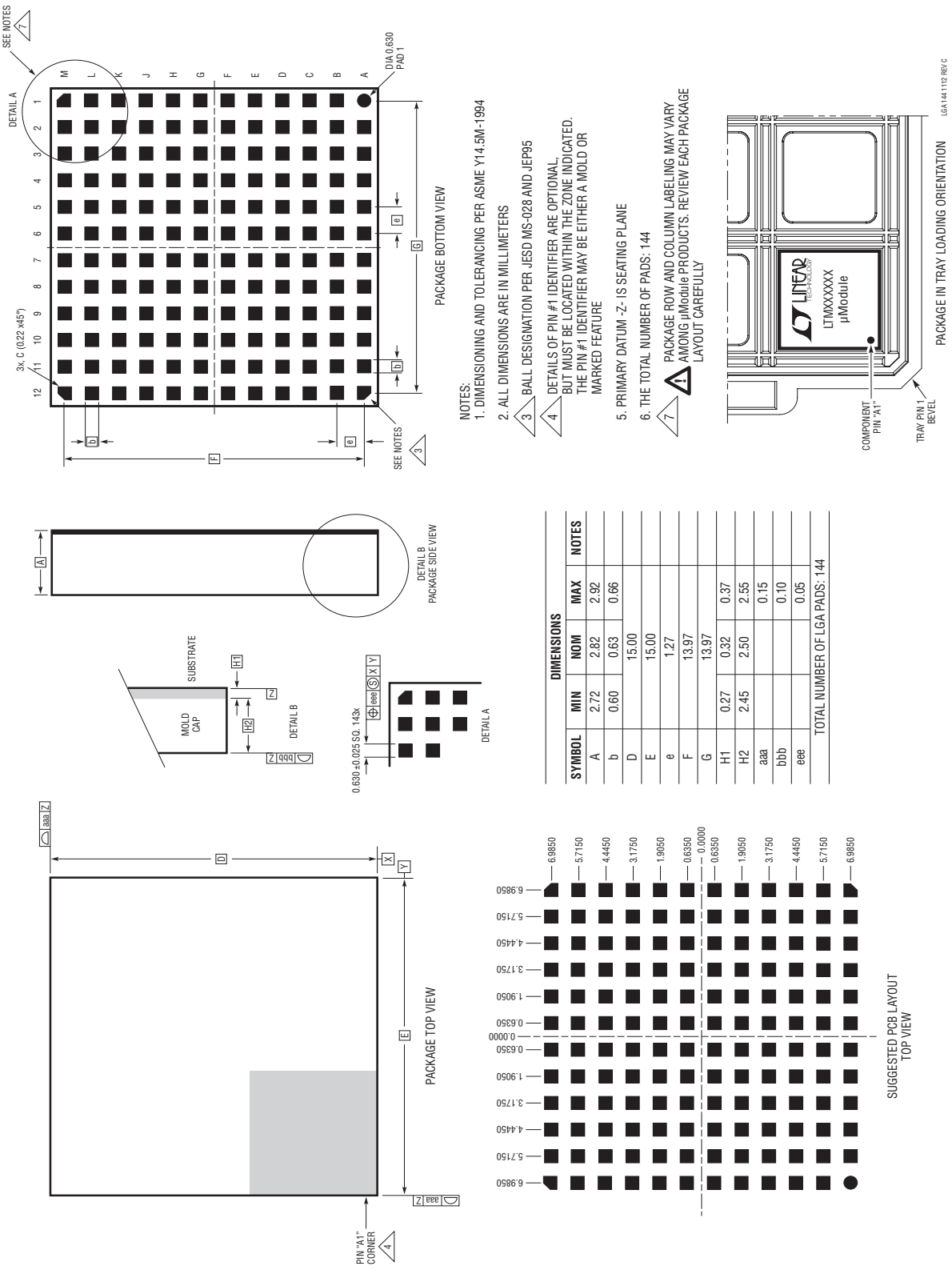


Figure 14. 3.3V and 2.5V at 4A with Output Voltage Tracking Design, 1.8V at 1A

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LGA Package
144-Lead (15mm × 15mm × 2.82mm)
(Reference LTC DWG # 05-08-1816 Rev C)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.72	2.82	2.92	
b	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 144				

PACKAGE DESCRIPTION

LTM4615 Component LGA Pinout

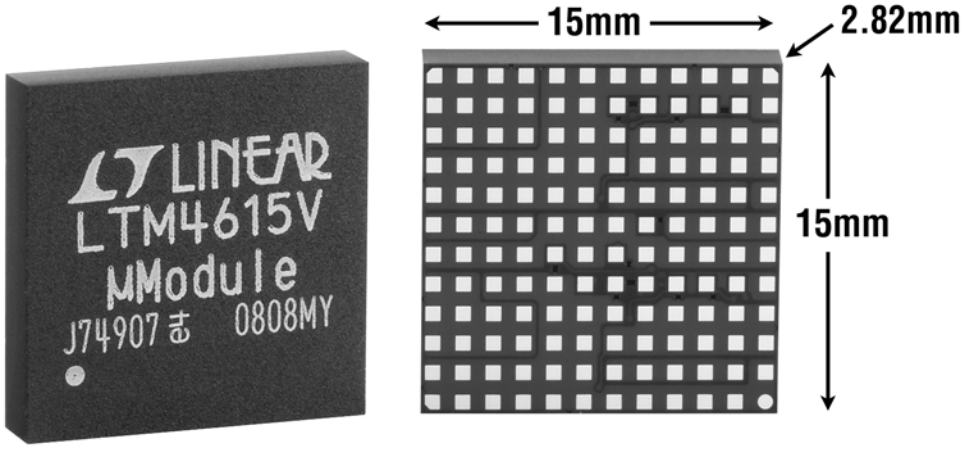
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND2	B1	GND2	C1	V_{IN2}	D1	V_{IN2}	E1	GND2	F1	GND3
A2	GND2	B2	SW2	C2	V_{IN2}	D2	V_{IN2}	E2	RUN/SS2	F2	GND3
A3	GND2	B3	SW2	C3	V_{IN2}	D3	V_{IN2}	E3	TRACK2	F3	GND3
A4	GND2	B4	SW2	C4	V_{IN2}	D4	V_{IN2}	E4	PGOOD2	F4	GND3
A5	GND2	B5	SW2	C5	V_{IN2}	D5	V_{IN2}	E5	COMP2	F5	GND3
A6	GND2	B6	SW2	C6	V_{IN2}	D6	GND2	E6	FB2	F6	FB3
A7	GND2	B7	GND2	C7	GND2	D7	GND2	E7	BOOST3	F7	GND3
A8	GND2	B8	GND2	C8	GND2	D8	GND2	E8	GND2	F8	EN3
A9	GND2	B9	GND2	C9	V_{OUT2}	D9	V_{OUT2}	E9	GND2	F9	GND3
A10	GND2	B10	GND2	C10	V_{OUT2}	D10	V_{OUT2}	E10	GND2	F10	GND3
A11	GND2	B11	GND2	C11	V_{OUT2}	D11	V_{OUT2}	E11	V_{OUT2}	F11	GND3
A12	GND2	B12	GND2	C12	V_{OUT2}	D12	V_{OUT2}	E12	V_{OUT2}	F12	GND3

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	LDO_IN	H1	GND1	J1	V_{IN1}	K1	V_{IN1}	L1	GND1	M1	GND1
G2	LDO_IN	H2	SW1	J2	V_{IN1}	K2	V_{IN1}	L2	RUN/SS1	M2	GND1
G3	LDO_IN	H3	SW1	J3	V_{IN1}	K3	V_{IN1}	L3	TRACK1	M3	GND1
G4	LDO_IN	H4	SW1	J4	V_{IN1}	K4	V_{IN1}	L4	PGOOD1	M4	GND1
G5	PGOOD3	H5	SW1	J5	V_{IN1}	K5	V_{IN1}	L5	COMP1	M5	GND1
G6	GND3	H6	SW1	J6	GND1	K6	GND1	L6	FB1	M6	GND1
G7	GND3	H7	GND1	J7	GND1	K7	GND1	L7	GND1	M7	GND1
G8	GND3	H8	GND1	J8	GND1	K8	GND1	L8	GND1	M8	GND1
G9	LDO_OUT	H9	GND1	J9	GND1	K9	V_{OUT1}	L9	V_{OUT1}	M9	V_{OUT1}
G10	LDO_OUT	H10	GND1	J10	GND1	K10	V_{OUT1}	L10	V_{OUT1}	M10	V_{OUT1}
G11	LDO_OUT	H11	GND1	J11	GND1	K11	V_{OUT1}	L11	V_{OUT1}	M11	V_{OUT1}
G12	LDO_OUT	H12	GND1	J12	GND1	K12	V_{OUT1}	L12	V_{OUT1}	M12	V_{OUT1}

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/12	Added pin functions to the Pin Configuration diagram. Updated EN3 in the Absolute Maximum Ratings section. Corrected the V_{OUT} accuracy limit.	2
		Clarified the SW1 and SW2 electrical connections.	8
		Added the internal power inductor value to the Block Diagram.	9
		Clarified the PGOOD behavior.	13
		Clarified the reverse current protection behavior.	14
		Added the suggested heat sink.	17
B	07/13	Changed “Overcurrent Foldback” to “Overtemperature”	12

PACKAGE PHOTOGRAPH



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4628	26V, Dual 8A, DC/DC Step-Down µModule Regulator	$4.5V \le V_{IN} \le 26.5V$, $0.6V \le V_{OUT} \le 5V$, Remote Sense Amplifier, Internal Temperature Sensing Output, 15mm × 15mm × 4.32mm LGA
LTM4627	20V, 15A DC/DC Step-Down µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5V$, PLL Input, V_{OUT} Tracking, Remote Sense Amplifier, 15mm × 15mm × 4.32mm LGA
LTM4611	$1.5V_{IN(MIN)}$, 15A DC/DC Step-Down µModule Regulator	$1.5V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking, 15mm × 15mm × 4.32mm LGA
LTM4618	6A DC/DC Step-Down µModule Regulator	$4.5V \le V_{IN} \le 26.5V$, $0.8V \le V_{OUT} \le 5V$, PLL Input, V_{OUT} Tracking, 9mm × 15mm × 4.32mm LGA
LTM4613	8A EN55022 Class B DC/DC Step-Down µModule Regulator	$5V \le V_{IN} \le 36V$, $3.3V \le V_{OUT} \le 15V$, PLL Input, V_{OUT} Tracking and Margining, 15mm × 15mm × 4.32mm LGA
LTM4601AHV	28V, 12A DC/DC Step-Down µModule Regulator	$4.5V \le V_{IN} \le 28V$, $0.6V \le V_{OUT} \le 5V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking and Margining, 15mm × 15mm × 2.8mm LGA or 15mm × 15mm × 3.42mm BGA
LTM4601A	20V, 12A DC/DC Step-Down µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking and Margining, 15mm × 15mm × 2.8mm LGA or 15mm × 15mm × 3.42mm BGA
LTM8027	60V, 4A DC/DC Step-Down µModule Regulator	$4.5V \le V_{IN} \le 60V$, $2.5V \le V_{OUT} \le 24V$, CLK Input, 15mm × 15mm × 4.32mm LGA
LTM8033	36V, 3A EN55022 Class B DC/DC Step-Down µModule Regulator	$3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 24V$, Synchronizable, 11.25mm × 15mm × 4.32mm LGA
LTM8061	32V, 2A Step-Down µModule Battery Charger with Programmable Input Current Limit	Compatible with Single Cell or Dual Cell Li-Ion or Li-Poly Battery Stacks (4.1V, 4.2V, 8.2V, or 8.4V), $4.95V \le V_{IN} \le 32V$, C/10 or Adjustable Timer Charge Termination, NTC Resistor Monitor Input, 9mm × 15mm × 4.32mm LGA

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