30V to 58V Input, Dual 30A, Single 60A µModule Regulator with Digital Power System Management

FEATURES

- **Complete 48V Input to Low Voltage Dual 30A Supply that Can Scale to 300A, Nonisolated**
- Dual Analog Loops with Digital Interface for Compensation, Control and Monitoring
- Input Voltage Range: 30V to 58V
- Output Voltage Range: 0.5V to 1.2V at 30A/Channel
- ±3% Output Current Readback Accuracy (–20° to 125°C)
- 87% Efficiency for 48V to 1V at 60A, 90% at 40A
- ±0.5% Output Voltage Accuracy Over Temperature
- 400kHz PMBus-Compliant I^2C Serial Interface
- 16mm × 16mm × 7.72mm BGA Package

APPLICATIONS

- 48V Systems
- Computer and Networking Equipment
- Electronic Test Equipment
- Storage Systems

Click to view associated TechClip Videos.

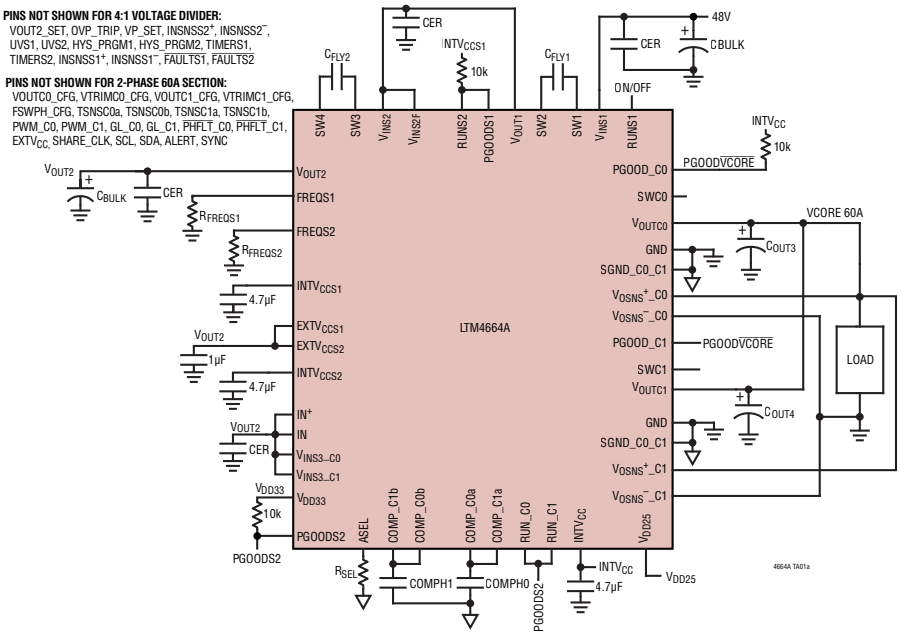
DESCRIPTION

The LTM®4664A is a complete nonisolated 48V input high efficiency step-down µModule® regulator with dual 30A outputs. The switching controllers, power MOSFETs, inductors and supporting components are included. Only external capacitors are needed to complete the design. Operating over a 30V to 58V input voltage range, the LTM4664A supports an output voltage of 0.5V to 1.5V at up to 75W. An intermediate output at 25% • V_{IN} is also available. The LTM4664A product video is available on the website.

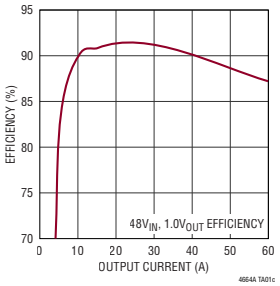
The LTM4664A dual 30A regulators utilize digitally programmable analog control loops, precision data acquisition circuitry and EEPROM with ECC. The LTM4664A's 2-wire serial interface allows the 30A outputs to be margined, tuned and ramped up and down at programmable slew rates and sequencing delay times. True input current sense, output currents and voltages, input and output power, temperatures, uptime and peak values are all readable for Dual 30A Power System Management (PSM) channels.

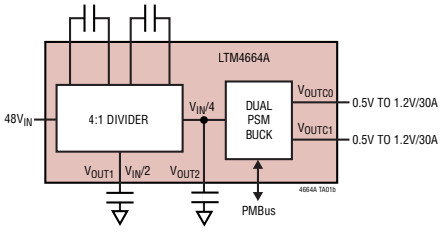
TYPICAL APPLICATION

48V to VCORE at 60A



48V to 1V Up to 60A





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ABSOLUTE MAXIMUM RATINGS

(Note 1)

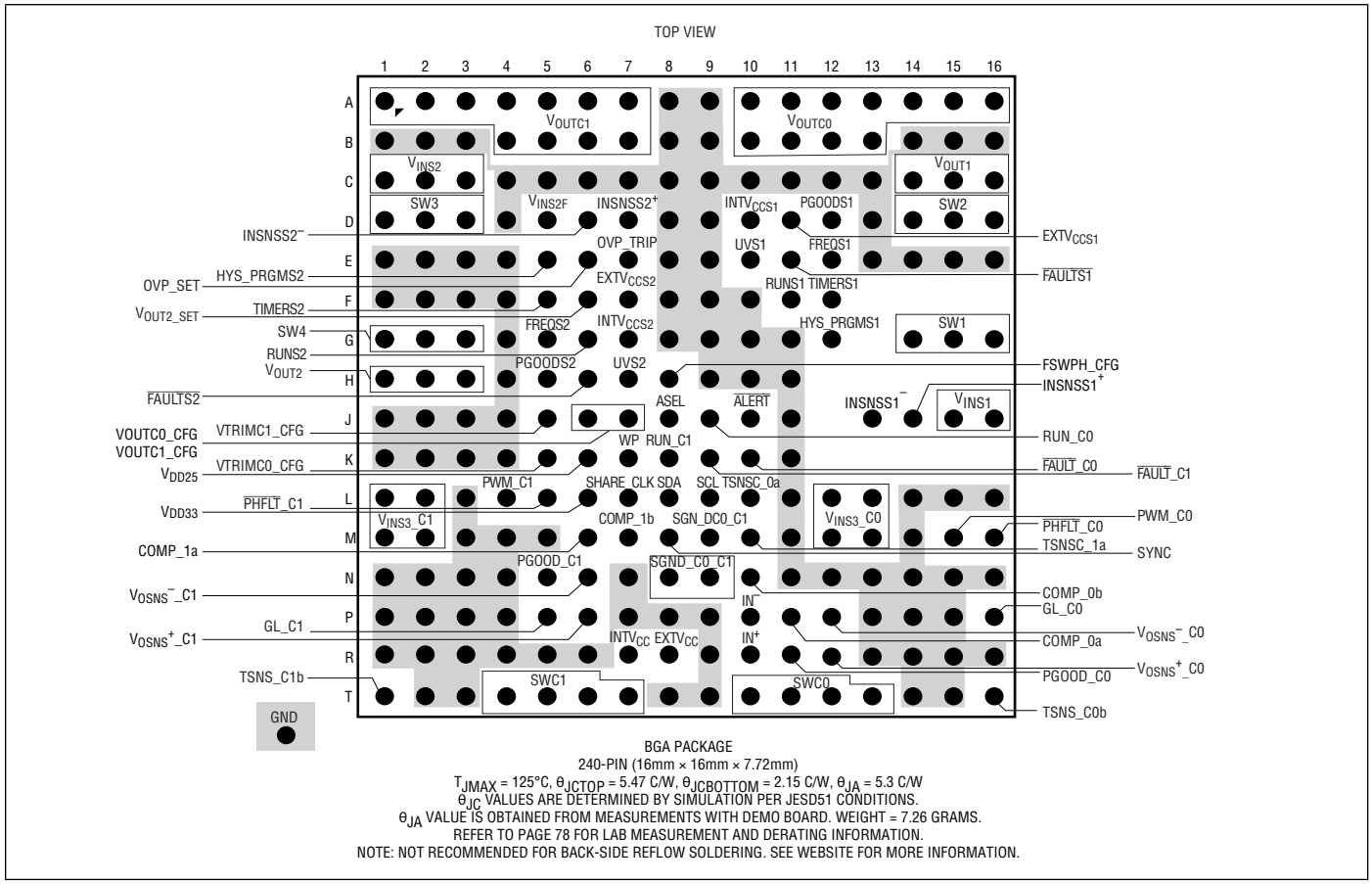
4:1 Divider

V_{INS1}, SW1, SW2, INSNSS1+, INSNSS1–, $\overline{FAULTS1}$, $\overline{FAULTS2}$ ..... –0.3V to 60V
V_{INS2}, V_{INS2F}, INSNSS2+, INSNSS2–, PGOODS1, PGOODS2, $EXTV_{CCS1}$, $EXTV_{CCS2}$, SW3, SW4, OVP_SET, VOUT2_SET, OVP_TRIP, V_{OUT1} ..... –0.3V to 40V
V_{OUT2} ..... 0.3V to 20V
$INTV_{CCS1}$, $INTV_{CCS2}$ ..... OUTPUT ONLY, RATED 6V
RUNS1, RUNS2 ..... –0.3V to 6V
UVS1, UVS2, HYS_PRGMS1, HYS_PRGMS2, TIMERS1, TIMERS2, FREQS1, FREQS2 ..... –0.3V to $INTV_{CCS1}$, –0.3 to $INTV_{CCS2}$

DUAL 25A/30A PSM SECTION

V_{INS3_Cn}, IN+, IN– ..... –0.3V to 18V
(V_{INS3_Cn} – IN+), (IN+ – IN–) ..... –0.3V to 0.3V
SWC0, SWC1 ..... –1V to 18V, –5V to 18V Transient
$EXTV_{CC}$ ..... –0.3V to 6V
V_{OUTCn} ..... –0.3V to 3.6V
V_{OSNS}+_C*n* ..... –0.3V to 6V
V_{OSNS}–_C*n* ..... –0.3V to 0.3V
RUN_C*n*, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
FSWPH_CFG, VOUTC*n*_CFG, VTRIMC*n*_CFG, ASEL, COMP_1a, COMP_1b, COMP_0a, COMP_0b ..... –0.3V to 2.75V
$\overline{FAULT}$_C*n*, SYNC, SHARE_CLK, WP, PGOOD_C*n*, PWM_C*n*, $\overline{PHFLT}$_C*n* ..... –0.3V to 3.6V
TSNS_C*n*a, ... –0.3V to 2.2V
TSNS_C*n*b ..... –0.3V to 0.8V, < 5mA
OVP-SET I_{MAX} Sink 5mA
$INTV_{CC}$ V_{DD33}, V_{DD25} and GL_C*n* are Outputs.
Internal Operating Temperature Range (Notes 2, 14, 15) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow (Package Body) Temperature 245°C

PIN CONFIGURATION



BGA PACKAGE
240-PIN (16mm × 16mm × 7.72mm)
T_{JMAX} = 125°C, θ_{JCTOP} = 5.47 C/W, $\theta_{JCBOTTOM}$ = 2.15 C/W, θ_{JA} = 5.3 C/W
θ_{JC} VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
θ_{JA} VALUE IS OBTAINED FROM MEASUREMENTS WITH DEMO BOARD. WEIGHT = 7.26 GRAMS.
REFER TO PAGE 78 FOR LAB MEASUREMENT AND DERATING INFORMATION.
NOTE: NOT RECOMMENDED FOR BACK-SIDE REFLOW SOLDERING. SEE WEBSITE FOR MORE INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4664AIY#PBF	SAC305 (RoHS)	LTM4664AY	e1	BGA	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the internal operating junction temperature. T_A = 25°C, V_{INS1} = 48V, and RUN*n* = 5V where *n* = stage # unless otherwise noted. See Figure 46 configuration for setup. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
4:1 Divider Section							
V_{INS1}	Input DC Voltage Stage 1	Note 4		30		58	V
V_{INS2}	Input DC Voltage Stage 2	Note 4		15		29	V
V_{OUT1} Range	V_{OUT1} Output Range	Note 4		15		29	V
V_{OUT2} Range	V_{OUT2} Output Range	Note 4		7.5V		14.5	V
Maximum Power	Maximum Output Power	All Conditions, Note 4				75	W
$V_{OUT1(DC)}$	V_{OUT1} OUTPUT	Note 4, Based on Figure 49 V_{INS1} = 48V, RUN = 5V, IV_{OUT1} = 0A	●	23.5	24	24.5	V
$V_{OUT2(DC)}$	V_{OUT2} OUTPUT	Note 4, Based on Figure 49 V_{INS2} = 24V, RUN = 5V, IV_{OUT2} = 0A	●	11.5	12	12.5	V
V_{UVLO}	Undervoltage Lockout	$INTV_{CC}$ Falling $INTV_{CC}$ Rising			4.85 5.05		V V
IQ V_{INSn}	V_{INS1}, V_{INS2} Quiescent Current Each Stage	RUN*n* = 0V RUN*n* = 5V, No Switching RUN*n* = 5V, Switching			150 1.6 44		µA mA mA
Overcurrent Protection Section							
$INSNSS1^+$	Stage 1 Current Sense+	$INSNSS1^+$ = $INSNSS1^-$ = 60V V_{OUT1} = 30V, RUNS1 = 5V			220	350	µA
$INSNSS2^+$	Stage 2 Current Sense+	$INSNSS2^+$ = $INSNSS2^-$ = 30V V_{OUT2} = 15V, RUNS2 = 5V			220	350	µA
$INSNSS1^-$	Stage 1 Current Sense–	$INSNSS1^+$ = $INSNSS1^-$ = 60V, RUNS1 = 0V	●	–5	1	5	µA
$INSNSS2^-$	Stage 2 Current Sense–	$INSNSS2^+$ = $INSNSS2^-$ = 30V, RUNS2 = 0V	●	–5	1	5	µA
INSNSS1, INSNSS2 Threshold	Current Limit Threshold for Each Stage		●	45	50	55	mV
Pre Charge Balance							
R_{VINS2F}	V_{INS2} Resistance to GND	See Block Diagram (Note 10)			1		MΩ
R_{VF2}	Resistance Between Pins V_{INS2} to V_{INS2F}	See Block Diagram Part of a RC Filter Stage 2			1		kΩ
$INSNSS1^+$ Balance Current	Stage 1 Current Sense + Source	Pre-Balance Phase V_{INS1} = 60V $INSNSS1^+$ = $INSNSS1^-$ = 60V, V_{OUT1} = 15V , Timer = 1V			95		mA
$INSNSS2^+$ Balance Current	Stage 2 Current Sense + Source	Pre-Balance Phase V_{INS2} = 30V $INSNSS2^+$ = $INSNSS2^-$ = 30V, V_{OUT2} = 10V, Timer = 1V			95		mA
I_{SOURCE} V_{OUTn}	I_{SOURCE} Current to Pre-Start Up Balance V_{OUTn} and C_{FLYn}, n = Stage #	$INSNSS_n$ = V_{INSn} = 24V V_{OUTn} = 10V, Timer = 0.8V See Block Diagram			95		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the internal operating junction temperature. T_A = 25°C, V_{INS1} = 48V, and RUN*n* = 5V where *n* = stage # unless otherwise noted. See Figure 46 configuration for setup. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SINK} V_{OUTn}	I_{SINK} Current to Pre-Start Up Balance V_{OUTn} and C_{FLYn}, *n* = Stage #	INSNSS*n* = V_{INSn} = 24V V_{OUTn} = 11V, Timer = 0.8V See Block Diagram			50		mA
RUNn Pins							
V_{TH_RUNn}	Run PIN Threshold *n* = Stage #	V_{RUN} Rising	●	1.1	1.22	1.4	V
V_{RUNn} HYS	Run Pin Hysteresis *n* = Stage #				90		mV
OVP Comparator							
OVP-SET In	OVP-SET Input Range MAX				25		V
$V_{OUT2\text{-}SET}$	$V_{OUT2\text{-}SET}$ Range MAX				25		V
I_B	Input Bias I	V_{CM} = 0V to 25V			30		mA
V_{OS}	Input Offset	0.5V < V_{CM} < 25V			3		mV
PSRR	Power Supply Rejection	0.5V < V_{CM} < 25V (Note 10)			85		db
CMRR	Common Mode Rejection	0.5V < V_{CM} < 25V (Note 10)			80		db
Delay	Propagation Delay				10		µs
OVP_Trip Sink	OVP_Trip Sink	I_{SINK} = 5mA (Note 10)			0.35		V
$INTV_{CC}$ Regulators							
$VINTV_{CCSn}$	Internal (LDO) Low Drop Out Regulator, *n* = Stage #	30V < V_{INS1} < 58V, $V_{EXTVCCS1}$ = 0V, Stage 1 15V < V_{INS2} < 19V, $V_{EXTVCCS2}$ = 0V, Stage 2		5.4	5.6	5.9	V
$VINTV_{CCSn}$ Load	LDO Load Regulation	I_{CC} = 50mA, $VEXTV_{CCSn}$ = 0V			0.5	2	%
$INTV_{CCSn}$ IPeak	$INTV_{CC}$ Stage Peak Output Current				150		mA
$VINTV_{CCSn}$ with $EXTV_{CC}$	LDO Output Range with $EXTV_{CCn}$, *n* = Stage #	12V < $VEXTV_{CCn}$ < 24V, V_{INSn} = 12V		5.4	5.6	5.9	V
$VINTV_{CCSn}$ Load EXT	LDO Load Regulation with $EXTV_{CC}$	I_{CC} = 50mA, $VEXTV_{CCn}$ = 6.5V			1	2	%
$VEXTV_{CCn}$ Threshold	$EXTV_{CCn}$ Switch Over	$VEXTV_{CCn}$ Ramping Positive		6.3	6.5	6.65	V
$VEXTV_{CCn}$ HYS	$EXTV_{CCn}$ Hysteresis				400		mV
Switching Oscillator							
Frequency Range *n*	Frequency Range	*n* = Stage #		100		1000	kHz
f_{NOM} Stage 1	Optimized Efficiency Freq. Stage 1	FREQS1. Pin Resistor = 36.5k			100		kHz
f_{NOM} Stage 2	Optimized Efficiency Freq. Stage 2	FREQS2. Pin Resistor = 60.4k			200		kHz
Output Specifications							
$\Delta V_{OUT}/V_{OUT}$ Stage 1	Stage 1 Load Regulation Accuracy	V_{OUT1} = 24V, 0A to 3.2A Maximum = 75W V_{INS1} = 48V, FREQS1 = 100kHz C_{INB1} = 33µF (Bulk Input Capacitor) C_{IN1} = 2.2µF 100V Ceramic, C_{FLY1} = 10µF 50V X6 C_{OUT1} = 10µF 50V			3.5		%
V_{OUT1} Output Load	V_{OUT1} Max Load Current (Note 4)	V_{OUT1} = 24V, 0A to 3.2A Maximum = 75W V_{INS1} = 48V, FREQS1 = 100kHz C_{INB1} = 33µF (Bulk Input Capacitor) C_{IN1} = 2.2µF 100V Ceramic, C_{FLY1} = 10µF 50V X6 C_{OUT1} = 10µF 50V				3.2	A
M1-M4 RDS-ON	Stage 1 MOSFET On Resistance	VGS = 5V (Note 16)			18		mΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the internal operating junction temperature. T_A = 25°C, V_{INS1} = 48V, and RUN*n* = 5V where *n* = stage # unless otherwise noted. See Figure 46 configuration for setup. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{OUT}/V_{OUT}$ Stage 2	Stage 2 Load Regulation Accuracy	V_{OUT2} = 12V, 0A to 6.3A Maximum = 75W V_{INS2} = 24V, FREQS2 = 200kHz C_{INB2} = 33µF (Bulk Input Capacitor) C_{IN2} = 10µF 50V Ceramic, C_{FLY2} = 22µF 25V X6, C_{OUT2} = 22µF 25V			5		%
V_{OUT2} Output Load	V_{OUT1} Max Load Current (Note 4)	V_{OUT2} = 12V, 0A to 6.3A Maximum = 75W V_{INS2} = 24V, FREQS2 = 200kHz C_{INB2} = 33µF (Bulk Input Capacitor) C_{IN2} = 10µF 50V Ceramic, C_{FLY2} = 22µF 25V X6, C_{OUT2} = 22µF 25V				6.3	A
M5-M8 RDS-ON	Stage 2 MOSFET On Resistance	VGS = 5V (Note 16)			10		mΩ
V_{OUT1}, (AC)	Output Ripple Voltage	V_{OUT1} = 24V, 0A to 3A V_{INS1} = 48V, FREQS1 = 100kHz C_{INB1} = 33µF (Input Bulk Capacitor) C_{IN1} = 2.2µF 100V Ceramic, C_{FLY1} = 10µF 50V X6 C_{OUT1} = 10µF 50V			150		mV_{pk-pk}
V_{OUT2}, (AC)	Output Ripple Voltage	V_{OUT2} = 12V, 0A to 6A V_{INS2} = 12V, FREQS2 = 200kHz C_{INB2} = 33µF (Input Bulk Capacitor) C_{IN2} = 10µF 50V Ceramic, C_{FLY2} = 22µF 25V X6, C_{OUT2} = 22µF 25V			50		mV_{pk-pk}
t_{START} Stage 1	Turn-on Time From RUN 1	V_{OUT1} = 0V at Start Up to 24V, 0A, V_{INS1} = 48V, FREQS1 = 100kHz C_{INB1} = 33µF (Input Bulk Capacitor) C_{IN1} = 2.2µF 100V Ceramic, C_{FLY1} = 10µF 50V X6 C_{OUT1} = 10µF 50V, $C_{TIMERS1}$ = 0.22µF			40		msec
t_{START} Stage 2	Turn-on Time Stage 2 From RUN 2	V_{OUT2} = 0V at Start Up to 12V, 0A, V_{INS2} = 24V, FREQS2 = 200kHz C_{INB2} = 33µF (Input Bulk Capacitor) C_{IN1} = 2.2µF 100V Ceramic, C_{FLY1} = 22µF, 25V X6 C_{OUT2} = 22µF 25V, $C_{TIMERS2}$ = 0.47µF			75		msec
HYS_PRGMn and $\overline{\text{FAULTS}}$n							
$V_{\overline{FAULTSn}}$	$\overline{\text{FAULT}}$ Voltage Low	$I_{\overline{FAULT}}$ = 2mA			0.2	0.5	V
$I_{\overline{FAULT}\_LEAKSn}$	$\overline{\text{FAULT}}$ Leakage Current	$V_{\overline{FAULT}}$ = 5V				±1	µA
I_{HYS_PRGMSn}	HYS_PRGM Setting Current		●	9	10	11	µA
$V_{\overline{FAULTSn}}$	V_{OUTSn} Fault Trip Level	V_{INSn} = 24V, V_{OUTn}, HYS_PRGMS*n* = 0V, V_{OUTSn} Ramp Up V_{OUTSn} Ramp Down	 ● ●	 12.2 11.6	 12.3 11.7	 12.45 11.8	 V V
$V_{\overline{FAULTSn}}$	V_{OUTSn} Fault Trip Level	V_{INSn} = 24V, V_{OUTn}, HYS_PRGMS*n* = 5V, V_{OUTSn} Ramp Up V_{OUTSn} Ramp Down	 ● ●	 12.7 11.1	 12.8 11.2	 12.9 11.4	 V V
$V_{\overline{FAULTSn}}$	V_{OUTSn} Fault Trip Level	V_{INSn} = 24V, V_{OUTn}, HYS_PRGMS*n* = 2.4V, V_{OUTSn} Ramp Up V_{OUTSn} Ramp Down	 ● ●	 14.15 9.5	 14.3 9.65	 14.45 9.8	 V V
UV COMPARATORn and PGOODn							
$V_{UVTHSSn}$	Undervoltage Threshold	UV Pin Voltage Rising		0.99	1.01	1.03	V
V_{HYS_PRGMSn}	Undervoltage Hysteresis				120		mV
$V_{PGOODSn}$	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.35	0.5	V
$I_{PGOODSn\_LEAK}$	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
TimerS*n*							
TimerS*n* Current	I_{TIMERn}	V_{TIMER} < 0.5V or V_{TIMER} > 1.2V			3.5		µA
		0.5V < V_{TIMER} < 1.2V			7		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 1, 2, 3). Specified as each individual output channel designated with *n* (Note 3). T_A = 25°C, V_{INS3} = 12V, RUN_C*n* = 3.3V, $EXTV_{CC}$ = 0V, FREQUENCY_SWITCH = 350kHz and V_{OUTC}*n* commanded to 1.000V unless otherwise noted. Configured with factory default EEPROM settings, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DUAL 25A/30A PSM OUTPUT							
V_{INS3}	Input DC Voltage Operating		●	7		16	V
V_{OUTC}*n*	Range of Output Voltage Regulation	V_{OUTC}*n* Diff Sensed on V_{OSNS}^{+}_C*n*/V_{OSNS}^{-}_C*n*-Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on VOUTC*n*_CFG, Differential Remote Sense Path Voltage (Notes 4, 6)	●	0.5		1.5	V
V_{OUTC}*n*(DC)	Output Voltage, Total Variation with Line and Load	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0b) VOUTC*n*_CFG Commanded to 1.000V, V_{OUTC}*n* Low Range (MFR_PWM_MODE*n*[1] = 1b) (Note 6)	● ●	0.995 0.985	1.000 1.000	1.005 1.015	V V
VINS3 UVLO	Undervoltage Lockout Threshold	$VINTV_{CC}$ Falling $VINTV_{CC}$ Rising			3.55 3.9		V V
$I_{INRUSH(VINS3)}$	Input Inrush Current at Start-Up	V_{OUTC}*n* =1V, V_{INS3} = 12V; No Load Besides Capacitors; TON_RISE*n* = 3ms			400		mA
$I_{S(VINS3,DCM)}$	Input Supply Current in Discontinuous Mode Operation	Discontinuous Mode, MFR_PWM_MODE*n*[0] = 0b, I_{OUTC}*n* = 100mA			60		mA
$I_{S(VINS3,FCM)}$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, MFR_PWM_MODE*n*[0] = 1b I_{OUT}*n* = 100mA I_{OUT}*n* = 30A V_{INS3} = 12V, V_{OUT}*n* = 1V			 80 3.0		 mA A
$I_{S(VINS3,SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN_C*n* = 0V			25		mA
Output Specifications							
I_{OUTC}*n*	Output Continuous Current Range	Utilizing MFR_PWM_MODE[7] = 0 , and Using ~I_{OUT} = 34A , Page103, (Note 4)		0		30	A
$\frac{\Delta V_{OUT}n(LINE)}{V_{OUT}n}$	Line Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 0b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0b) Open Circuit; I_{OUTC}*n* = 0A, 7V ≤ V_{IN} ≤ 16V, V_{OUT} Low Range (MFR_PWM_MODE*n*[1] = 1b), FREQUENCY_SWITCH = 350kHz (Note 6)			0.03 0.03	 ±0.2	%/V %/V
$\frac{\Delta V_{OUT}n(LOAD)}{V_{OUT}n}$	Load Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0b) 0A ≤ I_{OUT}*n* ≤ 30A, V_{OUT} Low Range, (MFR_PWM_MODE*n* [1] = 1b) (Note 6)	 ●		0.03 0.2	 0.5	% %
V_{OUT}*n*(AC)	Output Voltage Ripple				10		mV
$f_{S\ (Each\ Channel)}$	V_{OUTC}*n* Ripple Frequency	FREQUENCY_SWITCH Set to 350kHz (0xFABC)	●	320	350	380	kHz
$\Delta V_{OUTCn(START)}$	Turn-On Overshoot	TON_RISE*n* = 3ms (Note 7)			8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to 12V to Rising Edge PGOOD_C*n*, TON_DELAY*n* = 0ms, TON_RISE*n* = 3ms			30		ms
$t_{DELAY(0ms)}$	Turn-On Delay Time	Time from First Rising Edge of RUN_C*n* to Rising Edge of PGOOD_C*n*. TON_DELAY*n* = 0ms, TON_RISE*n* = 3ms, V_{INS3} Having Been Established for at Least 70ms	●	2.9	3.3	3.7	ms
ΔV_{OUT}*n*(LS)	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 12.5A and 12.5A to 0A at 12.5A/µs, V_{OUTn} = 1V, V_{INS3} = 12V (Note 7) See Load Transient Graph			40		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0A to 12.5A and 12.5A to 0A at 12.5A/µs, V_{OUTn} = 1V, V_{INS3} = 12V (Note 7) See Load Transient Graph			30		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 1, 2, 3). Specified as each individual output channel designated with *n* (Note 3). T_A = 25°C, V_{INS3} = 12V, RUN_C*n* = 3.3V, $EXTV_{CC}$ = 0V, FREQUENCY_SWITCH = 350kHz and V_{OUTC}*n* commanded to 1.000V unless otherwise noted. Configured with factory default EEPROM settings, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{OUTn(OCL\_AVg)}$	Output Current Limit, Time Averaged	Time-Averaged Output Inductor Current Limit Inception Threshold, Commanded by IOUT_OC_FAULT_LIMIT*n* (Note 7) Utilizing MFR_PWM_MODE[7] = 0b, and Using ~I_{OUT} = 34A , Page103			34		A
Control Section							
V_{FBCMn}	Feedback Input Common Mode Range	V_{OSNS}^-_C*n* Valid Input Range (Referred to SGND) V_{OSNS}^+_C*n* Valid Input Range (Referred to SGND)	● ●	–0.1		0.3 3.6	V V
$V_{OUTn\text{-}RNGL}$	Full-Scale Command Voltage Range Low (0.5V to 2.75V) Set Point Accuracy Resolution LSB Step Size	Limit Design to 1.5V Operating for Module MFR_PWM_MODE*n*[1] = 1b, VOUT*n* Commanded to 2.75V (Notes 8, 10)		 –0.5	2.75 12 0.688	 0.5	 V % Bits mV
$V_{OUTn\text{-}RNGH}$	Full-Scale Command Voltage Range High (0.5V to 3.6V) Set Point Accuracy Resolution LSB Step Size	Limit Design to 1.5V Operating for Module MFR_PWM_MODE*n*[1] = 0b, VOUT*n* Commanded to 3.60V (Notes 8, 10)		 –0.5	3.60 12 1.375	 0.5	 V % Bits mV
$R_{VSENSEn^+}$	V_{OSNS}^+_C*n* Impedance to SGND	0.05V ≤ V_{VOSNS}^+_C*n* – VSGND ≤ 3.3V			50		kΩ
$t_{ON(MIN)}$	Minimum On-Time	(Note 10)			60		nsec
$g_{m0,1}$	Resolution Error Amplifier $g_{m(max)}$ Error Amplifier $g_{m(min)}$ LSB Step Size	COMP0,1 = 1.35V, MFR_PWM_CONFIG[7:5] = 0 to 7 MFR_PWW_CONFIG Section (Note 10)			3 5.76 1 0.68		Bits mmho mmho mmho
RCOMP0, 1	Resolution Compensation Resistor RCOMP(MAX) Compensation Resistor RCOMP(MIN)	MFR_PWM_CONFIG[4:0] = 0 to 31 (See Figure 1, Note 10)			5 62 0.5		Bits kΩ kΩ
Analog OV/UV Ch 0,1(Overvoltage/Undervoltage) Output Voltage Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_ LIMIT Monitors)							
N_{OV/UV_COMP}	Resolution, Output Voltage Supervisors	(Notes 9, 10)			9		Bits
$V_{OV\text{-}RNG}$	Output OV Comparator Threshold Detection Range	(Notes 9, 10) Limit Design to 1.5V Operating for Module Low Range Scale, MFR_PWM_MODEn[1] = 1b High Range Scale, MFR_PWM_MODEn[1] = 0b		 0.5 1		 2.7 3.6	 V V
V_{OUSTP}	Output OV and UV Comparator Threshold Programming LSB Step Size	(Notes 9, 10) Low Range Scale, MFR_PWM_MODEn[1] = 1b High Range Scale, MFR_PWM_MODEn[1] = 0b			 5.6 11.2		 mV mV
$V_{OV\text{-}ACC\text{-}Cn}$	Output OV Threshold Accuracy Range Low Range High	(Notes 9, 10) 0.5V ≤ V_{VOSNS}^+_C*n* – V_{VOSNS}^-_C*n* ≤ 2.7V, MFR_PWM_ MODEn[1] = 1b 1V ≤ V_{VOSNS}^+_C*n* – V_{VOSNS}^-_C*n* ≤ 3.6V, MFR_PWM MODEn[1] = 0b	 ● 		 ±1.5	 ±40 	 mV %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 1, 2, 3). Specified as each individual output channel designated with *n* (Note 3). T_A = 25°C, V_{INS3} = 12V, RUN_C*n* = 3.3V, $EXTV_{CC}$ = 0V, FREQUENCY_SWITCH = 350kHz and V_{OUTC}*n* commanded to 1.000V unless otherwise noted. Configured with factory default EEPROM settings, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{UV-RNG}	Output UV Comparator Threshold Detection Range	(Note 10) Limit Design to 1.5V Operating for Module Low Range Scale, MFR_PWM_MODE*n*[1] = 1b High Range Scale, MFR_PWM_MODE*n*[1] = 0b		 0.5 1		 2.7 3.6	 V V
$V_{UV-ACC\ Cn}$	Output UV Threshold Accuracy Range Low Range High	(Notes 9, 10) 0.5V ≤ V_{VOSNS}^+_C*n* – V_{VOSNS}^-_C*n* ≤ 2.7V, MFR_PWM_MODEn[1] = 1b 1V ≤ V_{VOSNS}^+_C*n* – V_{VOSNS}^-_C*n* ≤ 3.6V, MFR_PWM_MODEn[1] = 0b	 ● 	 	 ±1.5	 ±40 	 mV %
$t_{PROP-OV}$	Output OV Comparator Response Times	Overdrive to 10% Above Programmed Threshold				100	µs
$t_{PROP-UV}$	Output UV Comparator Response Times	Underdrive to 10% Below Programmed Threshold				100	µs
Analog OV/UV V_{INS3} Input Voltage Supervisor Comparators (Threshold Detectors for VIN_ON and VIN_OFF)							
$N_{VINS3-OV/UV-COMP}$	V_{INS3} OV/UV Comparator Threshold-Programming Resolution	(Notes 9, 10)			9		Bits
$V_{INS3-OU-RANGE}$	V_{INS3} OV/UV Comparator Threshold-Programming Range	ABS MAX = 18V for Module Design	●	4.5		16	V
$V_{INS3-OU-STP}$	V_{INS3} OV/UV Comparator Threshold-Programming LSB Step Size	(Note 10)			76		mV
$V_{INS3-OU-ACC}$	V_{INS3} OV/UV Comparator Threshold Accuracy	4.5V < V_{INS3} ≤ 16V, Operating Range, 16V Max for Module	●			±350	mV
$t_{PROP-VINS3-LOW-VIN}$	V_{INS3} OV/UV Comparator Response Time, High V_{IN} Operating Configuration	Test Circuit 1, and: VIN_ON = 9V; V_{INS3} Driven from 8.775V to 9.225V VIN_OFF = 9V; V_{INS3} Driven from 9.225V to 8.775V				 100 100	 µs µs
$t_{PROP-VINS3-LOW-VIN}$	V_{INS3} OV/UV Comparator Response Time, Low V_{IN} Operating Configuration	Test Circuit 2, and: VIN_ON = 4.5V; V_{INS3} Driven from 4.225V to 4.725V VIN_OFF = 4.5V; V_{INS3} Driven from 4.725V to 4.225V				 100 100	 µs µs
Input Voltage (V_{INS3}) Readback (READ_VIN)							
$N_{VINS3-RB}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 5, 10)			10 15.625		Bits mV
$V_{INS3-F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 7, 11) 18V for Module Design			43		V
$V_{INS3-RB-ACC}$	Input Voltage Readback Accuracy	READ_VIN, 4.5V ≤ V_{INS3} ≤ 16V, (V_{IN} = V_{INS3})	●			2	%
$t_{CONVERT-VINS3-RB}$	Input Voltage Readback Update Rate	MFR_ADC_CONTROL = 0.00 (Notes 10, 12) MFR_ADC_CONTROL = 0.01 (Notes 10, 12)			90 8		ms ms
Channels 0 and 1 Output Voltage Readback (READ_VOUTn)							
N_{VO-RB}	Output Voltage Readback Resolution and LSB Step Size	(Note 10)			16 244		Bits µV
$V_{O-F/S}$	Output Voltage Full-Scale Digitizable Range	V_{RUN}*n* = 0V (Note 10) Design Limited to 1.5V			8		V
$V_{O-RB-AC-Cn}$	Output Voltage Readback Accuracy	0.5V ≤ V_{VOSNS}^+_C*n* – V_{VOSNS}^-_C*n* ≤ 1.0V 1V ≤ V_{VOSNS}+_C*n* – V_{VOSNS} – _C*n* ≤ 3.6V	●			Within ± 5mV, Reading Within ± 0.5%, Reading	
Channels 0 and 1 Output Current (READ_IOUTn)							
N_{IO-RB}	Output Current Readback Resolution and LSB Step Size	(Notes 5, 10) Based on MFR_PWM_MODE[7] = 1 Using the OUT_OC_FAULT_LIMIT of 34A			10 34.1		Bits mA
$I_{O-F/S}$	Output Current Full-Scale Digitizable Range	(Notes 5, 10) Based on MFR_PWM_MODE[7] = 1 Using the IOUT_OC_FAULT_LIMIT of 40A			34		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 1, 2, 3). Specified as each individual output channel designated with *n* (Note 3). T_A = 25°C, V_{INS3} = 12V, RUN_C*n* = 3.3V, $EXTV_{CC}$ = 0V, FREQUENCY_SWITCH = 350kHz and V_{OUTC}*n* commanded to 1.000V unless otherwise noted. Configured with factory default EEPROM settings, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{O-RB-ACC}$	Output Current, Readback Accuracy	READ_IOUT*n*, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 25A, Forced-Continuous Mode, MFR_PWM_MODEn[0] = 1b With Offset Adjustment (–20°C to 125°C) (Note 7) See Histograms in Typical Performance Characteristics Section	● 			5 3.5	% %
$I_{O-RB(25A)}$	Full Load Output Current Readback	I_{OUTn} = 30A Max by Module Design Up to 1.2V (Note 7)			25	30	A
$t_{CONVERT-IO-RB}$	Output Current Readback Update Rate	MFR_ADC_CONTROL = 0×00 (Notes 10, 12) MFR_ADC_CONTROL = 0×06 (CH0 I_{OUT})or 0×0A (CH1 I_{OUT}) (Notes 9, 17) See MFR_ADC_CONTROL Section			90 8		ms ms
Input Current Readback							
N	Resolution	(Notes 5, 10)			10		Bits
V_{IINSTP}	LSB Step Size Full-Scale Range = 16mV LSB Step Size Full-Scale Range = 32mV LSB Step Size Full-Scale Range = 64mV	Gain = 8, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 5mV Gain = 4, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 20mV Gain = 2, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 50mV			15.26 30.52 61		µV µV µV
I_{IN_TUE}	Total Unadjusted Error	Gain = 8, 2.5mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ (Note 13) Gain = 4, 4mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ (Note 13) Gain = 2, 6mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ (Note 13)	● ● ●			3.5 2.5 1.8	% % %
V_{OS}	Zero-Code Offset Voltage	(Note 10)				±50	µV
$t_{CONVERT}$	Update Rate	(Note 12)			90		ms
Internal Controller Supply Current Readback V_{INS3}							
N	Resolution	(Notes 5,12) See MFR_ADC_CONTROL Section for Faster Update Rates			10		Bits
$V_{ICONTROL\ STP}$	LSB Step Size Full-Scale Range = 256mV				244		µV
$I_{CONTROL\ TUE}$	Total Unadjusted Error	20mV ≤ $\lvert V_{IINS3\_C1} - SV_{IN}\rvert$ ≤ 150mV) See Block Diagram (Note 10)				±3	%
$t_{CONVERT}$	Update Rate	(Note 12)			90		ms
Temperature Readback (TSNS_C0, TSNS_C1)							
T_{RES_T}	Resolution				0.25		°C
T0_TUE	External Temperature Total Unadjusted Readback Error	Supporting Only Delta V_{BE} Sensing (Note 13)			3		°C
T1_TUE	Internal TSNS TUE	$V_{RUN\_C0,C1}$ = 0.0, f_{SYNC} = 0kHz (Note 8)			3		°C
$t_{CONVERT}$	Update Rate	MFR_ADC_CONTROL = 0×04 or 0×0C (Notes 9, 12, 15)			90 8		ms ms
$INTV_{CC}$ Regulator/$EXTV_{CC}$							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V ≤ V_{IN} ≤ 16V		5.25	5.5	5.75	V
V_{LDO_INT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, 6V ≤ V_{IN} ≤ 16V			0.5	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	V_{INS3_C1} ≥ 7V, $EXTV_{CC}$ Rising		4.5	4.7	4.9	V
V_{LDO_HYS}	$EXTV_{CC}$ Hysteresis				340		mV
V_{LDO_EXT}	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, $VEXTV_{CC}$ = 5.5V			60	120	mV
V_{IN_THR}	V_{IN} Threshold to Enable $EXTV_{CC}$ Switchover	V_{IN} Rising			7.1		V
$V_{IN\_THF\_HYS}$	V_{IN} Hysteresis to Disable $EXTV_{CC}$ Switchover	V_{IN} Falling			600		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 1, 2, 3). Specified as each individual output channel designated with *n* (Note 3). T_A = 25°C, V_{INS3} = 12V, RUN_C*n* = 3.3V, $EXTV_{CC}$ = 0V, FREQUENCY_SWITCH = 350kHz and V_{OUTC}*n* commanded to 1.000V unless otherwise noted. Configured with factory default EEPROM settings, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC} or 4.8V < V_{EXTVCC}		3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	V_{DD33} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			100		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold	(Note 10)			3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold	(Note 10)			3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage				2.5		V
L_{IM}	V_{DD25} Current Limit	V_{DD25} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			80		mA
Oscillator and Phase-Locked Loop							
f_{RANGE}	PLL SYNC Range	Synchronized with Falling Edge of SYNC	●	250		1000	kHz
f_{OSC}	Oscillator Frequency Accuracy	Frequency Switch = 250.0kHz to 1000.0kHz (Note 10)	●			±7.5	%
$V_{TH(SYNC)}$	SYNC Input Threshold	V_{SYNC} Falling V_{SYNC} Rising			1 1.5		V V
$V_{OL(SYNC)}$	SYNC Low Output Voltage	I_{LOAD} = 3mA			0.2	0.4	V
$I_{LEAK(SYNC)}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA
θSYNC-θ0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of SWC0)	MFR_PWM_CONFIG[2:0] = 0,2,3 MFR_PWM_CONFIG[2:0] = 5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0]= 4,6 (Note 10)			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of SWC1	MFR_PWM_CONFIG[2:0] = 3 MFR_PWM_CONFIG[2:0] = 0 MFR_PWM_CONFIG[2:0] = 2,4,5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0] = 6 (Note 10)			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Notes 15, 16)	0°C < T_J < 85°C EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 15, 16)	T_J < 125°C	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operation	●		440	4100	ms
Input Leakage Current SDA, SCL, $\overline{\text{ALERT}}$, RUN							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{\text{FAULT}}$*n*, PGOOD_C*n*							
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
Digital Inputs SCL, SDA, RUN_C*n*, $\overline{\text{FAULT}}$_C*n* (Note 10)							
V_{IH}	Input High Threshold Voltage		●			1.35	V
V_{IL}	Input Low Threshold Voltage		●	0.8			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP (Note 10)							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{\text{FAULT}}$_C*n*, $\overline{\text{ALERT}}$, RUN_C*n*, SHARE_CLK, PGOOD_C*n*							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA				0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 1, 2, 3). Specified as each individual output channel designated with *n* (Note 3). T_A = 25°C, V_{INS3} = 12V, RUN_C*n* = 3.3V, $EXTV_{CC}$ = 0V, FREQUENCY_SWITCH = 350kHz and $V_{OUTC n}$ commanded to 1.000V unless otherwise noted. Configured with factory default EEPROM settings, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs SHARE_CLK, WP (Note 10)							
V_{IH}	Input High Threshold Voltage	I_{SINK} = 3mA	●		1.5	1.8	V
V_{IL}	Input Low Threshold Voltage		●	0.6	1		V
Digital Filtering of $\overline{FAULTC}n$ (Note 10)							
T_{FLTF}	Input Digital Filtering $\overline{FAULT}n$				3		µs
Digital Filtering of PGOOD_C*n* (Note 10)							
T_{PGF}	Output Digital Filtering PGOOD_C*n*				60		µs
Digital Filtering of RUN_C*n* (Note 10)							
T_{RUNF}	Input Digital Filtering RUN_C*n*				10		µs
PMBus Interface Timing Characteristics (Note 10)							
f_{SCL}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD(STA)}$	Hold Time After Repeated Start Condition After This Period, the First Clock is Generated		●	0.6			µs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	0.6		10000	µs
$t_{SU(STO)}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD(DAT)}$	Date Hold Time Receiving Data Transmitting Data		● ●	0 0.3		 0.9	µs µs
$t_{SU(DAT)}$	Data Setup Time Receiving Data			0.1			µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event			3 255		ms ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs
Channel 0 and Channel 1 Power Stages (Note 10)							
PWM_C*n* LOW	PWM Drive Low Level, C0, C1					0.6	V
PWM_C*n* HIGH	PWM Drive High Level, C0, C1			2.6			V
$\overline{PHFLT}$_C*n* T	Warning Temperature				140		C
$\overline{PHFLT}$_C*n* ACC	Thermal Warning Accuracy			–10		10	Kelvin
$\overline{PHFLT}$_C*n* HYS	Hysteresis				10		Kelvin
$\overline{PHFLT}$_C*n* Res	On Resistance	Sink = 8mA			37.5	80	Ω
$\overline{PHFLT}$_C*n* Leak					0.1	5	µA
$\overline{PHFLT}$_C*n* Pull-Up	Pull-Up Resistor	Tied to V_{DD33}			10		kΩ

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. All voltages are referred to GND pin unless otherwise specified.

Note 2: The LTM4664A is tested under pulsed load conditions such that $T_J \approx T_A$. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: All Currents into the device pins are positive, all currents out of the device are negative. Each channel of PSM is tested independently in production. A shorthand notation is used in this document that allows these parameters to be referred to by "V_{INS3_Cn}" and "V_{OUTCn}", where *n* is permitted to take on a value of 0 or 1. This italicized "*n*" notation and convention is extended to encompass all such pin names, as well as register names with channel-specific, i.e., paged data. For example, VOUT_COMMAND*n* refers to the VOUT_COMMAND command code data located in Pages 0 and 1, which in turn relate to channel 0 (V_{OUTC0}) and channel 1 (V_{OUTC1}). Registers containing non-page-specific data, i.e., whose data is "global" to the module or applies to both of the module's channels lack the italicized, "*n*", e.g., FREQUENCY_SWITCH.

Note 4: See output current derating curves for different V_{IN}, V_{OUT}, Load Current and T_A, located in the Dual 25A/30A PSM Applications Information section. For output voltage up to 1.2V, Dual 30A loads are rated.

Note 5: The data format in PMBus is 5 bits exponent (signed) and 11 bits mantissa (signed). This limits the output resolution to 10 bits though the internal ADC is 16 bits and the calculations use 32-bit words.

Note 6: $V_{OUTC}n$ (DC) and line and load regulation tests are performed in production with digital servo disengaged (MFR_PWM_MODE*n*[6] = 0b) and low VOUTC*n* range selected MFR_PWM_MODE*n*[1] = 1b. The digital servo control loop is exercised in production (setting MFR_PWM_MODE*n*[6] = 1b), but convergence of the output voltage to its final settling value is not necessarily observed in final test—due to potentially long time constants involved—and is instead guaranteed by the output voltage readback accuracy specification. Evaluation in application demonstrates capability; see the Typical Performance Characteristics section.

Note 7: These typical parameters are based on bench measurements and are not production tested.

Note 8: Even though V_{OUTC0} and V_{OUTC1} are specified for 3.6V absolute maximum, the maximum recommended command voltage to regulate output channels 0 and 1 is 1.5V with V_{OUT} range-setting bit set using MFR_PWM_MODE*n*[1].

Note 9: Channel *n* OV/UV comparator threshold accuracy for MFR_PWM_MODEn[1] = 1b tested in ATE at V_{VOSNS}^{+}_C*n* – V_{VOSNS}^{-}C*n* = 0.5V and 2.7V. MFR_PWM_MODE*n*[1] = 1b is the Low Range.

Note 10: Tested at IC-level ATE

Note 11: The absolute maximum rating for the V_{INS3} pin is 18V. Input voltage telemetry (READ_VIN) is obtained by digitizing a voltage scaled down from the V_{INS3} pin.

Note 12: The data conversion is done by default in round robin fashion. All inputs signals are continuously converted for a typical latency of 90ms. Setting MFR_ADC_CONTRL value to be 0 to 12, LTM4664A can do fast data conversion with only 8ms to 10ms. See section PMBus Command for details.

Note 13: Part tested with PWM disabled. Evaluation in application demonstrates capability. TUE(%) = ADC Gain Error (%) +100 • (Zero code Offset + ADC Linearity Error)/Actual Value.

Note 14: EEPROM endurance and retention are guaranteed by wafer-level testing for data retention. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification, and whose EEPROM data was written to at 0°C ≤ T_J ≤ 85°C. The RESTORE_USER_ALL or MFR_RESET is valid over the entire operating temperature range and does not influence EEPROM characteristics.

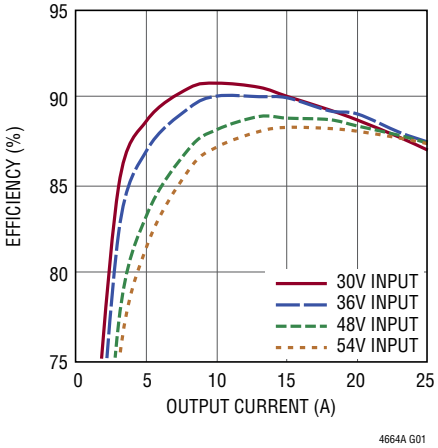
Note 15: Write operations above T_J = 85°C or below 0°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures below 125°C will not degrade the EEPROM Writing to the EEPROM above 85°C will result in a degradation of retention characteristics.

Note 16: M1-M8 power MOSFET are final tested separately before assembly in to the µModule.

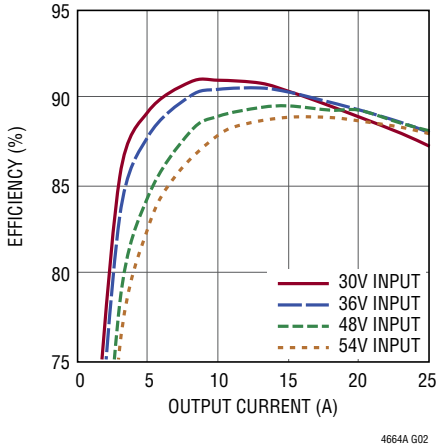
Note 17: MFR_PWM_MODE[2] = 1 or 0 sets device in low DCR mode or regular DCR mode respectively. MFR_PWM_MODE[7]=1 or 0 sets device in high output current range or low current range. See "Output Current Sensing and sub milliohm DCR Current Sensing" in Operation Section for details. Only V_{ILIMIT} codes 2–8 are supported for DCR sensing.

TYPICAL PERFORMANCE CHARACTERISTICS

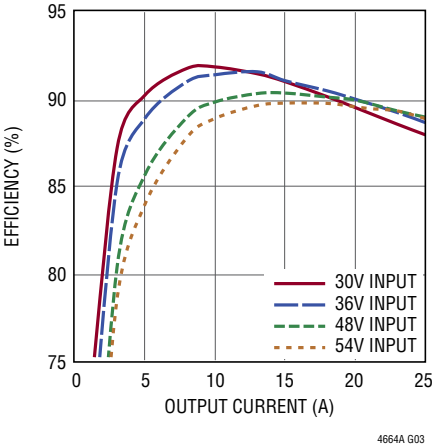
0.9V Individual Single Output
1st Stage = 100kHz,
2nd Stage = 200kHz,
Final 25A/30A Stages = 250kHz,
$EXTV_{CC}$ = 5V



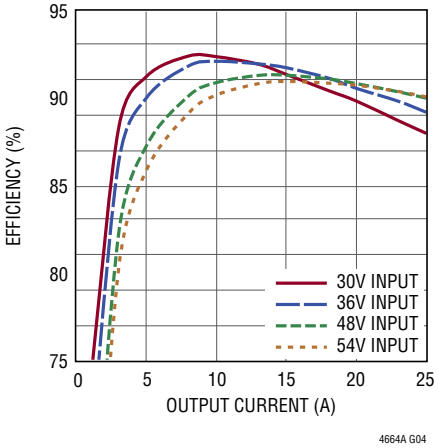
1V Individual Single Output
1st Stage = 100kHz,
2nd Stage = 200kHz,
Final 25A/30A Stages = 250kHz,
$EXTV_{CC}$ = 5V



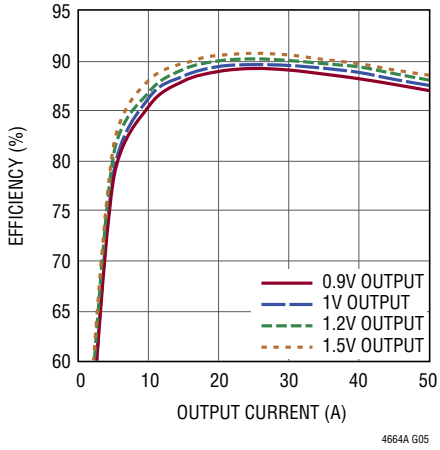
1.2V Individual Single Output
1st Stage = 100kHz,
2nd Stage = 200kHz,
Final 25A/30A Stages = 250kHz,
$EXTV_{CC}$ = 5V



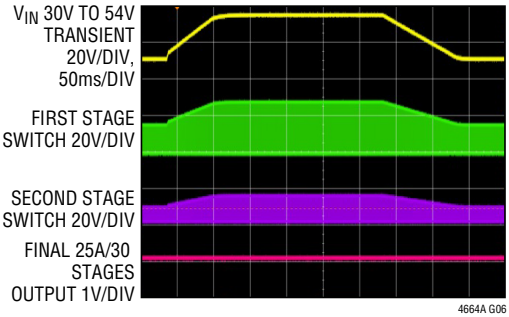
1.5V Individual Single Output
1st Stage = 100kHz,
2nd Stage = 200kHz,
Final 25A/30A Stages = 350kHz,
$EXTV_{CC}$ = 5V



54V Input, 2-Phase 50A Single Output
1st Stage = 100kHz,
2nd Stage = 200kHz,
Final 25A/30A Stages = 350kHz,
$EXTV_{CC}$ = 5V

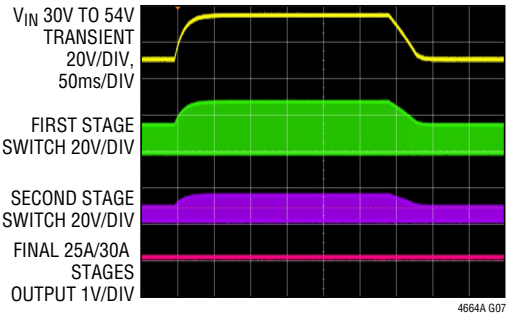


54V Input Voltage Change,
No Load



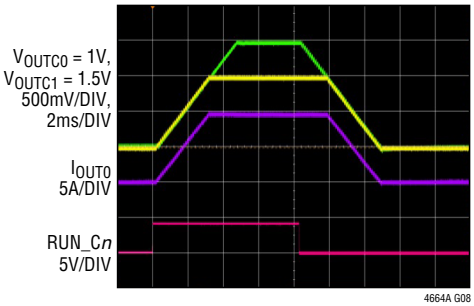
54V TO 1V, NO LOAD
4:1 DIVIDER: FIRST STAGE 100kHz,
SECOND STAGE 200kHz,
FINAL 25A/30A STAGES 250kHz

54V Input Voltage Change,
Load 25A Each



54V TO 1V, 25A LOAD EACH
4:1 DIVIDER: FIRST STAGE 100kHz,
SECOND STAGE 200kHz,
FINAL 25A/30A STAGES 250kHz

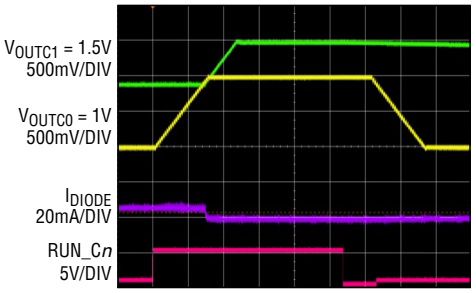
Dual Output Tracking
Start-Up/Shutdown



48V_{IN}, 10A LOAD ON V_{OUT0}, NO LOAD ON V_{OUTC1},
TON_RISE 0 = 3ms, TON_RISE 1 = 4.5ms,
TOFF_DELAY 1 = 0ms, TOFF_DELAY 0 = 1.5ms
TOFF_FALL 1 = 4.5ms, TOFF_FALL 0 = 3ms,
ON_OFF_CONFIG*n* = 0x1E

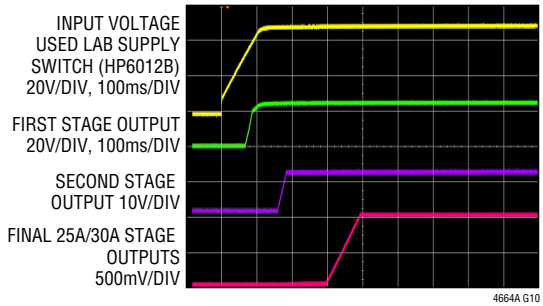
TYPICAL PERFORMANCE CHARACTERISTICS

Dual Output Start-Up/Shutdown with a Prebiased Load



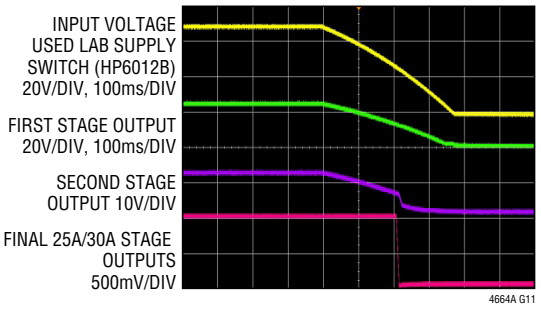
48V_{IN}, 10A LOAD ON V_{OUTC0}, 7.5mA LOAD ON V_{OUT1}, V_{OUT1} PREBIASED THROUGH A DIODE TON_RISE 0 = 3ms, TON_RISE 1 = 4.5ms, TOFF_DELAY 1 = 0ms, TOFF_DELAY 0 = 1.5ms TOFF_FALL 1 = 4.5ms, TOFF_FALL 0 = 3ms, ON_OFF_CONFIG*n* = 0x1E

Start-Up



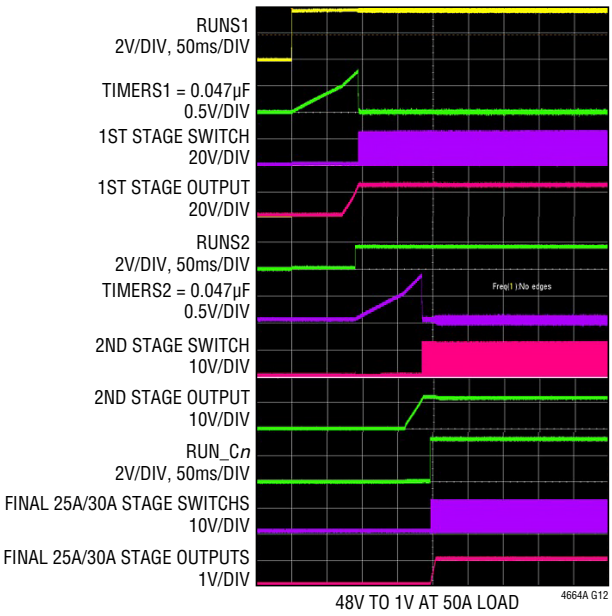
48V TO 1V AT 0A LOAD, EACH 25A/30A STAGE FINAL STAGE TON DELAY AND TON RISE SET TO 100ms

Shutdown



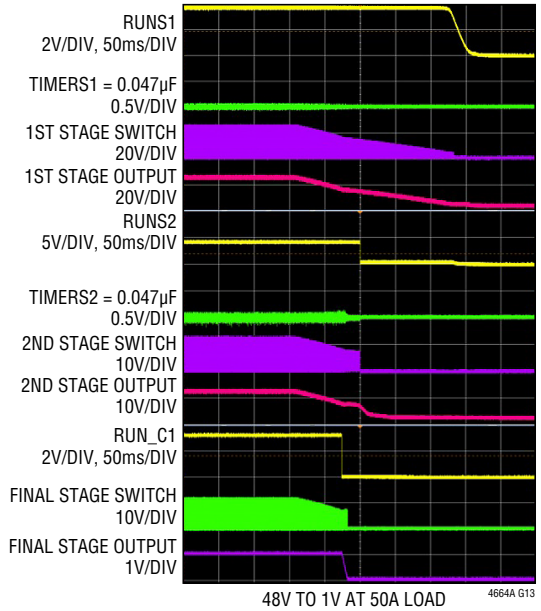
48V TO 1V AT 0A LOAD, EACH 25A/30A STAGE FINAL STAGE TON DELAY AND TON RISE SET TO 100ms

Full Sequence Turn On



48V TO 1V AT 50A LOAD

Full Sequence Turn Off

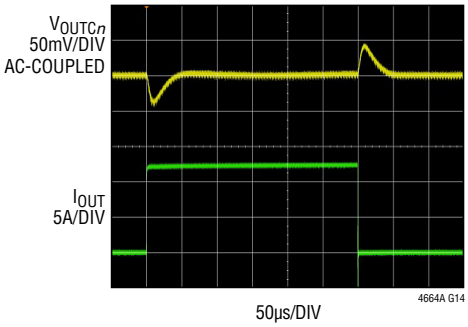


48V TO 1V AT 50A LOAD

Rev. 0

TYPICAL PERFORMANCE CHARACTERISTICS

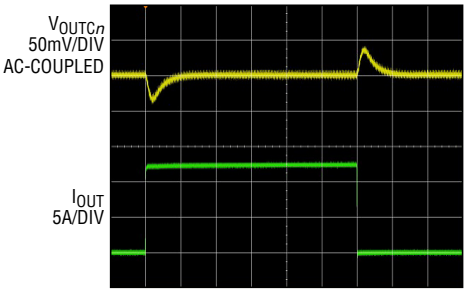
$V_{OUTC}n$ (1V) Load Transient



50µs/DIV

48V TO 1V SINGLE CHANNEL,
0A TO 12.5A/µs LOAD STEP
C_{OUT} = 470µF ×2 POSCAP, 100µF ×5 CER,
COMP_Cna = 2200pF, COMP_Cnb = 100pF,
EA-GM = 3.69ms, RCOMP = 5k,
PSM FREQ = 250kHz, I_{LIMIT} RANGE = LOW
V_{OUT} RANGE = LOW

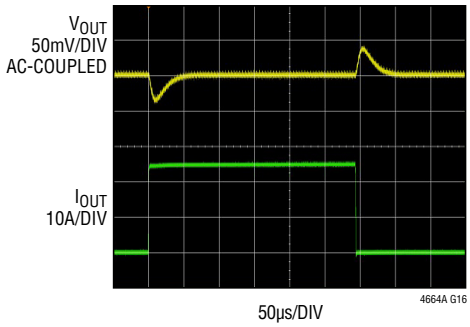
$V_{OUTC}n$ (1.5V) Load Transient



50µs/DIV

48V TO 1.5V SINGLE CHANNEL, 0A TO 12.5A/µs LOAD STEP
C_{OUT} = 470µF ×1 POSCAP, 330µF ×2 CER,
COMP_C*n*a = 2200pF, COMP_C*n*b = 220pF,
EA-GM = 3.02ms, RCOMP = 6k,
PSM FREQ = 350kHz

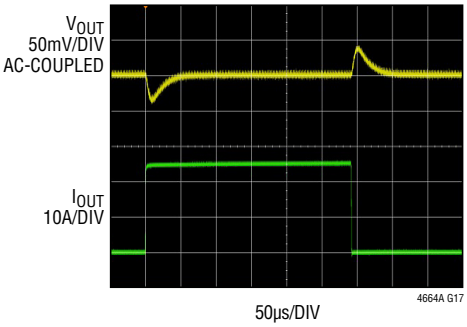
Dual Phase (50A/0.9V) Load Transient



50µs/DIV

48V TO 0.9V DUAL PHASE SINGLE OUTPUT, 0A TO 25A/µs LOAD STEP
C_{OUT} = 470µF ×2 POSCAP, 330µF ×5 CER,
COMP_C0, 1 = 1500pF, COMP_C01b = 100pF,
EA-GM = 4.36ms, RCOMP = 13k,
PSM FREQ = 250kHz, I_{LIMIT} RANGE = LOW
V_{OUT} RANGE = LOW

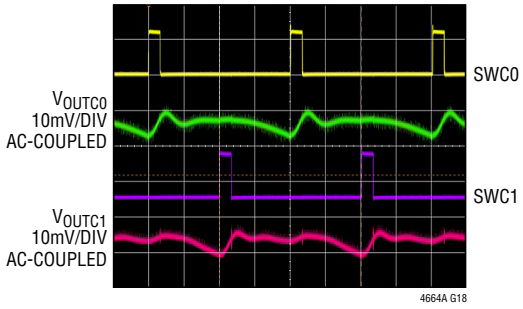
Dual Phase (50A/1V) Load Transient



50µs/DIV

48V TO 1V DUAL PHASE SINGLE OUTPUT, 0A TO 25A/µs LOAD STEP
C_{OUT} = 470µF ×2 POSCAP, 5 × 330µF CER,
COMP_C0,1 = 1500pF, COMP_C01b = 100pF,
EA-GM = 4.36ms, RCOMP = 13k,
PSM FREQ = 350kHz, I_{LIMIT} RANGE = LOW
V_{OUT} RANGE = LOW

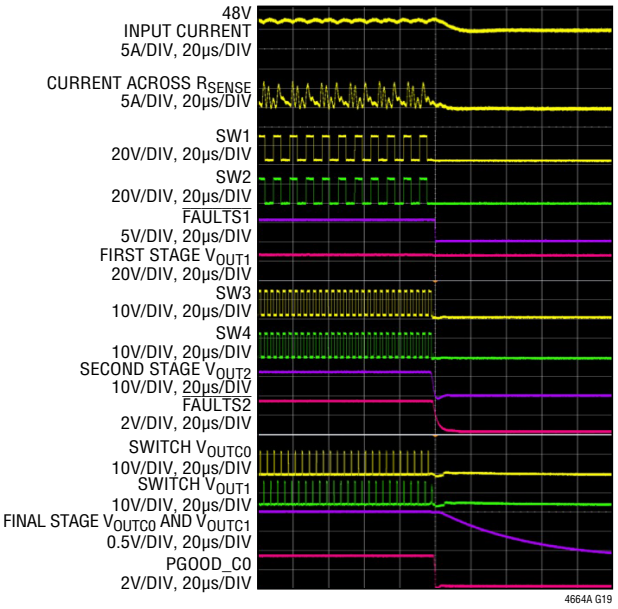
25A AC Ripple Noise



48V TO V_{OUTC0} = 1V, AND V_{OUTC1} = 1V

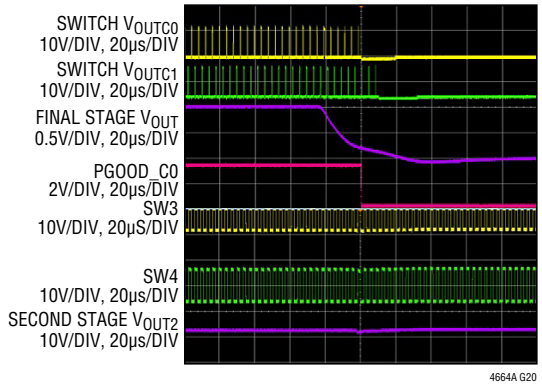
TYPICAL PERFORMANCE CHARACTERISTICS

48V to 1V, Second Stage (12V) Shorted



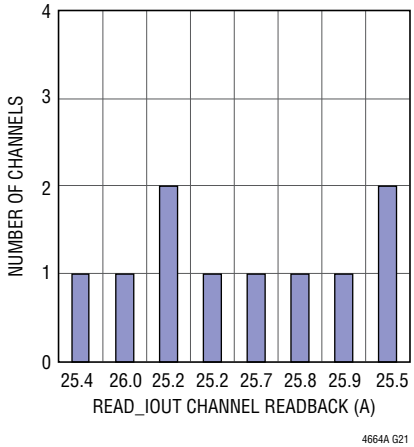
48V TO 1V AT 50A V_{OUT2} STAGE 12V OUTPUT SHORTED

48V to 1V at 50A Shorted

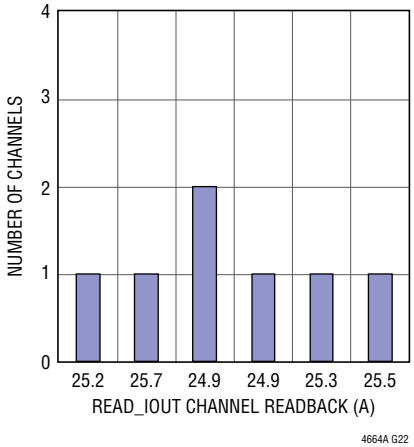


48V TO 1V AT 50A SHORTED LAST STAGE 1V OUTPUT V_{OUTC0} AND V_{OUTC1} IN PARALLEL

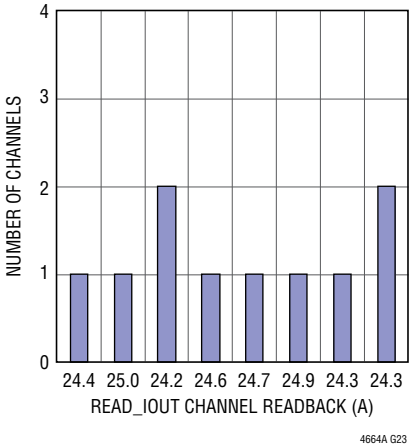
READ_IOUT of 16 LTM4664A Channels $12V_{IN}$, $1V_{OUT}$, T_J = –40°C, I_{OUTn} = 25A, System Having Reached Thermally Steady-State Condition, No Airflow



READ_IOUT of 16 LTM4664A Channels $12V_{IN}$, $1V_{OUT}$, T_J = 25°C, I_{OUTn} = 25A, System Having Reached Thermally Steady-State Condition, No Airflow



READ_IOUT of 16 LTM4664A Channels $12V_{IN}$, $1V_{OUT}$, T_J = 125°C, I_{OUTn} = 25A, System Having Reached Thermally Steady-State Condition, No Airflow



PIN FUNCTIONS

4:1 Divider Section (Stage 1)

GND: (A8-A9, B1-B3, B8-B9, B14-B16, C4-C13, D4,D8,D9, D13, E1-E4, E8-E9, E13-E16, F1-F4, F8-F10, G4, G8-G11, H4, H9-H11, J1-J4, J11, K1-K4, K11, L3, L11, L14-L16, M3-M5, M11, M14, N1-N4, N7, N11-N16, P1-P4, P7-P9, P13-P15, R1-R6, R9, R13-16, T2-T3, T8-T9, T14-T15) Main ground pins for all ground returns. Input and output capacitors are connected to these pin. See recommended layout Figure 45.

V_{OUT1}: (C14-C16) 1st stage divide by two output pins. These pins connect to the 2nd stage V_{INS2} pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

$INTV_{CCS1}$: (D10) Output of the 5.5V internal linear low dropout regulator. The driver and control circuits are powered from this voltage source. Must be bypassed to power ground with a minimum of 4.7µF ceramic or other low ESR capacitor. Do not use the $INTV_{CCS1}$ pin for any other ICs.

$EXTV_{CCS1}$: (D11) External Power Input to the Internal LDO Connected to $INTV_{CCS1}$. This LDO supplies $INTV_{CCS1}$ power, bypassing the internal LDO powered from V_{INS1} whenever $EXTV_{CCS1}$ is higher than 6.5V and V_{INS1} is higher than 7V. Do not exceed 30V on this pin. This pin can be driven with the V_{OUT2} output to limit power loss in LDO with V_{INS1} at higher input voltage. See Applications section.

PGOODS1: (D12) This is an open drain output pin. PGOODS1 is pulled to ground if there are any faults or the voltage at UVS1 pin is lower than 1V. Use PGOODS1 or $\overline{FAULTS1}$ to sequence on RUNS2 for the second stage.

UVS1: (E10) Undervoltage Comparator. If the UVS1 pin voltage is lower than 1V, the PGOODS1 pin is pulled down. If the UV pin voltage is higher than 1V and no faults, PGOODS1 pin is released. Connect to $INTV_{CCS1}$ if not used. This pin is used to validate proper output regulation.

$\overline{FAULTS1}$: (E11) This is an open drain output pin. $\overline{FAULTS1}$ is pulled to ground when the V_{OUT1} voltage is out of the $(V_{INS1})/2$ window threshold or the voltage between $INSNSS1^+$ and $INSNSS1^-$ is higher than 50mV. $\overline{FAULTS1}$ pin is released after $INTV_{CCS1}$ starts up and passes UVLO. Use $\overline{FAULTS1}$ or PGOODS1 to sequence on RUNS2 for the second stage.

FREQS1: (E12) Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. See the 4:1 Divider Application Information section for detailed information.

RUNS1: (F11) Stage 1 Run Control Input. Forcing RUNS1 below 1.2V shuts down the controller. When RUNS1 is higher than 1.2V, internal circuitry starts up. There is a 1µA pull-up current flowing out of RUNS1 pin when the RUNS1 pin voltage is below 1.2V and an additional 5µA current flowing out of RUNS1 pin when the RUNS1 pin voltage is above 1.2V.

TIMERS1: (F12) Charge Balance and Fault Timer Control Input. A capacitor between this pin and ground sets the amount of time to charge V_{OUT1} to $(V_{INS1})/2$. It also sets the short-circuit retry time. See the 4:1 Divider Application Information.

HYS_PRGMS1: (G12) A resistor connected between this pin and ground will set the window threshold of the window comparator that monitors the voltage difference between $(V_{INS1})/2$ and V_{OUT1}. There is a 10µA current flowing out of this pin. See Applications section.

SW1, SW2: (G14-G16), (D14-D16) Switching nodes for the 1st stage C_{FLY} Flying capacitor. See Block Diagram.

I $INSNSS1^-$: (J13) Current sense comparator negative input, connected to the negative node of the current sensing resistor. Short to $INSNSS1^+$ if not used.

$NSNSS1^+$: (J14) Current sense comparator positive input, connected to the positive node of the external current sensing resistor. The current sensing resistor has to be placed on the drain of the very top MOSFET. When the voltage between $INSNSS1^+$ pin and $INSNSS1^-$ pin is higher than 50mV, the Stage 1 controller indicates an overcurrent fault by pulling the $\overline{FAULTS1}$ pin down. The $INSNSS1^+$ pin is also used to source 95mA current to the V_{OUT1} pin during the pre-balance time in divider applications. Connect directly to the drain of the very top MOSFET if not used. See application schematic section.

PIN FUNCTIONS

V_{INS1}: (J15-J16) Power input pins to the first stage divide by two. Place input capacitance between these pins and GND.

4:1 Divider Section (Stage 2)

V_{INS2}: (C1-C3) Power input pins to the second stage divide by two. Place input capacitance between these pin and GND.

SW3, SW4: (D1-D3), (G1-G3) Switching nodes for the 2nd stage C_{FLY} Flying capacitor. See Block Diagram.

V_{INS2F}: (D5) Input Voltage Sensing with Filtering. This pin has a 1kΩ resistor in series from V_{INS2}, and a 4700pf capacitor to GND. The pin has a 1MΩ resistance to GND. See Block Diagram.

$INSNSS2^-$: (D6) Current sense comparator negative input, connected to the negative node of the current sensing resistor. Short to $INSNSS2^+$ if not used.

$INSNSS2^+$: (D7) Current sense comparator positive input, connected to the positive node of the external current sensing resistor. The current sensing resistor has to be placed on the drain of the very top MOSFET. When the voltage between $INSNSS2^+$ pin and $INSNSS2^-$ pin is higher than 50mV, the controller indicates an overcurrent fault by pulling the $\overline{FAULTS2}$ pin down. The $INSNSS2^+$ pin is also used to source 95mA current to the V_{OUT2} pin during the pre-balance time in divider applications. Connect directly to the drain of the very top MOSFET if not used. See Application Schematic section.

HYS_PRGMS2: (E5) A resistor connected between this pin and ground will set the window threshold of the window comparator that monitors the voltage difference between $(V_{INS2})/2$ and V_{OUT2}. There is a 10µA current flowing out of this pin. See applications section.

OVP_SET: (E6) External + input for setting the V_{OUT2} trip level. The OVP_SET pin will have a voltage divider to monitor the V_{OUT2} voltage and set to trip when the divider midpoint on the OVP_SET pin exceeds the reference trip level on the VOUT2_SET pin. For example, if the OVP_SET trip point was set for V_{TRIP}, then RTOP = $((V_{TRIP}/5.1V)-1) \bullet 7.5K$, with RTOP being the top resistor in the divider, and RBOT is the bottom resistor in the divider. RBOT set to 7.5k. If not used, tie this pin to $INTV_{CCS2}$. See 4:1 Divider Application Information section.

OVP_TRIP: (E7) Open collector output that is used to trip off input power and clamp hold up energy during an over voltage fault on V_{OUT2}. See Applications section.

TIMERS2: (F5) Charge Balance and Fault Timer Control Input. A capacitor between this pin and ground sets the amount of time to charge V_{OUT2} to $(V_{INS2})/2$. It also sets the short-circuit retry time. See the 4:1 Divider Application Information.

VOUT2_SET: (F6) External – comparator input for setting the V_{OUT2} trip reference level. This can be done with a resistor and 5.1V Zener from V_{IN}. This secondary fault protection is in and above the Fault protection for Stage 1 and Stage 2. The overall input voltage is divided down by four, so V_{OUT2} will be 1/4 of V_{IN}. The OVP_SET pin will have a voltage divider to monitor the V_{OUT2} voltage and set to trip when the divider midpoint on the OVP_SET pin exceeds the reference trip level. If not used, tie this pin to ground. See 4:1 Divider Application Information section.

$EXTV_{CCS2}$: (F7) External Power Input to the Internal LDO Connected to $INTV_{CCS2}$. This LDO supplies $INTV_{CCS2}$ power, bypassing the internal LDO powered from V_{IN2} whenever $EXTV_{CCS2}$ is higher than 6.5V and V_{INS2} is higher than 7V. Do not exceed 30V on this pin. This pin can be driven with the V_{OUT2} output to limit power loss in LDO with V_{INS2} at higher input voltage. See 4:1 Divider Application Information section.

FREQS2: (G5) Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. See the 4:1 Divider Application Information section for detailed information.

RUNS2: (G6) Stage 2 Run Control Input. Forcing RUNS2 below 1.2V shuts down the controller. When RUNS2 is higher than 1.2V, internal circuitry starts up. There is a 1µA pull-up current flowing out of RUNS2 pin when the RUNS2 pin voltage is below 1.2V and an additional 5µA current flowing out of RUNS2 pin when the RUNS2 pin voltage is above 1.2V. Use PGOODS1, and $\overline{FAULTS1}$ from stage one to enable stage 2.

PIN FUNCTIONS

$INTV_{CCS2}$: (G7) Output of the 5.5V internal linear low dropout regulator. The driver and control circuits are powered from this voltage source. Must be bypassed to power ground with a minimum of 4.7µF ceramic or other low ESR capacitor. Do not use the $INTV_{CCS2}$ pin for any other ICs.

V_{OUT2}: (H1-H3) 2nd stage divide by two output pins. These pins connect to the V_{INS3} input of dual 25A/30A PMBus converter. Recommend placing output decoupling capacitance directly between these pins and GND pins.

PGOODS2: (H5) This is an Open Drain Output Pin. PGOODS2 is pulled to ground if there are any faults or the voltage at UVS2 pin is lower than 1V. Use PGOOD2 or $\overline{FAULTS2}$ to sequence on RUN_C0, and RUN_C1 for the dual 25A/30A stage.

$\overline{FAULTS2}$: (H6) This is an Open Drain Output Pin. $\overline{FAULTS2}$ is pulled to ground when the V_{OUT2} voltage is out of the $(V_{INS2})/2$ window threshold or the voltage between $INSNSS2^+$ and $INSNSS2^-$ is higher than 50mV. $\overline{FAULTS2}$ pin is released after $INTV_{CCS2}$ starts up and passes UVLO. Use $\overline{FAULTS2}$ or PGOOD2 to sequence on RUN_C0, and RUN_C1 for the dual 25A/30A PSM stage.

UVS2: (H7) Undervoltage Comparator. If the UVS2 pin voltage is lower than 1V, the PGOODS2 pin is pulled down. If the UV pin voltage is higher than 1V and no faults, PGOODS2 pin is released. Connect to $INTV_{CCS2}$ if not used. This pin is used to validate proper output regulation.

PMBus Dual 25A/30A Section

V_{OUTC1} (A1-A7, B4-B7): Channel 1 Output Voltage. Place recommended output capacitors from this connection to GND. See recommended layout in Figure 45.

V_{OUTC0}: (A10-A16, B10-B13): Channel 0 Output Voltage. Place recommended output capacitors from this connection to GND. See recommended layout in Figure 45.

FSWPH_CFG (H8): Switching Frequency, Channel Phase Interleaving Angle and Phase Relationship to SYNC Configuration Pin. If this pin is left open—or, if the dual 25A/30A regulator is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LTM4664A's switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SV_{IN} power-up according to the LTM4664A's NVM contents. Default factory values are: 350kHz operation; Channel 0 at 0°; and Channel 1 at 180°C (convention throughout this document: a phase angle of 0° means the channel's switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor divider from V_{DD25} to SGND_C0_C1, see page 4 (and using the factory default NVM setting of MFR_CONFIG_ALL[6] = 0b) allows a convenient way to configure multiple LTM4664As with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to "custom preprogram" module NVM contents. (See the Dual 25A/30A PSM Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

VTRIMC1_ CFG (J5): Output Voltage Select Pin for V_{OUTC1}, Fine Setting. Works in combination with VOUTC1_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 1, at SV_{IN} power-up. (See VOUTC1_CFG and the Dual 25A/30A PSM Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs on VOUTC1_CFG/VTRIMC1_CFG can affect the V_{OUTC1} range setting (MFR_PWM_MODE1 [1]) and loop gain. A resistor divider from V_{DD25} to SGND_C0_C1 can set the trim value, see page 43.

VOUTC0_CFG (J6): Output Voltage Select Pin for V_{OUTC0}, Coarse Setting. If the VOUTC0_CFG and VTRIMC0_CFG pins are both left open—or, if the LTM4664A is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LTM4664A's target V_{OUTC0} output voltage setting (VOUT_COMMAND0) and associated power good and OV/UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4664A's NVM contents. A resistor connected from this pin to SGND—in combination with resistor pin settings on VTRIMC0_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used

PIN FUNCTIONS

to configure the LTM4664A's Channel 0 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the 4:1 Divider Application Information section.) Minimize capacitance especially when the pin is left open to assure accurate detection of the pin state. Note that use of RCONFIGs on VOUTC0_CFG/VTRIMC0_CFG can affect the V_{OUTC0} range setting (MFR_PWM_MODE0 [1]) and loop gain.

VOUTC1_CFG (J7): Output Voltage Select Pin for V_{OUTC1}, Coarse Setting. If the VOUTC1_CFG and VTRIMC1_CFG pins are both left open or, if the LTM4664A is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL [6] = 1b then the LTM4664A's target V_{OUTC1} output voltage setting (VOUT_COMMAND1) and associated OV/UV warning and fault thresholds are dictated at SV_{IN} power up according to the LTM4664A's NVM contents, in precisely the same fashion that the VOUTC1_CFG and VTRIMC1_CFG pins affect the respective settings of V_{OUT1}/Channel 1. (See VOUTC1_CFG, VTRIMC1_CFG and the 4:1 Divider Application Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs on VOUTC1_CFG/VTRIMC1_CFG can affect the V_{OUTC1} range setting (MFR_PWM_MODE1 [1]) and loop gain. A resistor divider from V_{DD25} to SGND_C0_C1. See page 43.

ASEL (J8): Serial Bus Address Configuration Pin. On any given I^2C/SMBus serial bus segment, every device must have its own unique slave address. If this pin is left open, the LTM4664A powers up to a slave address set by MFR_ADDRESS[6:0] (see Table 4). The factory-default setting is 0x4F (hexadecimal), i.e., 1001111b (industry standard convention is used throughout this document: 7-bit slave addressing). The lower four bits of the LTM4664A's slave address can be altered from the NVM-set value by connecting a resistor from this pin to SGND. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. See 4:1 Divider Application Information section.

RUN_C0, RUN_C1 (J9, K8 Respectively): Enable Run Input for Channels 0 and 1, respectively. Open-drain input and output. Logic high on these pins enables the respective outputs of the LTM4664A. These open-drain output pins hold the pin low until the LTM4664A is out of reset and V_{IN3_C1} is detected to exceed VIN_ON. A pull-up resistor to 3.3V is required in the application. The LTM4664A pulls RUN_C0 and/or RUN_C1 low, as appropriate, when a global fault and/or channel-specific fault occurs whose fault response is configured to latch off and cease regulation; issuing a CLEAR_FAULTS command via I^2C or power cycling SV_{IN} is necessary to restart the module, in such cases. Do not pull RUN logic high with a low impedance source. Use PGOODS2 and $\overline{FAULTS2}$ to sequence on RUN_C0, and RUN_C1 for the dual 25A/30A stage.

$\overline{ALERT}$ (J10): Open-Drain Digital Output. A pull-up resistor to 3.3V is required in the application only if SMBALERT interrupt detection is implemented in one's SMBus system.

VTRIMC0_CFG (K5): Output Voltage Select Pin for V_{OUTC0}, Fine Setting. Works in combination with VOUTC0_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 0, at SV_{IN} power-up. (See VOUTC0_CFG and the Dual 25A/30A PSM Applications Information section.) Minimize capacitance especially when the pin is left open to assure accurate detection of the pin state. Note that use of RCONFIGs on VOUTC0_CFG/VTRIMC0_CFG can affect the V_{OUTC0} range setting (MFR_PWM_MODE0 [1]) and loop gain.

V_{DD25} (K6): Internally Generated 2.5V Power Supply Output Pin. Do not load this pin with external current; it is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

WP (K7): Write Protect Pin, Active High. An internal 10µA current source pulls this pin to V_{DD33}. If WP is open circuit or logic high, only I^2C writes to PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS and MFR_EE_UNLOCK are supported. Additionally, Individual faults can be cleared by writing 1b's to bits of interest in registers prefixed with "STATUS". If WP is low, I^2C writes are unrestricted.

PIN FUNCTIONS

$\overline{\text{FAULT}}$_C0/$\overline{\text{FAULT}}$_C1 (K10/K9): Digital Programmable FAULT Inputs and Outputs. Open-drain output. A pull-up resistor to 3.3V is required in the application.

V_{INS3_C1}, V_{INS3_C0}: (L1-L2, M1-M2), (L12-L13, M12-M13): Main power input to channel 0, and channel 1 power stages. Provide sufficient decoupling capacitance in the form of multilayer ceramic capacitors (MLCCs) and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stages. MLCCs should be placed as close to the V_{INS3} as physically possible. The V_{INS3_C1} input provides the input power for the $INTV_{CC}$ LDO regulator. See Layout Recommendations in the Dual 25A/30A PSM Applications Information section.

V_{DD33} (L6): Internally Generated 3.3V Power Supply Output Pin. This pin should only be used to provide external current for the pull-up resistors required for $\overline{\text{FAULT}}$_C*n*, SHARE_CLK, and SYNC, and may be used to provide external current for pull-up resistors on RUN_C*n*, SDA, SCL, $\overline{\text{ALERT}}$ and PGOOD_C*n*. No external decoupling is required.

SHARE_CLK (L7): Share_Clock, Bidirectional Open- Drain Clock Sharing Pin. Nominally 100kHz. Used for synchronizing the time base between multiple LTM4664As (and any other Analog Devices products with a SHARE_ CLK pin)—to realize well-defined rail sequencing and rail tracking. Tie the SHARE_CLK pins of all such devices together; all devices with a SHARE_CLK pin will synchronize to the fastest clock. A pull-up resistor to 3.3V is required.

SDA (L8): Serial Bus Data Open-Drain Input and Output. A pull-up resistor to 3.3V is required in the application.

SCL (L9): Serial Bus Clock Open-Drain Input (Can Be an Input and Output, if Clock Stretching is enabled). A pull-up resistor to 3.3V is required in the application for digital communication to the SMBus master(s) that nominally drive this clock. The LTM4664A will never encounter scenarios where it would need to engage clock stretching unless SCL communication speeds exceed 100kHz—and even then, LTM4664A will not clock stretch unless clock stretching is enabled by means of setting MFR_CONFIG_ALL[1] = 1b. The factory-default NVM configuration setting has MFR_CONFIG_ALL [1] = 0b: clock stretching disabled. If communication on the bus at clock speeds above 100kHz is required, the user's SMBus master(s) needs to implement clock stretching support to assure solid serial bus communications, and only then should MFR_CONFIG_ALL [1] be set to 1b. When clock stretching is enabled, SCL becomes a bidirectional, open-drain output pin on LTM4664A.

TSNS_C0a, TSNS_C0b (L10 and T16, Respectively): Channel 0 Temperature Excitation/Measurement and Thermal Sensor Pins, respectively. Connect TSNS_C0a to TSNS_C0b. This allows the LTM4664A to monitor the Power Stage Temperature of Channel 0.

SYNC (M8): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If clock master mode is enabled, this pin will pull low at the switching frequency with a 500ns pulse to ground. A resistor pull-up to 3.3V is required in the application if the LTM4664A is the master.

SGND_C0_C1 (M9, N8-N9): SGND_C0_C1 is the signal ground return path of the dual 25A/30A control. SGND_C0_C1 is not internally connected to GND. Connect SGND_C0_C1 to GND at the A9, B9, and C9 pins that is close to the output capacitor ground connections. See recommended layout.

TSNS_C1a, TSNS_C1b (M10 and T1, Respectively): Channel 1 Temperature Excitation/Measurement and Thermal Sensor Pins, respectively. In most applications, connect TSNS_C1a to TSNS_C1b. This allows the LTM4664A to monitor the Power Stage Temperature of Channel 1. See the Applications section.

PWM_C0, PWM_C1 (M15, L4): PWM drive signal to Channel 0, Channel 1 power stage. Utilized for debugging or monitoring purposes.

$\overline{\text{PHFLT}}$_C0, $\overline{\text{PHFLT}}$_C1 (M16, L5): Thermal Warning for Channel 0 and Channel 1. When the thermal protection threshold is tripped, the $\overline{\text{PHFLT}}$_C*n* pin is being pulled low. The power stage does not shut off, and is only a thermal monitor. These pins are internally pulled up to 3.3V through 10k resistor. COMP_0b/COMP_1b (N10/M7): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel's current comparator tripping threshold increases with its Comp voltage. Each channel has a 22pF to SGND.

PIN FUNCTIONS

V_{OSNS}^-_C1 (N6): Channel 1 Negative Differential. Voltage Sense Input. See V_{OSNS}^+_C1.

V_{OSNS}^+_C1 (P6): Channel 1 Positive Differential Voltage Sense Input. Together, V_{OSNS}^+_C1 and V_{OSNS}^-_C1 serve to kelvin sense the V_{OUTC1} output voltage at V_{OUTC1}'s point of load (POL) and provide the differential feedback signal directly to Channel 1's feedback loop. Command V_{OUTC1}'s target regulation voltage by serial bus. Its initial command value at V_{INS3} power-up is dictated by NVM (non-volatile memory) contents (factory default: 1.000V)—or, optionally, may be set by configuration resistors; see VOUTC1_CFG and the 4:1 Divider Application Information section.

IN^- (P10): Negative Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the IN^+ and V_{IN3} pins. See 4:1 Divider Application Information section for detail about the input current sensing.

COMP_0a/COMP_1a (P11/M6): Loop Compensation Nodes. The internal PWM loop compensation resistors RCOMPn of the LTM4664A can be adjusted using bit [4:0] of the MFR_PWM_COMP command. The transconductance of the LTM4664A PWM error amplifier can be adjusted using bit [7:5] of the MFR_PWM_COMP command. These two loop compensation parameters can be programmed when device is in operation. Refer to the Programmable Loop Compensation subsection in the 4:1 Divider Application Information section for further details. See MFR_PWM_COMP section.

V_{OSNS}^-_C0: (P12): Channel 0 Negative Differential Voltage Sense Input. See V_{OSNS}^+_C0.

GL_C0, GL_C1 (P16, P5): Bottom MOSFET gate drive in the Channel 0 power stage, Channel 1 power stage. Utilized for debugging or monitoring purposes.

$INTV_{CC}$ (R7): Internal Regulator, 5.5V output. When operating the V_{INS3} from $7V \le V_{INS3} \le 16V$, a LDO generates $INTV_{CC}$ from V_{INS3_C1} to bias internal control circuits and the MOSFET drivers of the dual 25A/30A power supply. An external 2.2µF ceramic decoupling is required. $INTV_{CC}$ is regulated regardless of the RUN_C*n* pin state.

$EXTV_{CC}$ (R8): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal regulator whenever $EXTV_{CC}$ is higher than 4.7V and V_{IN} is higher than 7V. $EXTV_{CC}$ also powers up V_{DD33} when $EXTV_{CC}$ is higher than 4.7V and $INTV_{CC}$ is lower than 3.8V. Do not exceed 6V on this pin. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. If the $EXTV_{CC}$ pin is not used to power $INTV_{CC}$, the $EXTV_{CC}$ pin must be tied GND. Its recommended to use this pin if a bias is available to reduce power loss.

IN^+ (R10): Positive Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the IN^- and V_{INS3} pins. See 4:1 Divider Application Information section for detail about the input current sensing.

PGOOD_C0/PGOOD_C1 (R11/N5): Power Good Indicator Outputs. Open-drain logic output that is pulled to ground when the output exceeds the UV and OV regulation window. The output is deglitched by an internal 100µs filter. A pull-up resistor to 3.3V is required in the application.

V_{OSNS}^+_C0: (R12) Channel 0 Positive Differential Voltage Sense Input. Together, V_{OSNS}^+_C0 and V_{OSNS}^-_C0 serve to kelvin-sense the V_{OUTC0} output voltage at V_{OUTC0}'s point of load (POL) and provide the differential feedback signal directly to Channel 0's feedback loop. Command V_{OUTC0}'s target regulation voltage by serial bus. Its initial command value at V_{INS3} power-up is dictated by NVM (non-volatile memory) contents (factory default: 1.000V)—or, optionally, may be set by configuration resistors; see VOUTC0_CFG and the 4:1 Divider Application Information section.

SWC0, SWC1 (T10-T13), (T4-T7): Switching Node of Channel 0 and Channel 1. Used for test purposes or EMI snubbing.

4:1 DIVIDER BLOCK DIAGRAM

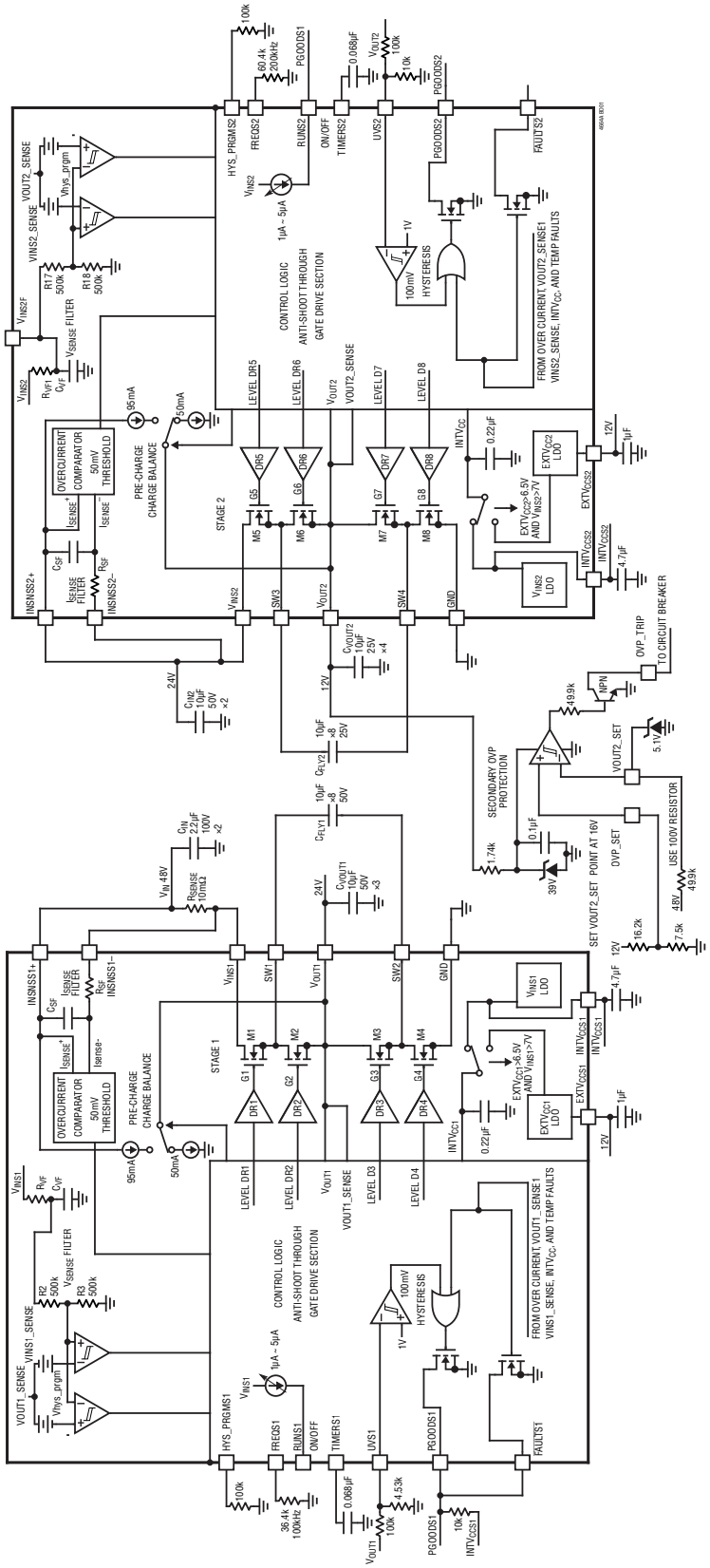


Figure 1. Simplified LTM4664A 4:1 Divider Block Diagram

DUAL 25A/30A POWER SYSTEM MANAGEMENT (PSM) BLOCK DIAGRAM

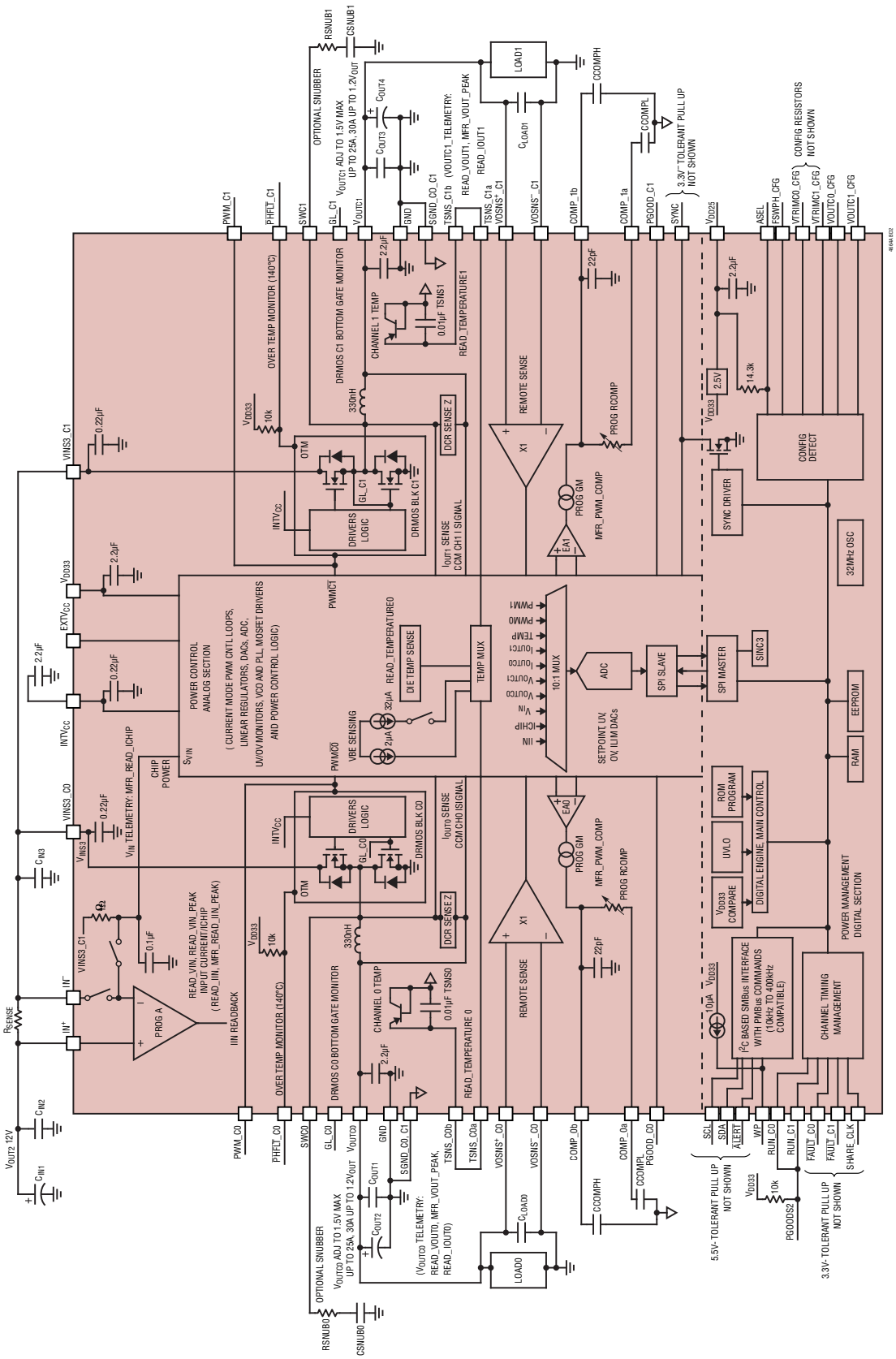


Figure 2. LTM4664A PSM Section Dual Channel 25A/30A PSM Block Diagram

4:1 DIVIDER OPERATION

4:1 DIVIDER DESCRIPTION

The LTM4664A incorporates a high performance 4:1 switched capacitor divider that divides down the input voltage by a factor of four over an input voltage range of 30V to 58V. This 4:1 divider then powers a dual 25A/30A PMBus compliant core power rails that can regulate from 0.5V to 1.5V at up to 25A, per channel—and from 0.5V to 1.2V at up to 30A per channel. The LTM4664A will convert this high input range down directly to the low output voltages.

MAIN CONTROL

The LTM4664A internal 4:1 divider utilizes two constant frequency, open loop switched capacitor/charge pump stages for high voltage step down. The conversion efficiency is very high at ~ 99% for stage 1, and ~98.6% efficient for stage 2. Refer to Figure 1 for the block diagram. In stage 1 steady state operation, the N-channel MOSFETs M1 and M3 are turned on and off in the same phase with around 50% duty cycle at a pre-programmed 100kHz switching frequency. The N-channel MOSFETs M2 and M4 are turned on and off complementary to MOSFETs M1 and M3. The gate drive waveforms are shown in Figure 3.

During phase 1, M1 and M3 are on and the flying capacitor C_{FLY1} is in series with C_{OUT1}. During phase 2, M2 and M4 are on and C_{FLY1} is in parallel with C_{OUT1}. The V_{OUT1} voltage is always close to half of the top voltage at the drain of MOSFET M1 (refer to GND pin) and in steady state and it is not sensitive to variable loads due to the very low impedance at its output. Stage 2 operates exactly the same way, the N-channel MOSFETs M5 and M7 are turned on and off in the same phase with around 50% duty cycle at a pre-programmed 300kHz switching frequency. The N-channel MOSFETs M6 and M8 are turned on and off complementary to MOSFETs M5 and M7. The main input voltage rail is connected to V_{INS1}, and V_{OUT1} is connected directly into the V_{INS2}. The LTM4664A front end divider stages do not regulate the output voltage with a closed-loop feedback system. However, it stops switching when fault conditions occur, such as V_{OUT} pin overvoltage or undervoltage, an overcurrent event, or an over temperature protection event.

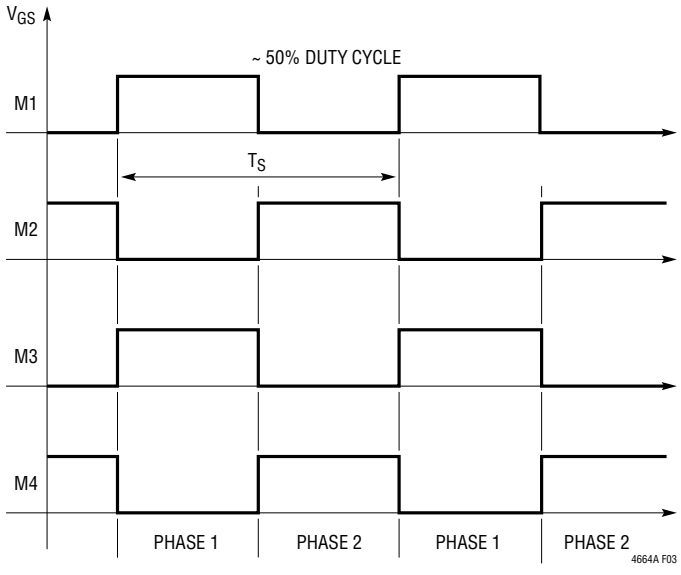


Figure 3. Stage 1 MOSFET Switching Waveforms

The V_{OUT2} (V_{INS1}/4) is connected to the V_{INS3_CSn} which is the inputs to the dual 25A/30A PMBus channels. This will be discussed in more detail in the dual 25A/30A operation section. There is a secondary fault protection comparator circuit that can be used to monitor V_{OUT2} for over voltage. This will be discussed in more detail in the application section. The LTM4664A can operate over a 30V to 58V input range that does have abrupt input voltage changes that move quicker than a few milliseconds after reaching steady state. See the window comparator section.

$INTV_{CCS1,2}$/$EXTV_{CCS1,2}$ POWER

Power for the quad N-channel MOSFET drivers and most other internal circuitry is derived from the $INTV_{CCSn}$ pin. Normally an internal 5.5V linear regulator supplies $INTV_{CCS1,2}$ power from either V_{INS1} or V_{INS2} as indicated in Figure 1. Both of these input supplies have high input voltage, and increases power loss due to the LDO drop. An optional external voltage source on $EXTV_{CCS1,2}$ pin enables a second 5.5V linear regulator and supplies $INTV_{CCS1,2}$ power from the $EXTV_{CCS1,2}$ pin. To enable this more efficient second regulator, $V_{INS1,2}$ has to be higher than 7V and the $EXTV_{CCS1,2}$ pin voltage has to be higher than 6.5V. Do not exceed 40V on the $EXTV_{CCSn}$ pin. Figure 1 shows the V_{OUT2} supply (12V) connected to both $EXTV_{CCS1}$ and $EXTV_{CCS2}$ to lower power loss in the LDO after startup.

4:1 DIVIDER OPERATION

Each of these can supply a peak current of 150mA. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CCSn}$ and GND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. These high input voltages along with the power MOSFETs being driven at high frequencies may cause the maximum junction temperature rating for the LTM4664A to be exceeded. The $INTV_{CCSn}$ current, which is dominated by the gate charge current, may be supplied by either the 5.5V linear regulator from V_{INSn} or the linear regulator from $EXTV_{CCSn}$. When the voltage on the $EXTV_{CCSn}$ pin is less than 6.5V, the linear regulator from V_{INSn} is enabled. Power dissipation for the internal controller in this case is highest and is equal to $V_{INSn} \bullet IINTV_{CCSn}$. The gate charge current is dependent on operating frequency. This is why it is highly recommended to use the V_{OUT2} voltage to supply power to the $EXTV_{CCS1,2}$ pins.

START-UP AND SHUTDOWN

The LTM4664A divider stages are in shutdown mode when their RUNS pins are pulled down and lower than 1.1V. In this mode, most internal circuitry is turned off including the $INTV_{CCS1,2}$ regulators and the 4:1 divider consumes less than 200µA current per stage. All gates drives are actively pulled low to turn off the external power MOSFETs in shutdown. Releasing RUNS1,2 allows an internal 1µA current to pull up these pins and enable the controller stage. Once the RUNS1,2 pin raises above 1.22V, an additional 5µA is flowing out of the respective pin. Alternately, the RUNS pin may be externally pulled up or driven directly by logic. Do not exceed the Absolute Maximum Rating of 6V on these pins. After RUNS1,2 pin is released and the $INTV_{CCS1,2}$ voltage passes UVLO, then that particular stage starts up and monitors the V_{INn} and V_{OUTn} voltage continuously. The LTM4664A divider stages start switching only if the V_{OUTn} voltage is close to half of the V_{INSn} voltage or both V_{OUTn} and V_{INSn} voltages are close to GND. In voltage divider applications, $V_{OUT1,2}$ is pre-balanced to half the $V_{INS1,2}$ voltage and the LTM4664A divider stages may start up with capacitors at different initial conditions and balancing will be invoked if necessary.

FAULT PROTECTION AND THERMAL SHUTDOWN

The LTM4664A divider stages monitor system voltage, current and temperature for faults. The stage 1 or 2 stops switching and pulls down its $\overline{FAULT}$ pin when fault conditions occur. To clear voltage faults, the V_{OUTn} pin voltage has to be within the programmed window around half of the V_{INSn} voltage or the V_{INSn} and V_{OUTSn} voltages must be lower than 1V and 0.5V respectively. To clear current faults, the voltage drop from $INSNSn^+$ pin to $INSNSn^-$ pin has to be lower than 50mV. To clear temperature faults, the IC temperature has to be lower than 165°C. The $\overline{FAULT}$ pin is allowed to be pulled up by external resistors to voltages up to 60V. It can also be used to control disconnect FETs that isolates the input and output during fault conditions. See Figure 1 block diagram.

HIGH SIDE CURRENT SENSING

For over current protection, the LTM4664A uses a sensing resistor R_{SENSE} to monitor the current. The sensing resistor has to be placed at the drain of the very top MOSFET M1. See Typical Application section for examples. In most applications, the current through the sensing resistor is a pulse current and the peak value is much higher than the average load current. An internal RC filter on the I_{SENSE}^- pin, with a time constant lower than switching frequency, is used to set the precision average current protection. If over current protection is not desired, short the I_{SENSE}^+ and I_{SENSE}^- pins together and connect them to the drain of top MOSFET M1 directly. This is done in stage 2 since stage 1 already monitors for current faults. See Figure 1.

FREQUENCY SELECTION

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger capacitance to maintain low output ripple voltage and low output impedance. The FREQS*n* pin can be used to program the controller's operating frequency from 100kHz to 1MHz. There is a precision 10µA current flowing out of the FREQS*n* pin, so the user can program the controller's switching frequency

4:1 DIVIDER OPERATION

with a single resistor to GND. The voltage on the FREQS*n* pin is equal to the resistance multiplied by 10µA current (e.g. the voltage is 1V with a 100k resistor from the FREQS*n* pin to GND). A curve is provided below showing the relationship between the voltages on the FREQS*n* pin and switching frequency. Stage 1 is operated at 100kHz, and Stage 2 is operated at 200kHz for optimal efficiency. See Figure 4.

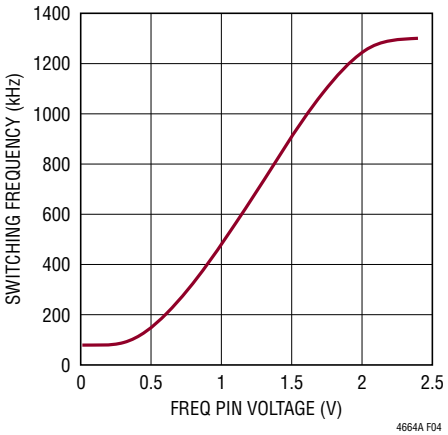


Figure 4. Relationship Between Switching Frequency and Voltage at FREQ Pin

f_{SW} (kHz) = R_{FREQ} (kΩ) • 8 – 317kHz

POWER GOOD AND UV (PGOODS*n* AND UVS*n* PINS)

When the UVS*n* pin voltage is lower than 1V, the PGOODS*n* pin is pulled low. The PGOODS*n* pin is also pulled low when the RUNS*n* pin is low or when the LTM4664A divider stages are starting up. The PGOODS*n* pin is released only when the LTM4664A stage is switching and UVS*n* pin is higher than 1V. The PGOODS*n* pin will flag power bad immediately when the UVS*n* pin is low. However, there is an internal 20µs power good mask and 100mV hysteresis when UVS*n* is higher than 1V. The PGOODS*n* pin is pulled up by external resistor to $INTV_{CC}$. The UVS1 pin is used to monitor the V_{OUT1} level for proper regulation, the PGOODS1 signal is used to sequence on the stage 2's RUNS2 pin. Then PGOODS2 is used to sequence on the downstream dual 25A/30A regulators. Proper setup on the UV pin to set a specific regulation point will release the PGOOD*n* pin when the output voltage is at that value. See Figure 1 block diagram.

ADDITIONAL OVERVOLTAGE PROTECTION

The OVP_SET, VOUT2_SET, and OVP_TRIP pins can be used to monitor the V_{OUT2} voltage for an overvoltage fault. These pins can be used in conjunction with the circuit in Figure 46 to provide a secondary OVP protection in and above the 4:1 divider fault protection. This feature can be used to trip off the input power, and further protect the low voltage outputs.

4:1 DIVIDER APPLICATION INFORMATION

A Typical Application in the Figure 1 block diagram shows the 4:1 voltage divider circuit. For the 1st stage voltage divider, the VINS1 input voltage is at the drain of very top MOSFET M1 and the output voltage is at the V_{OUT1} pin which is connected to the source of MOSFET M2 and the drain of MOSFET M3. The output voltage is around half of the input voltage in steady state. For the 2nd stage voltage divider, the V_{INS2} input voltage is at the drain of very top MOSFET M5 and the output voltage is at the V_{OUT2} pin which is connected to the source of MOSFET M6 and the drain of MOSFET M7. This completes the 4:1 divider.

For divider applications, if the load current is applied before startup or heavy resistive loads are connected to the VOUT*n* pin, the divider stages may not start up due to the limited drive current of the pre-balance circuit.

Therefore the PGOODS1 signal is used to sequence on stage 2 RUN2 pin, and the PGOODS2 pin is used to stage on the dual 25A/30A regulator.

VOLTAGE DIVIDER PRE-BALANCE BEFORE SWITCHING

In voltage divider applications, the V_{OUTn} voltage should be always close to $V_{INSn}/2$ in the steady state. The voltages on the flying capacitors (C_{FLYn}) and V_{OUTn} capacitors are all very close to each other and equal to the half of the input voltage. The charging inrush current is minimized during each switching cycle because the voltage difference between capacitors is small. However, without a special charging method such as the LTM4664A controller pre-charging circuitry, during start-up or fault conditions such as V_{OUTn} short to GND, the difference between capacitors can be large and huge charging currents may be large enough to cause very large MOSFETs currents. When switches M1 and M3 are on in the 1st stage, and M5 and M7 are on in the 2nd stage. Ideally, the inrush charge current is:

$$I = \frac{V_{INSn} - V_{CFLYn} - V_{OUTn}}{R_{ONMn} + R_{ONMn}}$$

When switches M2 and M4 are on or it is limited by the power MOSFET saturation current in the 1st stage, and M6 and M8 in the 2nd stage:

$$I = \frac{V_{CFLYn} - V_{OUTn}}{R_{ONMn} + R_{ONMn}}$$

With very low $R_{DS(ON)}$ of the power MOSFETs, the inrush charge current could easily achieve several hundreds of Amperes which can be higher than the MOSFET's Safe Operating Area (SOA).

The LTM4664A provides a proprietary pre-balance method to minimize the inrush charging current in voltage divider applications. The LTM4664A controller detects the V_{OUTn} pin voltage before switching and compares it with the $V_{INSn}/2$ internally. If the V_{OUTn} pin voltage is much lower than the $V_{INSn}/2$, a current source will source 95mA current to the V_{OUTn} pin to pull the V_{OUTn} pin up. If the V_{OUTn} pin voltage is much higher than the $V_{INSn}/2$, another current source will sink 50mA from V_{OUTn} pin to pull the V_{OUTn} pin down.

If the V_{OUTn} pin voltage is close to $V_{INSn}/2$ and within the pre-programmed window, both current sources are disabled and the divider stages start switching. After 68 switching cycles and the V_{OUTn} pin is still within the window, the $\overline{FAULTSn}$ pin is released.

For the 4:1 voltage divider with pre-balance startup, the LTM4664A assumes no load current or very small load current (less than 50mA) at the V_{OUTn} (output) otherwise the V_{OUTn} cannot reach $V_{INSn}/2$ and LTM4664A never starts up. This no load condition can be achieved by connecting the PGOOD*n* pin to the enable pins of the following electrical loads. If load current cannot be controlled off such as resistive loads, a disconnected FETs is required to disconnect the load to the V_{OUTn} during startup as shown in the typical applications. The input power source can operate over the 30V to 58V range, but the supply variation needs to be constrained to move much slower than the switching frequency and not exceed the hysteresis set by the HYS_PRGMS*n* pin. Large fast voltage excursions changes will force the 4:1 divider into pre-balance phase.

4:1 DIVIDER APPLICATION INFORMATION

Usually front end circuit breakers control the rate change and slew rate on the main input power which will eliminate this problem. As long as the input supply moves much slower than the operating frequency of the 4:1 divider, then the regulator will be able to balance without a need to pre-balance.

OVERCURRENT PROTECTION

The LTM4664A 4:1 divider provides overcurrent protection through a sensing resistor placed on the high voltage side. A precision rail to rail comparator monitors the differential voltage between INSNSS*n*$^+$ pin and INSNSS*n*$^-$ pin which are Kelvin connected to a sensing resistor. Whenever the INSNSS*n*$^+$ pin voltage is 50mV higher than INSNSS*n*$^-$ pin voltage, overcurrent fault is triggered and the $\overline{\text{FAULTSn}}$ pin is pulled down to ground. At the same time the divider stage stops switching and starts retry mode based on the timer pin setup. The overcurrent fault will be cleared when the TIMER*Sn* pin voltage reaches 4V and the voltage across the sensing resistor is less than 50mV.

The current through the sensing resistor is a pulse current during charging/discharging of the flying capacitors, which may result a voltage higher than the 50mV threshold at heavy loads. To prevent the inrush current from falsely triggering the overcurrent protection, an RC filter is required at the INSNSSn$^+$ pin and INSNSSn$^-$ The RC filter timer constant has to be larger than a switching period. Typically a 100Ω and 0.1µF filter is good for most of applications, and this filter is already included inside the LTM4664A. The current limit can be selected by choosing different sense resistor values. For example, 10mΩ sensing resistor sets current limit at 50mV/10mΩ = 5A ideally. Due to the switching ripple, the actual current limit is always lower than the ideal case. In real circuits, the current limit is around 4.2A with the 0.1µF/100Ω filter and 200kHz switching frequency. If overcurrent protection is not used, short INSNSSn$^+$ pin and INSNSSn$^-$ pin together and connect them to the drain of the top as shown in Figure 1 stage 2. Stage 2 current limit is not usually necessary since stage 1 already has it implemented. Also the dual 25A/30A regulators have overcurrent protection discussed later in the data sheet.

WINDOW COMPARATOR PROGRAMMING

In normal operation, V_{OUTn} voltage should be always close to half of the V_{INSn} voltage. A floating window comparator monitors the voltage on the V_{OUTn} pin and compares it with $V_{INSn}/2$. The window hysteresis voltage can be programmed and is equal to the voltage at the HYS_PRGMS*n* pin. There is a precision 10µA current flowing out of HYS_PRGMS*n* pin. A single resistor from HYS_PRGMSn pin to GND sets the HYS_PRGMS*n* pin voltage, which equals the resistor value multiplied by 10µA current (e.g. the voltage is 1V with a 100k resistor from the HYS_PRGM*Sn* pin to GND). With a 100k resistor on the HYS_PRGM*Sn* pin, the $V_{INSn}/2$ voltage has to be within (V_{OUTn} ± 1V) window during startup and normal operation, otherwise a fault is triggered and the LTM4664A divider stages stop switching.

The window hysteresis voltage can be linearly programmed from 0.3V to 2.4V with different resistor values on HYS_PRGMNS*n* pin. If the HYS_PRGMS*n* pin is tied to $INTV_{CC}$, a default 0.8V hysteresis window is applied internally. The hysteresis window voltage has to be programmed large enough to tolerate the V_{OUTn} pin voltage ripple and voltage drop at maximum load conditions. See Figure 5. Small internal RC filters can be used on these two pins to reject noise higher than the switching frequency.

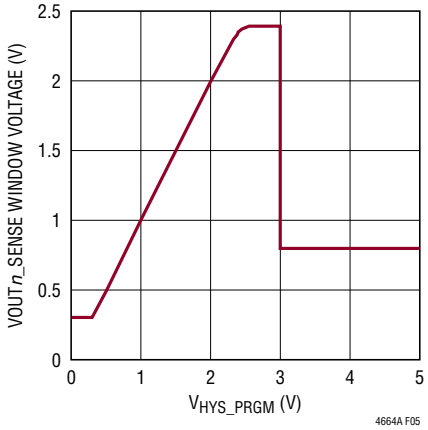


Figure 5. Relationship Between HYS_PRGM Pin Voltage and VOUT*n*_SENSE Window Comparator Voltage

4:1 DIVIDER APPLICATION INFORMATION

EFFECTIVE OPEN LOOP OUTPUT RESISTANCE AND LOAD REGULATION

The LTM4664A divider stages do not regulate the output voltage through a closed loop feedback system. However, the output voltage is not sensitive to load conditions due to the low output resistance when it is operating with a certain quantity of flying capacitors and high switching frequency. The Thevenin equivalent circuit of voltage divider circuit is shown in the Figure 6.

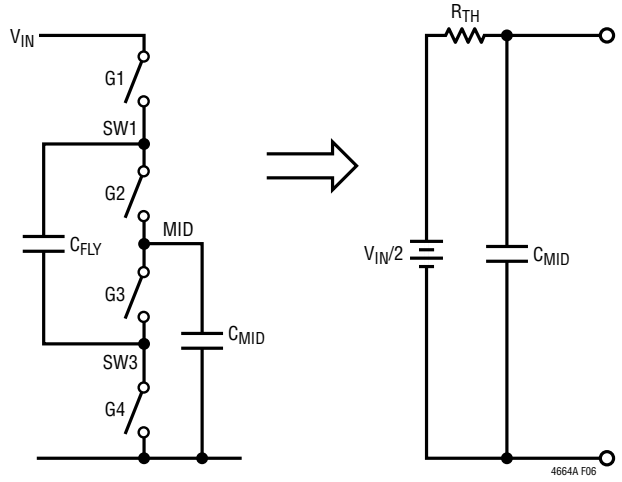


Figure 6.

When duty cycle is around 50%:

$$R_{OUT} = \frac{1+e^{-\frac{1}{4f_S R_{DS(ON)} C_{FLY}}}}{4f_S C_{FLY}\left(1-e^{-\frac{1}{4f_S R_{DS(ON)} C_{FLY}}}\right)}$$

Where:

f_S is the switching frequency.

C_{FLY} is the flying capacitor.

$R_{DS(ON)}$ is the on resistance of one MOSFET.

At low switching frequencies, $R_{TH} = 1/(4f_S\ C_{FLY})$. As frequency increases, the R_{TH} will finally approach $2R_{DS(ON)}$. In high power applications, it is suggested to select the switching frequency around $1/(16C_{FLY}\ R_{DS(ON)})$ or higher for decent load regulation and efficiency. At heavy load conditions, the output voltage will drop from $V_{INS}n/2$ by $R_{TH} \bullet I_{LOAD}$. In many applications, multi-layer ceramic capacitors (MLCC) are selected as flying capacitors. The voltage coefficients of MLCC capacitors strongly depend on the type and size of capacitors. Normally larger size X7R MLCC capacitors are better than X5R in terms of voltage coefficient. The capacitance still drops 20% to 30% capacitance with high DC bias voltage. Capacitance derating needs to be considered when estimating the output resistance of the switched capacitor circuits.

UNDERVOLTAGE LOCKOUT

The LTM4664A divider stages have a precision UVLO comparator constantly monitoring the $INTV_{CCS}n$ voltage to ensure that an adequate gate drive voltage is present. It locks out the switching action when $INTV_{CCS}n$ is below 4.9V. To prevent oscillation when there is a distu$_S$rbance on the $INTV_{CCS}n$, the UVLO comparator has 200mV of precision hysteresis. Another way to detect an under voltage condition is to monitor the input supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to the $V_{INS}n$ to turn on the stage when the input voltage is high enough. An extra 5µA of current flows out of the RUN pin once the RUNS*n* pin voltage passes 1.22V. One can program the hysteresis of the RUNS*n* comparator by adjusting the values of the resistive divider.

FAULT RESPONSE AND TIMER PROGRAMMING

The LTM4664A divider stages stop switching and pull the FAULTS*n* pins low during fault conditions. A capacitor connected from the TIMERS*n* pin to GND sets retry time to start-up if fault conditions are removed. The typical waveform on TIMERS*n* pin during fault condition is shown in Figure 7.

After the FAULTSn pin is pulled low, a 3.5µA pull-up current flows out of TIMER pin and starts to charge the TIMERS*n* capacitor. The pull-up current increases to 7µA when then TIMERS*n* pin voltage is higher than 0.5V and back to 3.5µA when the TIMERS*n* pin voltage is higher than 1.2V. The TIMERS*n* pin will be strongly pulled down whenever the fault conditions are removed or the TIMERS*n* pin voltage is higher than 4V. When the TIMERS*n* pin voltage

4:1 DIVIDER APPLICATION INFORMATION

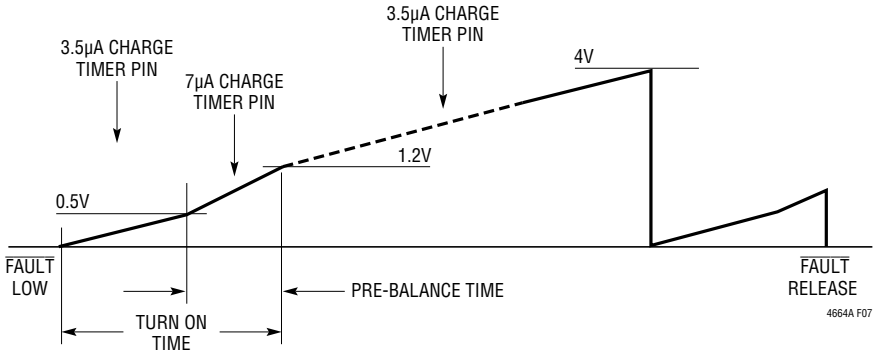


Figure 7. Timer Behavior During Fault or Startup

is between 0.5V and 1.2V, the internal pre-balance circuit will source or sink current to the V_{OUTn} pin and regulate the V_{OUTn} pin to $V_{INSn}/2$ with around 95mA/50mA capability. The pre-balance time can be calculated based on the capacitor $C_{TIMERSn}$ on the TIMERS*n* pin: $T_{PRE-BALANCE} = C_{TIMER} \bullet 0.7V/7\mu A$, so the pre-balance time is 100ms/µF (e.g. the pre-balance time is 10ms with 0.1µF C_{TIMER}). For voltage divider applications, if the flying capacitor C_{FLYn} and the V_{OUTn} capacitor are very large and input voltage is high, it may take several pre-balance time periods to pre-balance the V_{OUTn} pin to $V_{INSn}/2$ with a fixed C_{TIMER}. A longer start-up time is expected. Assuming zero initial conditions, the time to charge the capacitors, τcharge can be estimated from the equation:

$$\tau Charge = (C_{OUT} + C_{FLY}) \bullet (V_{IN} / 2 / 93mA)$$

Keep in mind that the approximate capacitor value will be the value at both voltage bias and temperature, this information can be derived from the capacitor data sheet curves.

Input/Output Capacitor and Flying Capacitor Selection

In high power switched capacitor applications, large AC currents flow through the flying capacitors and input/output capacitors. Low ESR ceramic capacitors are highly recommended for high power switch capacitor applications.

Make sure the maximum RMS capacitor current is within the spec or higher rated capacitors are preferred. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor.

Design Example

As a design example using LTM4664A divider stages for a the 4:1 divider at 72W, assume V_{INS1} = 48V (nominal), V_{INS1} = 60V (maximum), V_{OUT1} = 24V (nominal), I_{OUT1} = 3A (maximum) for stage 1. For high power and high voltage applications, always start with a low switching frequency e.g. 100kHz to minimize the switching losses. To set the stage 1 to 100kHz switching frequency, a 36.5k 1% resistor is connected from FREQS1 pin to ground. Set the C_{FLY1} voltage ripple to be 2% of the output voltage is a good starting point with tradeoff between efficiency and power density. The C_{FLY1} can be calculated based on the equation below:

$$I_{OUT1(MAX)} = 3A$$

$$C_{FLY} = \frac{I_{OUT1(MAX)}}{2 \bullet f_{SW} \bullet V_{CFLY1(RIPPLE)}}$$

$$\sim 31\mu F = \frac{3A}{2 \bullet 100kHz \bullet 0.48V}$$

Consider the ceramic capacitance derating at 24VDC bias voltage, 8 of 10µF/X7R/50V ceramic capacitors are paralleled as flying capacitors.

The 4:1 divider at 72W, assume V_{INS2} = 24V (nominal), V_{IN} = 30V (maximum), V_{OUT2} = 12V (nominal), I_{OUT2} = 6A (maximum) for stage 2. For stage 2 start with a switching frequency of 200kHz to minimize the switching losses. To set the 200kHz switching frequency, a 60.4k 1% resistor is connected from FREQS2 pin to ground. Set the C_{FLY2} voltage ripple to be 2% of the output voltage is a good starting point with trade-off between efficiency and

4:1 DIVIDER APPLICATION INFORMATION

power density. The C_{FLY2} can be calculated based on the equation below:

$$I_{OUT2(MAX)} = 6A$$

$$C_{FLY} = \frac{I_{OUT2(MAX)}}{2 \bullet f_{SW} \bullet V_{CFLY2(RIPPLE)}}$$

$$\sim 62\mu F = \frac{6A}{2 \bullet 200kHz \bullet 0.24V}$$

Consider the ceramic capacitance derating at 12VDC bias voltage, 8 of 10µF/X7R/50V ceramic capacitors are paralleled as flying capacitors.

Consider the ceramic capacitance derating at 24V and 12V DC bias voltage.

The worst case RMS current may be 40% higher than the maximum output current. So the worst case RMS on each capacitor can be estimated by this equation:

$$I_{RMS1(MAX)} = \frac{I_{OUT1(MAX)} \bullet 140\%}{N},$$

$N = \#$ of C_{FLY1} capacitor s in parallel in stage1

$$0.525A = \frac{3A \bullet 1.4}{8}$$

Each capacitor is rated for 2A IRMS, no issue

$$I_{RMS2(MAX)} = \frac{I_{OUT2(MAX)} \bullet 140\%}{N},$$

$N = \#$ of C_{FLY1} capacitor s in parallel in stage1

$$1.05A = \frac{6A \bullet 1.4}{8}$$

The output capacitor selection is similar to the flying capacitor selection. More output capacitors result smaller output voltage ripple. The output capacitor has less than 1/3 the CFLY RMS current, and the output capacitor can be much less than the flying capacitor. Some of output capacitors may be connected between input and output to serve as input capacitors at the same time. However the voltage rating of those capacitors has to be selected based on the input voltage instead of the output voltage.

Capacitors to use for 4:1 Divider

CAPACITOR VENDOR	VALUE (µF)	VOLTAGE (V)	PART NUMBER
Murata	10	50	GRM32ER71H106KA12
TDK	10	50	C3225X7R1H106M250AC
Murata	22	25	GRM32ER71G226KE15L
Taiyo Yuden	22	25	TMK325BJ226MMHT

DUAL 25A/30A PSM OPERATION

The LTM4664A Power System Management (PSM) includes a highly configurable dual 25A/30A output standalone nonisolated switching mode step-down DC/DC power supply with built-in EEPROM NVM (non-volatile memory) with ECC and I^2C-based PMBus/ SMBus 2-wire serial communication interface capable of 400kHz SCL bus speed. Two output voltages can be regulated (V_{OUTC0}, V_{OUTC1}—collectively, V_{OUTn}) with a few external input and output capacitors and pull-up resistors. Readback telemetry data of input and output voltages and input and output currents, and module temperatures are continually digitized cyclically by an integrated 16-bit ADC (analog-to-digital converter). Many fault thresholds and responses are customizable. Data can be autonomously saved to EEPROM when a fault occurs, and the resulting fault log can be retrieved over I^2C at a later time, for analysis. See Figure 2 for Block Diagram.

PSM SECTION OVERVIEW, MAJOR FEATURES

Major Features Include:

- Dedicated Power Good Indicators
- Direct Input and Chip Current Sensing
- Programmable Loop Compensation Parameters
- T_{INIT} Start-Up Time: 30ms
- PWM Synchronization Circuit, (See Frequency and Phasing Section for Details)
- MFR_ADC_CONTROL for Fast ADC Sampling of One Parameter (as Fast as 8ms) (See PMBus Command for Details)
- Fully Differential Output Sensing for Both Channels; V_{OUT0}/V_{OUT1} Both Programmable Up to 1.5V
- Power-Up and Program EEPROM with $EXTV_{CC}$
- Input Voltage Up to 18V
- ΔV_{BE} Temperature Sensing
- SYNC Contention Circuit (Refer to Frequency and Phase Section for Details)
- Fault Logging
- Programmable Output Voltage
- Programmable Input Voltage On and Off Threshold Voltage
- Programmable Current Limit per channel
- Programmable Switching Frequency
- Programmable OV and UV Threshold voltage
- Programmable ON and Off Delay Times
- Programmable Output Rise/Fall Times
- Phase-Locked Loop for Synchronous PolyPhase Operation (2, 3, 4 or 6 Phases)
- Nonvolatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Timebase Interconnect for Synchronization Between Multiple Controllers
- WP Pin to Protect Internal Configuration
- Stand Along Operation After User Factory Configuration
- PMBus, Version 1.2, 400kHz Compliant Interface

The PMBus interface provides access to important power management data during system operation including:

- Internal Controller Temperature
- Internal Power Channel Temperature Average Output Current
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Average Chip Input Current from V_{IN}
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.

Fault reporting and shutdown behavior are fully configurable. Two individual $\overline{FAULT\_C0}$, $\overline{FAULT\_C1}$ outputs are provided, both of which can be masked independently.

DUAL 25A/30A PSM OPERATION

Three dedicated pins for $\overline{\text{ALERT}}$, PGOOD_C0/PGOOD_C1 functions are provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (hiccup) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage
- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- Communication, Memory or Logic (CML) Fault

EEPROM WITH ECC

The LTM4664A PSM dual 25A/30A regulators contain internal EEPROM with ECC (Error Correction Coding) to store user configuration settings and fault log information. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations above T_J = 85°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures between –40°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, the slight degradation in the data retention characteristics of the fault log will not take away from the usefulness of the function.

It is recommended that the EEPROM not be written when the die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTM4664A PSM will disable all EEPROM write operations. All EEPROM write operations will be re-enabled when the die temperature drops below 125°C. (The controller will also disable all the switching when the die temperature exceeds the internal overtemperature fault limit 160°C with a 10°C hysteresis).

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using the following equation:

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

K = 8.617 • 10^{-5} eV/°K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature in °C

Example: Calculate the effect on retention when operating at a junction temperature of 135°C for 10 hours.

T_{STRESS} = 130°C

T_{USE} = 125°C,

$AF = e^{([(1.4/8.617 \bullet 10^{-5}) \bullet (1/398 - 1/403)])} = 16.6$

The equivalent operating time at 125°C = 16.6 hours.

Thus the overall retention of the EEPROM was degraded by 16.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the $\overline{\text{ALERT}}$ and RUN pins pulled low (PWM channels off). At that point the device will only respond at special address 0x7C, which is activated only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but use of these addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved. See the application Information section or contact

DUAL 25A/30A PSM OPERATION

the factory for details on efficient in-system EEPROM programming, including bulk EEPROM Programming, which the LTM4664A PSM also supports.

The LTM4664A PSM contains dual integrated constant frequency current mode control buck regulators (channel 0 and channel 1) whose built-in power MOSFETs are capable of fast switching speed. The factory NVM-default switching frequency clocks SYNC at 350kHz, to which the regulators synchronize their switching frequency. The default phase-interleaving angle between the channels is 180°. A pin-strapping resistor on FSWPH_CFG configures the frequency of the SYNC clock (switching frequency) and the channel phase relationship of the channels to each other and with respect to the falling edge of the SYNC signal. (Most possible combinations of switching frequency and phase-angle assignments are settable by resistor pin programming; see Table 3. Configure the LTM4664A's PSM NVM to implement settings not available by resistor-pin strapping.) When a FSWPH_CFG pin-strap resistor sets the channel phase relationship of the LTM4664A's PSM channels, the SYNC clock is not driven by the module; instead, SYNC becomes strictly a high impedance input and channel switching frequency is then synchronized to SYNC provided by an externally-generated clock or sibling LTM4664A with pull-up resistor to V_{DD33}. Switching frequency and phase relationship can be altered via the I^2C interface, but only when switching action is off, i.e., when the module is not regulating either output. See the Dual 25A/30A PSM Applications Information section for details.

Programmable analog feedback loop compensation for channel 0 and channel 1 is accomplished with a capacitor connection from COMP_C0a, 1a to SGND, and a capacitor from COMP_C0b, 1b to SGND.) The COMP_C0b, 1b pin is for the high frequency gain roll off and is the g_m amplifier output that has a programmable range, and the COMP_C0a, 1a pin has the programmable resistor range along with a capacitor to SGND that sets the frequency compensation. See Programmable Loop Compensation section. The LTM4664A dual 25A/30A regulators module have sufficient stability margins and good transient performance with a wide range of output capacitors—even all-ceramic MLCCs. Table 12 provides guidance on input and output capacitors recommended for many common operating conditions along with the programmable compensation settings. The Analog Devices LTpowerCAD tool is available for transient and stability analysis, and experienced users who prefer to adjust the module's feedback loop compensation parameters can use this tool.

POWER-UP AND INITIALIZATION

The LTM4664A dual 25A/30A regulators are designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It operates from a single input supply (4.5V to 16V) while three on-chip linear regulators generate internal 2.5V, 3.3V and 5.5V. The controller configuration is initialized by an internal threshold based UVLO where V_{IN} must be approximately 4V and the 5.5V, 3.3V and 2.5V linear regulators must be within approximately 20% of the regulated values. In addition to the power supply, a PMBus RESTORE_USER_ALL or MFR_RESET command can initialize the part too.

The $EXTV_{CC}$ pin is driven by an external regulator to improve efficiency of the circuit and minimize power loss when V_{INS3} is high. The $EXTV_{CC}$ pin must exceed approximately 4.7V, and V_{INS3} must exceed approximately 7V before the $INTV_{CC}$ LDO operates from the $EXTV_{CC}$ pin. To minimize application power, the $EXTV_{CC}$ pin can be supplied by a switching regulator.

During initialization, the external configuration resistors are identified and/or contents of the NVM are read into the controller's commands and the power train is held off. The RUN_C*n* and $\overline{\text{FAULT}}$_C*n* and PGOOD_C*n* are held low. The LTM4664A dual 25A/30A regulators will use the contents of Table 1 thru Table 5 to determine the resistor defined parameters. See the Resistor Configuration section for more details. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in NVM either at the factory or by the user.

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL configuration command), the LTM4664A PSM will use only the contents of NVM to determine the DC/DC characteristics. The ASEL value read at power-up or reset is always respected unless the pin is open. The ASEL will set the bottom 4LSBs and the MSBs are set by NVM. See the Dual 25A/30A PSM Applications Information section for more details.

DUAL 25A/30A PSM OPERATION

After the part has initialized, an additional comparator monitors V_{INS3}. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require 70ms to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional 0ms to 90ms.

SOFT-START

The method of start-up sequencing described below is time-based. The part must enter the run state prior to soft-start. Stage 2 of the 4:1 Divider will release RUN_C0 and RUN_C1 once it has reached regulation defined by the program valve set by UV_{S2}, and FAULT*n* is released. The RUN_C*n* pins are released by the LTM4664A PSM after the part is initialized and V_{INS3} is greater than the VIN_ON threshold. If multiple LTM4664A PSMs are used in an application, they all hold their respective RUN_C*n* pins low until all devices are initialized and V_{INS3} exceeds the VIN_ON threshold for every device. The SHARE_CLK pin assures all the devices connected to the signal use the same time base. The SHARE_CLK pin is held low until the part has been initialized after V_{INS3} is applied. The LTM4664A PSM can be set to turn-off (or remain off) if SHARE_CLK is low (set bit 2 of MFR_CHAN_CONFIG to 1). This allows the user to assure synchronization across numerous PSM devices even if the RUN_C*n* pins cannot be connected together due to board constraints. In general, if the user cares about synchronization between chips it is best not only to connect all the respective RUN_C*n* pins together but also to connect all the respective SHARE_CLK pins together and pulled up to V_{DD33} with a 10k resistor. This assures all chips begin sequencing at the same time and use the same time base.

After the RUN_C*n* pins release and prior to entering a constant output voltage regulation state, the LTM4664A PSM performs a monotonic initial ramp or “soft-start” on each of the 25A/30A outputs. Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTM4664A dual 25A/30A regulators are commanded to turn on (after power up and initialization), the controller waits for the user specified turn-on delay (TON_DELAY) prior to initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTM4664A PWM_C*n* always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom MOSFET is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a prebiased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit and the part transitions to the desired conduction mode after TON_RISE completes and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. However, setting TON_MAX_FAULT_LIMIT to a value of 0 is not recommended.

TIME-BASED SEQUENCING

The default mode for sequencing the outputs on and off is time-based. Each output is enabled after waiting TON_DELAY amount of time following either a RUN_C*n* pin going high, a PMBus command to turn on or the V_{IN} rising above a preprogrammed voltage. Off sequencing is handled in a similar way. To assure proper sequencing, make sure all ICs connect the SHARE_CLK pin together and RUN_C*n* pins together. If the RUN_C*n* pins cannot be connected together for some reasons, set bit 2 of MFR_CHAN_CONFIG to 1. This bit requires the SHARE_CLK pin to be clocking before the power supply output can start. When the RUN_C*n* pin is pulled low, the LTM4664A PSM will hold the pin low for the MFR_ RESTART_DELAY. The minimum MFR_RESTART_ DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTM4664A PSM calculates this delay internally and will not process a shorter delay. However, a longer commanded MFR_RESTART_DELAY can be used by the part. The maximum allowed value is 65.52 seconds.

VOLTAGE-BASED SEQUENCING

The sequence can also be voltage-based. As shown in Figure 8, The PGOOD_C*n* pins are asserted when the

DUAL 25A/30A PSM OPERATION

UV threshold is exceeded for each output. It is possible to feed the PGOOD_C*n* pin from one LTM4664A PSM channel into the RUN_C*n* pin of the next LTM4664A PSM channel in the sequence, especially across multiple LTM4664As. The PGOOD_C*n* has a 60µs filter. If the V_{OUT} voltage bounces around the UV threshold for a long period of time it is possible for the PGOOD_C*n* output to toggle more than once. To minimize this problem, set the TON_RISE time under 100ms.

If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

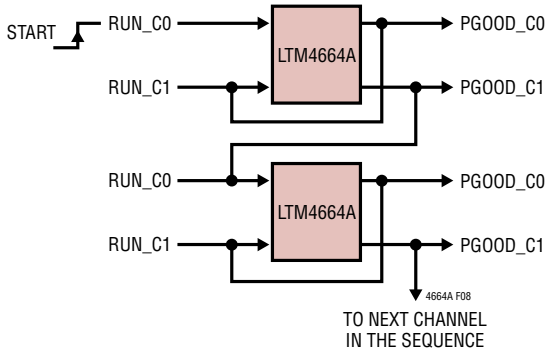


Figure 8. Event (Voltage) Based Sequencing

SHUTDOWN

The LTM4664A PSM Regulators supports two shutdown modes. The first mode is closed-loop shutdown response, with user defined turn-off delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the mode of operation for TOFF_FALL. The second mode is discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current, instead of TOFF_FALL.

The shutdown occurs in response to a fault condition or loss of SHARE_CLK (if bit 2 of MFR_CHAN_ CONFIG is set to a 1) or V_{IN} falling below the VIN_OFF threshold or $\overline{FAULT}$ pulled low externally (if the MFR_FAULT_ RESPONSE is set to inhibit). Under these conditions, the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states or through user intervention.

There are two ways to respond to faults; which are retry mode and latched off mode. In retry mode, the controller responds to a fault by shutting down and entering the inactive state for a programmable delay time (MFR_RETRY_ DELAY). This delay minimizes the duty cycle associated with autonomous retries if the fault that causes the shutdown disappears once the output is disabled. The retry delay time is determined by the longer of the MFR_RETRY_ DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If multiple outputs are controlled by the same $\overline{FAULT}$_C*n* pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG. Alternatively, latched off mode means the controller remains latched-off following a fault and clearing requires user intervention such as toggling RUN_C*n* or commanding the part OFF then ON.

LIGHT-LOAD CURRENT OPERATION

The LTM4664A PSM Regulators have two modes of operation: high efficiency discontinuous conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM _MODE command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

If a controller is enabled for discontinuous operation, the inductor current is not allowed to reverse. The reverse current comparator's output turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the COMP_C*n* pins. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry, but may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_ LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take

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up to $t_{CONVERT}$ to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction mode.

If the part is set to discontinuous mode operation, as the inductor average current increases, the controller will automatically modify the operation from discontinuous mode to continuous mode.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the PWM_C1 can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes the PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the master clock to other devices through PMBus command, NVM setting, or external configuration resistors as outlined in Table 3.

As clock master, a LTM4664A PSM device will drive its open-drain SYNC pin at the selected rate with a pulse width of 500ns. An external pull-up resistor between SYNC and V_{DD33} is required in this case. Only one device connected to SYNC should be designated to drive the pin. The other LTM4664A PSM devices will automatically revert to an external SYNC input, disabling its own SYNC, as long as the external SYNC frequency is greater than 80% of the programmed SYNC frequency. The external SYNC input shall have a duty cycle between 20% and 80%.

Whether configured to drive SYNC or not, the LTM4664A PSM devices can continue PWM operation using its own internal oscillator if an external clock signal is subsequently lost.

The device can also be programmed to always require an external oscillator for PWM operation by setting bit 4 of MFR_CONFIG_ALL. The status of the SYNC driver circuit is indicated by bit 10 of MFR_PADS.

The MFR_PWM_CONFIG command can be used to configure the phase of each channel. Desired phase can also be set from EEPROM or external configuration resistors as outlined in Table 3. Designated phase is the relationship between the falling edge of SYNC and the internal clock edge that sets the PWM latch to turn on the top power switch. Additional small propagation delays to the PWM control pins will also apply. Both PSM channels must be off before the FREQUENCY_SWITCH and MFR_PWM_CONFIG commands can be written to the LTM4664A PSM.

The phase relationships and frequency options provide for numerous application options. Multiple LTM4664A PSM channels modules can be synchronized to realize a PolyPhase array. In this case the phases should be separated by 360/*n* degrees, where *n* is the number of phases driving the output voltage rail.

PWM LOOP COMPENSATION

The internal PWM loop compensation resistors R_{COMPna} of the LTM4664A PSM can be adjusted using bit[4:0] of the MFR_PWM_COMP command.

The transconductance (gm) of the LTM4664A PSM channel PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_COMP command. These two loop compensation parameters can be programmed when the device is in operation. Refer to the Programmable Loop Compensation subsection in the Dual 25A/30A PSM Applications Information section for further details.

OUTPUT VOLTAGE SENSING

Both PSM channels in LTM4664A have differential amplifiers, which allow the remote sensing of the load voltage between V^+ and V^- pins. The telemetry ADC is also fully differential and makes measurements between V_{OSNS}^+_C*n* and V_{OSNS}^-_C*n* voltages for both channels at the V^+ and V^- pins, respectively. The maximum allowed is 1.5V, but the LTM4664A design is limited to 1.8V.

$INTV_{CC}/EXTV_{CC}$ POWER

Power for the internal MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is shorted to GND or tied to a voltage less than 4.7V, an internal 5.5V linear regulator supplies $INTV_{CC}$ power from V_{INS3}. If $EXTV_{CC}$ is taken above approximately 4.7V and V_{INS3_C1} is higher than 7.0V, the 5.5V regulator is turned off and an internal switch is turned on,

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connecting $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as a switching regulator output. $EXTV_{CC}$ can provide power to the internal 3.3V linear regulator even when V_{INS3} is not present, which allows the LTM4664A PSM to be initialized and programmed even without main power being applied.

The $INTV_{CC}$ regulator is powered from the V_{INS3_C1} pin, the power through the IC is equal to $V_{INS3\_C1} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency. The $INTV_{CC}$ regulator can supply up to 100mA, and the typical $INTV_{CC}$ current for the LTM4664A PSM is ~50mA. A 12V input voltage would equate to a difference of 7V drop across the internal controller, when multiplied by 50mA equals a 350mW power loss. This loss can be eliminated by providing an external 5V bias on the $EXTV_{CC}$ pin.

Do not tie $INTV_{CC}$ on the LTM4664A PSM to an external supply because $INTV_{CC}$ will attempt to pull the external supply high and hit current limit, significantly increasing the die temperature.

OUTPUT CURRENT SENSING AND SUB MILLIOHM DCR CURRENT SENSING

The LTM4664A PSM channels use a unique sub-milliohm inductor current sensing technique that provides a high level signal to noise ratio while sensing very low signals in current mode operation. This enables higher conversion efficiencies with the use of the internal sub-milliohm inductors in heavy load applications. The current limit threshold can be accurately set with the MFR_PWM_MODE[7] for high and low range. The low range setting MFR_PWM_MODE [7] = 0 should be used (see page103).

The internal DCR sensing network, thus current limit are calculated based on the DCR of the inductor at room temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor is written to the MFR_IOUT_CAL_GAIN_TC register. The external temperature is sensed near the inductor and used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. The current sensed is then digitized by the LTM4664A PSM telemetry ADC with an input range of ±128mV, a noise floor of $7\mu V_{RMS}$, and a peak-peak noise of approximately 46.5µV. The LTM4664A PSM computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in command MFR_IOUT_CAL_GAIN_TC. The resulting current value is returned by the READ_IOUT command.

INPUT CURRENT SENSING

To sense total input current consumed by the LTM4664A's 25A/30A two power stages , a sense resistor is placed between the supply voltage and V_{INS3} path. The I_{IN}^+ and I_{IN}^- pins are connected to the sense resistor. The filtered voltage is amplified by the internal high side current sense amplifier and digitized by the LTM4664A's PSM telemetry ADC. The input current sense amplifier has three gain settings of 2x, 4x, and 8x set by the bit[6:5] of the MFR_PWM_CONFIG command. The maximum input sense voltage for the three gain settings is 50mV, 20mV, and 5mV respectively. The LTM4664A PSM computes the input current using the internal R_{SENSE} value stored in the IIN_CAL_GAIN command. The resulting measured power stage current is returned by the READ_IIN command.

The LTM4664A uses a 1Ω resistor to measure the chip supply current being consumed by the LTM4664A PSM Controller. This value is returned by the MFR_READ_ICHIP command. The chip current is calculated by using the 1Ω value stored in the MFR_RVIN command. Refer to the subsection titled Input Current Sense Amplifier in the Dual 25A/30A PSM Applications Information section for further details.

PolyPhase LOAD SHARING

Multiple LTM4664As can be arrayed in order to provide a balanced load-share solution by bussing the necessary pins. Figure 48 illustrates a 4-Phase design sharing connections required for load sharing.

If an external oscillator is not provided, the SYNC pin should only be enabled on one of the LTM4664A's PSM Channels. The other(s) should be programmed to disable SYNC using bit 4 of MFR_CONFIG_ALL. If an external oscillator is present, the chip with the SYNC

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pin enabled will detect the presence of the external clock and disable its output.

Multiple channels need to tie all the V_{OSNS}^+_C*n* pins together, and all the V_{OSNS}^-_C*n* pins together, C_{OMP}_*n*a and C_{OMP}_*n*b pins together as well. Do not assert bit[4] of MFR_CONFIG_ALL except in a PolyPhase application.

The user must share the SYNC, SHARE_CLK, $\overline{\text{FAULT}}$_C*n*, and $\overline{\text{ALERT}}$ pins of these parts. Be sure to use pull-up resistors on SYNC, $\overline{\text{FAULT}}$_C*n*, SHARE_CLK and $\overline{\text{ALERT}}$.

EXTERNAL/INTERNAL TEMPERATURE SENSE

Temperature is measured using the internal diode-connected PNP transistors on either of the TSNS_C0b or TSNS_C1b pins corresponding to channel 0 or 1. TSNS_C*n*b pins should be connected to their respective TSNS_C*n*a pins, and these returns are directly connected to the LTM4664A PSM SGND_C0_C1 pin. Two different currents are applied to the diode (nominally 2µA and 32µA) and the temperature is calculated from a ΔV_{BE} measurement made with the internal 16-bit monitor ADC (see Figure 2, Block Diagram).

The LTM4664A PSM channels will only implement ΔV_{BE} temperature sensing, therefore MFR_PWM_MODE bit[5] is reserved.

RCONFIG (RESISTOR CONFIGURATION) PINS

There are six input pins utilizing 1% resistors for these pins to select key operating parameters. The pins are ASEL, FSWPH_CFG, VOUTC0_CFG, VOUTC1_CFG, VTRIMC0_CFG, VTRIMC1_CFG. If pins are floated, the value stored in the corresponding NVM command is used. If bit 6 of the MFR_CONFIG_ALL configuration command is asserted in NVM, the resistor input is ignored upon power-up except for ASEL which is always respected. The resistor configuration pins are only measured during a power-up reset or after a MFR_RESET or after a RESTORE_USER_ALL command is executed.

The VOUT*n*_CFG pin settings are described in Table 1. These pins set the LTM4664A V_{OUTC0} and V_{OUTC1} output voltage coarse settings. If the pin is open, the VOUT_COMMAND command is loaded from NVM to determine the output voltage. The default setting is to have the switcher off unless the voltage configuration pins are installed. The VTRIMn_CFG pins in Table 2 are used to set the output voltage fine adjustment setting. Both combine to offer several distinct output voltages.

The following parameters are set as a percentage of the output voltage if the RCONFIG pins are used to determine the output voltage:

- VOUT_OV_FAULT_LIMIT.....+10%
- VOUT_OV_WARN_LIMIT.....+7.5%
- VOUT_MAX.....+7.5%
- VOUT_MARGIN_HIGH.....+5%
- VOUT_MARGIN_LOW.....–5%
- VOUT_UV_FAULT_LIMIT.....–7%

The FSWPH_CFG pin settings are described in Table 3. This pin selects the switching frequency and phase of each channel. The phase relationships between the two channels and SYNC pin are determined in Table 3. To synchronize to an external clock, the part should be put into external clock mode (SYNC output disabled but frequency set to the nominal value). If no external clock is supplied, the part will clock at the programmed frequency. If the application is multiphase and the SYNC signal between chips is lost, the parts will not operate at the designed phase even if they are programmed and trimmed to the same frequency.

This may increase the ripple voltage on the output, possibly produce undesirable operation. If the external SYNC signal is being generated internally and external SYNC is not selected, bit 10 of MFR_PADS will be asserted. If no frequency is selected and the external SYNC frequency is not present, a PLL_FAULT will occur. If the user does not wish to see the $\overline{\text{ALERT}}$ from a PLL_FAULT even if there is not a valid synchronization signal at power-up, the $\overline{\text{ALERT}}$ mask for PLL_FAULT must be written. See the description on SMBALERT_MASK for more details. If the SYNC pin is connected between multiple ICs only one of the ICs should have the SYNC pin enabled using the MFR_CONFIG_ALL[4] =1, and all other ICs should be configured to have the SYNC pin disabled with MFR_CONFIG_ALL[4] =0.

The ASEL pin settings are described in Table 4. ASEL selects slave address for the LTM4664A PSM. For more detail, refer to Table 5.

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NOTE: Per the PMBus specification, pin programmed parameters can be overridden by commands from the digital interface with the exception of ASEL which is always honored. Do not set any part address to 0x5A or 0x5B because these are global addresses and all parts will respond to them.

Table 1. VOUTC*n*_CFG Pin Strapping Look-Up Table for the LTM4664A's PSM Output Voltages, Coarse Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1b)

R_{VOUTn_CFG} TOP (kΩ)	R_{VOUTn_CFG}* BOT (kΩ)	V_{OUTn} (V) SETTING COARSE	MFR_PWM MODE*n*[1] BIT
14.3	Open	NVM	NVM
14.3	32.4	NVM	NVM
14.3	22.6	3.3	0
14.3	18.0	3.1	0
14.3	15.4	2.9	0
14.3	12.7	2.7	0
14.3	10.7	2.5	0, if V_{TRIMn} > 0mV 1, if V_{TRIMn} ≤ 0mV
14.3	9.09	2.3	1
14.3	7.68	2.1	1
14.3	6.34	1.9	1
14.3	5.23	1.7	1
14.3	4.22	1.5	1
14.3	3.24	1.3	1
14.3	2.43	1.1	1
14.3	1.65	0.9	1
14.3	0.787	0.7	1
14.3	0	0.5	1

*R_{VOUTCn_CFG} value indicated is nominal. Select R_{VOUTCn_CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect R_{VOUTCn_CFG}'s value over time. All such effects must be taken into account in order for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_ USER_ALL, over the lifetime of one's product.

Table 2. VTRIM*n*_CFG Pin Strapping Look-Up Table for the LTM4664A's PSM Output Voltages, Fine Adjustment Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1b)

R_{VTRIMn_CFG}* BOT (kΩ)	V_{TRIM} (mV) FINE ADJUSTMENT TO V_{OUTn} SETTING WHEN RESPECTIVE	R_{VTRIMn_CFG} TOP (kΩ)
Open	0	14.3
32.4	99	14.3
22.6	86.625	14.3
18.0	74.25	14.3
15.4	61.875	14.3
12.7	49.5	14.3
10.7	37.125	14.3
9.09	24.75	14.3
7.68	12.375	14.3
6.34	–12.375	14.3
5.23	–24.75	14.3
4.22	–37.125	14.3
3.24	–49.5	14.3
2.43	–61.875	14.3
1.65	–74.25	14.3
0.787	–86.625	14.3
0	–99	14.3

*$R_{VTRIMCn\_CFG}$ value indicated is nominal. Select $R_{VTRIMCn\_CFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{VTRIMCn\_CFG}$'s value over time. All such effects must be taken into account in order for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET, or RESTORE_USER_ALL over the lifetime of one's product.

Example:

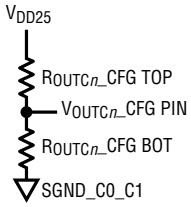

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Table 3. FSWPH_CFG Pin Strapping Look-Up Table to Set the LTM4664A's PSM Switching Frequency and Channel Phase-Interleaving Angle (Not Applicable if MFR_CONFIG_ALL[6] = 1b)

R_{FSWPH_CFG} TOP (kΩ)	R_{FSWPH_CFG}* BOT (kΩ)	SWITCHING FREQUENCY (kHz)	θSYNC TO θ0	θSYNC TO θ1	bits [2:0] of MFR_PWM_CONFIG	bit [4] of MFR_CONFIG_ALL
14.3	Open	NVM; LTM4664A PSM Default = 500	NVM; LTM4664A Default = 0°	NVM; LTM4664A PSM Default = 180°	NVM; LTM4664A PSM Default = 000b	NVM; LTM4664A PSM Default = 0b
14.3	32.4	250	0°	180°	000b	0b
14.3	22.6	350	0°	180°	000b	0b
14.3	18.0	425	0°	180°	000b	0b
14.3	15.4	575	0°	180°	000b	0b
14.3	12.7	650	0°	180°	000b	0b
14.3	10.7	750	0°	180°	000b	0b
14.3	7.68	500	120°	240°	100b	0b
14.3	6.34	500	90°	270°	001b	0b
14.3	5.23	External**	0°	240°	010b	1b
14.3	4.22	External**	0°	120°	011b	1b
14.3	3.24	External**	60°	240°	101b	1b
14.3	2.43	External**	120°	300°	110b	1b
14.3	1.65	External**	90°	270°	001b	1b
14.3	0.787	External**	0°	180°	000b	1b
14.3	0	External**	120°	240°	100b	1b

*R_{FSWPH_CFG} value indicated is nominal. Select R_{FSWPH_CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect R_{FSWPH_CFG}'s value over time. All such effects must be taken into account in order for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

**External setting corresponds to FREQUENCY_SWITCH (Register 0x33) value set to 0x0000; the device synchronizes its switching frequency to that of the clock provided on the SYNC pin, provided MFR_CONFIG_ALL[4] = 1b.

Example:

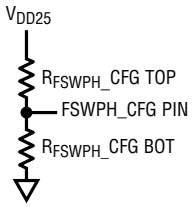

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Table 4. ASEL Pin Strapping Look-Up Table to Set the LTM4664A's PSM Slave Address (Applicable Regardless of MFR_CONFIG_ALL[6] Setting)

R_{ASEL}* (kΩ)	SLAVE ADDRESS
Open	MFR_ADDRESS[6:0]_R/W
32.4	MFR_ADDRESS[6:4]_1111_R/W
22.6	MFR_ADDRESS[6:4]_1110_R/W
18.0	MFR_ADDRESS[6:4]_1101_R/W
15.4	MFR_ADDRESS[6:4]_1100_R/W
12.7	MFR_ADDRESS[6:4]_1011_R/W
10.7	MFR_ADDRESS[6:4]_1010_R/W
9.09	MFR_ADDRESS[6:4]_1001_R/W
7.68	MFR_ADDRESS[6:4]_1000_R/W
6.34	MFR_ADDRESS[6:4]_0111_R/W
5.23	MFR_ADDRESS[6:4]_0110_R/W
4.22	MFR_ADDRESS[6:4]_0101_R/W
3.24	MFR_ADDRESS[6:4]_0100_R/W
2.43	MFR_ADDRESS[6:4]_0011_R/W
1.65	MFR_ADDRESS[6:4]_0010_R/W
0.787	MFR_ADDRESS[6:4]_0001_R/W
0	MFR_ADDRESS[6:4]_0000_R/W

Where:

R/W = Read/Write bit in control byte

All PMBus device addresses listed in the specification are 7 bits wide unless otherwise noted.

Note: The LTM4664A PSM will always respond to slave address 0x5A and 0x5B regardless of the NVM or ASEL resistor configuration values.

*R_{CFG} value indicated is nominal. Select R_{CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect R_{CFG}'s value over time. All such effects must be taken into account in order for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

Example:

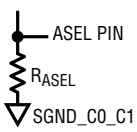

Table 5. LTM4664A PSM MFR_ADDRESS Command Examples Expressed in 7- and 8-Bit Addressing

	HEX DEVICE ADDRESS		BIT								
DESCRIPTION	7-BIT	8-BIT	7	6	5	4	3	2	1	0	R/W
Rail[4]	0x5A	0xB4	0	1	0	1	1	0	1	0	0
Global[4]	0x5B	0xB6	0	1	0	1	1	0	1	1	0
Default	0x4F	0x9E	0	1	0	0	1	1	1	1	0
Example 1	0x40	0x80	0	1	0	0	0	0	0	0	0
Example 2	0x41	0x82	0	1	0	0	0	0	0	1	0
Disabled[2,3]			1	0	0	0	0	0	0	0	0

Note 1. This table can be applied to the MFR_RAIL_ADDRESS*n* commands, but not the MFR_ADDRESS command.

Note 2. A disabled value in one command does not disable the device, nor does it disable the global address.

Note 3. A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

Note 4. It is not recommended to write the value 0x00, 0x0C (7-bit), 0x5A (7-bit), 0x5B (7-bit) or 0x7C(7-bit) to the MFR_CHANNEL_ADDRESS*n* or the MFR_RAIL_ADDRESSn commands.

FAULT DETECTION AND HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV $\overline{\text{FAULT}}$ Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal control Die and Internal Module Overtemperature Fault and Warn Protection
- Internal Undertemperature Fault and Warn Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional $\overline{\text{FAULT}}$_C*n* Pins

In addition, the LTM4664A PSM can map any combination of fault indicators to their respective $\overline{\text{FAULT}}$_C*n* pin using the propagate $\overline{\text{FAULT}}$*n* response commands, MFR_FAULT_ PROPAGATE. Typical usage of a $\overline{\text{FAULT}}$_C*n* pin is as a driver for an external crowbar device, overtemperature alert, overvoltage alert or as an interrupt

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to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{\text{FAULT}}$_C*n* pins can be used as inputs to detect external faults downstream of the controller that require an immediate response.

Any fault or warning event will always cause the $\overline{\text{ALERT}}$ pin to assert low unless the fault or warning is masked by the SMBALERT_MASK. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1 or bias power is cycled or a MFR_RESET command is issued, or the RUN pins are toggled OFF/ON or the part is commanded OFF/ON via PMBus or an ARA command operation is performed. The MFR_FAULT_PROPAGATE command determines if the $\overline{\text{FAULT}}$_C*n* pins are pulled low when a fault is detected.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Table 3 thru 17. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault conditions not present after the retry interval has elapsed, a new soft-start is attempted.

If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling, assuming the fault condition itself is not immediately destructive. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Status Registers and $\overline{\text{ALERT}}$ Masking

Figure 9 summarizes the internal LTM4664A PSM status registers accessible by PMBus command. These contain indication of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands also summarize contents of other status registers. Refer to PMBus Command Summary for specific information.

NONE OF THE ABOVE in the STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

In general, any asserted bit in a STATUS_x register also pulls the $\overline{\text{ALERT}}$ pin low. Once set, $\overline{\text{ALERT}}$ will remain low until one of the following occurs.

- A CLEAR_FAULTS or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTM4664A PSM Successfully Transmits Its Address During a PMBus ARA
- Bias Power Is Cycled

With some exceptions, the SMBALERT_MASK command can be used to prevent the LTM4664A PSM from asserting $\overline{\text{ALERT}}$ for bits in these registers on a bit-by-bit basis. These mask settings are promoted to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if $\overline{\text{ALERT}}$ is masked for all bits in channel 0 STATUS_VOUT, then $\overline{\text{ALERT}}$ is effectively masked for the V_{OUT} bit in STATUS_WORD for PAGE 0. The BUSY bit in STATUS_BYTE also asserts $\overline{\text{ALERT}}$ low and cannot be masked. This bit can be set as a result of various internal interactions with PMBus communication. This fault occurs when a command is received that cannot be safely executed with one or both channels enabled. As discussed in the 4:1 Divider Application Information, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

If masked faults occur immediately after power up, $\overline{\text{ALERT}}$ may still be pulled low because there has not been time to retrieve all of the programmed masking information from EEPROM.

Status information contained in MFR_COMMON and MFR_PADS can be used to further debug or clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the $\overline{\text{ALERT}}$ pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.

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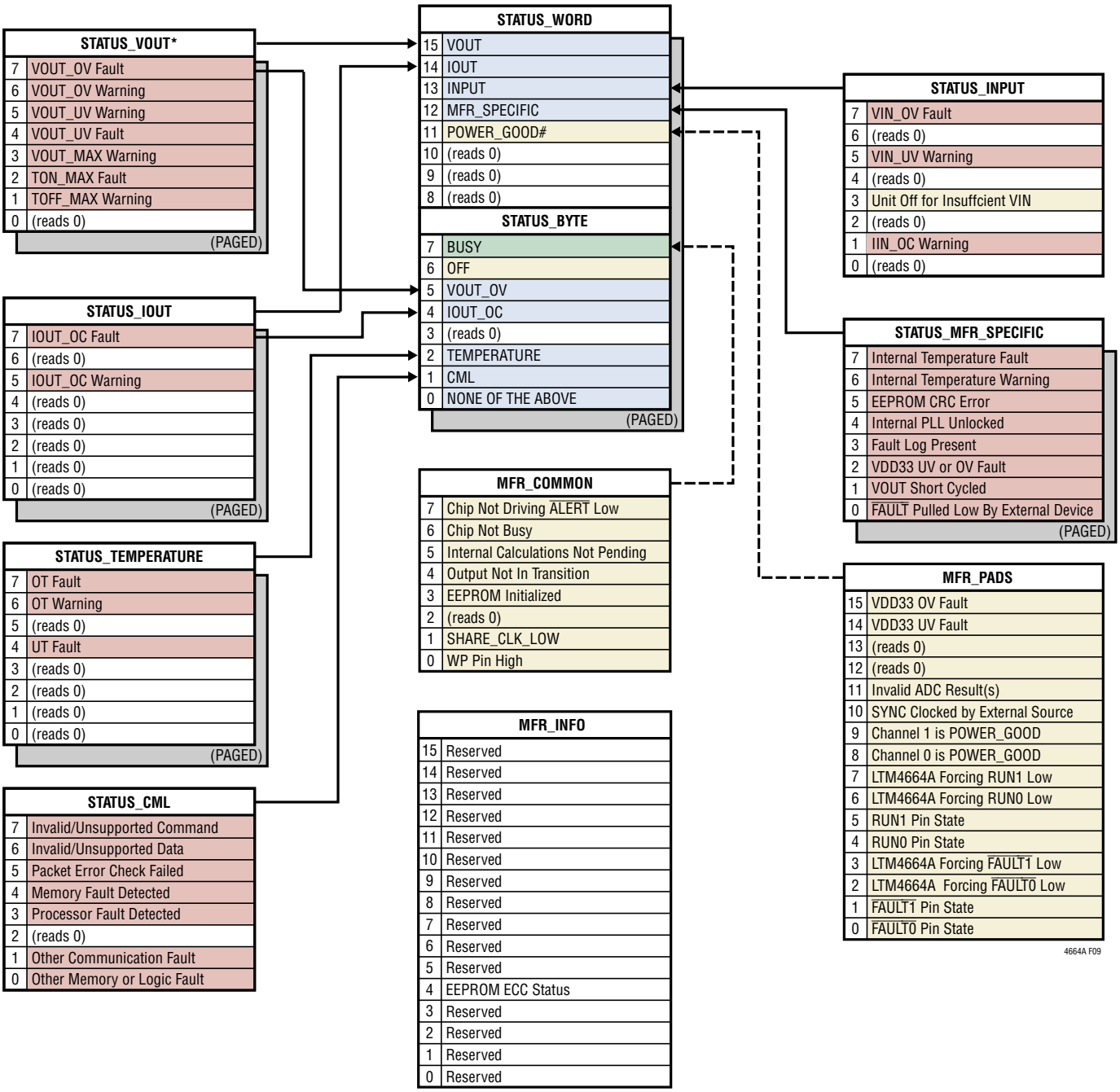

DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
General Non-Maskable Event	No	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

Figure 9. LTM4664A PSM Status Register Summary

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Mapping Faults to $\overline{\text{FAULT}}$ Pins

Channel-to-channel fault (including channels from multiple LTM4664A PSMs) dependencies can be created by connecting $\overline{\text{FAULT}}$_C*n* pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{FAULT}}$_C*n* pins low. The other channels are then configured to shut down when the $\overline{\text{FAULT}}$_C*n* pins are pulled low. For autonomous group retry, the faulted channel is configured to let go of the $\overline{\text{FAULT}}$_C*n* pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{FAULT}}$_C*n* pin remains asserted low until either the RUN_C*n* pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN_C*n* either by the pin or OFF/ON command will clear faults associated with the channel. If it is desired to have all faults cleared when either RUN_C*n* pin is toggled or, set bit 0 of MFR_CONFIG_ALL to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities are: See Table 18.

Power Good Pins

The PGOOD_C*n* pins of the LTM4664A PSM are connected to the open drains of internal MOSFETs. The MOSFETs turn on and pull the PGOOD_C*n* pins low when the channel output voltage is not within the channel's UV and OV voltage thresholds. During TON_DELAY and TON_RISE sequencing, the PGOOD_C*n* pin is held low. The PGOOD_C*n* pin is also pulled low when the respective RUN_C*n* pin is low. The PGOOD_C*n* pin response is deglitched by an internal 100µs digital filter. The PGOOD_C*n* pin and PGOOD status may be different at times due to communication latency of up to 10µs.

CRC Protection

The integrity of the NVM memory is checked after a power on reset. A CRC error will prevent the controller from leaving the inactive state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ pin will be pulled low. NVM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command.

The LTM4664A manufacturing section of the NVM is mirrored. If both copies are corrupted, the "NVM CRC Fault" in the STATUS_MFR_SPECIFIC command is set. If this bit remains set after being cleared by issuing a CLEAR_FAULTS or writing a 1 to this bit, an irrecoverable internal fault has occurred. The user is cautioned to disable both output power supply rails associated with this specific part. There are no provisions for field repair of NVM faults in the manufacturing section.

SERIAL INTERFACE

The LTM4664A serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the NVM or an external resistor divider. In addition the LTM4664A always responds to the global broadcast address of 0x5A (7-bit) or 0x5B (7-bit).

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word and 7) read block. 8) write block. All read operations will return a valid PEC if the PMBus master requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTM4664A.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTM4664A PSM offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

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Global addressing provides a means of the PMBus master to address all LTM4664A PSM devices on the bus. The LTM4664A PSM global address is fixed 0x5A (7-bit) or 0xB4 (8-bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7-bit) or 0xB6 (8-bit) is paged and allows channel specific command of all LTM4664A PSM devices on the bus. Other LTC device types may respond at one or both of these global addresses. Reading from global addresses is strongly discouraged.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTM4664A PSM. The value of the device address is set by a combination of the ASEL configuration pin and the MFR_ ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

Rail addressing provides a means for the bus master to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Reading from rail addresses is also strongly discouraged.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTM4664A PSM devices at global and rail addresses should be limited to command write operations.

RESPONSES TO V_{OUT} AND I_{IN}/I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in three ways:

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In NVM if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus these values are based on average currents and can have a time latency of up to $t_{CONVERT}$. The I_{OUT} calculation accounts for the DCR and their temperature coefficient. The input current is equal to the voltage measured across the R_{SENSE} resistor divided by the resistors value as set with the MFR_IIN_CAL_GAIN command. If this calculated input current exceeds the IN_OC_WARN_LIMIT the $\overline{ALERT}$ pin is pulled low and the IIN_OC_WARN bit is asserted in the STATUS_INPUT command.

The digital processor within the LTM4664A PSM provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_ DELAY and can be from 120ms to 83.88 seconds in 1ms increments. The shutdown for OV/UV and OC can be done immediately or after a user selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots as well as long-term overvoltages at the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on. However, the reverse output current is monitored while device is in OV fault. When it reaches the limit, both top and bottom MOSFETs are turned off. The top and bottom MOSFETs will keep their state until the overvoltage condition is cleared regardless of the PMBus VOUT_OV_ FAULT_RESPONSE command byte value. This hardware level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_ OV_FAULT_RESPONSE command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV Cannot Be Ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be de-glitched in increments of (0-7) • 10µs. See Table 14.

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Output Undervoltage Response

The response to an undervoltage comparator output can be the following:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The UV responses can be deglitched. See Table 14.

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak output current across the inductor is always limited on a cycle-by-cycle basis. The value of the peak current limit is specified in Electrical Characteristics table. The current limit circuit operates by limiting the COMP_C*n* maximum voltage. Since internal DCR sensing is used, the COMP_C*n* maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LTM4664A PSM automatically monitors the external temperature sensors and modifies the maximum allowed COMP_C*n* to compensate for this term. The IOUT_OC_FAULT_LIMIT section provides data points for I_{OUT} Limiting on page103.

The overcurrent fault processing circuitry can execute the following behaviors:

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The overcurrent responses can be deglitched in increments of (0-7) • 16ms. See Table 15.

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT condition is predicated upon detection of the VOUT_UV_FAULT_LIMIT as the output is undergoing a SOFT_START sequence. The TON_MAX_ FAULT_LIMIT time is started after TON_DELAY has been reached and a SOFT_START sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT _LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value. This response may be one of the following:

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT means the fault is ignored. The TON_MAX_FAULT_LIMIT should be set longer than the TON_RISE time. It is recommended TON_MAX_FAULT_LIMIT always be set to a non-zero value, otherwise the output may never come up and no flag will be set to the user. See Table 16.

RESPONSES TO V_{IN} OV FAULTS

V_{IN} overvoltage is measured with the ADC. The response is naturally deglitched by the 100ms typical response time of the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 16.

RESPONSES TO OT/UT FAULTS

Internal Overtemperature Fault Response

An internal temperature sensor protects against NVM damage. Above 85°C, no writes to NVM are recommended. Above 130°C, the internal overtemperature warn threshold is exceeded and the part disables the NVM and does not re-enable until the temperature has dropped to 125°C. When the die temperature exceed 160°C the internal temperature fault response is enabled and the PWM is disabled until the die temperature drops below 150°C. Temperature is measured by the ADC. Internal

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temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user. See Table 14.

External Overtemperature and Undertemperature Fault Response

Two internal temperature sensors are used to sense the temperature of critical circuit elements like inductors and power MOSFETs on each channel. The OT_FAULT_ RESPONSE and UT_FAULT_ RESPONSE commands are used to determine the appropriate response to an overtemperature and under temperature condition, respectively. If no external sense elements are used (not recommended) set the UT_FAULT_ RESPONSE to ignore—and set the UT_FAULT_LIMIT to 275°C. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time

Interval Specified in MFR_RETRY_DELAY. See Table 16.

RESPONSES TO INPUT OVERCURRENT AND OUTPUT UNDERCURRENT FAULTS

Input overcurrent and output undercurrent are measured with the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 15.

RESPONSES TO EXTERNAL FAULTS

When either $\overline{\text{FAULT}}$_C*n* pin is pulled low, the OTHER bit is set in the STATUS_WORD command, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down then retry in response to its $\overline{\text{FAULT}}$_C*n* pin going low by modifying the MFR_FAULT_RESPONSE command. To avoid the $\overline{\text{ALERT}}$ pin asserting low when $\overline{\text{FAULT}}$_C*n* is pulled low, assert bit 1 of MFR_CHAN_CONFIG, or mask the ALERT using the SMBALERT_MASK command.

FAULT LOGGING

The LTM4664A PSM has fault logging capability. Data is logged into memory in the order shown in Table 19. The data is stored in a continuously updated buffer in RAM. When a fault event occurs, the fault log buffer is copied from the RAM buffer into NVM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C the fault logging is delayed until the die temperature drops below 125°C. The fault log data remains in NVM until a MFR_FAULT _LOG_CLEAR command is issued. Issuing this command re-enables the fault log feature. Before re-enabling fault log, be sure no faults are present and a CLEAR_FAULTS command has been issued.

When the LTM4664A PSM powers-up or exits its reset state, it checks the NVM for a valid fault log. If a valid fault log exists in NVM, the "Valid Fault Log" bit in the STATUS_ MFR_SPECIFIC command will be set and an $\overline{\text{ALERT}}$ event will be generated. Also, fault logging will be blocked until the LTM4664A PSM has received a MFR_FAULT_LOG_ CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller on either channel. A $\overline{\text{FAULT}}$_C*n* being externally pulled low will not trigger a fault logging event.

BUS TIMEOUT PROTECTION

The LTM4664A PSM implements a timeout feature to avoid persistent faults on the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 30ms or the LTM4664A PSM will three-state the bus and ignore the given data packet. If more time is required, assert bit 3 of MFR_CONFIG_ALL to allow typical bus timeouts of 255ms. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

The LTM4664A PSM allows longer PMBus timeouts for block read data packets. This timeout is proportional to the length of the block read. The additional block read timeout applies primarily to the MFR_FAULT_LOG command. The timeout period defaults to 32ms.

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The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTM4664A PSM supports the full PMBus frequency range from 10kHz to 400kHz.

SIMILARITY BETWEEN PMBus, SMBus AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent persistent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

The LTM4664A PSM supports the maximum SMBus clock speed of 100kHz and is compatible with the higher speed PMBus specification (between 100kHz and 400kHz) if MFR_ COMMON polling or clock stretching is enabled. For robust communication and operation refer to the Note section in the PMBus command summary. Clock stretching is enabled by asserting bit 1 of MFR_CONFIG_ALL.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.2: Paragraph 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus SERIAL DIGITAL INTERFACE

The LTM4664A PSM communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 10, shows the timing relationship of the signals on the bus. The two-bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LTM4664A is a slave device. The master can communicate with the LTM4664A using the following formats:

- Master Transmitter, Slave Receiver
- Master Receiver, Slave Transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read, Block Write
- Alert Response Address

Figure 11 thru Figure 28 illustrate the aforementioned PMBus protocols. All transactions support PEC and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

Figure 11 is a key to the protocol diagrams in this section. PEC is optional.

A value shown below a field in the following figures is mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/Wbit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

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Refer to Figure 11 for a legend.

Handshaking features are included to ensure robust system communication. Please refer to the PMBus Communication and Command Processing subsection of the Dual 25A/30A PSM Applications Information section for further details.

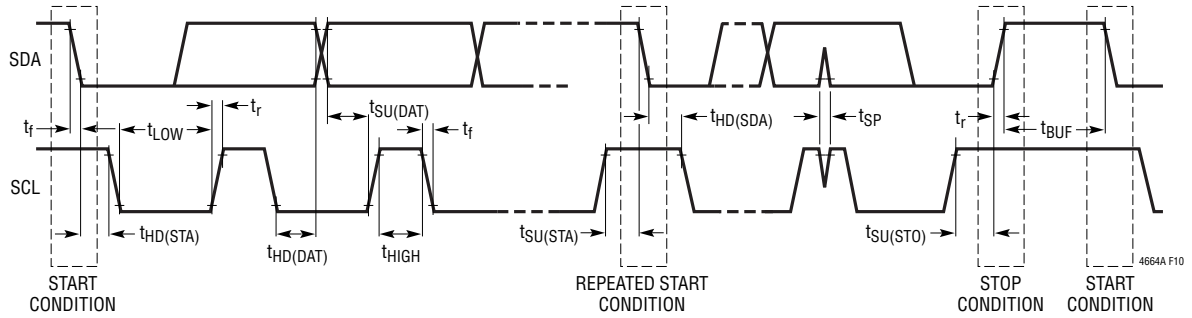

Figure 10. PMBus Timing Diagram

Table 6. Abbreviations of Supported Data Formats

	PMBus		LTC TERMINOLOGY	DEFINITION	EXAMPLE
	TERMINOLOGY	SPECIFICATION REFERENCE			
L11	Linear	Part II ¶7.1	Linear_5s_11s	Floating point 16-bit data: value = Y • 2^N, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers	b[15:0] = 0x9807 = 10011_000_0000_0111 value = 7 • 2^{-13} = 854E-6
L16	Linear VOUT_MODE	Part II ¶8.2	Linear_16u	Floating point 16-bit data: value = Y • 2^{-12}, where Y = b[15:0], an unsigned integer	b[15:0] = 0x4C00 = 0100_1100_0000_0000 value = 19456 • 2^{-12} = 4.75
CF	DIRECT	Part II ¶7.2	Varies	16-bit data with a custom format defined in the detailed PMBus command description	Often an unsigned or two's compliment integer
Reg	Register Bits	Part II ¶10.3	Reg	Per-bit meaning defined in detailed PMBus command description	PMBus STATUS_BYTE command
ASC	Text Characters	Part II ¶22.2.1	ASCII	ISO/IEC 8859-1 [A05]	LTC (0x4C5443)

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FIGURE 11 THRU FIGURE 28 PMBus PROTOCOLS

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P	STOP CONDITION
PEC	PACKET ERROR CODE
☐	MASTER TO SLAVE
▒	SLAVE TO MASTER
...	CONTINUATION OF PROTOCOL

4664A F11

Figure 11. PMBus Packet Protocol Diagram Element Key

Figure 12. Quick Command Protocol

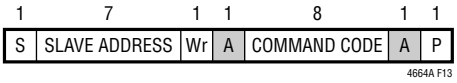

Figure 13. Send Byte Protocol

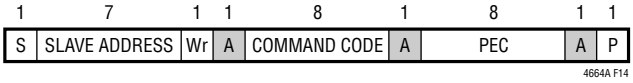

Figure 14. Send Byte Protocol with PEC

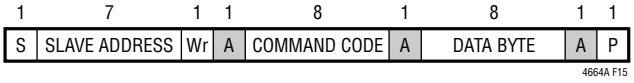

Figure 15. Write Byte Protocol

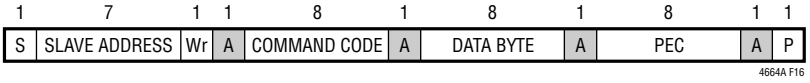

Figure 16. Write Byte Protocol with PEC

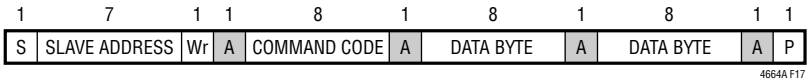

Figure 17. Write Word Protocol

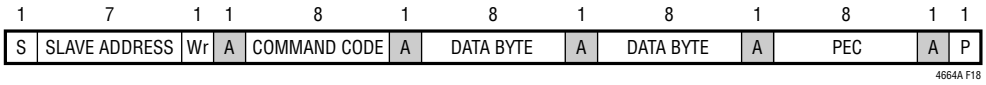

Figure 18. Write Word Protocol with PEC

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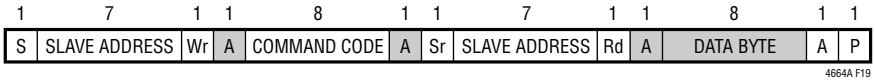

Figure 19. Read Byte Protocol

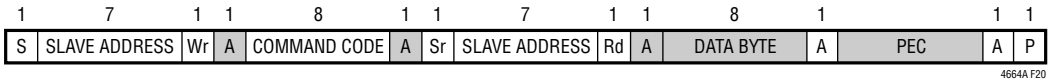

Figure 20. Read Byte Protocol with PEC

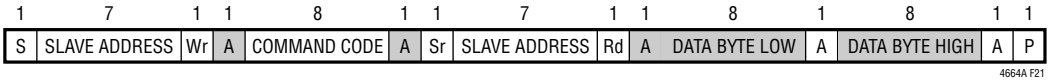

Figure 21. Read Word Protocol

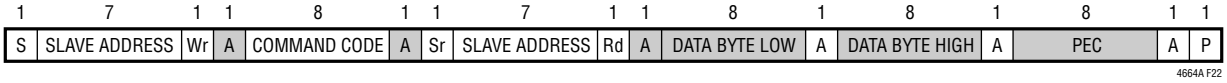

Figure 22. Read Word Protocol with PEC

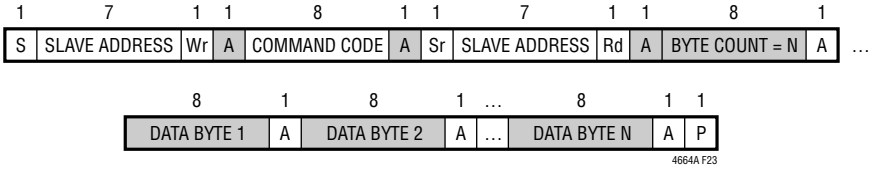

Figure 23. Block Read Protocol

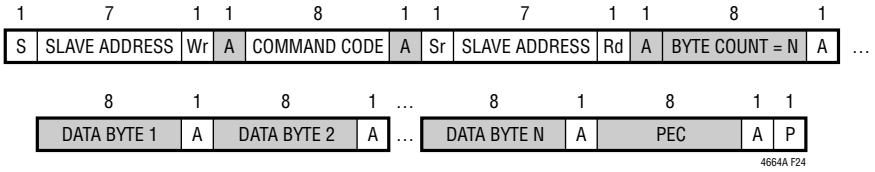

Figure 24. Block Read Protocol with PEC

DUAL 25A/30A PSM OPERATION

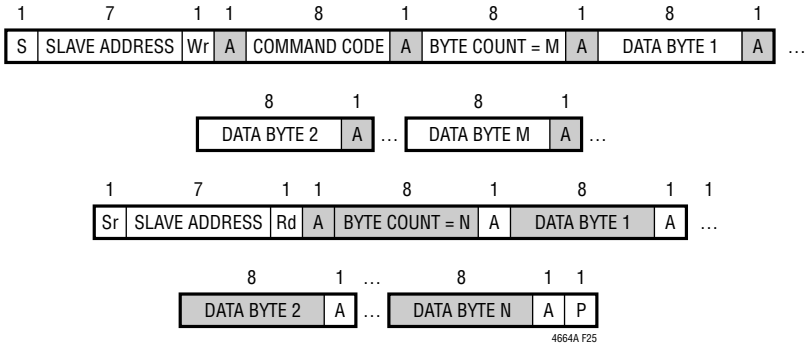

Figure 25. Block Write – Block Read Process Call

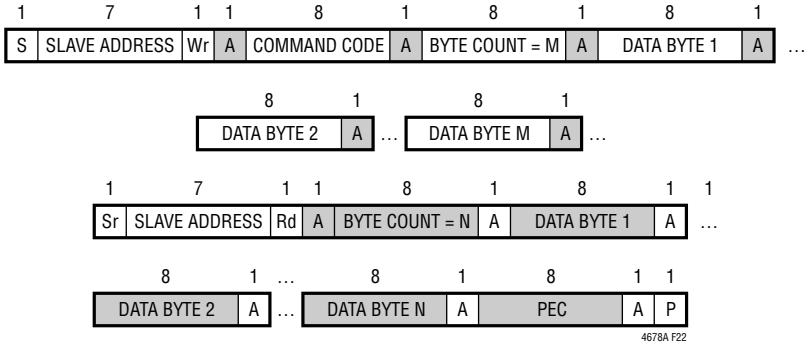

Figure 26. Block Write – Block Read Process Call with PEC

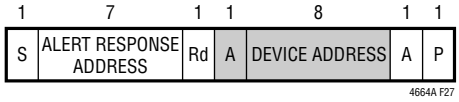

Figure 27. Alert Response Address Protocol

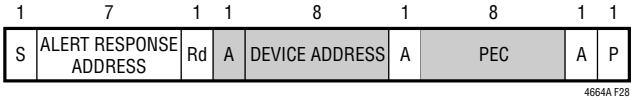

Figure 28. Alert Response Address Protocol with PEC

PMBus COMMAND SUMMARY

PMBus COMMANDS

Table 7 lists supported PMBus commands and manufacturer specific commands. A complete description of these commands can be found in the "PMBus Power System Mgt Protocol Specification – Part II – Revision 1.2". Users are encouraged to reference this specification. Exceptions or manufacturer specific implementations are listed in Table 7. Floating point values listed in the "DEFAULT VALUE" column are either Linear 16-bit Signed (PMBus Section 8.3.1) or Linear_5s_11s (PMBus Section 7.1) format, whichever is appropriate for the command. All commands from 0xD0 through 0xFF not listed in Table 7 are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid undesired operation of the part. All commands from 0x00 through 0xCF not listed in Table 7 are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of 2^{-12}.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances the part follows the protocols defined in the PMBus Specification v1.2, Part II, Section 10.8.7, to communicate that it is busy. The part includes handshaking features to eliminate busy errors and simplify error handling software while ensuring robust communication and system behavior. Please refer to the subsection titled PMBus Communication and Command Processing in the Dual 25A/30A PSM Applications Information section for further details.

Table 7. PMBus Commands Summary (Note: The Data Format Abbreviations are Detailed in Table 8)

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00	90
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80	94
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E	94
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA	119
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N					90
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N					90
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	91
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA	130
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA	130
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	118
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ activity	Block R/W	Y	Reg		Y	See CMD	119
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14	100
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000	101
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HI.	R/W Word	Y	L16	V	Y	1.8 0x1CCD	100

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD	101
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33	101
VOUT_TRANSITION_ RATE	0X27	Rate the output changes when V_{OUT} commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0x8042	107
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	350k 0xFABC	98
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	4.75 0xCA60	99
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	4.5 0xCA40	99
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A	100
VOUT_OV_FAULT_ RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	109
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133	100
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD	101
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66	101
VOUT_UV_FAULT_ RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	110
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	40 0xE280	103
IOUT_OC_FAULT_ RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	112
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	30.0 0xDBC0	104
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	128 0xF200	105
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8	114
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	125 0xEBE8	105
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–45 0xE530	106
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	114
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0	100
VIN_OV_FAULT_ RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	109
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	4.68 0xCA53	99
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280	104

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000	106
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the V_{OUT} commanded value.	R/W Word	Y	L11	ms	Y	3 0xC300	106
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VO_{UT} to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	5 0xCA80	107
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_ MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	112
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000	107
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	3 0xC300	107
TOFF_MAX_WARN_ LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	0 0x8000	108
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA	120
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA	121
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA	121
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA	122
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA	122
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA	123
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA	123
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA	124
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA	127
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA	127
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA	127
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA	127
READ_TEMPERATURE_1	0x8D	External temperature sensor temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA	127
READ_TEMPERATURE_2	0x8E	Internal die junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA	127
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA	127
READ_POUT	0x96	Measured output power	R Word	Y	L11	W		N/A	127
READ_PIN	0x97	Calculated input power	R Word	Y	L11	W		N/A	128
PMBus_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg			0x22	118
MFR_ID	0x99	The manufacturer ID of the LTM4664A in ASCII.	R String	N	ASC			LTC	118

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTM4664	118
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		1.8 0x1CCD	102
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command	R Byte	N	%			5.0%	128
USER_DATA_00	0xB0	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	118
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay®.	R/W Word	Y	Reg		Y	NA	118
USER_DATA_02	0xB2	OEM RESERVED. Typically used for part serialization	R/W Word	N	Reg		Y	NA	118
USER_DATA_03	0xB3	An NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000	118
USER_DATA_04	0xB4	An NVM word available for the user.	R/W Word	N	Reg		Y	0x0000	118
MFR_EE_UNLOCK	0xBD	Contact factory.							135
MFR_EE_ERASE	0xBE	Contact factory.							135
MFR_EE_DATA	0xBF	Contact factory.							135
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1D	92
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21	93
MFR_FAULT_ PROPAGATE	0xD2	Configuration that determines which faults are propagated to the $\overline{\text{FAULT}}$ pin.	R/W Word	Y	Reg		Y	0x6993	115
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0x28	96
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7	95
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the $\overline{\text{FAULT}}$ pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0	113
MFR_OT_FAULT_ RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0	113
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_ IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA	128
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back	R/W Byte	N	Reg			0x00	129
MFR_RETRY_DELAY	0xDB	Retry interval during $\overline{\text{FAULT}}$ retry mode.	R/W Word	Y	L11	ms	Y	250.0 0xF3E8	108
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LTM4664A.	R/W Word	Y	L11	ms	Y	150 0xF258	108
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA	128
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA	128
MFR_TEMPERATURE_1_ PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA	128
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS	R Word	N	L11	A		NA	128
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA	120
MFR_READ_ICHIP	0xE4	Measured supply current of the SV_{IN} pin	R Word	N	L11	A		NA	128

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_IOUT_CAL_GAIN	0xDA	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor. It is the resistance value in mohm. OxAA8B set at factory	R Word	Y	L11			0.350mΩ	102
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg		Y	NA	124
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F	92
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTM4664A and revision	R Word	N	Reg			0x4100	118
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	2.0 0xC200	104
MFR_FAULT_LOG_ STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	131
MFR_INFO	0xB6	Contact factory.							135
MFR_FAULT_LOG_ CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA	135
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	Reg		Y	NA	131
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC chips.	R Byte	N	Reg			NA	125
MFR_COMPARE_USER_ ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA	130
MFR_TEMPERATURE_2_ PEAK	0xF4	Peak internal die temperature since last MFR_ CLEAR_PEAKS.	R Word	N	L11	C		NA	129
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10	97
MFR_IOUT_CAL_GAIN_ TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF	ppm/°C	Y	3900 0x0F3C	102
MFR_RVIN	0xF7	The resistance value of the V_{IN} pin filter element in mΩ. Set at Factory	R Word	N	L11	mΩ	N	1000 0x03E8	99
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	0.9 0x3FAE	105
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to –273.1°C	R/W Word	Y	L11	C	Y	0.0 0x8000	105
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80	92
MFR_REAL_TIME	0xFB	48-bit share-clock counter value.	R Block	N	CF			NA	xx
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				NA	94

Note 1. Commands indicated with Y in the NVM column indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

Note 2. Commands with a default value of NA indicate “not applicable”. Commands with a default value of FS indicate “factory set on a per part basis”.

Note 3. The LTM4664A contains additional commands not listed in Table 7. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Note 4. Some of the unpublished commands are read-only and will generate a CML bit 6 fault if written.

Note 5. Writing to commands not published in Table 7 is not permitted.

Note 6. The user should not assume compatibility of commands between different parts based upon command names. Always refer to the manufacturer’s data sheet for each part for a complete definition of a command’s function. LTC strives to keep command functionality compatible between all LTC devices. Differences may occur to address specific product requirements.

PMBus COMMAND SUMMARY

Table 8. Data Format Abbreviations

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \bullet 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Example: For b[15:0] = 0x9807 = 'b10011_000_0000_0111 Value = $7 \bullet 2^{-13} = 854 \bullet 10^{-6}$ From "PMBus Spec Part II: Paragraph 7.1"
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \bullet 2^N$ where Y = b[15:0] is an unsigned integer and N = VOUT_MODE_PARAMETER is a 5-bit two's complement exponent that is hardwired to –12 decimal Example: For b[15:0] = 0x9800 = 'b1001_1000_0000_0000 Value = $19456 \bullet 2^{-12} = 4.75$ From "PMBus Spec Part II: Paragraph 8.2"
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Description.
L16	Integer Word	PMBus data field b[15:0] Value = Y where Y = b[15:0] is a 16-bit unsigned integer Example: For b[15:0] = 0x9807 = 'b1001_1000_0000_0111 Value = 38919 (decimal)
CF	Custom Format	Value is defined in detailed PMBus Command Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.
ASC	ASCII Format	A variable length string of text characters conforming to ISO/IEC 8859-1 standard.

DUAL 25A/30A PSM APPLICATIONS INFORMATION

V_{IN} TO V_{OUT} STEP-DOWN RATIOS

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4664A PSM is capable of 95% duty cycle at 500kHz, but the V_{IN} to V_{OUT} minimum dropout is still a function of its load current and will limit output current capability related to high duty cycle on the topside switch.

Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 60ns. See Note 6 in the Electrical Characteristics section for output current guideline. Since the LTM4664A front end 4:1 divider feeds the two 25A/30A PSM channels with a V_{OUT2} range of 7.5V to 14.5V, there should be no minimum on time issue.

INPUT CAPACITORS

The LTM4664A PSM channels should be connected to a low AC impedance DC source. For the regulator input, four 22µF input ceramic capacitors are used to handle the RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D_n = \frac{V_{OUTn}}{V_{INn}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CINn(RMS)} = \frac{I_{OUTn(MAX)}}{\eta\%} \bullet \sqrt{D_n \bullet (1-D_n)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, or a polymer capacitor.

OUTPUT CAPACITORS

The LTM4664A PSM channel outputs are designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 400µF to 1000µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 12 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 12.5A to 25A step, 12A/µs transient each channel. Table 12 optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 12 matrix, and the LTpowerCAD Design Tool will be provided for stability analysis. Multiphase operation reduces effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The LTpowerCAD Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω resistor can be placed in series from V_{OUTn} to the V_{OSNS0}^+ pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The LTM4664A PSM stability compensation can be adjusted using two external capacitors, and the MFR_PWM_COMP commands.

LIGHT LOAD CURRENT OPERATION

The LTM4664A PSM channels have two modes of operation including high efficiency, discontinuous conduction mode or forced continuous conduction mode. The mode of operation is configured by bit 0 of the MFR_PWM_MODE*n* command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

If a channel is enabled for discontinuous mode operation, the inductor current is not allowed to reverse. The reverse

DUAL 25A/30A PSM APPLICATIONS INFORMATION

current comparator, I_{REV}, turns off the bottom MOSFET (MB*n*) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous (pulse-skipping) operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the COMP_C*n*a pin. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this on V_{IN3} and turn off the offending channel. However, this fault is based on an ADC read and can nominally take up to 100ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction operation.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTM4664A's PSM channels is established by its analog phase-locked-loop (PLL) locking on to the clock present at the module's SYNC pin. The clock waveform on the SYNC pin can be generated by the LTM4664A's PSM internal circuitry when an external pull-up resistor to 3.3V (e.g., V_{DD33}) is provided, in combination with the LTM4664A PSM control IC's FREQUENCY_SWITCH command being set to one of the following supported values: 250kHz, 350kHz, 425kHz, 500kHz, 575kHz, 650kHz, 750kHz. In this configuration, the module is called a "sync master": (using the factory-default setting of MFR_CONFIG_ALL[4] = 0b), SYNC becomes a bidirectional open-drain pin, and the LTM4664A PSM pulls SYNC logic low for nominally 500ns at a time, at the prescribed clock rate. The SYNC signal can be bused to other LTM4664A PSM device modules (configured as "sync slaves"), for purposes of synchronizing switching frequencies of multiple modules within a system—but only one LTM4664A PSM devices should be configured as a "sync master"; the other LTM4664A(s) should be configured as "sync slaves".

The most straightforward way is to set its FREQUENCY_ SWITCH command to 0x0000 and MFR_CONFIG_ALL[4] = 1b. This can be easily implemented with resistor pin-strap settings on the FSWPH_CFG pin (see Table 3). Using MFR_CONFIG_ALL[4] = 1b, the LTM4664As SYNC pin becomes a high impedance input, only—i.e., it does not drive SYNC low. The module synchronizes its frequency to that of the clock applied to its SYNC pin. The only shortcoming of this approach is: in the absence of an externally applied clock, the switching frequency of the module will default to the low end of its frequency-synchronization capture range (~225kHz).

If fault-tolerance to the loss of an externally applied SYNC clock is desired, the FREQUENCY_SWITCH command of a "sync slave" can be left at the nominal target switching frequency of the application, and not 0x0000 However, it is then still necessary to configure MFR_CONFIG_ALL[4] = 1b. With this combination of configurations, the LTM4664A's SYNC pin becomes a high impedance input and the module synchronizes its frequency to that of the externally applied clock, provided that the frequency of the externally applied clock exceeds ~½. of the target frequency (FREQUENCY_SWITCH). If the SYNC clock is absent, the module responds by operating at its target frequency, indefinitely. If and when the SYNC clock is restored, the module automatically phase-locks to the SYNC clock as normal. The only shortcoming of this approach is: the EEPROM must be configured per above guidance; resistor pin-strapping options on the FSWPH_CFG pin alone cannot provide fault-tolerance to the absence of the SYNC clock.

The FREQUENCY_SWITCH register can be altered via I^2C commands, but only when switching action is disengaged, i.e., the module's outputs are turned off. The FREQUENCY_SWITCH command takes on the value stored in NVM at V_{INS3} power-up, but is overridden according to a resistor pin-strap applied between the FSWPH_CFG pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0b). Table 3 highlights available resistor pin-strap and corresponding FREQUENCY_SWITCH settings.

The relative phasing of all active channels in a PolyPhase rail should be optimally phased. The relative phasing of each rail is 360°/*n*, where *n* is the number of phases in the rail. MFR_PWM_CONFIG[2:0] configures channel relative

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phasing with respect to the SYNC pin. Phase relationship values are indicated with 0° corresponding to the falling edge of SYNC being coincident with the turn-on of the top MOSFETs, MT*n*.

The MFR_PWM_CONFIG command can be altered via I^2C commands, but only when switching action is disengaged, i.e., the module's outputs are turned off. The MFR_PWM_CONFIG command takes on the value stored in NVM at SV_{IN} power-up, but is overridden according to a resistor pin-strap applied between the FSWPH_CFG pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0b). Table 3 highlights available resistor pin-strap and corresponding MFR_PWM_CONFIG[2:0] settings.

Some combinations of FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] are not available by resistor pin-strapping the FSWPH_CFG pin. All combinations of supported values for FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] can be configured by NVM programming—or, I^2C transactions, provided switching action is disengaged, i.e., the module's outputs are turned off.

Care must be taken to minimize capacitance on SYNC to assure that the pull-up resistor versus the capacitor load has a low enough time constant for the application to form a "clean" clock. (See "Open-Drain Pins", later in this section.)

When an LTM4664A PSM is configured as a sync slave, it is permissible for external circuitry to drive the SYNC pin from a current-limited source (less than 10mA), rather than using a pull-up resistor. Any external circuitry must not drive high with arbitrarily low impedance at SV_{IN} power-up, because the SYNC output can be low impedance until NVM contents have been downloaded to RAM.

Recommended LTM4664A PSM switching frequencies of operation for many common V_{IN}-to-V_{OUT} applications are indicated below. When the two channels of an LTM4664A PSM are stepping input voltage(s) down to output voltages whose recommended switching frequencies below are significantly different, operation at the higher of the two recommended switching frequencies is preferable, but minimum on-time must be considered. (See Minimum On-Time Considerations section.)

Table 9. Recommended PSM Switching Frequency for Various V_{IN}-to-V_{OUT} Step-Down Scenarios

V	$7.5V_{IN}$	$10V_{IN}$	$12V_{IN}$	$14.5V_{IN}$
0.5	250kHz	250kHz	250kHz	250kHz
0.7				
0.8				
0.9				
1.0				
1.2	350kHz	350kHz	350kHz	350kHz
1.5				

OUTPUT CURRENT LIMIT PROGRAMMING

The cycle-by-cycle current limit (= V_{ISENSE}/DCR) is proportional to COMP_C*n*, which can be programmed from 1.45V to 2.2V using the PMBus command IOUT_OC_FAULT_LIMIT. The LTM4664A PSM uses only the sub-milliohm sensing to detect current levels. See page103. The LTM4664A PSM has two ranges of current limit programming. The value of MFR_PWM_MODE[2] is reserved and the MFR_PWM_MODE[7], and IOUT_OC_FAULT_LIMIT are used to set the current limit level, see the section of the PMBus commands, the device can regulate output voltage with the peak current under the value of IOUT_OC_FAULT_LIMIT in normal operation. In case of output current exceeding that current limit, a OC fault will be issued. Each of the IOUT_OC_FAULT_LIMIT ranges will effects the loop gain, and subsequently effects the loop stability, so setting the range of current limiting is a part of loop design.

The LTpowerCAD Design Tool can be used to look at the loop stability changes if current limit is adjusted. The LTM4664A PSM will automatically update the current limit as the inductor temperature changes. Keep in mind this operation is on a cycle-by-cycle basis and is only a function of the peak inductor current. The average inductor current is monitored by the ADC converter and can provide a warning if too much average output current is detected. The overcurrent fault is detected when the COMP_C*n* voltage hits the maximum value. The digital processor within the LTM4664A PSM provides the ability to either ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). Refer to the overcurrent portion of the Dual 25A/30A PSM Operation section for more detail. The READ_POUT can be used to readback calculated output power.

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MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTM4664A PSM is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUTn}}{V_{INn} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTM4664A is 60ns.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTM4664A PSM must enter its run state prior to soft-start. The RUN_C*n* pins are released after the part initializes, and V_{INS3} is greater than the VIN_ON threshold and Stage 2 PGood pin releases the RUN_C*n* pins. If multiple LTM4664As are used in an application, they should be configured to share the same RUN_C*n* pins. They all hold their respective RUN_C*n* pins low until all devices initialize and V_{INS3} exceeds the VIN_ON threshold for all devices. The SHARE_CLK pin assures all the devices connected to the signal use the same time base.

After the RUN_C*n* pin releases, the controller waits for the user-specified turn-on delay (TON_DELAY*n*) prior to initiating an output voltage ramp. Multiple LTM4664As and other LTC parts can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK) and all devices must share the RUN_C*n* pin.

This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Analog Devices ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±10% in frequency, thus the actual time delays will have some variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE*n* command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE*n* to any value less than 0.250ms. The LTM4664A PSM performs the necessary math internally to assure the voltage ramp is controlled to the desired slope. However, the voltage slope can not be any faster than the V_{OUTn} fundamental limits of the power stage. The number of $t_{ON(MIN)}$ < steps in the ramp is equal to TON_RISE/0.1ms. Therefore, the shorter the TON_RISE*n* time setting, the more discrete steps in the soft-start ramp appear.

The LTM4664A PSM PWM always operates in discontinuous mode during the TON_RISE*n* operation. In discontinuous mode, the bottom MOSFET (MB*n*) is turned off as soon as reverse current is detected in the inductor. This allows the regulator to start up into a prebiased load.

There is no analog tracking feature in the LTM4664A PSM; however, two outputs can be given the same TON_RISE*n* and TON_DELAY*n* times to achieve ratiometric rail tracking. Because the RUN*n* pins are released at the same time and both units use the same time base (SHARE_CLK), the outputs track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE command. In digital servo mode, the LTM4664A PSM will adjust the regulated output voltage based on the ADC voltage reading. Every 90ms the digital servo loop will step the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit) until the output is at the correct ADC reading. At power-up this mode engages after TON_MAX_FAULT_LIMIT unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT is set to 0 (infinite), the servo begins after TON_RISE is complete and V_{OUT} has exceeded the

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VOUT_UV_FAULT_LIMIT. This same point in time is when the output changes from discontinuous to the programmed mode as indicated in MFR_PWM_MODE bit 0. Refer to Figure 29 for details on the V_{OUT} waveform under time-based sequencing. If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time is reached; and
3. After the VOUT_UV_FAULT_LIMIT has been exceeded or the IOUT_OC_FAULT_LIMIT is no longer active.

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is not set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time has expired and both VOUT_UV_FAULT and IOUT_OC_FAULT are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration it is recommended only one of the control loops have the digital servo mode enabled. This will assure the various loops do not work against each other due to slight differences in the reference circuits.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTM4664A PSM also supports controlled turn-off. The TOFF_DELAY and TOFF_FALL functions are shown in Figure 30. TOFF_FALL is processed when the RUN pin goes low or if the part is commanded off. If the part faults off or $\overline{\text{FAULT}}$_C*n* is pulled low externally and the part is programmed to respond to this, the output will three-state rather than exhibiting a controlled ramp. The output will decay as a function of the load. The output voltage will operate as shown in Figure 30 as long as the part is in forced continuous mode and the TOFF_FALL time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage and controller can sink sufficient current to assure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero volt state. At the end of TOFF_FALL, the controller will cease to sink current and V_{OUT} will decay at the natural rate determined by the load impedance. If the controller is in discontinuous mode, the controller will not pull negative current and the output will be pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The shorter TOFF_FALL time is set, the larger the discrete steps in the TOFF_FALL ramp will appear. The number of steps in the ramp is equal to TOFF_FALL/0.1ms.

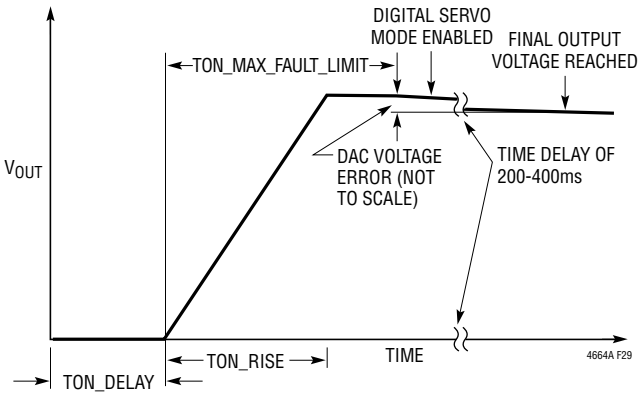

Figure 29. Timing Controlled V_{OUT} Rise

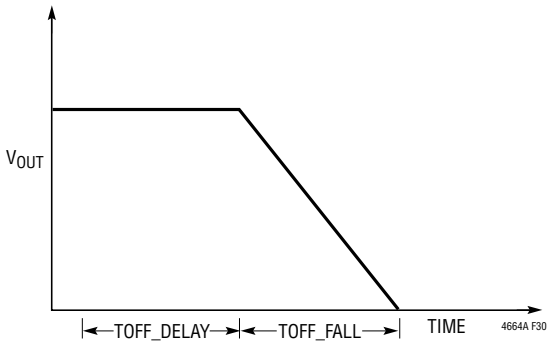

Figure 30. TOFF_DELAY and TOFF_FALL

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UNDERVOLTAGE LOCKOUT

The LTM4664A PSM is initialized by an internal threshold-based UVLO where V_{INS3} must be approximately 4V and $INTV_{CC}$, V_{DD33}, and V_{DD25} must be within approximately 20% of their regulated values. In addition, V_{DD33} must be within approximately 7% of the targeted value before the RUN_C*n* pin is released. After the part has initialized, an additional comparator monitors V_{INS3}. The VIN_ON threshold must be exceeded before the power sequencing can begin. When V_{INS3} drops below the VIN_OFF threshold, the SHARE_CLK pin will be pulled low and V_{INS3} must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed. If FAULTB is held low when V_{INS3} is applied, ALERT will be asserted low even if the part is programmed to not assert ALERT when FAULTB is held low. If I^2C communication occurs before the LTM4664A is out of reset and only a portion of the command is seen by the part, this can be interpreted as a CML fault. If a CML fault is detected, ALERT is asserted low.

It is possible to program the contents of the NVM in the application if the V_{DD33} supply is externally driven directly to V_{DD33} or through $EXTV_{CC}$. This will activate the digital portion of the LTM4664A PSM without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If V_{INS3} has not been applied to the LTM4664A PSM, bit 3 (NVM Not Initialized) in MFR_COMMON will be asserted low. If this condition is detected, the part will only respond to addresses 5A and 5B. To initialize the part issue the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired then issue a STORE_USER_ALL. When V_{IN} is applied a MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

FAULT DETECTION AND HANDLING

The LTM4664A $\overline{FAULT}$_C*n* pins are configurable to indicate a variety of faults including OV, UV, OC, OT, timing faults, and peak over current faults. In addition, the $\overline{FAULT}$_C*n* pins can be pulled low by external sources indicating a fault in some other portion of the system. The fault response is configurable and allows the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Refer to the PMBus section of the data sheet and the PMBus specification for more details.

The OV response is automatic. If an OV condition is detected, TG*n* goes low and BG*n* is asserted.

Fault logging is available on the LTM4664A PSM. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTM4664A PSM internal temperature is in excess of 85°C, writes into the NVM (other than fault logging) are not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C all NVM communication is disabled until the die temperature drops below 120°C.

OPEN-DRAIN PINS

The LTM4664A PSM has the following open-drain pins:

3.3V Pins

1. $\overline{FAULT}$_C*n*
2. SYNC
3. SHARE_CLK
4. PGOOD_C*n*

5V Pins (5V pins operate correctly when pulled to 3.3V.)

1. RUN_C*n*
2. $\overline{ALERT}$
3. SCL
4. SDA

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All the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low threshold on the pins is 0.8V; thus, there is plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high speed signals such as the SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time is:

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

The closest 1% resistor value is 1k. Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is a one time constant. The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz and the load is 100pF and a 3x time constant is required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k$$

The closest 1% resistor is 4.99k.

If timing errors are occurring or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. If not, reduce the pull-up resistor sufficiently to assure proper timing. The SHARE_CLK pull-up resistor has a similar equation with a period of 10µs and a pull-down time of 1µs. The RC time constant should be approximately 3µs or faster.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTM4664A PSM has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC pin. The phase relationship between the PWM controller and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_ CONFIG command. For PolyPhase applications, it is recommended that all the phases be spaced evenly. Thus for a 2-phase system the signals should be 180° out of phase and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 200kHz and 1MHz. Nominal parts will have a range beyond this; however, operation to a wider frequency range is not guaranteed.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the $\overline{\text{ALERT}}$ pin assert if a PLL_FAULT occurs, the SMBALERT_MASK command can be used to prevent the alert.

If the SYNC signal is not clocking in the application, the nominal programmed frequency will control the PWM circuitry. However, if multiple parts share the SYNC pins and the signal is not clocking, the parts will not be synchronized and excess voltage ripple on the output may be present. Bit 10 of MFR_PADS will be asserted low if this condition exists.

If the PWM signal appears to be running at too high a frequency, monitor the SYNC pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise versus the intended signal. Review routing of digital control signals and minimize crosstalk to the SYNC signal

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to avoid this problem. Multiple LTM4664As PSM sections are required to share one SYNC pin in PolyPhase configurations. For other configurations, connecting the SYNC pins to form a single SYNC signal is optional. If the SYNC pin is shared between LTM4664As PSM sections, only one LTM4664A section can be programmed with a frequency output. All the other LTM4664As sections should be programmed to disable the SYNC output. However their frequency should be programmed to the nominal desired value. See application schematic in Figure 51.

INPUT CURRENT SENSE AMPLIFIER

The LTM4664A input current sense amplifier can sense the supply current into the V_{INS3_Cn} power stages pins using an external sense resistor as shown in the Figure 2 Block Diagram. The R_{SENSE} value can be programmed using the MFR_IIN_CAL_GAIN command. Kelvin sensing is recommended across the R_{SENSE} resistor to eliminate errors. The MFR_PWM_CONFIG [6:5] sets the input current sense amplifier gain. See the MFR_PWM_CONFIG section. The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, that causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded. The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor.

There is an IR voltage drop from the supply to the V_{INS3} controller pin due to the current flowing into the V_{INS3} controller pin. To compensate for this voltage drop, the MFR_RVIN will be automatically set to the 1Ω internal sense resistor in the Figure 2 Block Diagram. The LTM4664A PSM will multiply the MFR_READ_ICHIP measurement value by this 1Ω resistor and add this voltage to the measured voltage at the V_{INS3} controller pin. Therefore, READ_VIN = VIN_CNTLPIN + (MFR_READ_ICHIP • 1Ω) The MFR_READ_ICHIP command is used to measure the internal controller current. Using the READ_PIN command allows for reading calculated input power.

PROGRAMMABLE LOOP COMPENSATION

The LTM4664A offers programmable loop compensation to optimize the transient response without any hardware change. The error amplifier gain g_m varies from 1.0m℧ to 5.73m℧, and the compensation resistor R_{COMP} varies from 0kΩ to 62kΩ inside the controller. Two compensation capacitors, COMP_*n*a and COMP_*n*b, are required in the design and the typical ratio between COMP_*n*a and COMP_*n*b is 10. Also see Figure 2 Block Diagram, and Figure 31.

By adjusting the g_m and R_{COMP} only, the LTM4664A PSM can provide a flexible Type II compensation network to optimize the loop over a wide range of output capacitors. Adjusting the g_m will change the gain of the compensation over the whole frequency range without moving the pole and zero location, as shown in Figure 32.

Adjusting the R_{COMP} will change the pole and zero location, as shown in Figure 33. It is recommended that the user determines the appropriate value for the g_m and R_{COMP} using the LTpowerCAD tool.

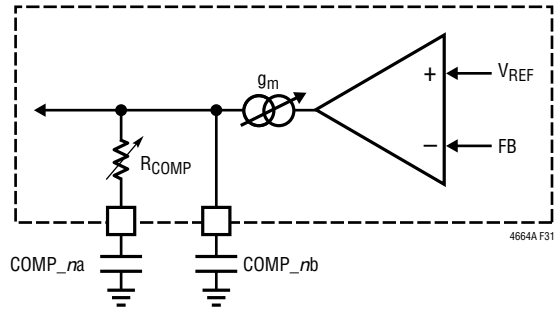

Figure 31. Programmable Loop Compensation

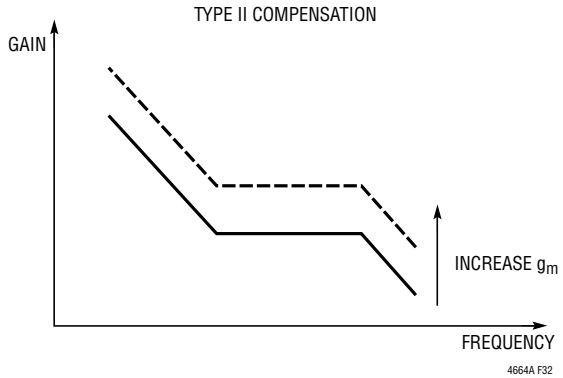

Figure 32. Error Amp g_m Adjust

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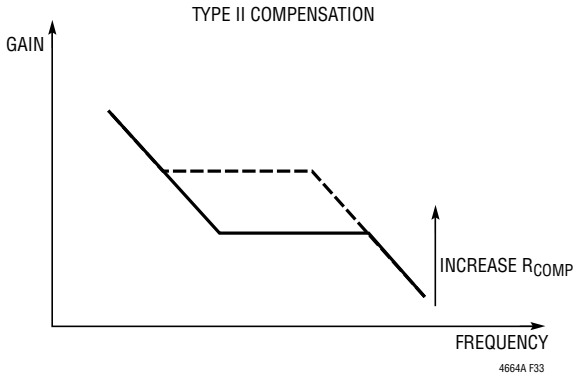

Figure 33. R_{COMP} Adjust

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the COMP pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The COMP_C*n*a external capacitor shown in the Typical Application circuit will provide an adequate starting point for most applications. The programmable parameters that affect loop gain are the voltage range, bit[1] of the MFR_PWM_CONFIG command, the current range bit[7] of the MFR_PWM_MODE command, the g_m of the PWM channel amplifier bits [7:5] of MFR_PWM_COMP, and the internal R_{COMP} compensation resistor, bits[4:0] of MFR_PWM_COMP. Be sure to establish these settings prior to compensation calculation.

The COMP_C*n*a series internal R_{COMP} and external C_{COMP_Cna} filter sets the dominant pole-zero loop compensation. The internal R_{COMP} value can be modified (from 0Ω to 62kΩ) using bits[4:0] of the MFR_PWM_ COMP command. Adjust the value of R_{COMP} to optimize transient response once the final PCB layout is done and the particular C_{COMP_bn} filter capacitor and output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and COMP pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET with a resistor to ground directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce to a load step. The MOSFET + R_{SERIES} will produce output currents approximately equal to V_{OUT}/R_{SERIES}. R_{SERIES} values from 0.1Ω to 2Ω are valid depending on the current limit settings and the programmed output voltage. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the COMP pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_{COMP} and the bandwidth of the loop will be increased by decreasing C_{COMP_Cna}. If R_{COMP} is increased by the same factor that C_{COMP} is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The gain of the loop will be proportional to the transconductance of the error amplifier which is set using bits[7:5] of the MFR_PWM_COMP command. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and

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it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PolyPhase® Configuration

When configuring a PolyPhase rail with multiple LTM4664As, the user must share the SYNC, COMP_*n*a, COMP_*n*b SHARE_CLK, $\overline{\text{FAULT}}$_C*n*, and $\overline{\text{ALERT}}$ pins of these parts. Be sure to use pull-up resistors on $\overline{\text{FAULT}}$_C*n*, SHARE_CLK and $\overline{\text{ALERT}}$. One of the part's SYNC pins must be set to the desired switching frequency, and all other FREQUENCY_SWITCH commands must be set to External Clock. If an external oscillator is provided, set the FREQUENCY_SWITCH command to External Clock for all parts. The relative phasing of all the channels should be spaced equally. The MFR_RAIL_ ADDRESS of all the devices should be set to the same value.

Multiple channels need to tie all the V_{OSNS}^+ pins together, and all the V_{OSNS}^- pins together COMP_*n*a and COMP_*n*b pins together as well. Do not assert bit[4] of MFR_CONFIG_ALL except in a PolyPhase application. See application example Figure 50.

CONNECTING THE USB TO I²C/SMBUS/PMBUS CONTROLLER TO THE LTM4664A IN-SYSTEM

The LTC USB-to-I²C/SMBus/PMBus adapter (DC1613A or equivalent) can be interfaced to the LTM4664A PSM on the user's board for programming, telemetry and system debug. The adapter, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status commands and the fault log. The final configuration can be quickly developed and stored to the LTM4664A PSM EEPROM. Figure 34 illustrates the application schematic for powering, programming and communication with one or more LTM4664As PSM via the LTC I²C/SMBus/PMBus adapter regardless of whether or not system power is present. If system power is not present, the dongle will power the LTM4664A PSM through the V_{DD33} supply pin. To initialize the part when V_{IN} is not applied and the V_{DD33} pin is powered, use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4.The LTM4664A PSM can now communicate with, and the project file Figure 34. Controller Connection can be updated. To write the updated project file to the NVM issue a STORE_USER _ALL command. When V_{IN} is applied, a MFR_RESET must be issued to allow the PWM POWER to be enabled and valid ADCs to be read.

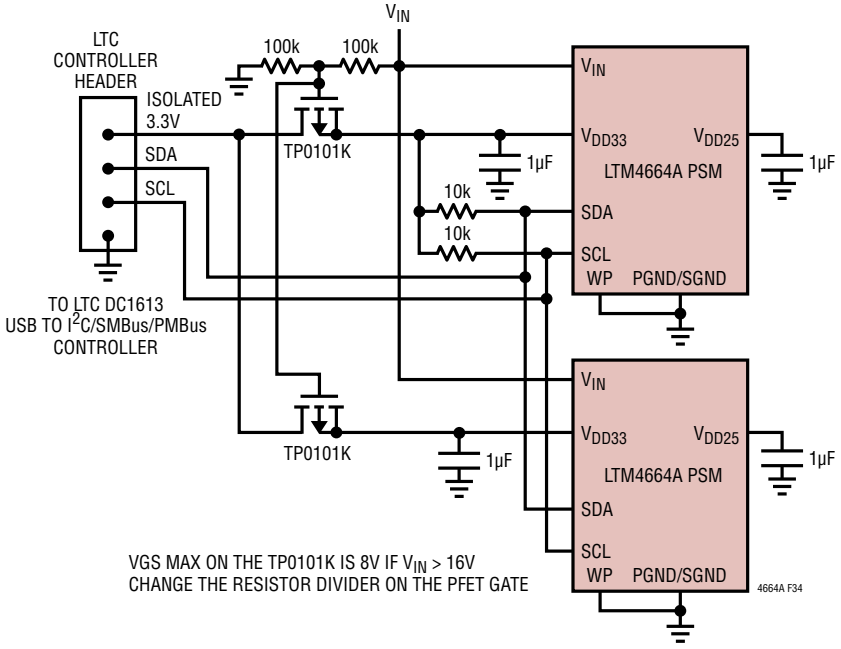

Figure 34. Controller Connection

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Because of the adapter's limited current sourcing capability, only the LTM4664As, PSM their associated pull-up resistors and the I^2C pull-up resistors should be powered from the ORed 3.3V supply. In addition any device sharing the I^2C bus connections with the LTM4664A PSM should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power. If V_{INS3} is applied, the DC1613A will not supply the power to the LTM4664As PSM on the board. It is recommended the RUN_C*n* pins be held low or no voltage configuration resistors inserted to avoid providing power to the load until the part is fully configured.

The LTM4664A PSM is fully isolated from the host PC's ground by the DC1613A.The 3.3V from the adapter and the LTM4664A V_{DD33} pin must be driven to each LTM4664A with a separate PFET. If both V_{INS3} and $EXTV_{CC}$ are not applied, the V_{DD33} pins can be in parallel because the on-chip LDO is off. The controller 3.3V current limit is 100mA but typical V_{DD33} currents are under 15mA. The V_{DD33} does back drive the $INTV_{CC}/EXTV_{CC}$ pin. Normally this is not an issue if V_{IN} is open.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

LTpowerPlay (Figure 35) is a powerful Windows-based development environment that supports Analog Devices digital power system management ICs including the LTM4664A PSM section. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Analog Devices ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an off-line mode (with no hardware present) in order to build multiple IC configuration files that can be saved and reloaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bring up rails. LTpowerPlay utilizes Analog Devices' USB-to-I^2C/SMBus/PMBus adapter to communication with one of the many potential targets including the DC2165A demo board, the DC2298A socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation.

A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos. Complete information is available at:

LTpowerPlay

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTM4664A PSM has a one deep buffer to hold the last data written for each supported command prior to processing as shown in Figure 36, Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed. Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing. Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process via bit 5 of MFR_COMMON ("calculations not pending"). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 37 which ensures that commands are processed in order while simplifying error handling routines.

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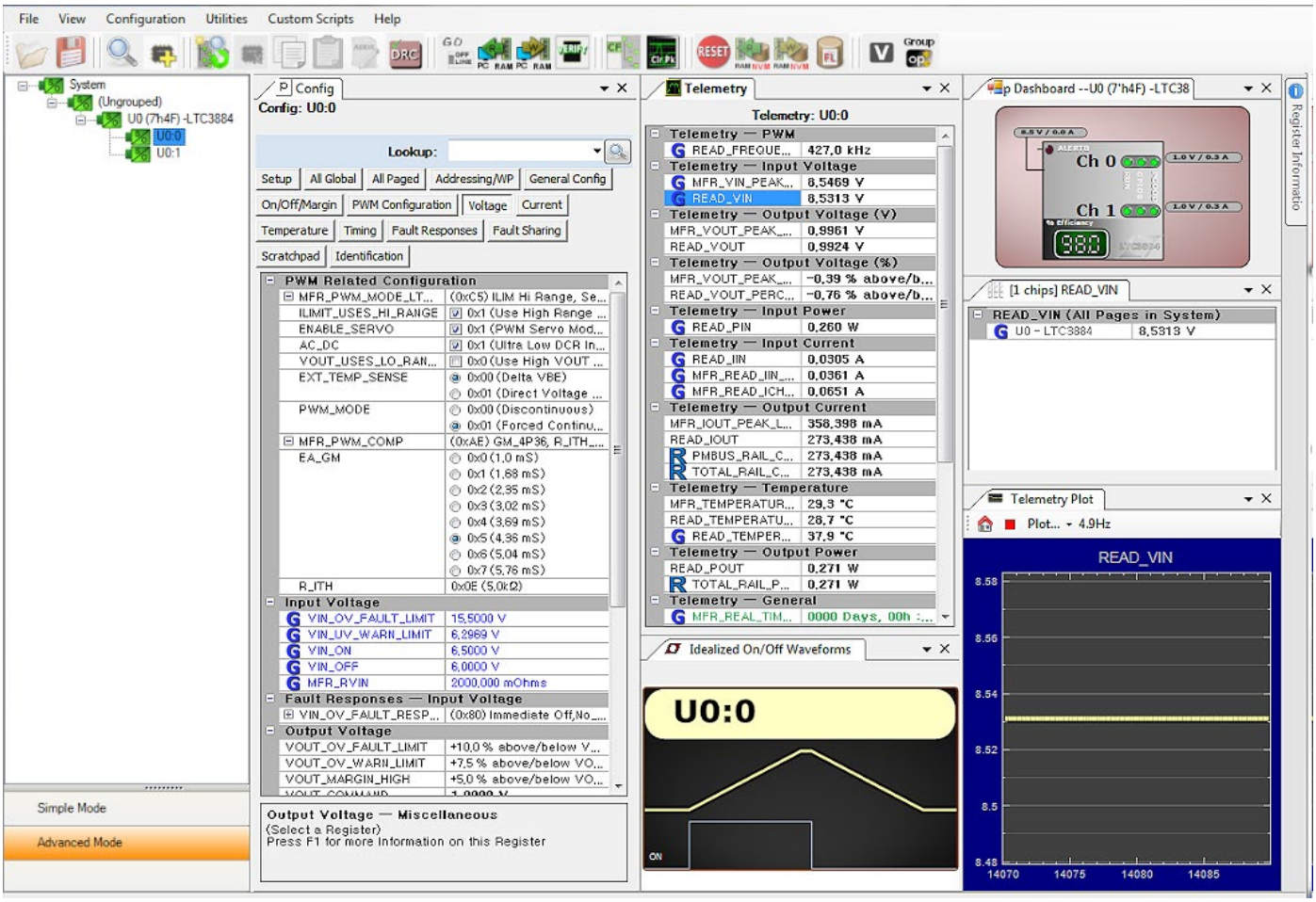

Figure 35. LTpowerPlay Screen Shot

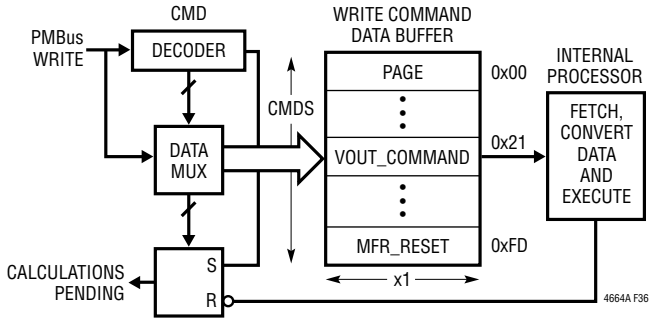

Figure 36. Write Command Data Processing

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When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information refer to PMBus Specification v1.1, Part II, Section 10.8.7 and SMBus v2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ ALL. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

```
// wait until chip is not busy
do
{
mfrCommonValue = PMBUS_READ_BYTE(0xEF);
partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)

// now the part is ready to receive the next
command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_
COMMAND to 2V
```

Figure 37. Example of a Command Write of VOUT_COMMAND

PMBus busy protocols are well accepted standards, but can make writing system level software somewhat complex. The part provides three 'hand shaking' status bits which reduce complexity while enabling robust system level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON ('chip not busy'). When the part is busy specifically because it is in a transitional V_{OUT} state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.) it will clear bit 4 of MFR_COMMON ('output not in transition'). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON ('calculations not pending'). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/ALERT notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 33.

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted $\overline{\text{ALERT}}$ notification. A simple way to achieve this is to create a SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutine. The above polling mechanism allows your software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the Analog Devices Application Notes.

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus master that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.1, Par II, Section 10.8.7 is required to communicate The LTM4664A PSM is not recommended in applications with bus speeds in excess of 400kHz.

THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the

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Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided later in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 38; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin

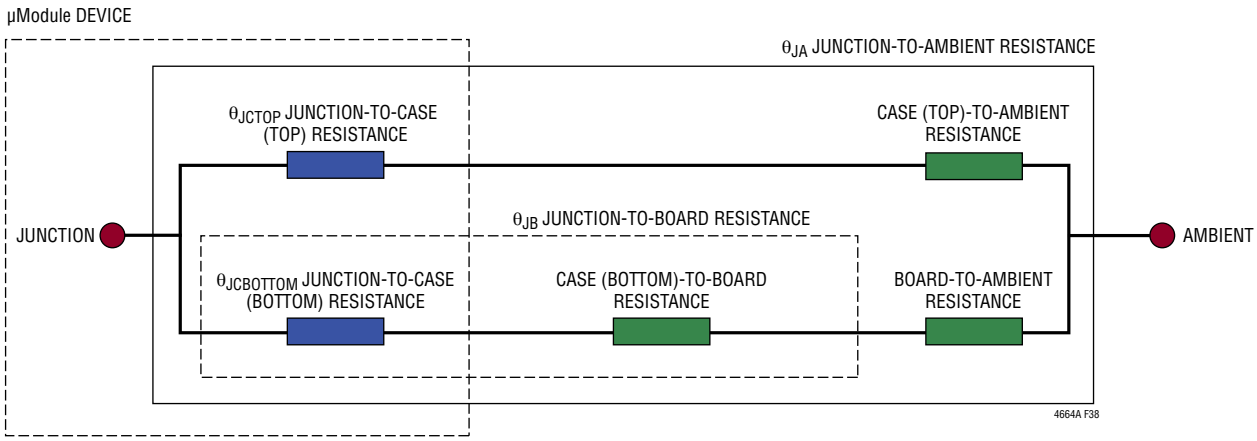

Figure 38. Graphical Representation of JESD51-12 Thermal Coefficients

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Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through the bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4664A, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4664A and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4664A with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet.

The 1.0V and 1.5V power loss curves in Figure 39 and 40 respectively can be used in coordination with the load current derating curves in Figure 41 to 44 for calculating an approximate θ_{JA} thermal resistance for the LTM4664A with various heat sinking and airflow conditions. These thermal resistances represent demonstrated performance of the LTM4664A on hardware; a 8-layer FR4 PCB measuring 99mm × 145mm × 1.6mm using 2oz copper on all layers. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.35 when the junction temperature reaches 125°C. The derating curves are plotted with the LTM4664A's paralleled outputs initially sourcing up to 50A and the ambient temperature at 50°C. The output voltages are 1.0V and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow.

The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 125°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 41, the load current is derated to ~30A at ~97°C ambient with no air or heat sink and the room temperature (25°C) power loss for this $48V_{IN}$ to $1.0V_{OUT}$ at $30A_{OUT}$ condition is ~3.2W. A 4.32W loss is calculated by multiplying the ~3.2W room temperature loss from the $48V_{IN}$ to $1.0V_{OUT}$ power loss curve at 30A (Figure 41), with the 1.35 multiplying factor. If the 97°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 23°C divided by 4.32W yields a thermal resistance, θ_{JA}, of 5.3°C/W—in good agreement with Table 11. Table 10 and 11 provide equivalent thermal resistances for 1.0V and 1.5V outputs with and without airflow. The derived

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thermal resistances in Table 10 and Table 11 are for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors.

Thermal performance expectations at up to 60A output (at up to $1.2V_{OUT}$) can be suitably approximated by studying this section's figures at analogous nearby output power conditions. For example: $1.2V_{OUT}$ at 60A is 72W output. For thermal purposes, this operating point can be approximated by $1.5V_{OUT}$ at 48A output (observe: also 72W output). The $1.5V_{OUT}$ curves shown in this section can thus be utilized to infer thermal performance at currents higher than 25A, per channel (for output voltages up to $1.2V_{OUT}$).

TABLE 10 AND TABLE 11: OUTPUT CURRENT DERATING (BASED ON DEMO BOARD)

Table 10. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 41, 42	48, 54	Figure 39, 40	0	None	5.3
Figure 41, 42	48, 54	Figure 39, 40	200	None	4.5
Figure 41, 42	48, 54	Figure 39, 40	400	None	4.0

Table 11. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 43, 44	48, 54	Figure 39, 40	0	None	5.3
Figure 43, 44	48, 54	Figure 39, 40	200	None	4.5
Figure 43, 44	48, 54	Figure 39, 40	400	None	4.0

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Table 12. LTM4664A Dual 25A/30A PSM Output Capacitor Matrix
All Below Parameters are Typical and Are Dependent on Board Layout

Murata	220µF 6.3V	GRM32ER60J227ME05	PANASONIC SP-CAP	470µF 2.5V	EEFSX0E471E4
Taiyo Yuden	220µf 4V	AMK325ABJ227MMHT	PANASONIC POSCAP	470µF 2.5V	ETPF470M5H
Murata	100µF 6.3V	GRM32ER60J107M	PANASONIC POSCAP	1000µF 2.5V	
Murata	100µF 4V	GRM21BR60G107ME15	PANASONIC POSCAP	1000µF 2.5V	ETCF1000M5H
Taiyo Yuden	100µF 4V	AMK325AD7MMHP			

Single 25A/30A Output						**Programmed Values**									
V_{OUT} (V)	**C_{OUT1} (CERAMIC) (µF)**	**C_{OUT2} (BULK) (µF)**	**COMP*n*a (pF)**	**COMP*n*b (pF)**	**EA-GM (ms)**	**R_{COMP} (kΩ)**	**I_{LIM} HI-RANGE**	**V_{OUT} LOW-RANGE**	**V_{INS1} (V)**	**V_{INS3} C1, C2**	**DROOP (mV)**	**PEAK-TO-PEAK DEVIATION (mV)**	**RECOVERY TIME(µs) LTpowerCAD/ MEASURE**	**LOAD STEP (A/µs)**	**FREQ. (kHz)**
0.9	5 × 100	2 × 470	2200	100	3.69	5	Yes	Yes	48	($V_{INS1/4}$) or 12V	42.5	85	36	12.5	250
0.9	5 × 100	1 × 1000	3300	220	3.02	5	Yes	Yes	48	($V_{INS1/4}$) or 12V	55.5	111	40	12.5	250
0.9	6 × 220	None	4700	100	3.69	4	Yes	Yes	48	($V_{INS1/4}$) or 12V	75	150	50	12.5	250
1	5 × 100	2 × 470	2200	100	3.69	5	Yes	Yes	48	($V_{INS1/4}$) or 12V	42.5	85	36	12.5	250
1	5 × 100	1 × 1000	3300	220	3.02	5	Yes	Yes	48	($V_{INS1/4}$) or 12V	56	112	40	12.5	250
1	6 × 220	None	4700	100	3.69	4	Yes	Yes	48	($V_{INS1/4}$) or 12V	75	150	50	12.5	250
1.2	3 × 100	1 × 470	2200	220	3.69	3	Yes	Yes	48	($V_{INS1/4}$) or 12V	67.5	135	27	12.5	350
1.2	3 × 100	1 × 470	2200	220	3.69	4	Yes	Yes	48	($V_{INS1/4}$) or 12V	60	120	27	12.5	350
1.2	3 × 220	None	2200	220	1.68	5	Yes	Yes	48	($V_{INS1/4}$) or 12V	85	170	20	12.5	350
1.2	1 × 100	1 × 470	2200	220	3.02	6	Yes	Yes	48	($V_{INS1/4}$) or 12V	68	136	33	12.5	350
1.5	3 × 220	None	2200	220	1.68	5	Yes	Yes	48	($V_{INS1/4}$) or 12V	115	230	30	12.5	350
1.5	1 × 100	1 × 470	2200	220	3.02	6	Yes	Yes	48	($V_{INS1/4}$) or 12V	70	140	27	12.5	350

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Table 13. LTM4664A Dual 25A/30A PSM Output Capacitor Matrix. All Below Parameters Are Typical and Are Dependent on Board Layout

Murata	220µF 6.3V	GRM32ER60J227ME05	PANASONIC SP-CAP	470µF 2.5V EEFSX0E471E4
Taiyo Yuden	220µF 4V	AMK325ABJ227MMHT	PANASONIC POSCAP	470µF 2.5V ETPF470M5H
Murata	100µF 6.3V	GRM32ER60J107M	PANASONIC POSCAP	1000µF 2.5V ETPF1000M5H
Murata	100µF 4V	GRM21BR60G107ME15	PANASONIC POSCAP	1000µF 2.5V ETCF1000M5H
Taiyo Yuden	100µF 4V	AMK325AD7MMHP		

Dual Phase Single 50A/60A Output

V_{OUT} (V)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	COMP*na* (pF)	COMP*nb* (pF)	EA-GM (ms)	R_{COMP} (kΩ)	I_{LIM} HI-RANGE	V_{OUT} LOW-RANGE	V_{INS1} (V)	V_{INS3} C1, C2	DROOP (mV)	PEAK-TO-PEAK DEVIATION (mV)	RECOVERY TIME(µs) LTpowerCAD/ MEASURE	LOAD STEP (A/µs)	FREQ. (kHz)
0.9	8 × 100	4 × 470	3300	220	3.69	8	No	Yes	48	($V_{INS1/4}$) or 12V	47.5	62/95	30	25	250
1	8 × 100	4 × 470	3300	220	3.69	8	No	Yes	48	($V_{INS1/4}$) or 12V	47.5	62/95	30	25	250
1.2	8 × 330	None	5600	100	3.02	5	No	Yes	48	($V_{INS1/4}$) or 12V	35	64	35	25	250
1.2	4 × 100	2 × 470	3300	220	3.02	6	No	Yes	48	($V_{INS1/4}$) or 12V	70	100/140	35	25	350
1.2	4 × 220	None	7500	220	3.02	5	No	Yes	48	($V_{INS1/4}$) or 12V	63	126/-	25	25	350
1.5	4 × 220	None	7500	220	3.02	2.5	No	Yes	48	($V_{INS1/4}$) or 12V	130	260	30	25	350
1.5	6 × 220	None	7500	220	3.69	3	No	Yes	48	($V_{INS1/4}$) or 12V	100	200	30	25	350
1.5	4 × 100	2 × 470	3300	220	3.02	6	No	Yes	48	($V_{INS1/4}$) or 12V	70	140	30	25	350
1.5	4 × 220	None	7500	220	3.02	5	No	Yes	48	($V_{INS1/4}$) or 12V	63	126	25	25	350

DUAL 25A/30A PSM APPLICATIONS INFORMATION–DERATING CURVES

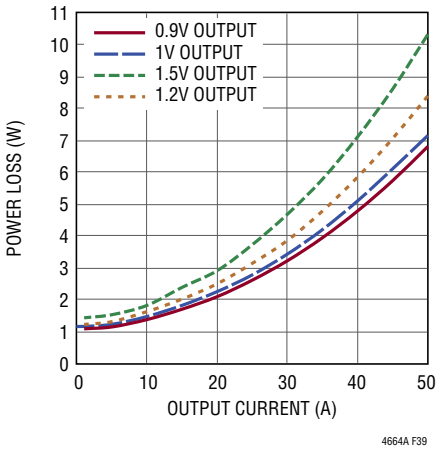

Figure 39. 48V Input Power Loss 2-Phase 50A Output

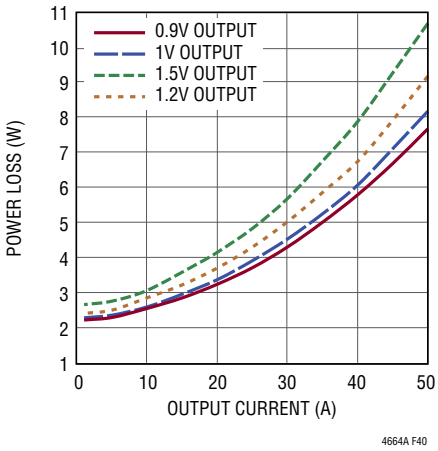

Figure 40. 54V Input Power Loss 2-Phase 50A Output

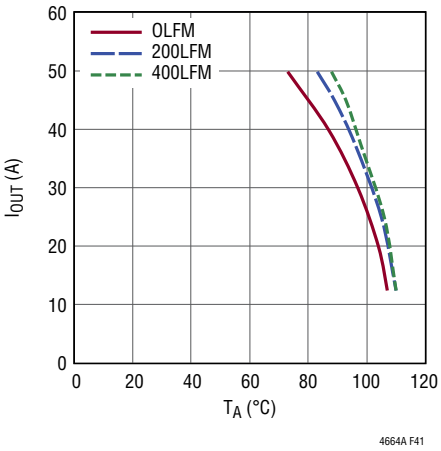

Figure 41. LTM4664A 48V_{IN} 1V_{OUT} Derating Curve No Heat Sink

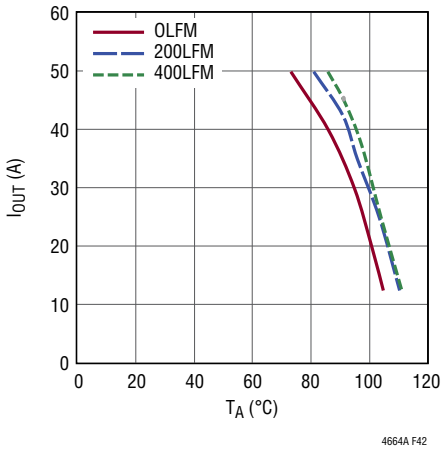

Figure 42. LTM4664A 54V_{IN} 1V_{OUT} Derating Curve No Heat Sink

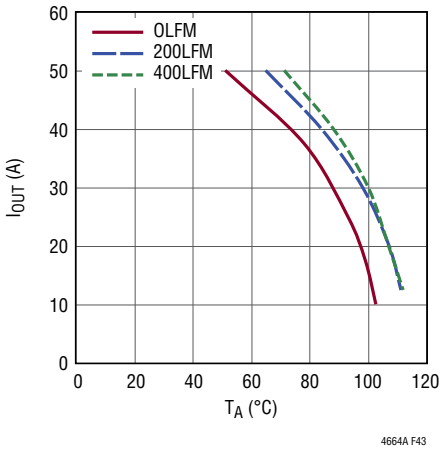

Figure 43. LTM4664A 48V_{IN} 1.5V_{OUT} 350kHz Derating Curve No Heat Sink

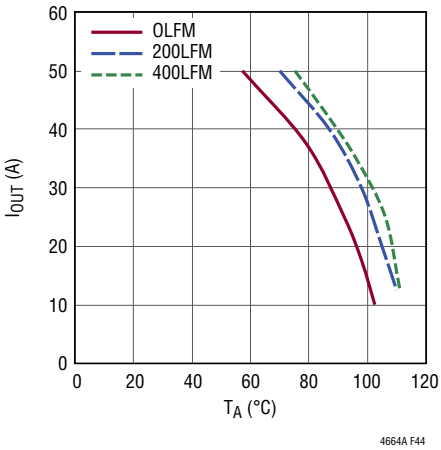

Figure 44. LTM4664A 54V_{IN} 1.5V_{OUT} 350kHz Derating Curve No Heat Sink

DUAL 25A/30A PSM APPLICATIONS INFORMATION

EMI PERFORMANCE

The SW_C*n* pin provides access to the midpoint of the power MOSFETs in LTM4664A's power stages.

Connecting an optional series RC network from SW_C*n* to GND can dampen high frequency (~30MHz+) switch node ringing caused by parasitic inductances and capacitances in the switched-current paths. The RC network is called a snubber circuit because it dampens (or "snubs") the resonance of the parasitics, at the expense of higher power loss. To use a snubber, choose first how much power to allocate to the task and how much PCB real estate is available to implement the snubber. For example, if PCB space allows a low inductance 0.5W resistor to be used then the capacitor in the snubber network (CSW) is computed by:

$$C_{SW} = \frac{P_{SNUB}}{V_{INS3n(MAX)}^{2} \bullet f_{SW}}$$

where $V_{IN3n(MAX)}$ is the maximum input voltage that the input to the power stage (V_{INn}) will see in the application, and f_{SW} is the DC/DC converter's switching frequency of operation. C_{SW} should be NPO, C0G or X7R-type (or better) material.

The snubber resistor (R_{SW}) value is then given by:

$$R_{SW} = \sqrt{\frac{5nH}{C_{SW}}}$$

The snubber resistor should be low ESL and capable of withstanding the pulsed currents present in snubber circuits. A value between 0.7Ω and 4.2Ω is normal.

A 2.2nF snubber capacitor is a good value to start with in series with the snubber resistor to ground. The no load input quiescent current can be monitored while selecting different RC series snubber components to get a increased power loss versus switch node ringing attenuation.

SAFETY CONSIDERATIONS

The LTM4664A modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The device does support over current and overtemperature protection.

DUAL 25A/30A PSM APPLICATIONS INFORMATION

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4664A makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including $V_{IN}n$, GND and $V_{OUTS}n$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{INS}n$, GND and $V_{OUT}n$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4664A.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.
- For parallel modules, tie the $V_{OUTC}n$, ,$V_{OSNS}^{+}\_Cn$/$V_{OSNS}^{-}\_Cn$ voltage-sense differential pair lines, RUN_*n*, COMP_C*n*a, COMP_*n*b pin together. The user must share the SYNC, SHARE_CLK, $\overline{\text{FAULT}}$, and $\overline{\text{ALERT}}$ pins of these parts. Be sure to use pull-up resistors on $\overline{\text{FAULT}}$, SHARE_CLK and $\overline{\text{ALERT}}$.
- Bring out test points on the signal pins for monitoring.

Figure 45 gives a good example of the recommended layout. Reference DC2672A demo manual.

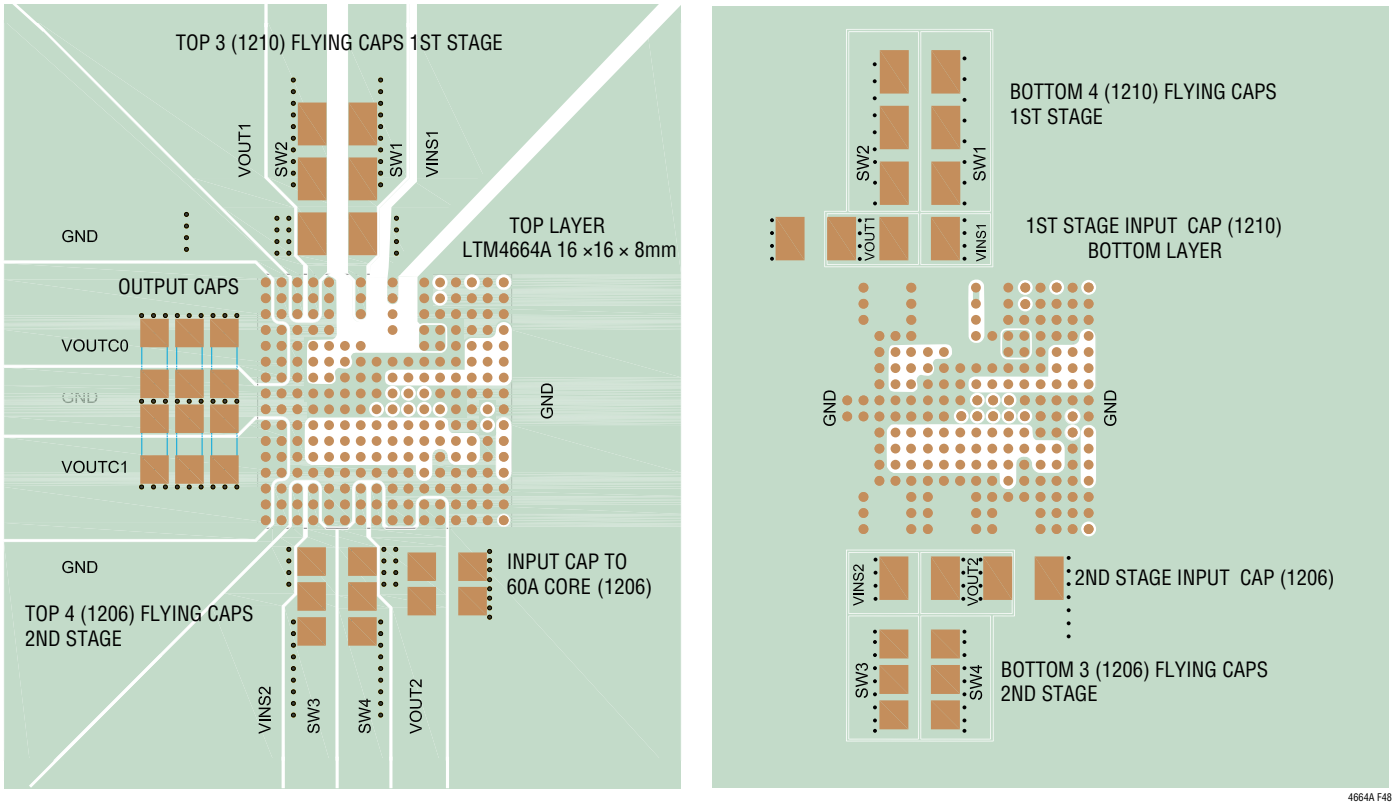

Figure 45. Recommended PCB Layout Package Top and Bottom View

TYPICAL APPLICATIONS

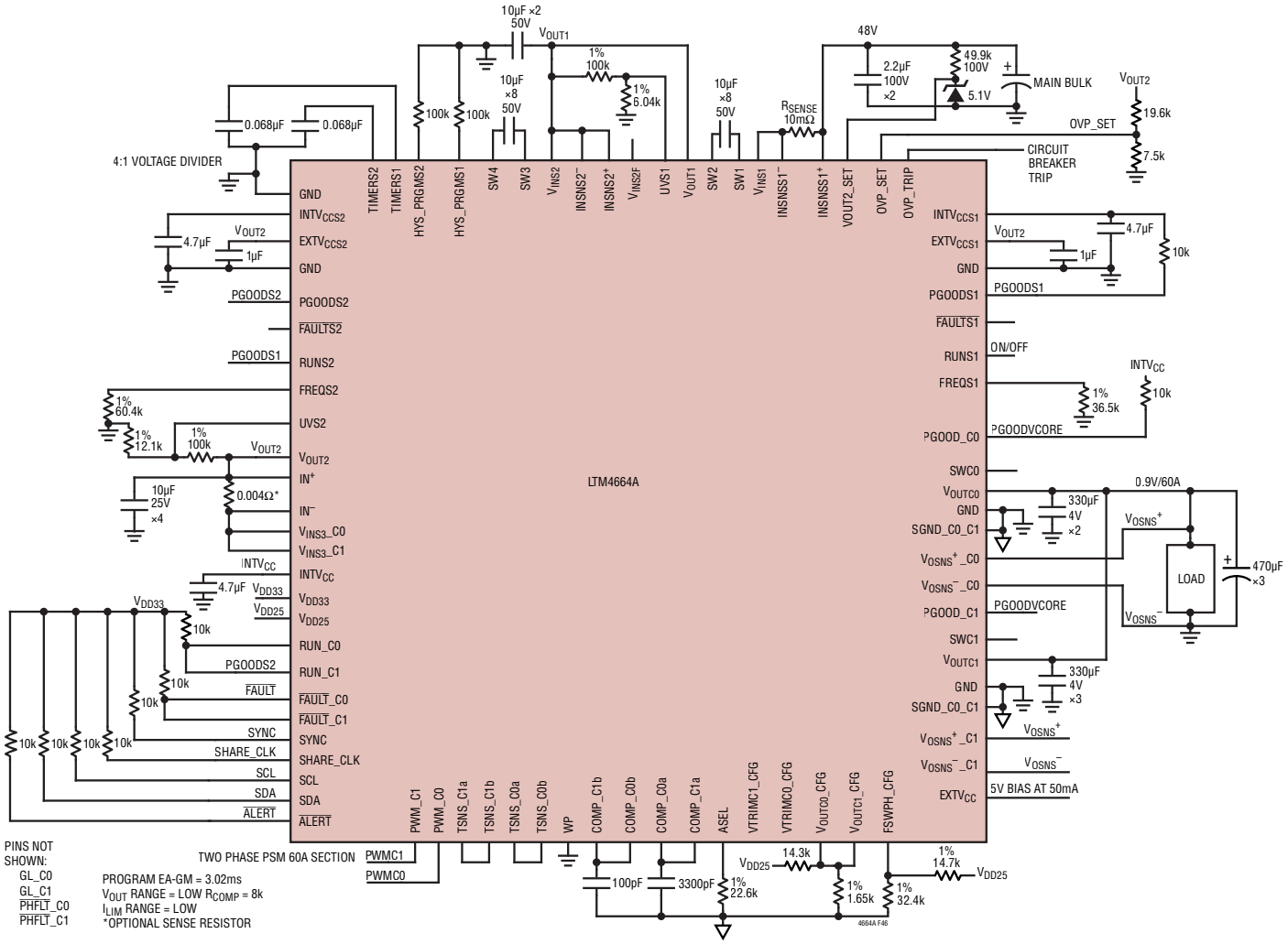

Figure 46. 0.9V at 60A Output DC/DC µModule Regulator with I²C/SMBus/PMBus Serial Interface Including Hot Swap Front End with V_{OUT2} OVP Protection

TYPICAL APPLICATIONS

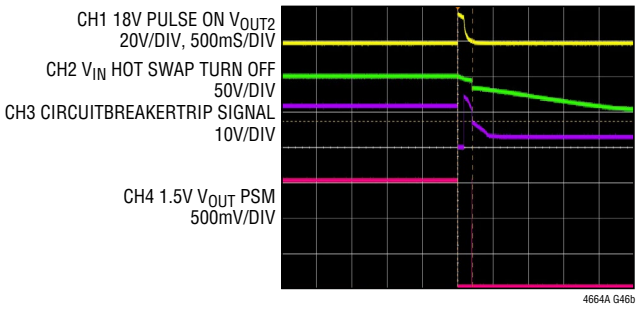

Figure 46b. V_{OUT2} Overvoltage Protection

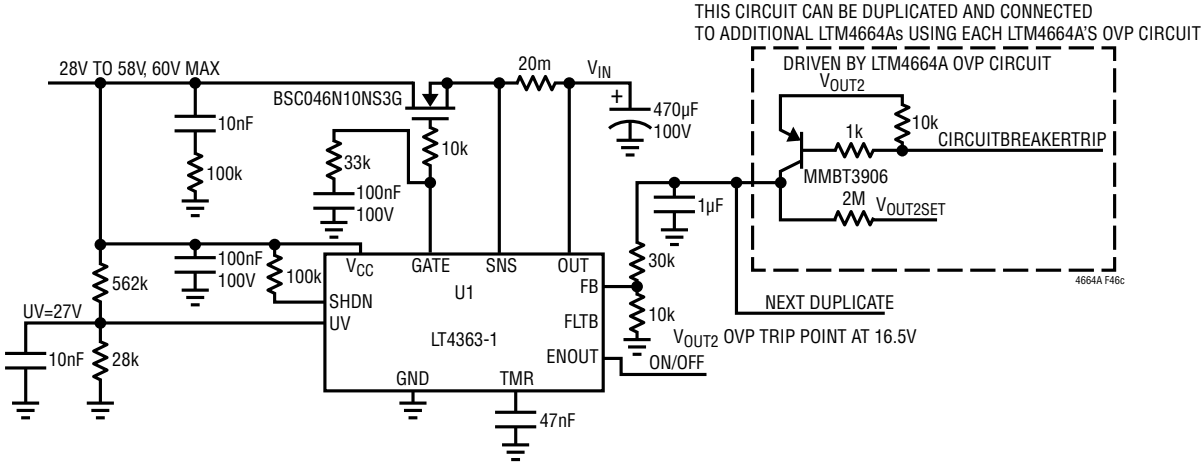

Figure 46c. Hot Swap Circuit Breaker Front End

TYPICAL APPLICATIONS

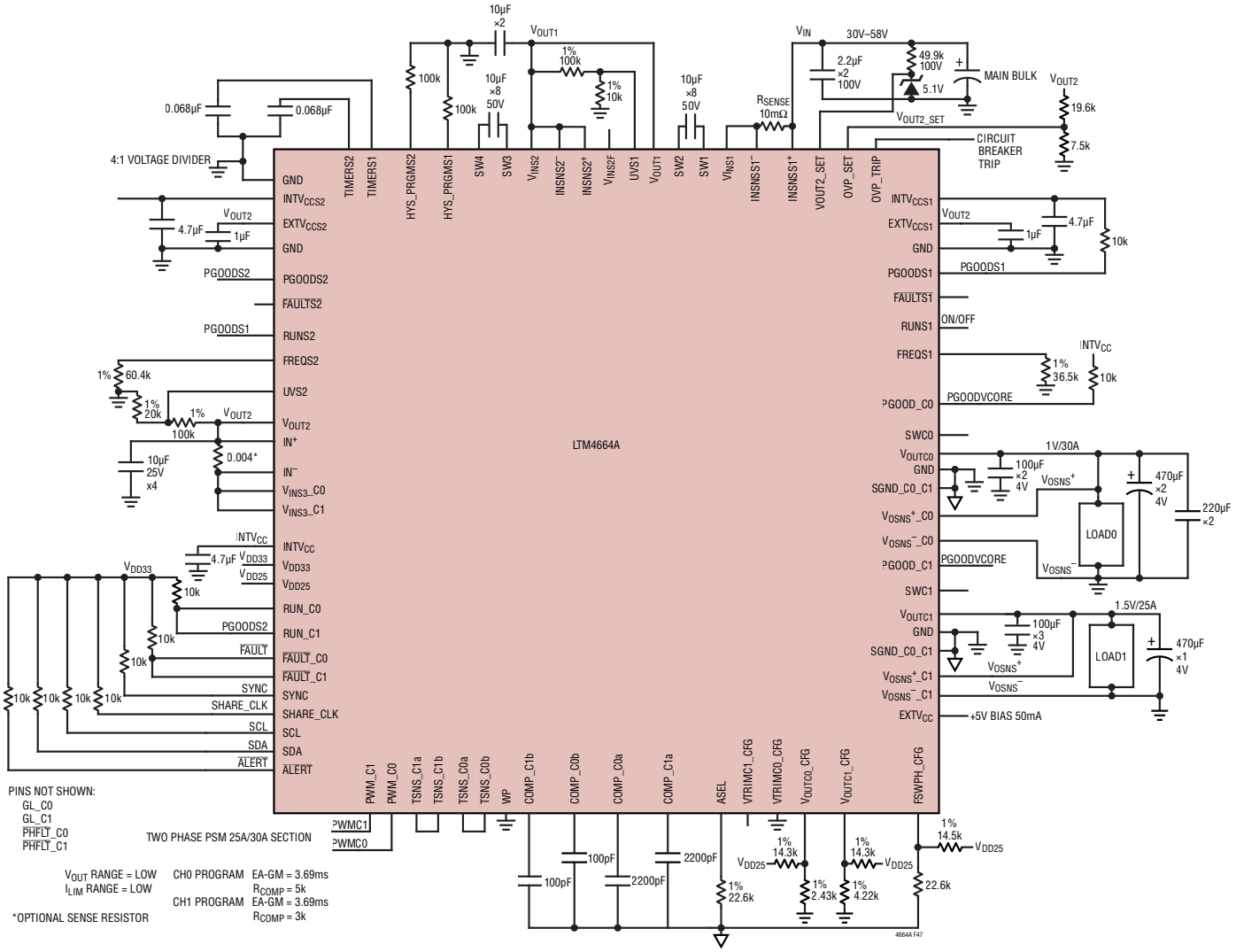

Figure 47. 54V to 1.0V at 30A and 1.5V Outputs at 25A With Providing I²C/SMBus/PMBus Serial Interface

TYPICAL APPLICATIONS

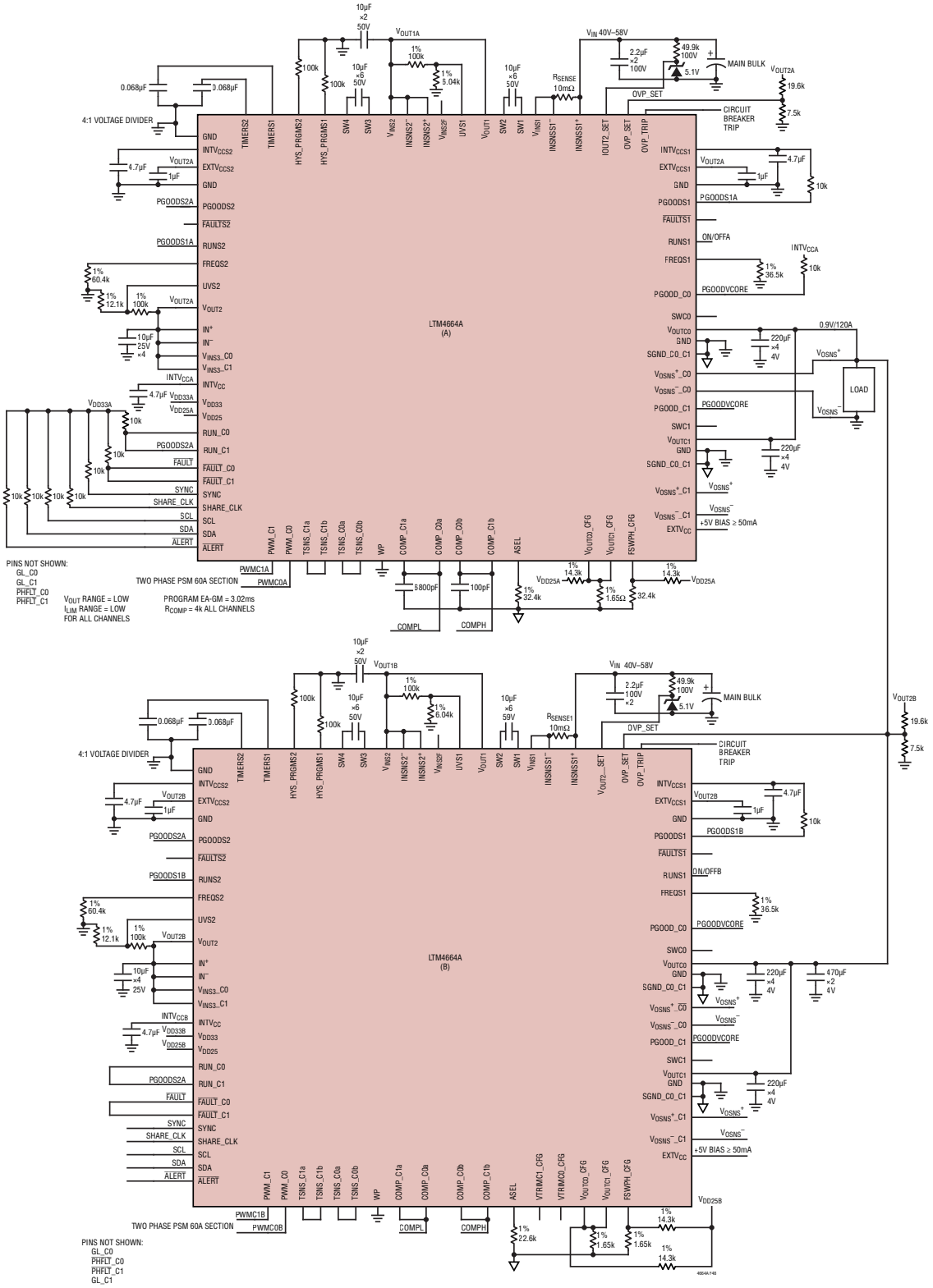

Figure 48. Two Paralleled LTM4664A Producing 54V to 0.9V_{OUT} at 120A. Integrated Power System Management Features Accessible Over 2-Wire I^2C/SMBus/PMBus Serial Interface

TYPICAL APPLICATIONS

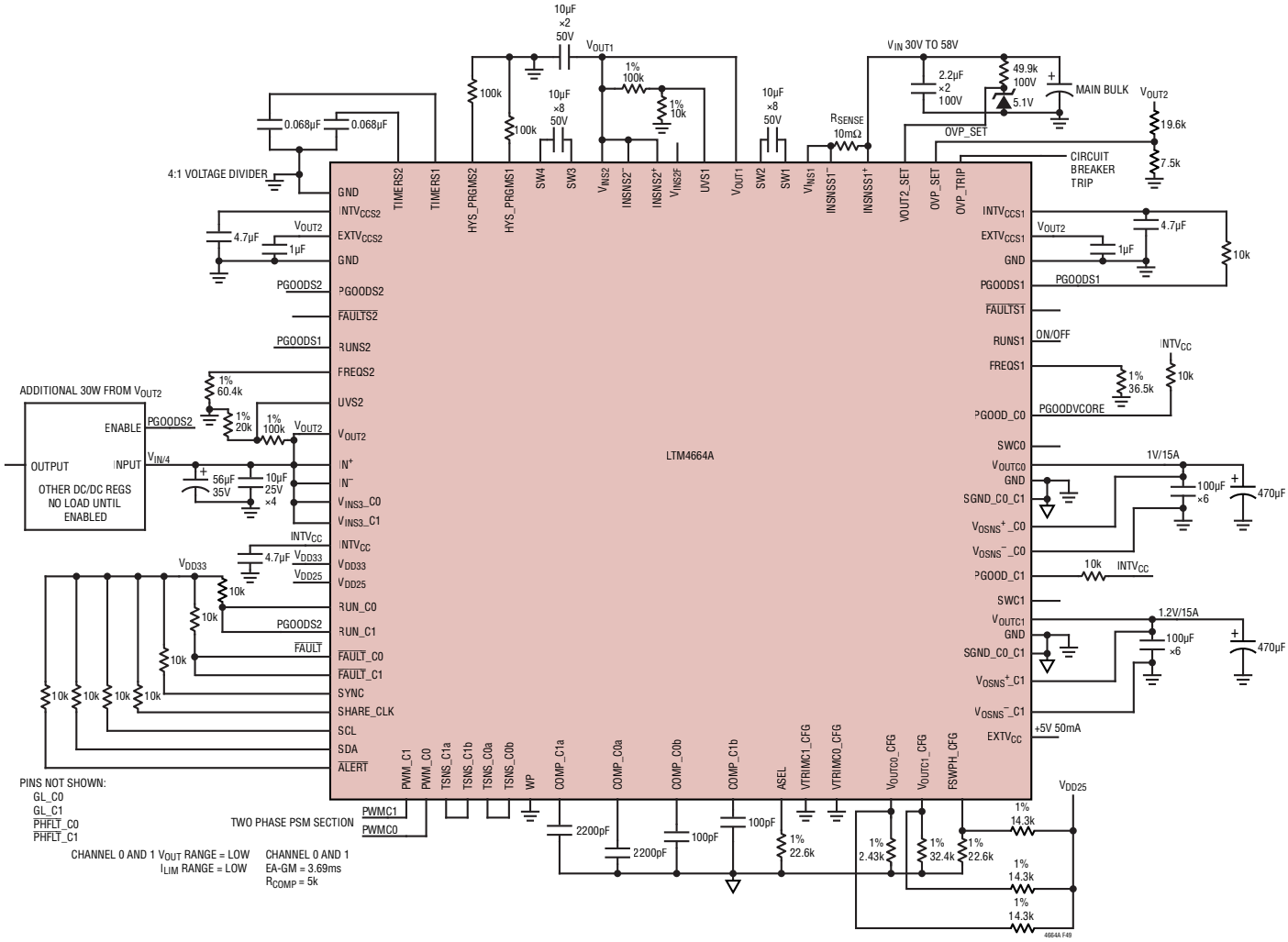

Figure 49. 30V – 58V to 1V and 1.2V at 15A, with Additional 30W from V_{OUT2}. Integrated Power System Management Features Accessible Over 2-Wire I²C/SMBus/PMBus Serial Interface. For Evaluation and More Information, See Demo Boards DC2143

TYPICAL APPLICATIONS

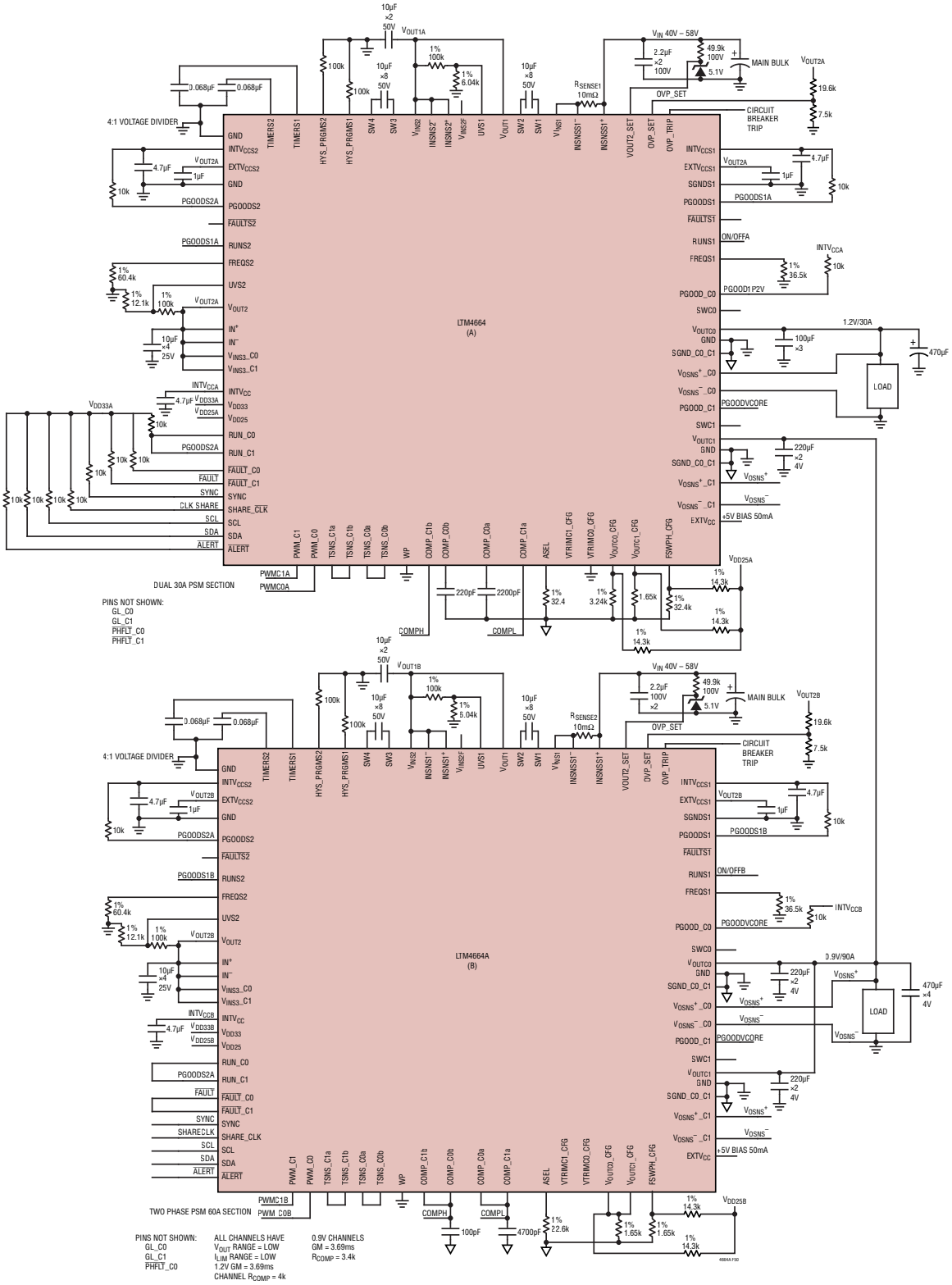

Figure 50. 48V-58V Input, Converting 1.2V at 30A, and 0.9V at 90A. Power System Management Features Accessible Through LTM4664A Over 2-Wire I²C/SMBus/PMBus Serial Interface.

PMBus COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00
PAGE_PLUS_WRITE	0x05	Write a supported command directly to a PWM channel.	W Block	N				
PAGE_PLUS_READ	0x06	Read a supported command directly from a PWM channel.	Block R/W	N				
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80

PAGE

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating commands for one PWM channel.

Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively, in this device.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF the LTM4664A will respond to read commands as if PAGE were set to 0x00 (Channel 0 results).

This command has one data byte.

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command, and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 51.

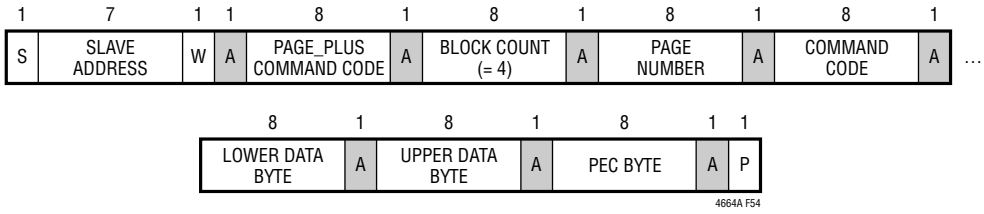

Figure 51. Example of PAGE_PLUS_WRITE

PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command, and then read the data returned by the command, all in one communication packet .

PMBus COMMAND DETAILS

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses the Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 52.

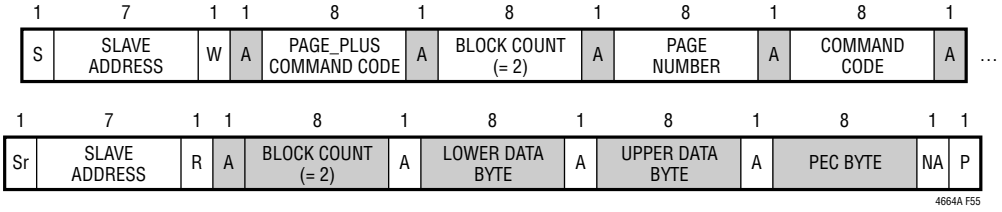

Figure 52. Example of PAGE_PLUS_READ

Note: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTM4664A will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LTM4664A device. This command does not indicate the status of the WP pin which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands.
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x10	Reserved, must be 0
0x08	Reserved, must be 0
0x04	Reserved, must be 0
0x02	Reserved, must be 0
0x01	Reserved, must be 0

Enable writes to all commands when WRITE_PROTECT is set to 0x00.

If WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK, WRITE_PROTECT and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.

PMBus COMMAND DETAILS

MFR_ADDRESS

The MFR_ADDRESS command byte sets the 7 bits of the PMBus slave address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If RCONFIG is set to ignore, the ASEL pin is still used to determine the LSB of the channel address. If the ASEL pin is open, the LTM4664A will use the MFR_ADDRESS value stored in NVM to construct the effective address of the part.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTM4664A will detect bus contention and may set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

GENERAL CONFIGURATION COMMANDS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x10
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21

MFR_CHAN_CONFIG

General purpose configuration command common to multiple LTC products.

BIT	MEANING
7	Reserved
6	Reserved
5	Reserved
4	Disable RUN Low. When asserted the RUN pin is not pulsed low if commanded OFF.
3	Enable short cycle recognition if this bit is set to a 1.
2	SHARE_CLOCK control. If SHARE_CLOCK is held low, the output is disabled.
1	No $\overline{\text{FAULT}}$ $\overline{\text{ALERT}}$, $\overline{\text{ALERT}}$ is not pulled low if $\overline{\text{FAULT}}$ is pulled low externally. Assert this bit if either POWER_GOOD or VOUT_UVUF are propagated on $\overline{\text{FAULT}}$.
0	Disables the V_{OUT} decay value requirement for MFR_RETRY_TIME and $t_{OFF(MIN)}$ processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value for any action that turns off the rail including a fault, an OFF/ON command, or a toggle of RUN from high to low to high.

This command has one data byte.

PMBus COMMAND DETAILS

A short cycle event occurs whenever the PWM channel is commanded back ON, or reactivated, after the part has been commanded OFF and is processing either the TOFF_DELAY or the TOFF_FALL states. The PWM channel can be turned ON and OFF through either the RUN pin and or the PMBus OPERATION command.

If the PWM channel is reactivated during the TOFF_DELAY, the part will perform the following:

1. Immediately tri-state the PWM channel output;
2. Start the retry delay timer as specified by the $t_{OFF(MIN)}$.
3. After the $t_{OFF(MIN)}$ value has expired, the PWM channel will proceed to the TON_DELAY state and the STATUS_MFR_SPECIFIC bit #1 will assert.

If the PWM channel is reactivated during the TOFF_FALL, the part will perform the following:

1. Stop ramping down the PWM channel output;
2. Immediately tri-state the PWM channel output;
3. Start the retry delay timer as specified by the $t_{OFF(MIN)}$.
4. After the $t_{OFF(MIN)}$ value has expired, the PWM channel will proceed to the TON_DELAY state and the STATUS_MFR_SPEFIFIC bit #1 will assert.

If the short cycle event occurs and the short cycle MFR_CHAN_CONFIG bit is not set, the PWM channel state machine will complete its TOFF_DELAY and TOFF_FALL operations as previously commanded by the user.

MFR_CONFIG_ALL

General purpose configuration command common to multiple LTC products.

BIT	MEANING
7	Enable Fault Logging
6	Ignore Resistor Configuration Pins
5	Mask PMBus, Part II, Section 10.9.1 Violations
4	Disable SYNC output
3	Enable 255ms PMBus timeout
2	A valid PEC required for PMBus writes to be accepted. If this bit is not set, the part will accept commands with invalid PEC.
1	Enable the use of PMBus clock stretching
0	Execute CLEAR_FAULTS on rising edge of either RUN pin.

This command has one data byte.

ON/OFF/MARGIN

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80
MFR_RESET	0xFD	Commanded reset without requiring a power-down.	Send Byte	N				NA

PMBus COMMAND DETAILS

ON_OFF_CONFIG

The ON_OFF_CONFIG command specifies the combination of RUN*n* pin input state and PMBus commands needed to turn the PWM channel on and off.

Supported Values:

VALUE	MEANING
0x1F	OPERATION value and RUN*n* pin must both command the device to start/run. Device executes immediate off when commanded off.
0x1E	OPERATION value and RUN*n* pin must both command the device to start/run. Device uses TOFF_ command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x16	RUN*n* pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN*n* pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN*n* pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next RESET or POWER_ON cycle will ramp to that state. If the OPERATION command is modified, for example ON is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE. The default operation command is sequence off. If V_{IN} is applied to a part with factory default programming and the VOUT_CONFIG resistor configuration pins are not installed, the outputs will be commanded off.

The part defaults to the Sequence Off state.

This command has one data byte.

Supported Values:

VALUE	MEANING
0xA8	Margin high.
0x98	Margin low.
0x80	On (V_{OUT} back to nominal even if bit 3 of ON_OFF_CONFIG is not set).
0x40*	Soft off (with sequencing).
0x00*	Immediate off (no sequencing).

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault and the command will be ignored.

This command has one data byte.

MFR_RESET

This command provides a means to reset the LTM4664A PSM from the serial bus. This forces the LTM4664A PSM to turn off both PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of both PWM channels, if enabled.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

PWM CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0x28
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	350kHz 0xFABC

MFR_PWM_MODE

The MFR_PWM_MODE command sets important PWM controls for each channel.

The MFR_PWM_MODE command allows the user to program the PWM controller to use discontinuous (pulse-skipping mode), or forced continuous conduction mode.

BIT	MEANING
7	Use High Range of I_{LIMIT}
0b	Low Current Range
1b	High Current Range
6	Enable Servo Mode
5	External temperature sense:
	0: ΔV_{BE} measurement.
	Now reserved, ΔV_{BE} only supported.
[4:3]	Reserved
2	Reserved, always low DCR current sense
1	V_{OUT} Range
1b	The maximum output voltage is 2.75V
0b	The maximum output voltage is 3.6V
Bit[0]	Mode
0b	Discontinuous
1b	Forced Continuous

Bit [7] of this command determines if the part is in high range or low range of the IOUT_OC_FAULT_LIMIT command. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit [6] The LTM4664A PSM will not servo while the part is OFF, ramping on or ramping off. When set to a one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

The LTM4664A PSM computes temperature in °C from ΔV_{BE} measured by the ADC at the TSNS*n* pin as

$$T = (G \bullet \Delta V_{BE} \bullet q/(K \bullet \ln(16))) - 273.15 + O$$

PMBus COMMAND DETAILS

For both equations,

G = MFR_TEMP_1_GAIN • 2^{-14}, and

O = MFR_TEMP_1_OFFSET

Bit[2] is now reserved, and Ultra Low DCR mode is default.

Bit[1] of this command determines if the part is in high range or low voltage range. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit[0] determines if the PWM mode of operation is discontinuous (pulse-skipping mode), or forced continuous conduction mode. Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this bit. This command has one data byte.

MFR_PWM_COMP

The MFR_PWM_COMP command sets the g_m of the PWM channel error amplifiers and the value of the internal R_{ITHn} compensation resistors. This command affects the loop gain of the PWM output which may require modifications to the external compensation network.

BIT	MEANING
BIT [7:5]	**Error Amplifier GM Adjust (ms)**
000b	1.00
001b	1.68
010b	2.35
011b	3.02
100b	3.69
101b	4.36
110b	5.04
111b	5.73
BIT [4:0]	**R_{COMP} (kΩ)**
00000b	0
00001b	0.25
00010b	0.5
00011b	0.75
00100b	1
00101b	1.25
00110b	1.5
00111b	1.75
01000b	2
01001b	2.5
01010b	3
01011b	3.5
01100b	4
01101b	4.5
01110b	5

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01111b	5.5
10000b	6
10001b	7
10010b	8
10011b	9
10100b	11
10101b	13
10110b	15
10111b	17
11000b	20
11001b	24
11010b	28
11011b	32
11100b	38
11101b	46
11110b	54
11111b	62

This command has one data byte.

MFR_PWM_CONFIG

The MFR_PWM_CONFIG command sets the switching frequency phase offset with respect to the falling edge of the SYNC signal. The part must be in the OFF state to process this command. Either the RUN pins must be low or the channels must be commanded off. If either channel is in the RUN state and this command is written, the command will be NACK'd and a BUSY fault will be asserted.

BIT	MEANING	
7	Reserved	
[6:5]	Input current sense gain.	
00b	2x gain. 0mV to 50mV range.	
01b	4x gain. 0mV to 20mV range.	
10b	8x gain. 0mV to 5mV range.	
11b	Reserved	
4	Share Clock Enable : If this bit is 1, the SHARE_CLK pin will not be released until V_{IN} > VIN_ON. The SHARE_CLK pin will be pulled low when V_{IN} < VIN_OFF. If this bit is 0, the SHARE_CLK pin will not be pulled low when VIN < VIN_OFF except for the initial application of VIN.	
BIT [2:0]	**CHANNEL 0 (DEGREES)**	**CHANNEL 1 (DEGREES)**
000b	0	180
001b	90	270
010b	0	240
011b	0	120
100b	120	240
101b	60	240
110b	120	300

PMBus COMMAND DETAILS

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of the LTM4664A.

Supported Frequencies:

VALUE [15:0]	RESULTING FREQUENCY (TYP)
0x0000	External Oscillator
0xF3E8	250kHz
0xFABC	350kHz
0xFB52	425kHz
0xFBE8	500kHz
0x023F	575kHz
0x028A	650kHz
0x02EE	750kHz
0x03E8	1000kHz

The part must be in the OFF state to process this command. The RUN pin must be low or both channels must be commanded off. If the part is in the RUN state and this command is written, the command will be NACK'd and a BUSY fault will be asserted. When the part is commanded off and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOLTAGE

Input Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	4.65 0xCA53
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	4.75 0xCA60
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	4.5 0xCA40
MFR_RVIN		The resistance value of the V_{IN} pin filter element in milliohms set at factory.	R Word	N	L11	mΩ	N	1000 0x03E8

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC that causes an input undervoltage warning. This warning is disabled until the input exceeds the input startup threshold value set by the VIN_ON command and the unit has been enabled. If the V_{IN} Voltage drops below the VIN_OV_WARN_LIMIT the device:

- Sets the INPUT Bit Is the STATUS_WORD
- Sets the V_{IN} Undervoltage Warning Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, unless Masked

VIN_ON

The VIN_ON command sets the input voltage, in Volts, at which the unit starts power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_OFF

The VIN_OFF command sets the input voltage, in Volts, at which the unit stops power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_RVIN

The MFR_RVIN command is not available, MFR_RVIN is set at factory assembly with 1Ω.

This command has two data bytes and is formatted in Linear_5s_11s format.

Output Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	1.8 0x2CCD
VOUT_OV_FAULT_ LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A
VOUT_OV_WARN_ LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33
VOUT_UV_WARN_ LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD
VOUT_UV_FAULT_ LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage.	R Word	Y	L16	V		7.8 0x1CCD

PMBus COMMAND DETAILS

VOUT_MODE

The data byte for VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte.

VOUT_MAX

The VOUT_MAX command sets an upper limit on any voltage, including VOUT_MARGIN_HIGH, the unit can command regardless of any other commands or combinations. The maximum allowed value of this command is 3.6V. The maximum output voltage the LTM4664A PSM can produce is 1.8V including VOUT_MARGIN_HIGH. However, the VOUT_OV_FAULT_LIMIT can be commanded as high as 3.6V.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured by the OV supervisor comparator at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the part is in the RUN state, allow 10ms after the command is modified to assure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of MFR_COMMON. Either bit is low if the part is busy. If this wait time is not honored and the VOUT_COMMAND is modified above the old overvoltage limit, an OV condition might temporarily be detected resulting in undesirable behavior and possible damage to the switcher.

If VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN or 0x00, the $\overline{\text{FAULT}}$ pin will not assert if VOUT_OV_FAULT is propagated. The LTM4664A PSM will pull the TG low and assert the BG bit as soon as the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage high warning. The MFR_VOUT_PEAK value can be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This condition is detected by the ADC so the response time may be up to $t_{CONVERT}$.

This command has two data bytes and is formatted in Linear_16u format.

PMBus COMMAND DETAILS

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in Volts, when the OPERATION command is set to “Margin High”. The value should be greater than VOUT_COMMAND. The maximum guaranteed value on VOUT_MARGIN_HIGH is 3.6V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_COMMAND

The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts. The maximum guaranteed value on VOUT is 3.6V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin Low”. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_WARN_LIMIT

The VOUT_UV_ WARN_LIMIT command reads the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Undervoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured by the UV supervisor comparator at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.

PMBus COMMAND DETAILS

MFR_VOUT_MAX

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel, including VOUT_OV_FAULT_LIMIT. If the output voltages are set to high range (Bit 6 of MFR_PWM_CONFIG set to a 0) MFR_VOUT_MAX is 3.6V. If the output voltage is set to low range (Bit 6 of MFR_PWM_CONFIG set to a 1) the MFR_VOUT_MAX is 2.75V. Entering a VOUT_COMMAND value greater than this will result in a CML fault and the output voltage setting will be clamped to the maximum level. This will also result in Bit 3 VOUT_MAX_Warning in the STATUS_VOUT command being set. The maximum value to program is 1.8V and maximum operating is 1.5V.

This read only command has 2 data bytes and is formatted in Linear_16u format.

OUTPUT CURRENT AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IOUT_CAL_GAIN	0xDA	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R Word	Y	L11	mΩ	Y	0.375 0xD018
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3900 0x0F3C
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	45.0 0xE2D0
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	34.0 0xE230

MFR_IOUT_CAL_GAIN

The MFR_IOUT_CAL_GAIN command is used to set the resistance value of the current sense resistor in milliohms. (see also MFR_IOUT_CAL_GAIN_TC).

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C.

This command has two data bytes and is formatted in 16-bit 2's complement integer ppm. N = –32768 to 32767 • 10^{-6}. Nominal temperature is 27°C. The MFR_IOUT_CAL_GAIN is multiplied by:

[1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-27)].

DCR sensing will have a typical value of 3900.

The MFR_IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters including: READ_IOUT, MFR_IOUT_PEAK, IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT.

PMBus COMMAND DETAILS

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in Amperes. When the controller is in current limit, the overcurrent detector will indicate an overcurrent fault condition. The following table lists the progammable peak output current limit value in mV between I_{SENSE}^+ and I_{SENSE}^-. The actual value of current limit is ($I_{SENSE}^+ – I_{SENSE}^-$)/MFR_IOUT_CAL_GAIN in Amperes.

MFR_PWM_MODE[7] = 1b, High Current Range (mV)	ILPEAK (A)	IOUT (A)	MFR_PWM_MODE[7] = 0b, Use ILIM Low Range Low Current Range (mV)	ILPEAK (A)	IOUT (A)
18.86	Not Needed	Not Needed	10.48	29.9	23.9
20.42	Not Needed	Not Needed	11.34	32.4	26.4
21.14	Not Needed	Not Needed	11.74*	33.54	27.54
22.27	Not Needed	Not Needed	12.37	35.3	29.3
23.41	Not Needed	Not Needed	13.01**	37.1	31.1
24.55	Not Needed	Not Needed	13.64	38.9	32.9
25.68	Not Needed	Not Needed	14.27	40.8	34.8
26.82	Not Needed	Not Needed	14.90	42.6	36.6

* = Recommended for 25A Current Limit Plus Some Headroom

** = Recommended for 30A Current Limit Plus Some Headroom for Up to 1.2V Output

Note: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

Peak Current Limit = MFR_IOUT_CAL_GAIN • (1 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERTURE_1-27.0)).

The LTM4664A automatically converts currents to the appropriate internal bit value.

The I_{OUT} range is set with bit 7 of the MFR_PWM_MODE command.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

If the IOUT_OC_FAULT_LIMIT is exceeded, the device:

- Sets the IOUT bit in the STATUS word
- Sets the IOUT Overcurrent fault bit in the STATUS_IOUT
- Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

**MFR_PWM_MODE[7]=1 is the high current range for ultra low DCR sensing. This range should be used since these current threshold values are too large for the LTM4664A.

*Recommended for 35% up above 25A current limit

PMBus COMMAND DETAILS

IOUT_OC_WARN_LIMIT

This command sets the value of the output current measured by the ADC that causes an output overcurrent warning in Amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Warning bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format

Input Current and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	L11	mΩ	Y	2 0xC200

MFR_IIN_CAL_GAIN

The MFR_IIN_CAL_GAIN command is used to set the resistance value of the input current sense resistor in milliohms. (see also READ_IIN).

This command has two data bytes and is formatted in Linear_5s_11s format.

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IIN_OC_WARN_LIMIT	0x5D	Input overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, that causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the IIN Overcurrent Warning bit[1] in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TEMPERATURE

External Temperature Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	0.995 0x3FAE
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor.	R/W Word	Y	L11	C	Y	0.0 0x8000

MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command will modify the slope of the external temperature sensor to account for nonidealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2's complement integer. The effective gain adjustment is $N \bullet 2^{-14}$. The nominal value is 1.

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command will modify the offset of the external temperature sensor to account for nonidealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in Linear_5s_11s format.

External Temperature Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_LIMIT	0x4F	Power stage overtemperature fault limit.	R/W Word	Y	L11	C	Y	128 0xF200
OT_WARN_LIMIT	0x51	Power stage overtemperature warning limit.	R/W Word	Y	L11	C	Y	125 0xEBE8
UT_FAULT_LIMIT	0x53	Power stage undertemperature fault limit.	R/W Word	Y	L11	C	Y	–45 0xE530

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This command has two data bytes and is formatted in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

PMBus COMMAND DETAILS

In response to the OT_WARN_LIMIT being exceeded, the device:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of the power stage sense temperature measured by the ADC, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

Note: If the temp sensors are not installed, the UT_FAULT_LIMIT can be set to –275°C and UT_FAULT_LIMIT response set to ignore to avoid $\overline{\text{ALERT}}$ being asserted.

This command has two data bytes and is formatted in Linear_5s_11s format.

TIMING

Timing—On Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	3 0xC300
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	5 0xCA80
VOUT_TRANSITION_RATE	0x27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.001 0x8042

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Values from 0ms to 83 seconds are valid. The resulting turn-on delay will have a typical delay of 270µs for TON_DELAY = 0 and an uncertainty of ±50µs for all values of TON_DELAY.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTM4664A digital slope will be bypassed and the output voltage transition will only be controlled by the analog performance of the PWM switcher. The number of steps in TON_RISE is equal to TON_RISE (in ms)/0.1ms with an uncertainty of ±0.1ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit.

A data value of 0ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change this command set the rate in V/ms at which the output voltage changes. The commanded rate of change does not apply when the unit is commanded on or off. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

Timing—Off Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	3 0xC300
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	0 0x8000

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid. The resulting turn off delay will have a typical delay of 270µs for TOFF_DELAY = 0 and an uncertainty of ±50µs for all values of TOFF_DELAY. TOFF_DELAY is not applied when a fault event occurs

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the V_{OUT} DAC. When the V_{OUT} DAC is zero, the PWM output will be set to high impedance state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The number of steps in TOFF_FALL is equal to TOFF_FALL (in ms)/0.1ms with an uncertainty of ±0.1ms.

In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the output voltage exceeds 12.5% of the programmed voltage before a warning is asserted. The output is considered off when the V_{OUT} voltage is less than 12.5% of the programmed VOUT_COMMAND value. The calculation begins after TOFF_FALL is complete.

A data value of 0ms means that there is no limit and that the output voltage exceeds 12.5% of the programmed voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

Precondition for Restart

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RESTART_ DELAY	0xDC	Minimum time the RUN pin is held low by the LTM4664A.	R/W Word	Y	L11	ms	Y	150 0xF258

MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

Note: The restart delay is different than the retry delay. The restart delay pulls RUN low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF_DELAY + TOFF_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To assure a minimum off time, set the MFR_RESTART_DELAY 16ms longer than the desired time. The output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the output decay bit 0 is enabled in MFR_CHAN_CONFIG and the output takes a long time to decay below 12.5% of the programmed value.

This command has two data bytes and is formatted in Linear_5s_11s format.

FAULT RESPONSE

Fault Responses All Faults

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RETRY_ DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	250 0xF3E8

MFR_RETRY_DELAY

This command sets the time in milliseconds between retries if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 10µs increments.

Note: The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

Fault Responses Input Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input supply overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The data byte is in the format given in Table 17.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN Overvoltage Fault bit in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

Fault Responses Output Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The data byte is in the format given in Table 13.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The only values recognized for this command are:

0x00–Part performs OV pull down only, or OV_PULLDOWN.

0x80–The device shuts down (disables the output) and the unit does not attempt to retry. (PMBus, Part II, Section 10.7).

PMBus COMMAND DETAILS

0xB8–The device shuts down (disables the output) and device attempts to retry continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4n The device shuts down and the unit does not attempt to retry. The output remains disabled until the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

0x78+n The device shuts down and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

Any other value will result in a CML fault and the write will be ignored.

This command has one data byte.

Table 14. VOUT_OV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4664A: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4664A.	00	Part performs OV pull down only or OV_PULLDOWN (i.e., turns off the top MOSFET and turns on lower MOSFET while V_{OUT} is > VOUT_OV_FAULT).
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The data byte is in the format given in Table 8.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT undervoltage fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

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The UV fault and warn are masked until the following criteria are achieved:

1) The TON_MAX_FAULT_LIMIT has been reached
2) The TON_DELAY sequence has completed
3) The TON_RISE sequence has completed
4) The VOUT_UV_FAULT_LIMIT threshold has been reached
5) The IOUT_OC_FAULT_LIMIT is not present

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

Table 15. VOUT_UV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4664A: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The PMBus device continues operation without interruption. (Ignores the fault functionally)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

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TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The data byte is in the format given in Table 13.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

Note: The PWM channel remains in discontinues mode until the TON_MAX_FAULT_LIMIT has been exceeded.

This command has one data byte.

Fault Responses Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The data byte is in the format given in Table 9.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Fault bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

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Table 16. IOUT_OC_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4664A: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The LTM4664A PSM continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage (known as constant-current or brick-wall limiting).
		01	Not supported.
		10	The LTM4664A PSM continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0]. If the device is still operating in current limit at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The LTM4664A PSM shuts down immediately and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN pin or removing bias power.
		111	The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. Only valid for deglitched off response.

Fault Responses IC Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action to take in response to an internal overtemperature fault. The data byte is in the format given in Table 12.

The LTM4664A also:

• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE

• Sets the MFR bit in the STATUS_WORD, and

• Sets the Overtemperature Fault bit in the STATUS_MFR_SPECIFIC command

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

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Table 17. Data Byte Contents MFR_OT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4664A: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4664A.	00	Not supported. Writing this value will generate a CML fault.
		01	Not supported. Writing this value will generate a CML fault
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-111	Not supported. Writing this value will generate CML fault.
2:0	Delay Time	XXX	Not supported. Value ignored

Fault Responses External Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_ RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8
UT_FAULT_ RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an external overtemperature fault on the external temp sensors. The data byte is in the format given in Table 8.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Overtemperature Fault bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an external undertemperature fault on the external temp sensors. The data byte is in the format given in Table 13.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Undertemperature Fault bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

PMBus COMMAND DETAILS

This condition is detected by the ADC so the response time may be up to $t_{CONVERT}$.

This command has one data byte.

Table 18. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4664A: • Sets the corresponding fault bit in the status commands, and • Notifies the host by asserting $\overline{ALERT}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The PMBus device continues operation without interruption.
		01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	Not supported. Values ignored

FAULT SHARING

Fault Sharing Propagation

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_PROPAGATE	0xD2	Configuration that determines which faults are propagated to the FAULT pins.	R/W Word	Y	Reg		Y	0x6993

MFR_FAULT_PROPAGATE

The MFR_FAULT_PROPAGATE command enables the faults that can cause the $\overline{FAULT}n$ pin to assert low. The command is formatted as shown in Table 15. Faults can only be propagated to the $\overline{FAULT}n$ pin if they are programmed to respond to faults.

This command has two data bytes.

PMBus COMMAND DETAILS

Table 19. $\overline{\text{FAULT}}n$ Propagate Fault Configuration

The $\overline{\text{FAULT0}}$ and $\overline{\text{FAULT1}}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
B[15]	VOUT disabled while not decayed.	This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG is a zero. If the channel is turned off, by toggling the RUN pin or commanding the part OFF, and then the RUN is reasserted or the part is commanded back on before the output has decayed, VOUT will not restart until the 12.5% decay is honored. The $\overline{\text{FAULT}}$ pin is asserted during this condition if bit 15 is asserted.
B[14]	Mfr_fault_propagate_short_CMD_cycle	0: No action 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high $t_{OFF(MIN)}$ after sequence off.
b[13]	Mfr_fault_propagate_ton_max_fault	0: No action if a TON_MAX_FAULT fault is asserted 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 TON_MAX_FAULT faults $\overline{\text{FAULT1}}$ is associated with page 1 TON_MAX_FAULT faults
b[12]	Reserved	
b[11]	Mfr_fault0_propagate_int_ot, Mfr_fault1_propagate_int_ot	0: No action if the MFR_OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted
b[10]	Reserved	
b[9]	Reserved	
b[8]	Mfr_fault0_propagate_ut, Mfr_fault1_propagate_ut	0: No action if the UT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 UT faults $\overline{\text{FAULT1}}$ is associated with page 1 UT faults
b[7]	Mfr_fault0_propagate_ot, Mfr_fault1_propagate_ot	0: No action if the OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OT faults $\overline{\text{FAULT1}}$ is associated with page 1 OT faults
b[6]	Reserved	
b[5]	Reserved	
b[4]	Mfr_fault0_propagate_input_ov, Mfr_fault1_propagate_input_ov	0: No action if the VIN_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted
b[3]	Reserved	
b[2]	Mfr_fault0_propagate_iout_oc, Mfr_fault1_propagate_iout_oc	0: No action if the IOUT_OC_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the IOUT_OC_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OC faults $\overline{\text{FAULT1}}$ is associated with page 1 OC faults
b[1]	Mfr_fault0_propagate_vout_uv, Mfr_fault1_propagate_vout_uv	0: No action if the VOUT_UV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_UV_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 UV faults $\overline{\text{FAULT1}}$ is associated with page 1 UV faults
b[0]	Mfr_fault0_propagate_vout_ov, Mfr_fault1_propagate_vout_ov	0: No action if the VOUT_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_OV_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OV faults $\overline{\text{FAULT1}}$ is associated with page 1 OV faults

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Fault Sharing Response

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the FAULT pin is asserted low.	R/W Byte	Y	Reg		Y	0xC0

MFR_FAULT_RESPONSE

The MFR_FAULT_RESPONSE command instructs the device on what action to take in response to the $\overline{\text{FAULT}}n$ pin being pulled low by an external source.

Supported Values:

VALUE	MEANING
0xC0	FAULT_INHIBIT The LTM4664A will three-state the output in response to the $\overline{\text{FAULT}}$ pin pulled low.
0x00	FAULT_IGNORE The LTM4664A continues operation without interruption.

The device also:

- Sets the MFR Bit in the STATUS_WORD.
- Sets Bit 0 in the STATUS_MFR_SPECIFIC Command to Indicate $\overline{\text{FAULT}}n$ Is Being Pulled Low
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
USER_DATA_00	0xB0	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA
USER_DATA_02	0xB2	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_03	0xB3	A NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000
USER_DATA_04	0xB4	A NVM word available for the user.	R/W Word	N	Reg		Y	0x0000

PMBus COMMAND DETAILS

USER_DATA_00 through USER_DATA_04

These commands are non-volatile memory locations for customer storage. The customer has the option to write any value to the USER_DATA_nn at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_nn commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2 data bytes and are in register format.

IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PMBus_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg		FS	0x22
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0
MFR_ID	0x99	The manufacturer ID of the LTM4664A in ASCII.	R String	N	ASC			LTC
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTM4664
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTM4664A.	R Word	N	Reg			0x020X

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTM4664A is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTM4664A supports packet error checking, 400kHz bus speeds, and $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

MFR_ID

The MFR_ID command indicates the manufacturer ID of the LTM4664A using ASCII characters.

This read-only command is in block format.

MFR_MODEL

The MFR_MODEL command indicates the manufacturer's part number of the LTM4664A using ASCII characters.

This read-only command is in block format.

MFR_SPECIAL_ID

The 16-bit word representing the part name and revision. 0x4C denotes the part is an LTM4664A, XX is adjustable by the manufacturer.

This read-only command has two data bytes.

PMBus COMMAND DETAILS

FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA
SMBALERT_MASK	0x1B	Mask activity.	Block R/W	Y	Reg		Y	See CMD Details
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	Y				NA
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA
STATUS_ TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA
STATUS_MFR_ SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC chips.	R Byte	N	Reg			NA

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal. If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the $\overline{\text{ALERT}}$ pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame it may be cleared before the status register is set.

This write-only command has no data bytes.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET command is issued.
- Bias power is removed and reapplied to the integrated circuit

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting $\overline{\text{ALERT}}$ as they are asserted.

Figure 33 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning

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would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

Figure 50 shows an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

SMBALERT_MASK Default Setting: (Refer Also to Figure 2)

STATUS RESISTER	ALERT Mask Value	MASKED BITS
STATUS_VOUT	0x00	None
STATUS_IOUT	0x00	None
STATUS_TEMPERATURE	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x00	None
STATUS_MFR_SPECIFIC	0x11	Bit 4 (internal PLL unlocked), bit 0 ($\overline{\text{FAULT}}$ pulled low by external device)

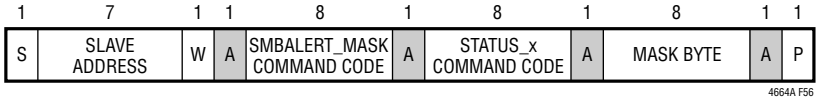

Figure 53. Example of Writing SMBALERT_MASK

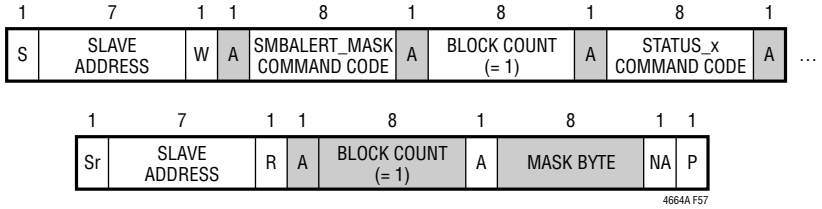

Figure 54. Example of Reading SMBALERT_MASK

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. A MFR_RESET command will also clear the MFR_*_PEAK data values.

This write-only command has no data bytes.

STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. This is the lower byte of the status word.

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STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7*	BUSY	A fault was declared because the LTM4664A was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTM4664A returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0*	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

*$\overline{\text{ALERT}}$ can be asserted if either of these bits is set. They may be cleared by writing a 1 to their bit position in the STATUS_BYTE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTM4664A has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTM4664A returns 0).
9	OTHER	Not supported (LTM4664A returns 0).
8	UNKNOWN	Not supported (LTM4664A returns 0).

If any of the bits in the upper byte are set, NONE_OF_THE_ABOVE is asserted.

This command has two data bytes.

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	V_{OUT} max warning.
2	TON max fault.
1	TOFF max fault.
0	Not supported (LTM4664A returns 0).

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The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTM4664A returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTM4664A returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. This command has one data byte.

STATUS_INPUT

The STATUS_INPUT command returns one byte of V_{IN} (VINS3_C1) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	V_{IN} overvoltage fault.
6	Not supported (LTM4664A returns 0).
5	V_{IN} undervoltage warning.
4	Not supported (LTM4664A returns 0).
3	Unit off for insufficient V_{IN}.
2	Not supported (LTM4664A returns 0).
1	I_{IN} overcurrent warning.
0	Not supported (LTM4664A returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. Bit 3 of this command is not latched and will not generate an $\overline{\text{ALERT}}$ even if it is set. This command has one data byte.

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STATUS_TEMPERATURE

The STATUS_TEMPERATURE commands returns one byte with status information on temperature. This is a paged command and is related to the respective READ_TEMPERATURE_1 value.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault.
6	External overtemperature warning.
5	Not supported (LTM4664A returns 0).
4	External undertemperature fault.
3:0	Not supported (LTM4664A returns 0).

.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

This command has one data byte.

STATUS_CML

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTM4664A returns 0).
1	Other communication fault.
0	Other memory or logic fault.

If either bit 3 or bit 4 of this command is set, a serious and significant internal error has been detected. Continued operation of the part is not recommended if these bits are continuously set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

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STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information.

The format for this byte is:

BIT	MEANING
7	Internal Temperature Fault Limit Exceeded.
6	Internal Temperature Warn Limit Exceeded.
5	Factory Trim Area NVM CRC Fault.
4	PLL is Unlocked
3	Fault Log Present
2	V_{DD33} UV or OV Fault
1	Short-cycle Event Detected
0	$\overline{FAULT}$ Pin Asserted Low by External Device

If any of these bits are set, the MFR bit in the STATUS_WORD will be set, and $\overline{ALERT}$ may be asserted.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. However, the fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an $\overline{ALERT}$ event.

This command has one data byte.

MFR_PADS

This command provides the user a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

BIT	ASSIGNED DIGITAL PIN
15	V_{DD33} OV Fault
14	V_{DD33} UV Fault
13	Reserved
12	Reserved
11	ADC Values Invalid, Occurs During Start-Up. May Occur Briefly on Current Measurement Channels During Normal Operation
10	SYNC clocked by external device (when LTM4664A configured to drive SYNC pin)
9	Channel 1 Power Good
8	Channel 0 Power Good
7	LTM4664A Driving RUN1 Low
6	LTM4664A Driving RUN0 Low
5	RUN1 Pin State
4	RUN0 Pin State
3	LTM4664A Driving $\overline{FAULT1}$ Low
2	LTM4664A Driving $\overline{FAULT0}$ Low
1	$\overline{FAULT1}$ Pin State
0	$\overline{FAULT0}$ Pin State

A 1 indicates the condition is true.

This read-only command has two data bytes.

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MFR_COMMON

The MFR_COMMON command contains bits that are common to all LTC digital power and telemetry products.

BIT	MEANING
7	Chip Not Driving $\overline{\text{ALERT}}$ Low
6	LTM4664A Not Busy
5	Calculations Not Pending
4	LTM4664A Outputs Not in Transition
3	NVM Initialized
2	Reserved
1	SHARE_CLK Timeout
0	WP Pin Status

This read-only command has one data byte.

MFR_INFO

The MFR_INFO command contains additional status bits that are LTC3884-specific and may be common to multiple ADI PSM products.

MFR_INFO Data Contents:

BIT	MEANING
15:5	Reserved.
4	EEPROM ECC status. 0: Corrections made in the EEPROM user space. 1: No corrections made in the EEPROM user space.
3:0	Reserved

EEPROM ECC status is updated after each RESTORE_USER_ALL or RESET command, a power-on reset or an EEPROM bulk read operation. This read-only command has two data bytes.

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TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA
READ_TEMPERATURE_1	0x8D	Power stage diode junction temperature. This is the value used for all temperature related processing, including MFR_IOUT_CAL_GAIN.	R Word	Y	L11	C		NA
READ_TEMPERATURE_2	0x8E	Power stage junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA
READ_PIN	0x97	Calculated input power.	R Word	N	L11	W		NA
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command	R Byte	N		%		5.0%
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS.	R Word	N	L11	A		NA
MFR_READ_ICHIP	0xE4	Measured current used by the LTM4664A.	R Word	N	L11	A		NA
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back.	R/W Byte	N	N	Reg		NA

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READ_VIN

The READ_VIN command returns the measured V_{IN} pin voltage, in volts added to READ_ICHIP • MFR_RVIN. This compensates for the IR voltage drop across the V_{IN} filter element due to the supply current of the LTM4664A.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the measured output voltage by the VOUT_MODE command.

This read-only command has two data bytes and is formatted in Linear_16u format.

READ_IIN

The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor (see also MFR_IIN_CAL_GAIN).

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The IOUT value is a function of:

a) the differential voltage measured across the I_{SENSE} pins

b) the MFR_IOUT_CAL_GAIN value

c) the MFR_IOUT_CAL_GAIN_TC value, and

d) READ_TEMPERATURE_1 value

e) The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the power stage sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the LTM4664A's die temperature, in degrees Celsius, of the internal sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_FREQUENCY

The READ_FREQUENCY command is a reading of the PWM switching frequency in kHz.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_POUT

The READ_POUT command is a reading of the DC/DC converter output power in Watts. POUT is calculated based on the most recent correlated output voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

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READ_PIN

The READ_PIN command is a reading of the DC/DC converter input power in Watts. PIN is calculated based on the most recent input voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_PIN_ACCURACY

The MFR_PIN_ACCURACY command returns the accuracy, in percent, of the value returned by the READ_PIN command.

There is one data byte. The value is 0.1% per bit which gives a range of ±0.0% to ±25.5%.

This read-only command has one data byte and is formatted as an unsigned integer.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN_PEAK

The MFR_READ_IIN_PEAK command reports the highest current, in Amperes, reported by the READ_IIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_ICHIP

The MFR_READ_ICHIP command returns the measured input current, in Amperes, used by the LTM4664A.

This command has two data bytes and is formatted in Linear_5s_11s format.

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MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_ADC_CONTROL

The MFR_ADC_CONTROL command determines the ADC read back selection. A default value of 0 in the command runs the standard telemetry loop with all parameters updated in a round robin fashion with a typical latency of $t_{CONVERT}$. The user can command a non-zero value to monitored a single parameter with an approximate update rate of 8ms. This command has a latency of up to 2 ADC conversions or approximately 16ms (external temperature conversions may have a latency of up to 3 ADC conversion or approximately 24ms). It is recommended the part remain in standard telemetry mode except for special cases where fast ADC updates of a single parameter is required. The part should be commanded to monitor the desired parameter for a limited period of time (less then 1 second) then set the command back to standard round robin mode. If this command is set to any value except standard round robin telemetry (0) all warnings and faults associated with telemetry other than the selected parameter are effectively disabled and voltage servoing is disabled. When round robin is reasserted, all warnings and faults and servo mode are re-enabled.

COMMANDED VALUE	TELEMETRY COMMAND NAME	DESCRIPTION
0x0F		Reserved
0x0E		Reserved
0x0D		Reserved
0x0C	READ_TEMPERATURE_1	Channel 1 external temperature
0x0B		Reserved
0x0A	READ_IOUT	Channel 1 measured output current
0x09	READ_VOUT	Channel 1 measured output voltage
0x08	READ_TEMPERATURE_1	Channel 0 external temperature
0x07		Reserved
0x06	READ_IOUT	Channel 0 measured output current
0x05	READ_VOUT	Channel 0 measured output voltage
0x04	READ_TEMPERATURE_2	Internal junction temperature
0x03	READ_IIN	Measured input supply current
0x02	MFR_READ_ICHIP	Measured supply current of the LTM4664A
0x01	READ_VIN	Measured input supply voltage
0x00		Standard ADC Round Robin Telemetry

If a reserved command value is entered, the telemetry will default to Internal IC Temperature and issue a CML fault. CML faults will continue to be issued by the LTM4664A until a valid command value is entered. The accuracy of the measured input supply voltage is only guaranteed if the MFR_ADC_CONTROL command is set to standard round robin telemetry.

This write-only command has 1 data byte and is formatted in register format.

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NVM MEMORY COMMANDS

Store/Restore

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the non-volatile user contents of the Operating Memory to the matching locations in the non-volatile User NVM memory.

Executing this command if the die temperature exceeds 85°C or is below 0°C is not recommended and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTM4664A and programming of the NVM can be initiated when $EXTV_{CC}$ or VDD33 is available and VIN is not applied. To enable the part in this state, using global address 0x5B write MFR_EE_UNLOCK to 0x2B followed by 0xC4. The LTM4664A will now communicate normally, and the project file can be updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When VIN is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the LTM4664A to copy the contents of the non-volatile User memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the User commands. The LTM4664A ensures both channels are off, loads the operating memory from the internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of both PWM channels if applicable.

STORE_USER_ALL, MFR_COMPARE_USER_ALL and RESTORE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in non-volatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

This write-only command has no data bytes.

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Fault Logging

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	CF		Y	NA
MFR_FAULT_LOG_ STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was written. The contents of this command are stored in non-volatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 15. If the user accesses the MFR_FAULT_LOG command and no fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAULT_LOG will return a block of data 147 bytes long. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

NOTE: The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to NVM just as if a fault event occurred. This command will set bit 3 of the STATUS_MFR_SPECIFIC fault if bit 7 “Enable Fault Logging” is set in the MFR_CONFIG_ALL command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

This write-only command has no data bytes.

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Table 20. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

Data Format Definitions				LIN 11 = PMBus = Rev 1.2, Part 2, section 7.1
				LIN 16 = PMBus Rev 1.2, Part 2, section 8. Mantissa portion only
				BYTE = 8 bits interpreted per definition of this command
DATA	**BITS**	**DATA FORMAT**	**BYTE NUM**	**BLOCK READ COMMAND**
Block Length		BYTE	147	The MFR_FAULT_LOG command is a fixed length of 147 bytes The block length will be zero if a data log event has not been captured
HEADER INFORMATION				
Fault Log Preface	[7:0]	ASC	0	Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary part to part.
	[7:0]		1	
	[15:8]	Reg	2	
	[7:0]		3	
Fault Source	[7:0]	Reg	4	Refer to Table 16.
MFR_REAL_TIME	[7:0]	Reg	5	48 bit share-clock counter value when fault occurred (200µs resolution).
	[15:8]		6	
	[23:16]		7	
	[31:24]		8	
	[39:32]		9	
	[47:40]		10	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	L16	11	Peak READ_VOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		12	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	L16	13	Peak READ_VOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		14	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	L11	15	Peak READ_IOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		16	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	L11	17	Peak READ_IOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		18	
MFR_VIN_PEAK	[15:8]	L11	19	Peak READ_VIN since last power-on or CLEAR_PEAKS command.
	[7:0]		20	
READ_TEMPERATURE1 (PAGE 0)	[15:8]	L11	21	External temperature sensor 0 during last event.
	[7:0]		22	
READ_TEMPERATURE1 (PAGE 1)	[15:8]	L11	23	External temperature sensor 1 during last event.
	[7:0]		24	
READ_TEMPERATURE2	[15:8]	L11	25	LTM4664A die temperature sensor during last event.
	[7:0]		26	

PMBus COMMAND DETAILS

CYCLICAL DATA				
EVENT n **(Data at Which Fault Occurred; Most Recent Data)**				Event "n" represents one complete cycle of ADC reads through the MUX at time of fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all 6 event pages to EEPROM
READ_VOUT (PAGE 0)	[15:8]	LIN 16	27	
	[7:0]	LIN 16	28	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	29	
	[7:0]	LIN 16	30	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	31	
	[7:0]	LIN 11	32	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	33	
	[7:0]	LIN 11	34	
READ_VIN	[15:8]	LIN 11	35	
	[7:0]	LIN 11	36	
READ_IIN	[15:8]	LIN 11	37	
	[7:0]	LIN 11	38	
STATUS_VOUT (PAGE 0)		BYTE	39	
STATUS_VOUT (PAGE 1)		BYTE	40	
STATUS_WORD (PAGE 0)	[15:8]	WORD	41	
	[7:0]	WORD	42	
STATUS_WORD (PAGE 1)	[15:8]	WORD	43	
	[7:0]	WORD	44	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	45	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	46	
EVENT n-1 **(data measured before fault was detected)**				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	47	
	[7:0]	LIN 16	48	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	49	
	[7:0]	LIN 16	50	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	51	
	[7:0]	LIN 11	52	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	53	
	[7:0]	LIN 11	54	
READ_VIN	[15:8]	LIN 11	55	
	[7:0]	LIN 11	56	
READ_IIN	[15:8]	LIN 11	57	
	[7:0]	LIN 11	58	
STATUS_VOUT (PAGE 0)		BYTE	59	
STATUS_VOUT (PAGE 1)		BYTE	60	
STATUS_WORD (PAGE 0)	[15:8]	WORD	61	
	[7:0]	WORD	62	
STATUS_WORD (PAGE 1)	[15:8]	WORD	63	
	[7:0]	WORD	64	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	65	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	66	

PMBus COMMAND DETAILS

EVENT n-5 (Oldest Recorded Data)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	127	
	[7:0]	LIN 16	128	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	129	
	[7:0]	LIN 16	130	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	131	
	[7:0]	LIN 11	132	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	133	
	[7:0]	LIN 11	134	
READ_VIN	[15:8]	LIN 11	135	
	[7:0]	LIN 11	136	
READ_IIN	[15:8]	LIN 11	137	
	[7:0]	LIN 11	138	
STATUS_VOUT (PAGE 0)		BYTE	139	
STATUS_VOUT (PAGE 1)		BYTE	140	
STATUS_WORD (PAGE 0)	[15:8]	WORD	141	
	[7:0]	WORD	142	
STATUS_WORD (PAGE 1)	[15:8]	WORD	143	
	[7:0]	WORD	144	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	145	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	146	

Table 21. Explanation of Position_Fault Values

POSITION_FAULT VALUE	SOURCE OF FAULT LOG
0xFF	MFR_FAULT_LOG_STORE
0x00	TON_MAX_FAULT
0x01	VOUT_OV_FAULT
0x02	VOUT_UV_FAULT
0x03	IOUT_OC_FAULT
0x05	TEMP_OT_FAULT
0x06	TEMP_UT_FAULT
0x07	VIN_OV_FAULT
0x0A	MFR_TEMP_2_OT_FAULT

PMBus COMMAND DETAILS

MFR_INFO

Contact the factory for details.

MFR_IOUT_CAL_GAIN

Contact the factory for details.

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.

This write-only command is send bytes.

Block Memory Write/Read

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA

All the NVM commands are disabled if the die temperature exceeds 130°C. NVM commands are re-enabled when the die temperature drops below 125°C.

MFR_EE_xxxx

The MFR_EE_xxxx commands facilitate bulk programming of the LTM4664A internal EEPROM. Contact the factory for details.

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

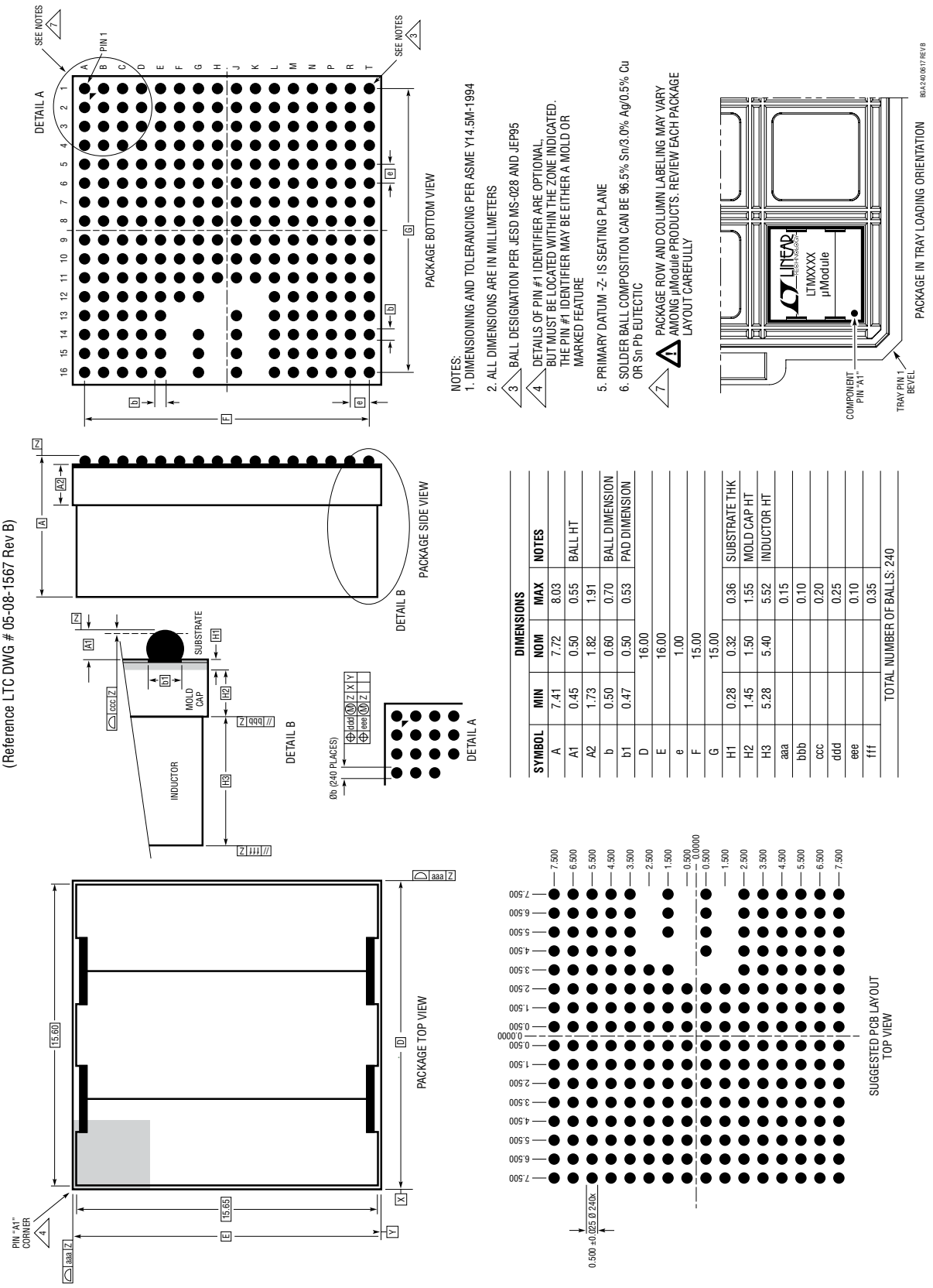
Table 22. LTM4664AY Pin Out Array BGA

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUTC1}	B1	GND	C1	V_{INS2}	D1	SW3	E1	GND	F1	GND	G1	SW4	H1	V_{OUT2}
A2	V_{OUTC1}	B2	GND	C2	V_{INS2}	D2	SW3	E2	GND	F2	GND	G2	SW4	H2	V_{OUT2}
A3	V_{OUTC1}	B3	GND	C3	V_{INS2}	D3	SW3	E3	GND	F3	GND	G3	SW4	H3	V_{OUT2}
A4	V_{OUTC1}	B4	V_{OUTC1}	C4	GND	D4	GND	E4	GND	F4	GND	G4	GND	H4	GND
A5	V_{OUTC1}	B5	V_{OUTC1}	C5	GND	D5	V_{INS2F}	E5	HYS_PRGMS2	F5	TIMERS2	G5	FREQS2	H5	PGOODS2
A6	V_{OUTC1}	B6	V_{OUTC1}	C6	GND	D6	I_{NSNSS2}^-	E6	OVP_SET	F6	VOUT2_SET	G6	RUNS2	H6	$\overline{FAULTS2}$
A7	V_{OUTC1}	B7	V_{OUTC1}	C7	GND	D7	I_{NSNSS2}^+	E7	OVP_TRIP	F7	$EXTV_{CCS2}$	G7	$INTV_{CCS2}$	H7	UVS2
A8	GND	B8	GND	C8	GND	D8	GND	E8	GND	F8	GND	G8	GND	H8	FSWPH_CFG
A9	GND	B9	GND	C9	GND	D9	GND	E9	GND	F9	GND	G9	GND	H9	GND
A10	V_{OUTC0}	B10	V_{OUTC0}	C10	GND	D10	$INTV_{CCS1}$	E10	UVS1	F10	GND	G10	GND	H10	GND
A11	V_{OUTC0}	B11	V_{OUTC0}	C11	GND	D11	$EXTV_{CCS1}$	E11	$\overline{FAULTS1}$	F11	RUNS1	G11	GND	H11	GND
A12	V_{OUTC0}	B12	V_{OUTC0}	C12	GND	D12	PGOODS1	E12	FREQS1	F12	TIMERS1	G12	HYS_PRGMS1	H12	
A13	V_{OUTC0}	B13	V_{OUTC0}	C13	GND	D13	GND	E13	GND	F13		G13		H13	
A14	V_{OUTC0}	B14	GND	C14	V_{OUT1}	D14	SW2	E14	GND	F14		G14	SW1	H14	
A15	V_{OUTC0}	B15	GND	C15	V_{OUT1}	D15	SW2	E15	GND	F15		G15	SW1	H15	
A16	V_{OUTC0}	B16	GND	C16	V_{OUT1}	D16	SW2	E16	GND	F16		G16	SW1	H16	

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
J1	GND	K1	GND	L1	V_{INS3_C1}	M1	V_{INS3_C1}	N1	GND	P1	GND	R1	GND	T1	TSNS_C1b
J2	GND	K2	GND	L2	V_{INS3_C1}	M2	V_{INS3_C1}	N2	GND	P2	GND	R2	GND	T2	GND
J3	GND	K3	GND	L3	GND	M3	GND	N3	GND	P3	GND	R3	GND	T3	GND
J4	GND	K4	GND	L4	PWM_C1	M4	GND	N4	GND	P4	GND	R4	GND	T4	SWC1
J5	VTRIMC1_CFG	K5	VTRIMC0_CFG	L5	$\overline{PHFLT}$_C1	M5	GND	N5	PGOOD_C1	P5	GL_C1	R5	GND	T5	SWC1
J6	VOUTC0_CFG	K6	V_{DD25}	L6	V_{DD33}	M6	COMP_1a	N6	V_{OSNS}^-_C1	P6	V_{OSNS}^+_C1	R6	GND	T6	SWC1
J7	VOUTC1_CFG	K7	WP	L7	SHARE_CLK	M7	COMP_1b	N7	GND	P7	GND	R7	$INTV_{CC}$	T7	SWC1
J8	ASEL	K8	RUN_C1	L8	SDA	M8	SYNC	N8	SGND_C0_C1	P8	GND	R8	$EXTV_{CC}$	T8	GND
J9	RUN_C0	K9	$\overline{FAULT}$_C1	L9	SCL	M9	SGND_C0_C1	N9	SGND_C0_C1	P9	GND	R9	GND	T9	GND
J10	$\overline{ALERT}$	K10	$\overline{FAULT}$_C0	L10	TSNS_C0a	M10	TSNS_C1a	N10	COMP_0b	P10	IN^-	R10	IN^+	T10	SWC0
J11	GND	K11	GND	L11	GND	M11	GND	N11	GND	P11	COMP_0a	R11	PGOOD_C0	T11	SWC0
J12		K12		L12	V_{INS3_C0}	M12	V_{INS3_C0}	N12	GND	P12	V_{OSNS}^-_C0	R12	V_{OSNS}^+_C0	T12	SWC0
J13	$INSNSS1^-$	K13		L13	V_{INS3_C0}	M13	V_{INS3_C0}	N13	GND	P13	GND	R13	GND	T13	SWC0
J14	$INSNSS1^+$	K14		L14	GND	M14	GND	N14	GND	P14	GND	R14	GND	T14	GND
J15	V_{INS1}	K15		L15	GND	M15	PWM_C0	N15	GND	P15	GND	R15	GND	T15	GND
J16	V_{INS1}	K16		L16	GND	M16	$\overline{PHFLT}$_C0	N16	GND	P16	GL_C0	R16	GND	T16	TSNS_C0b

PACKAGE DESCRIPTION

BGA Package
240-Lead (16mm × 16mm × 7.72mm)
(Reference LTC DWG # 05-08-1567 Rev B)



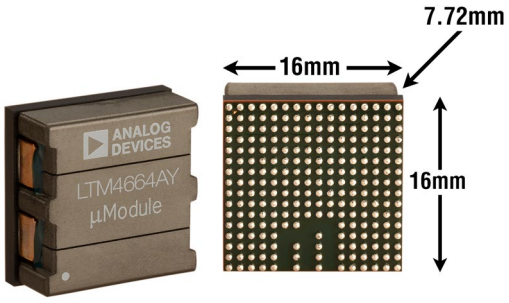
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION CAN BE 96.5% Sn/3.0% Ag/0.5% Cu OR Sn Pb EUTECTIC
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	7.41	7.72	8.03	
A1	0.45	0.50	0.55	BALL HT
A2	1.73	1.82	1.91	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		16.00		
E		16.00		
e		1.00		
F		15.00		
G		15.00		
H1	0.28	0.32	0.36	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
H3	5.28	5.40	5.52	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.25	
eee			0.10	
fff			0.35	
TOTAL NUMBER OF BALLS: 240				

BGA Z-240-0517 REV B

Rev. 0

TYPICAL APPLICATIONS



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4664	54V_{IN} Dual 25A or Single 50A µModule Regulator with PMBus Interface	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V. 16mm × 16mm × 7.72mm BGA
LTM4681	Quad 31.25A to Single 125A µModule Regulator with PMBus Interface	Quad 31.25A to Single 125A µModule Regulator with PMBus Interface
LTM4700	Dual 50A or Single 100A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 1.8V. 15mm × 22mm × 7.82mm BGA
LTM4680	Dual 30A or Single 60A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V. 16mm × 16mm × 7.72mm BGA
LTM4678	Dual 25A or Single 50A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V. 16mm × 16mm × 5.86mm BGA
LTM4686	Ultrathin Package, Dual 10A or Single 20A µModule Regulator with PMBus Interface	4.5V ≤ V_{IN} ≤ 17V, 0.5V ≤ V_{OUT} ≤ 2.75V. 11.9mm × 16mm × 1.82mm LGA
LTM4650	Dual 50A or Single 100A µModule Regulator	4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V. 16mm × 16mm × 5.01mm BGA
LTM4650A	Dual 50A or Single 100A µModule Regulator with High V_{OUT} Range	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V. 16mm × 16mm × 5.01mm BGA. 16mm × 16mm × 4.41mm LGA.
LTC®2977	Octal Digital Power Supply Manager with EEPROM	I²C/PMBus Interface, Configuration EEPROM, Fault Logging, 16-Bit ADC with ±0.25% TUE, 3.3V to 15V Operation
LTC2974	Quad Digital Power Supply Manager with EEPROM	I²C/PMBus Interface, Configuration EEPROM, Fault Logging, Per Channel Voltage, Current and Temperature Measurements

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