Quad 40V_{IN} Silent Switcher µModule Regulator with Configurable 1.2A Output Array

FEATURES

- **Four Complete Step-Down Switching Power Supplies**
- **Low Noise Silent Switcher® Architecture**
- **CISPR22 Class B Compliant**
- **CISPR25 Class 5 Compliant**
- **Wide Input Voltage Range: 3V to 40V**
- **Wide Output Voltage Range: 0.8V to 8V**
- **1.2A Continuous Output Current per Channel at 12V_{IN}, 3.3V_{OUT}, T_A = 85°C**
- **1.5A Continuous Output Current per Channel at 12V_{IN}, 3.3V_{OUT}, T_A = 60°C**
- **Multiphase or Multi-µModule Parallelable for Increased Output Current**
- Selectable Switching Frequency: 300kHz to 3MHz
- Compact Package (6.25mm × 11.25mm × 2.22mm) Surface Mount BGA

APPLICATIONS

- Automated Test Equipment
- Distributed Supply Regulation
- Industrial Supplies
- Medical Equipment

Click to view associated Video Design Idea.

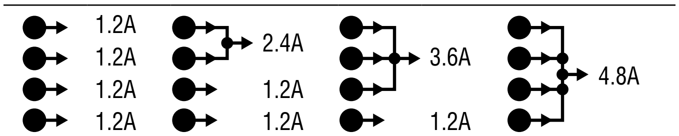
DESCRIPTION

The LTM®8051 is quad 40V_{IN}, 1.2A step-down Silent Switcher µModule® regulator. The Silent Switcher architecture minimizes EMI while delivering high efficiency at frequencies up to 3MHz. Included in the package are the controllers, power switches, inductors, and support components. Operating over a wide input voltage range, the LTM8051 supports output voltages from 0.8V to 8V, and a switching frequency range of 300kHz to 3MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design. The LTM8051 product video is available on website.

The LTM8051 is packaged in a compact (6.25mm × 11.25mm × 2.22mm) over-molded Ball Grid Array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8051 is available with SnPb (BGA) or RoHS compliant.

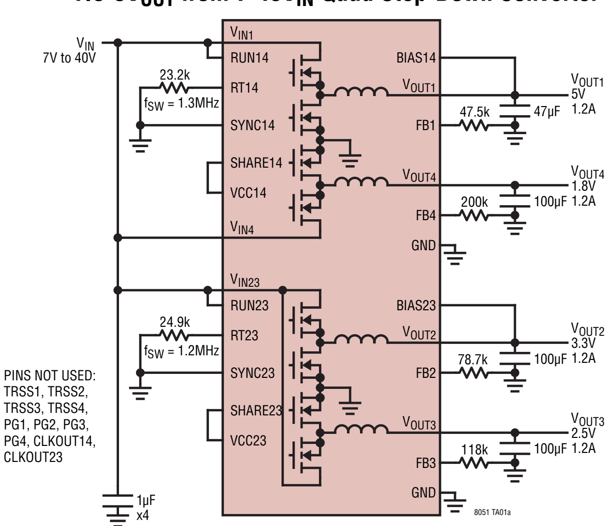
Configurable Output Array

The LTM8051 outputs can be paralleled in an array for up to 4.8A capability.

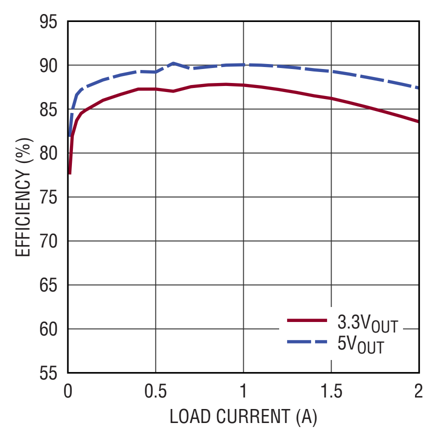


TYPICAL APPLICATION

1.8-5V_{OUT} from 7-40V_{IN} Quad Step-Down Converter



Efficiency, V_{IN} = 24V, BIAS = 5V



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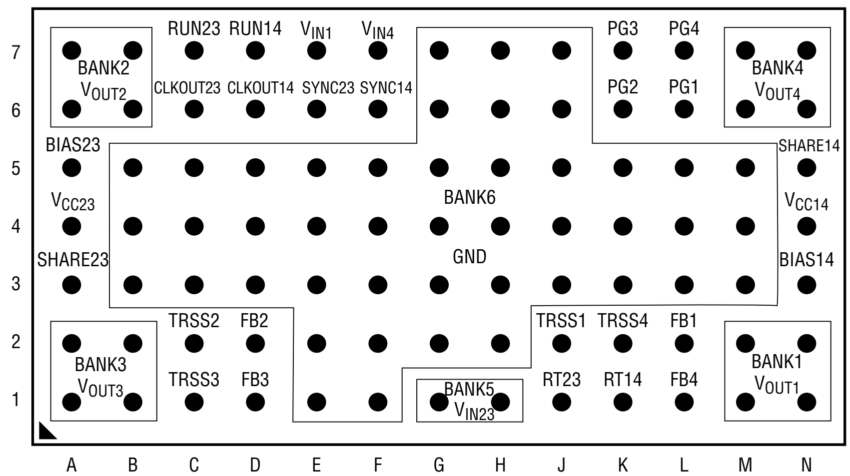
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{INn}, RUN*n*, PG*n* 42V
V_{OUTn}, BIAS*n* 10V
FB*n*, TRSS*n*, SHARE*n* , RT_n, VCC_n 4V
SYNC*n* 6V
Maximum Internal Temperature (Note 2) .... 125°C
Storage Temperature .... –55°C to 125°C
Peak Solder Reflow Package Body Temperature .. 260°C

PIN CONFIGURATION

TOP VIEW



BGA PACKAGE
91-LEAD (11.25mm × 6.25mm × 2.22mm)

T_{JMAX} = 125°C, θ_{JA} = 16°C/W, θ_{JCtop} = 11.4°C/W,
θ_{JCbot} = 3.5°C/W, WEIGHT = 0.42g
θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM8051EY#PBF	SAC305 (RoHS)	LTM8051Y	e1	BGA	3	–40°C to 125°C
LTM8051IY#PBF	SAC305 (RoHS)	LTM8051Y	e1	BGA	3	–40°C to 125°C
LTM8051IY	SnPb (63/37)	LTM8051Y	e0	BGA	3	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating internal temperature range, otherwise specifications are at T_A = 25°C. V_{INn} = 12V, RUN*n* = 2V unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{IN1} Input Voltage Minimum V_{IN23} Input Voltage Minimum V_{IN4} Input Voltage	 V_{IN1} = 3V	● ● ●			3.0 3.0 2.0	V V V
Output DC Voltage	FB*n* open FB*n* = 27.4kΩ			0.8 8		V V
Maximum Output DC Current	(Note 3)				2.5	A
Quiescent Current into V_{INn}	RUN*n* = 0 BIAS*n* = 5V, SYNC*n* = 0V, No load BIAS*n* = 5V, SYNC*n* = 3.3V, No load			2 60 10	4	µA µA mA
Current into $BIAS_n$	RUN*n* = 0, BIASn = 5V BIAS*n* = 5V, SYNCn = 3.3V, No load			 7	1	µA mA
Line Regulation	5V < V_{INn} < 40V			0.1		%
Load Regulation	12V_{INn}, 0.1A < I_{OUTn} <2A			0.2		%
Output RMS Ripple	3.3V_{OUTn}			10		mV
FB*n* Voltage		 ●	792 784	800 800	808 816	mV mV
Current out of FB*n*	V_{OUTn} = 1V, FB*n* = 0V, RUN*n* = 0V			4		µA
Minimum BIAS*n* for Proper Operation					3.2	V
Switching Frequency	RT*n* = 113kΩ, V_{INn} = 6V RT*n* = 30.9kΩ, V_{INn} = 6V RT*n* = 7.15kΩ, V_{INn} = 6V			300 1 3		KHz MHz MHz
RUN*n* Threshold				0.74		V
RUN*n* Input Current	RUN*n* = 0V				1	µA
PG*n* Threshold at FB*n*	Lower Threshold Upper Threshold			740 860		mV mV
PG*n* Output Sink Current	PG*n* = 0.1V		100			µA
CLKOUT*n* V_{OL}	V_{INn} = 6V			0		V
CLKOUT*n* V_{OH}	V_{INn} = 6V			3.3		V
SYNC*n* Input High Threshold			1.5			V
SYNC*n* Input Low Threshold					0.8	V
SYNC*n* Threshold to Enable Spread Spectrum			2.8		4	V
SYNC*n* Current	SYNC*n* = 6V, V_{INn} = 6V			65		µA
TRSS*n* Source Current	TRSS*n* = 0V			2		µA
TRSS*n* Pull-Down Resistance	Fault Condition, TRSS*n* = 0.1V			230		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

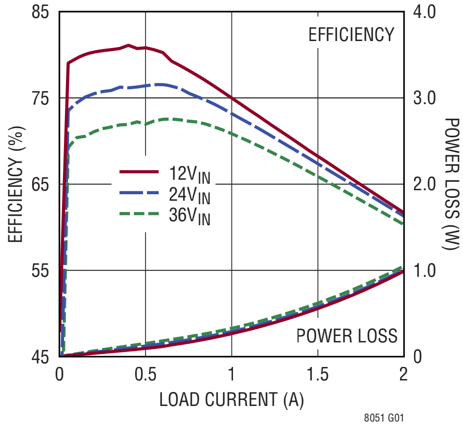
Note 2: The LTM8051E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8051I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The maximum current out of either channel may be limited by the internal temperature of the LTM8051. See output current derating curves for different V_{IN}, V_{OUT}, and T_A.

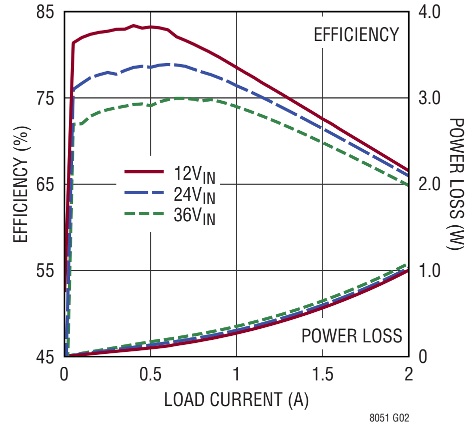
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, operating per Table 1,unless otherwise noted.

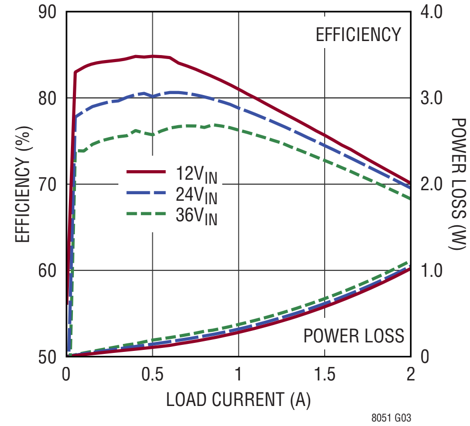
Efficiency, V_{OUT} = 0.8V
BIAS = 5V



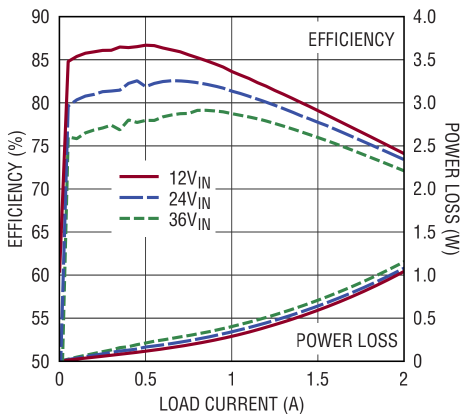
Efficiency, V_{OUT} = 1.0V
BIAS = 5V, Burst Mode



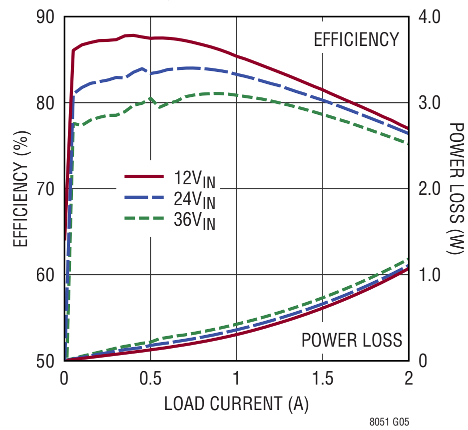
Efficiency, V_{OUT} = 1.2V
BIAS = 5V, Burst Mode



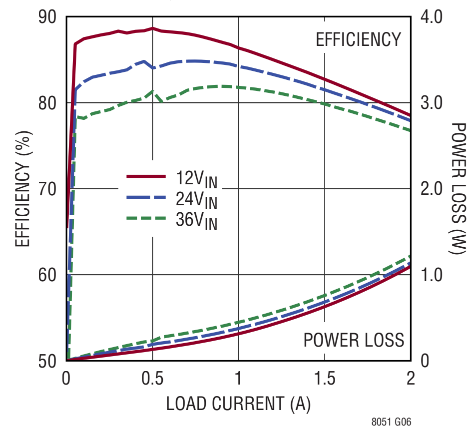
Efficiency, V_{OUT} = 1.5V
BIAS = 5V, Burst Mode



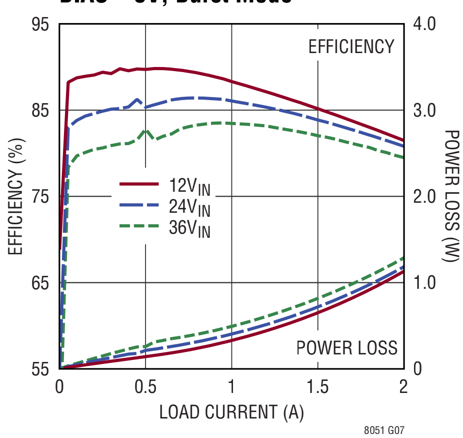
Efficiency, V_{OUT} = 1.8V
BIAS = 5V, Burst Mode



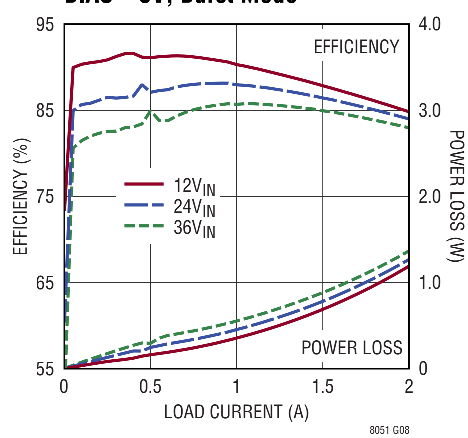
Efficiency, V_{OUT} = 2.0V
BIAS = 5V, Burst Mode



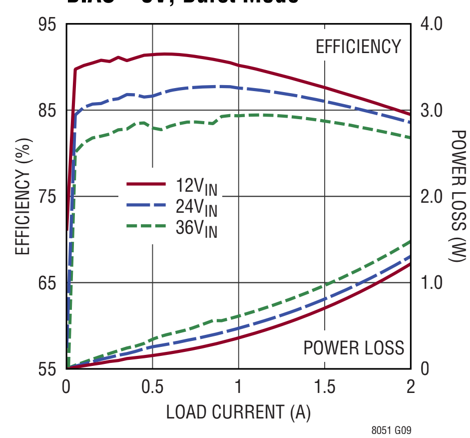
Efficiency, V_{OUT} = 2.5V
BIAS = 5V, Burst Mode



Efficiency, V_{OUT} = 3.3V
BIAS = 5V, Burst Mode



Efficiency, V_{OUT} = 3.3V, 2MHz
BIAS = 5V, Burst Mode



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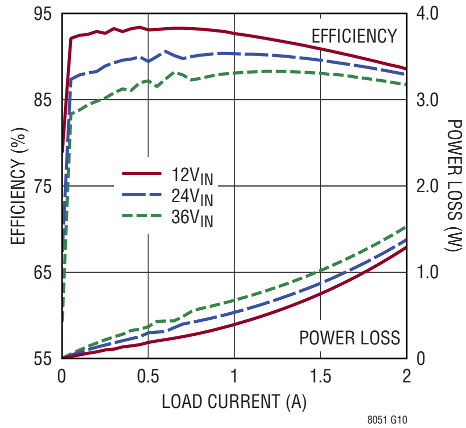
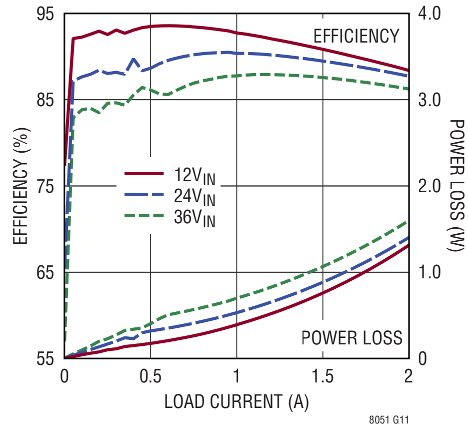
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, operating per Table 1,unless otherwise noted.

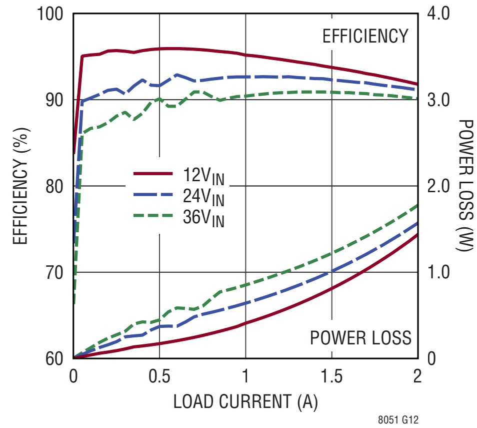
Efficiency, V_{OUT} = 5.0V
BIAS = 5V, Burst Mode



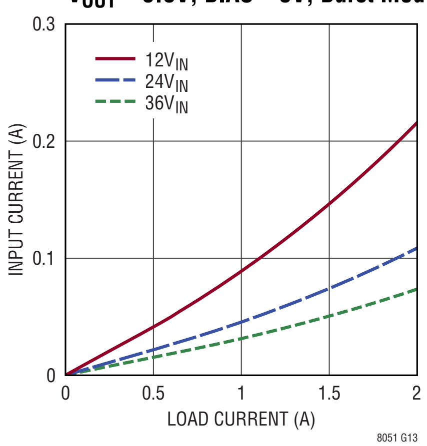
Efficiency, V_{OUT} = 5.0V, 2MHz
BIAS = 5V, Burst Mode



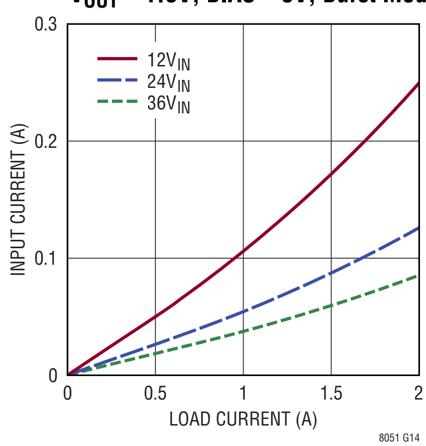
Efficiency, V_{OUT} = 8.0V
BIAS = 5V, Burst Mode



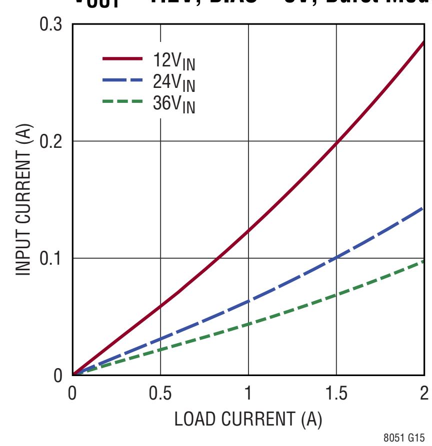
Input vs Load Current
V_{OUT} = 0.8V, BIAS = 5V, Burst Mode



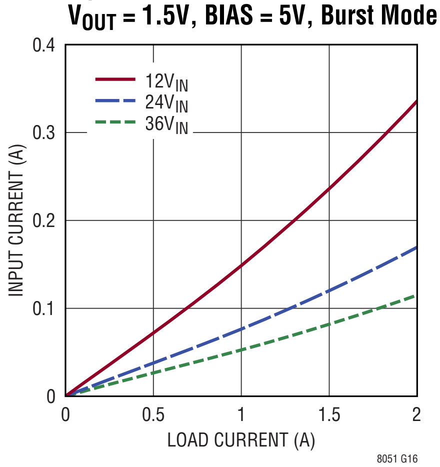
Input vs Load Current
V_{OUT} = 1.0V, BIAS = 5V, Burst Mode



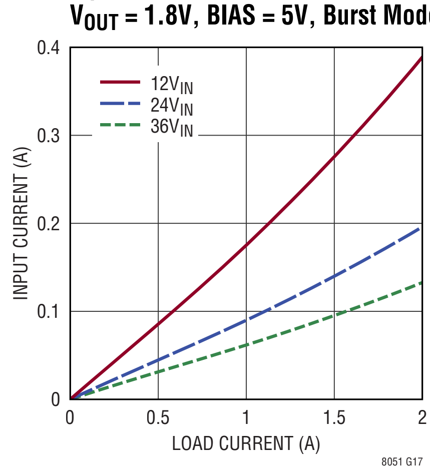
Input vs Load Current
V_{OUT} = 1.2V, BIAS = 5V, Burst Mode



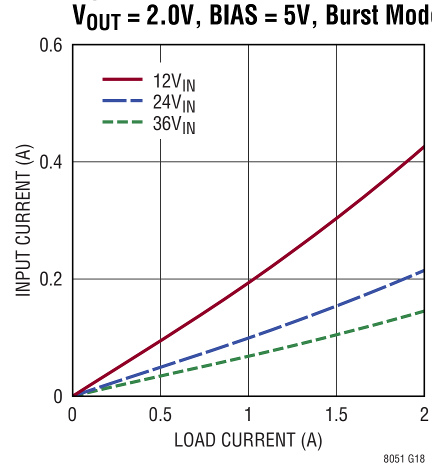
Input vs Load Current
V_{OUT} = 1.5V, BIAS = 5V, Burst Mode



Input vs Load Current
V_{OUT} = 1.8V, BIAS = 5V, Burst Mode



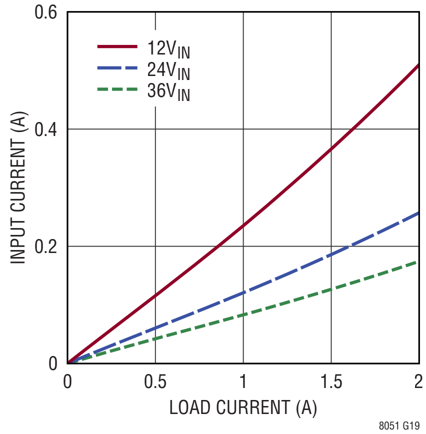
Input vs Load Current
V_{OUT} = 2.0V, BIAS = 5V, Burst Mode



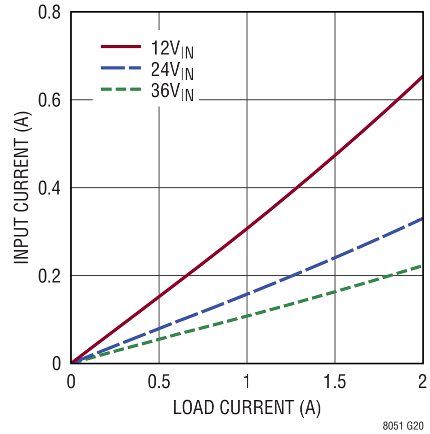
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, operating per Table 1,unless otherwise noted.

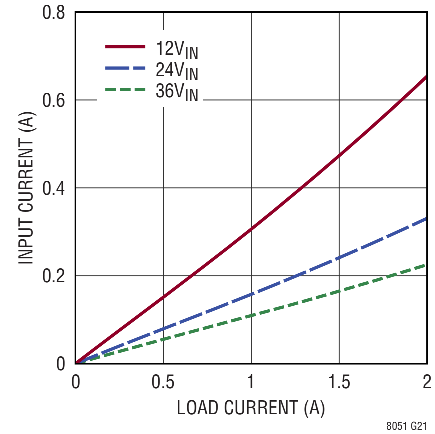
Input vs Load Current
V_{OUT} = 2.5V, BIAS = 5V, Burst Mode



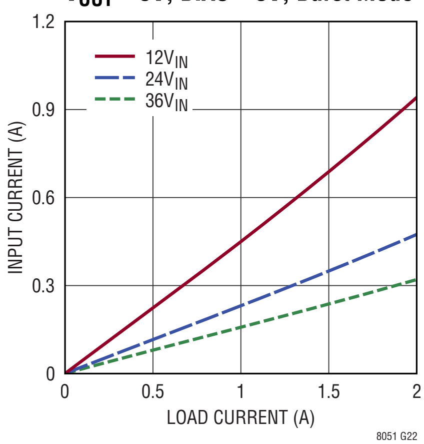
Input vs Load Current
V_{OUT} = 3.3V, BIAS = 5V, Burst Mode



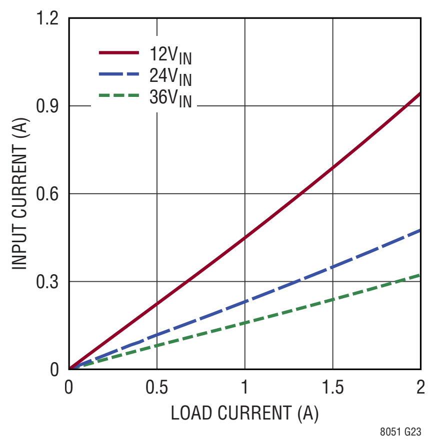
Input vs Load Current
V_{OUT} = 3.3V, 2MHz, BIAS = 5V, Burst Mode



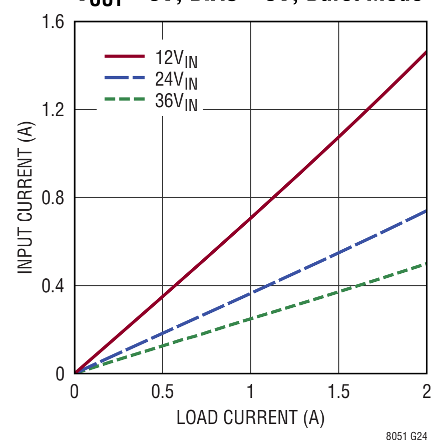
Input vs Load Current
V_{OUT} = 5V, BIAS = 5V, Burst Mode



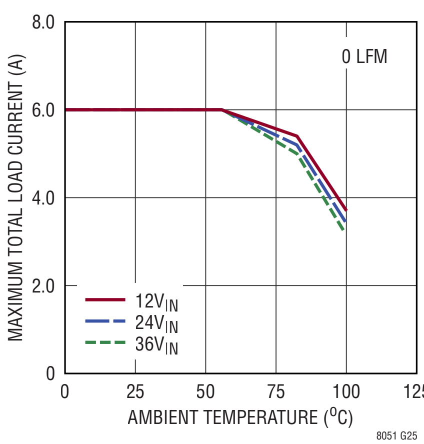
Input vs Load Current
V_{OUT} = 5V, 2MHz, BIAS = 5V, Burst Mode



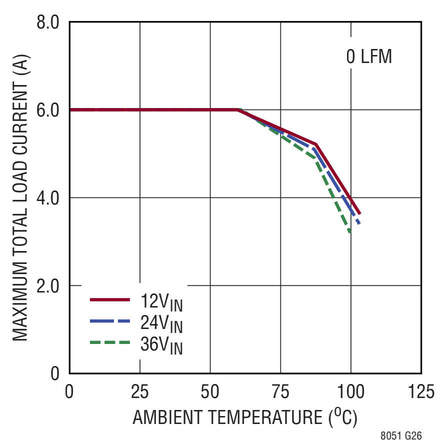
Input vs Load Current
V_{OUT} = 8V, BIAS = 5V, Burst Mode



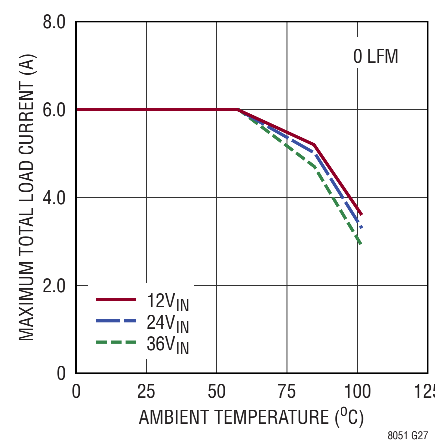
Derating, V_{OUT} = 0.8V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



Derating, V_{OUT} = 1V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



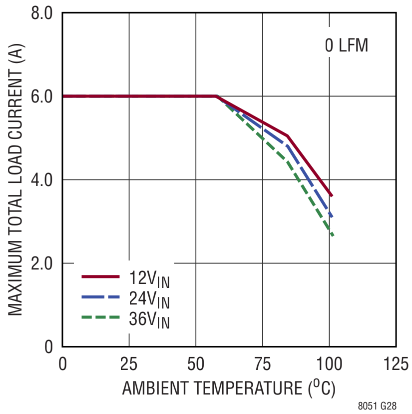
Derating, V_{OUT} = 1.2V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



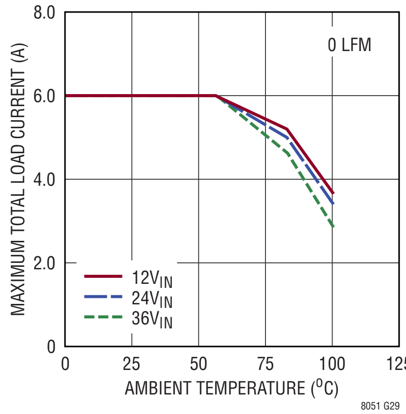
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, operating per Table 1, unless otherwise noted.

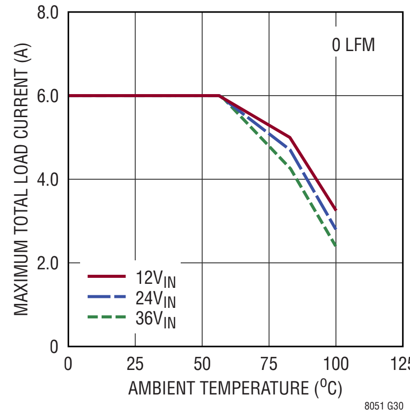
Derating, V_{OUT} = 1.5V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



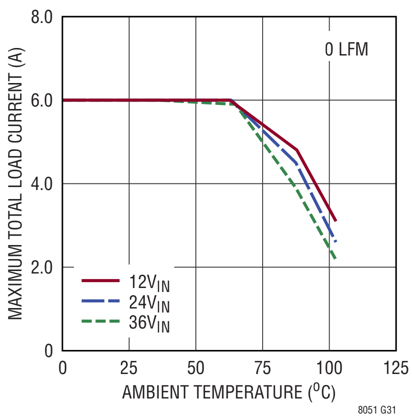
Derating, V_{OUT} = 1.8V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



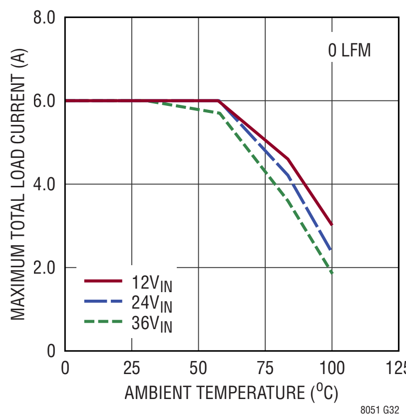
Derating, V_{OUT} = 2V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



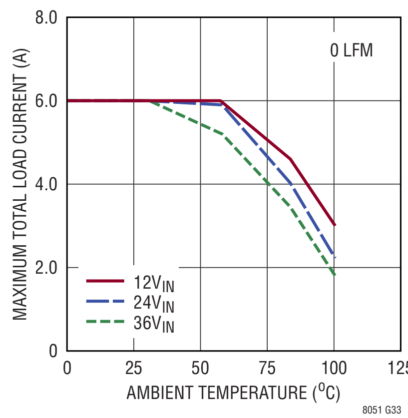
Derating, V_{OUT} = 2.5V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



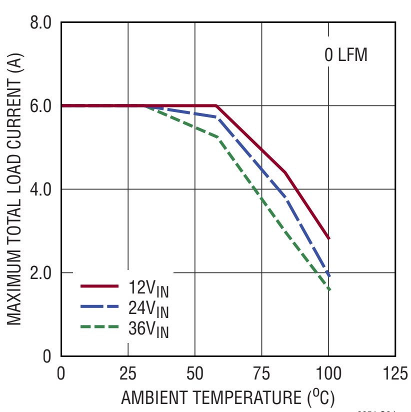
Derating, V_{OUT} = 3.3V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



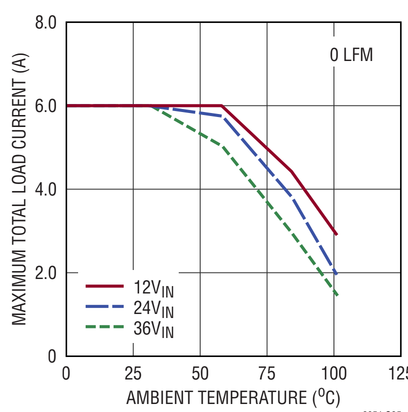
Derating, V_{OUT} = 3.3V, F_{SW} = 2MHz
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



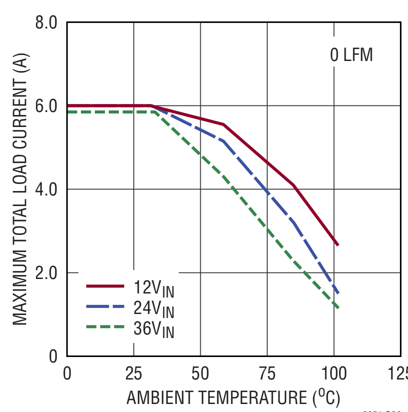
Derating, V_{OUT} = 5V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load



Derating, V_{OUT} = 5V, F_{SW} = 2MHz
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load

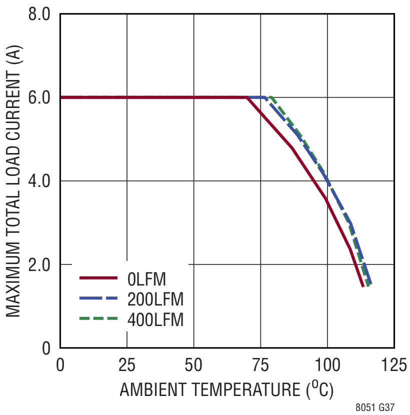


Derating, V_{OUT} = 8V
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode
All Channels At Same Load

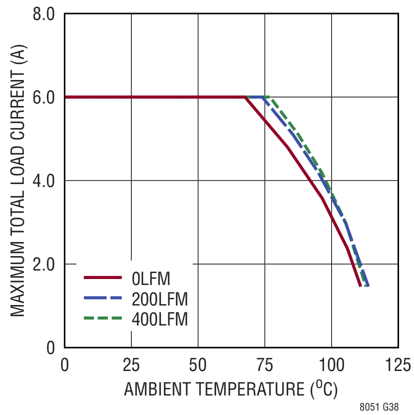


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, operating per Table 1, unless otherwise noted.

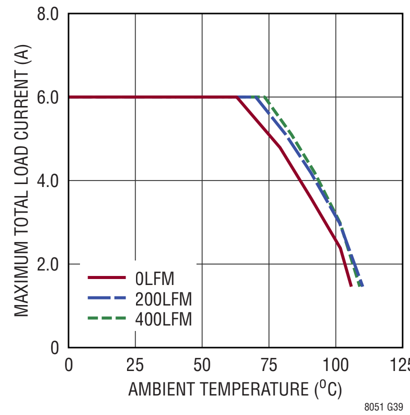
Derating with Airflow, $12V_{IN}$ to $1.5V_{OUT}$, T_J = 120°C BIAS = 5V, DC2860A Demo Board Forced Continuous Mode All Channels At Same Load



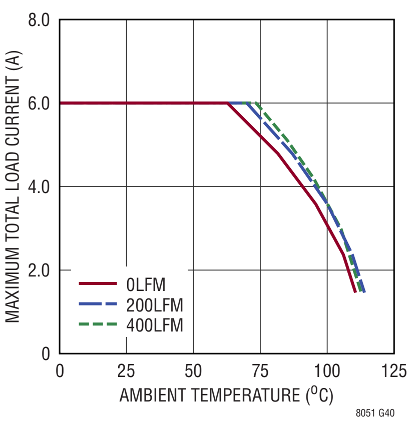
Derating with Airflow, $24V_{IN}$ to $1.5V_{OUT}$, T_J = 120°C BIAS = 5V, DC2860A Demo Board Forced Continuous Mode All Channels At Same Load



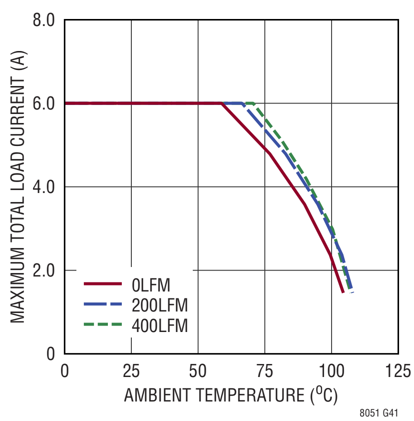
Derating with Airflow, $36V_{IN}$ to $1.5V_{OUT}$, T_J = 120°C BIAS = 5V, DC2860A Demo Board Forced Continuous Mode All Channels At Same Load



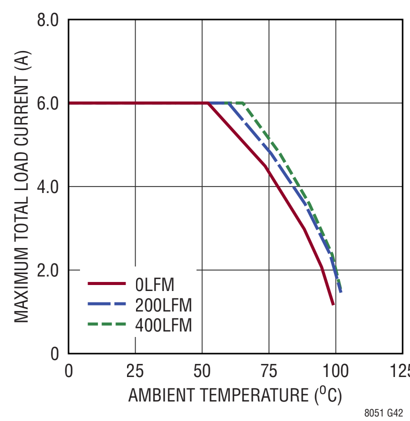
Derating with Airflow, $12V_{IN}$ to $3.3V_{OUT}$, T_J = 120°C BIAS = 5V, DC2860A Demo Board Forced Continuous Mode All Channels At Same Load



Derating with Airflow, $24V_{IN}$ to $3.3V_{OUT}$, T_J = 120°C BIAS = 5V, DC2860A Demo Board Forced Continuous Mode All Channels At Same Load



Derating with Airflow, $36V_{IN}$ to $3.3V_{OUT}$, T_J = 120°C BIAS = 5V, DC2860A Demo Board Forced Continuous Mode All Channels At Same Load

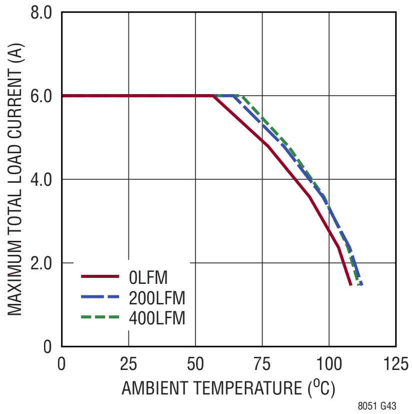


Rev. A

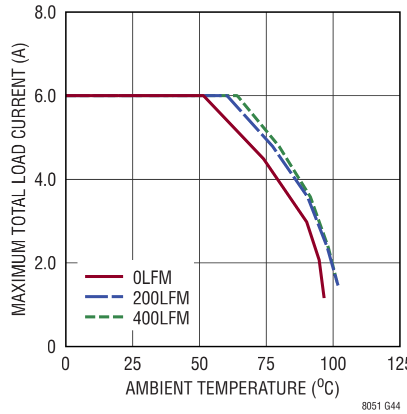
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, operating per Table 1,unless otherwise noted.

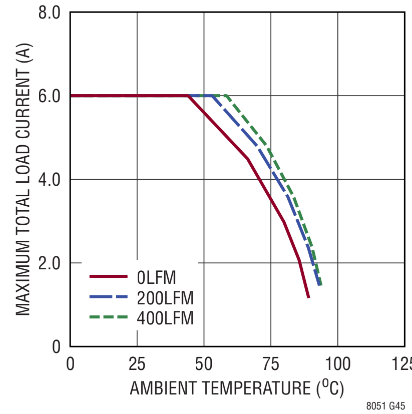
Derating with Airflow,
$12V_{IN}$ to $5V_{OUT}$, T_J =120°C
BIAS = 5V, DC2860A Demo Board
Forced Continuous Mode
All Channels At Same Load



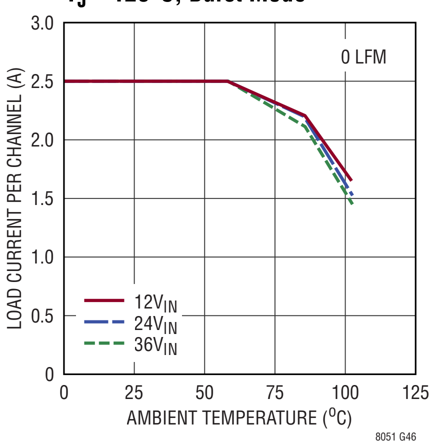
Derating with Airflow,
$24V_{IN}$ to $5V_{OUT}$, T_J =120°C
BIAS = 5V, DC2860A Demo Board
Forced Continuous Mode
All Channels At Same Load



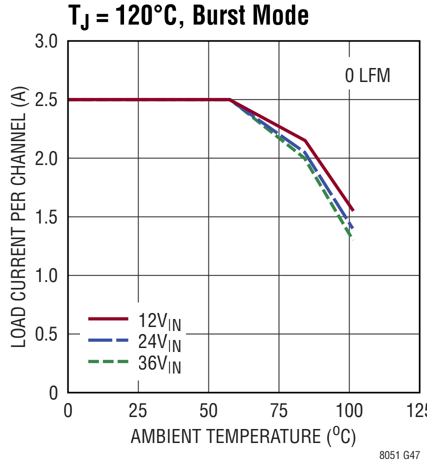
Derating with Airflow,
$36V_{IN}$ to $5V_{OUT}$, T_J =120°C
BIAS = 5V, DC2860A Demo Board
Forced Continuous Mode
All Channels At Same Load



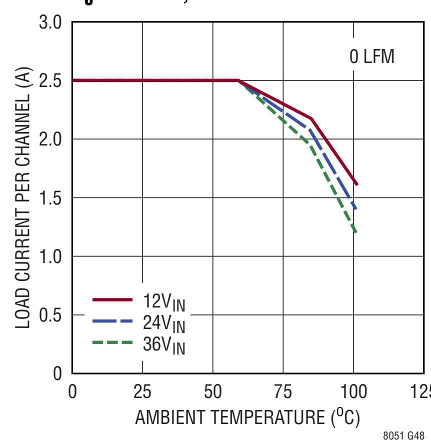
Single Channel Derating, V_{OUT} = 1.5V
CH1 ON, CH2/CH3/CH4 OFF
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode



Single Channel Derating, V_{OUT} = 3.3V
CH1 ON, CH2/CH3/CH4 OFF
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode

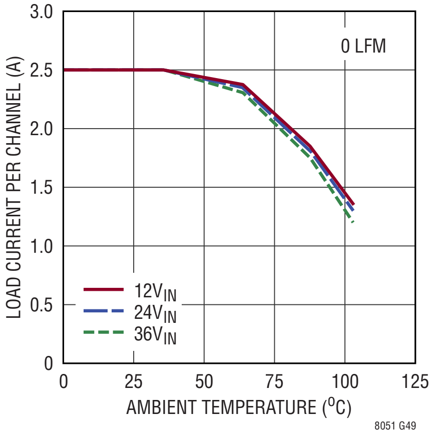


Single Channel Derating, V_{OUT} = 5V
CH1 ON, CH2/CH3/CH4 OFF
BIAS = 5V, DC2860A Demo Board
T_J = 120°C, Burst Mode

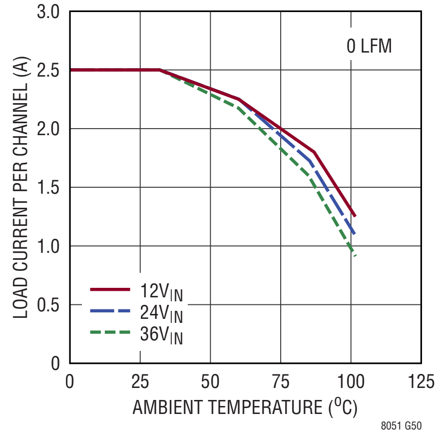


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, operating per Table 1,unless otherwise noted.

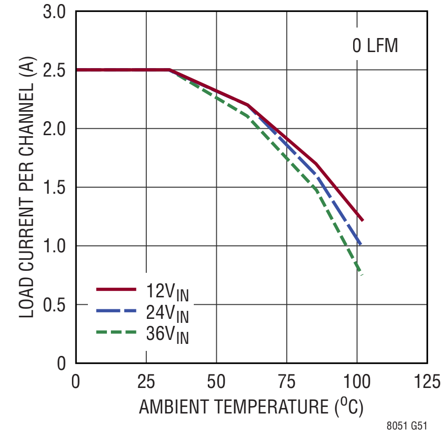
Dual Channel Derating, V_{OUT} = 1.5V CH1/CH2 ON, CH3/CH4 OFF BIAS = 5V, DC2860A Demo Board T_J = 120°C, Burst Mode



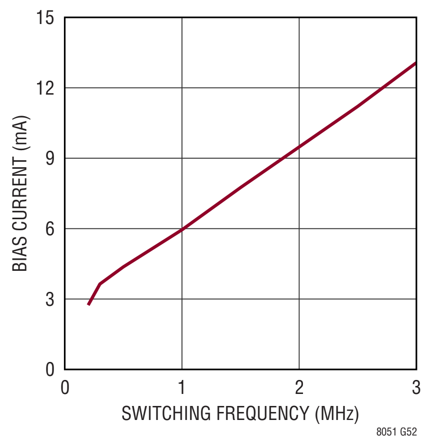
Dual Channel Derating, V_{OUT} = 3.3V CH1/CH2 ON, CH3/CH4 OFF BIAS = 5V, DC2860A Demo Board T_J = 120°C, Burst Mode



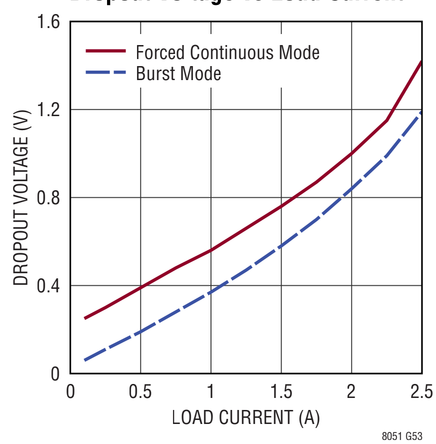
Dual Channel Derating, V_{OUT} = 5V CH1/CH2 ON, CH3/CH4 OFF BIAS = 5V, DC2860A Demo Board T_J = 120°C, Burst Mode



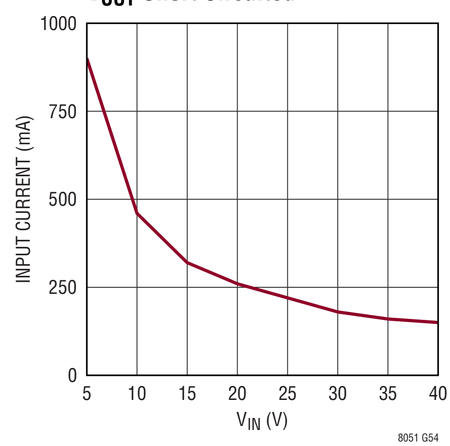
BIAS Current vs Frequency $12V_{IN}$ to 3.3 V_{OUT} Forced Continuous Mode



Dropout Voltage vs Load Current



Input Current vs V_{IN} V_{OUT} Short Circuited

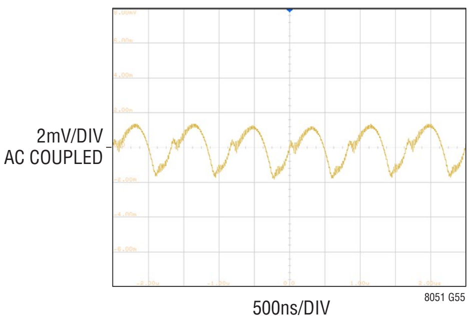


Rev. A

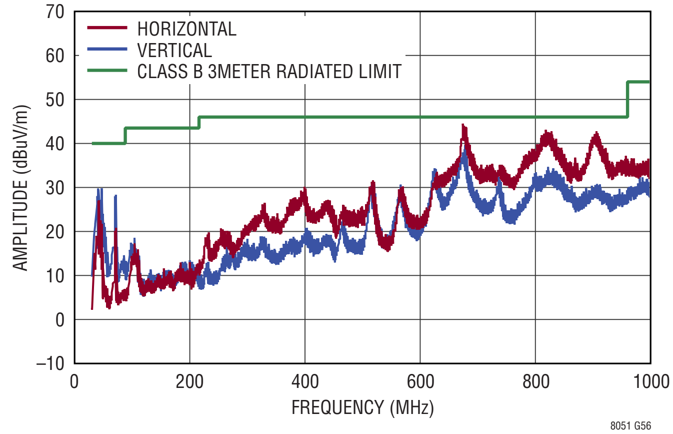
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, operating per Table 1,unless otherwise noted.

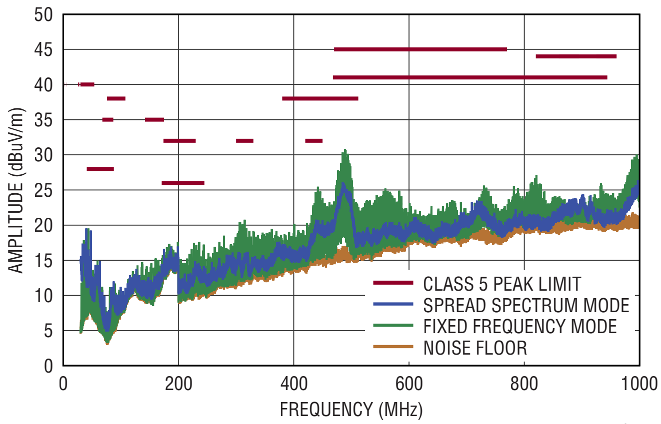
Output Voltage Ripple
DC2860A Demo Board
V_{IN} = 12V, V_{OUT} = 3.3V



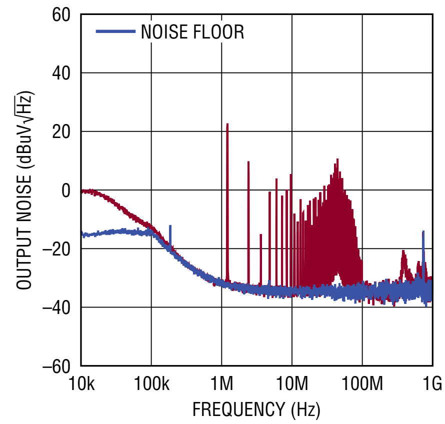
CISPR22 Class B Emissions DC2860A Demo Board
V_{INn} = 12V, I_{OUTn} = 1.2A, 5V_{OUT1}, 3.3V_{OUT2}, 2.5V_{OUT3}, 1.8V_{OUT4}, Spread Spectrum On, No EMI Filter



CISPR25 Radiated Emission with Class 5 Peak Limit
DC2860A Demo Board
V_{IN} = 14V, V_{OUT} = 3.3V, Four Channels Paralleled, I_{OUT} = 4.8A, f_{SW} = 2MHz



Output Noise Spectral Density
DC2860A Demo Board
V_{IN} = 12V, I_{OUT} = 1.2A, V_{OUT} = 3.3V, f_{SW} = 1.2MHz



10kHz TO 100kHz, RBW = 100Hz
100kHz TO 1MHz, RBW = 1kHz
1MHz TO 10MHz, RBW = 10kHz
10MHz TO 100MHz, RBW = 100kHz
100MHz TO 1GHz, RBW = 1MHz

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PIN FUNCTIONS

V_{IN1} (Pin E7): Input power for the channel 1 regulator. The V_{IN1} powers the internal control circuitry for channel 1/4 and is monitored by undervoltage lockout circuitry. The V_{IN1} voltage must be greater than 3.0V for either channel1/4 of the LTM8051 to operate. Decouple V_{IN1} to ground with an external, low ESR capacitor. See Table 1 for recommended values.

V_{IN4} (Pin F7): Input power for the channel 4 regulator. Decouple V_{IN4} to ground with an external, low ESR capacitor. See Table 1 for recommended values.

V_{IN23} (Bank 5): Input power for the channel 2/3 regulator. The V_{IN23} bank powers the internal control circuitry for both channel 2/3 and is monitored by undervoltage lockout circuitry. The V_{IN23} voltage must be greater than 3.0V for either channel2/3 of the LTM8051 to operate. Decouple V_{IN23} to ground with an external, low ESR capacitor. See Table 1 for recommended values.

$V_{OUT1/2/3/4}$ (Bank 1/2/3/4): Power Output for channel 1/2/3/4, respectively. Apply the output filter capacitor and the output load between these pins and GND pins.

GND (Bank 6): Tie these GND pins to a local ground plane below the LTM8051 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8051 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (RFB) to this net.

BIAS14/23 (Pin N3/A5): The internal regulator will draw current from BIAS*n* instead of V_{IN1} or V_{IN23} when BIAS*n* is tied to a voltage higher than 3.2V. For output voltages of 3.3V and above this pin should be tied to V_{OUTn}. If this pin is tied to a supply other than V_{OUTn} use a local bypass capacitor on this pin.

CLKOUT14/23 (Pin D6/C6): Synchronization output. When SYNC14/23>2.8V, the CLKOUT14/23 pin provides a waveform about 90 degrees out-of-phase with Channel 1/2 respectively. This allows synchronization with other regulators with up to four phases. When an external clock is applied to the SYNC pin, the CLKOUT pin will output a waveform with about the same phase, duty cycle, and frequency as the SYNC waveform. In Burst Mode operation, the CLKOUT pin will be internally grounded. Float this pin if the CLKOUT function is not used. Do not drive this pin.

FB1/2/3/4 (Pin L2/D2/D1/L1): The LTM8051 regulates the FB*n* pins to 800mV. Connect the feedback resistor to this pin to set the output voltage.

PG1/2/3/4 (Pin L6/K6/K7/L7): The PG*n* pin is the open-drain output of an internal comparator. PG*n* remains low until the FB*n* pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG*n* is pulled low during V_{INn} UVLO, Thermal Shutdown, or when the RUN*n* pin is low.

RT14/23 (Pin K1/J1): Connect a resistor between RT*n* and ground to set the switching frequency. Do not drive this pin.

RUN14/23 (Pin D7/C7): The corresponding channel of the LTM8051 is shutdown when this pin is low and active when this pin is high. Tie to V_{INn} if shutdown feature is not used. An external resistor divider from V_{INn} can be used to program a V_{INn} threshold below which the corresponding channel of the LTM8051 will shut down. Do not float this pin.

SHARE14/23 (Pin N5/A3): Sharing Control. Float SHARE14 when V_{OUT1} and V_{OUT4} are load sharing. Connect SHARE14 to V_{CC14} if V_{OUT1} and V_{OUT4} are independent. Float SHARE23 when V_{OUT2} and V_{OUT3} are load sharing. Connect SHARE23 to V_{CC23} if V_{OUT2} and V_{OUT3} are independent. Connect SHARE14 and SHARE23 if parallel all four channels. Connect this pin to the SHARE*n* pin of another LTM8051 when load sharing with another LTM8051.

$V_{CC14/23}$ (Pin N4/A4): Internal Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. V_{CCn} current will be supplied from

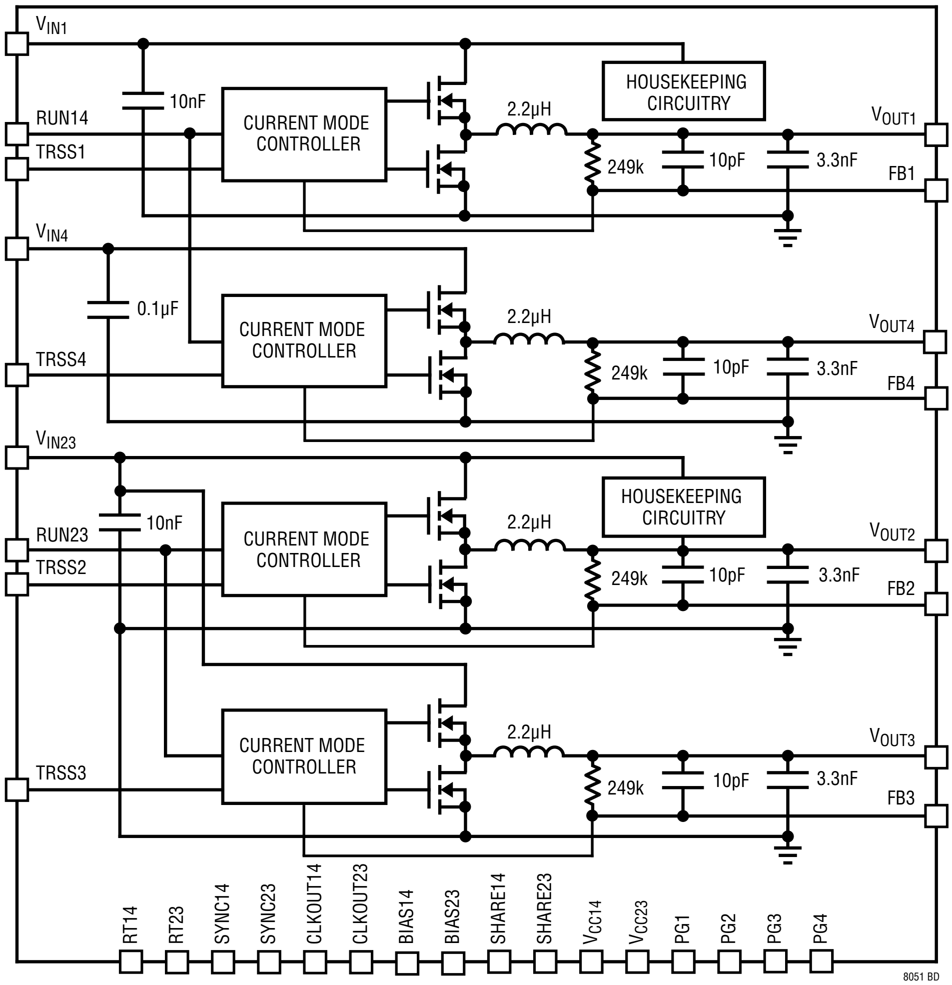
PIN FUNCTIONS

BIAS*n* if V_{BIASn} > 3.2V, otherwise current will be drawn from V_{INn}. If V_{OUT1} and V_{OUT4} are load sharing, leave V_{CC14} floating. If V_{OUT2} and V_{OUT3} are load sharing, leave V_{CC23} floating. If V_{OUT1} and V_{OUT4} are independent voltages, connect SHARE14 to V_{CC14}; if V_{OUT2} and V_{OUT3} are independent voltages, connect SHARE23 to V_{CC23}, otherwise the LTM8051 will not regulate properly. Do not load the V_{CCn} with external circuitry.

TRSS1/2/3/4 (Pin J2/C2/C1/K2): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during startup. A TRSS*n* voltage below 0.8V forces the LTM8051 to regulate the FB*n* pin to equal the TRSS*n* pin voltage. When TRSS*n* is above 0.8V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

SYNC14/23 (Pin F6/E6): External clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads; this will also disable the CLKOUT function. Apply a DC voltage between 2.8V and 4.2V for forced continuous mode operation with spread spectrum modulation. Float the SYNC*n* pin for forced continuous mode operation without spread spectrum modulation. Apply a clock source to the SYNC*n* pin for synchronization to an external frequency. The LTM8051 will be in forced continuous mode when an external frequency is applied.

BLOCK DIAGRAM



OPERATION

The LTM8051 is a quad standalone non-isolated step-down switching DC/DC power supply that can deliver a peak current of up to 2.5A per channel. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 8V. The input voltage range for V_{IN1}, V_{IN23} is 3V to 40V, while the input voltage range for V_{IN4} is 2V to 40V.

Given that the LTM8051 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. See simplified Block Diagram.

The LTM8051 contains current mode controllers, power switching elements, power inductors and a modest amount of input and output capacitance. The LTM8051 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT*n* pin to GND.

Internal regulators provide power to the control circuitries. Bias regulators normally draw power from the V_{INn} pin, but if the BIAS*n* pin is connected to an external voltage higher than 3.2V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency. Tie BIAS*n* to GND if it is not used.

To enhance efficiency, the LTM8051 automatically switches to Burst Mode operation in light or no load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to just a few µA.

The TRSS*n* node acts as an auxiliary input to the error amplifier. The voltage at FB*n* servos to the TRSS*n* voltage until TRSS*n* goes above 0.8V. Soft-start is implemented by generating a voltage ramp at the TRSS*n* pin using an external capacitor which is charged by an internal 2µA constant current. Alternatively, driving the TRSS*n* pin with a signal source or resistive network provides a tracking function. Do not drive the TRSS*n* pin with a low impedance voltage source. See the Applications Information section for more details.

The LTM8051 contains power good comparators which trip when the FB*n* pin is at about 92% to 108% of its regulated value. The PG*n* output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG*n* pin high.

The LTM8051 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

Set Output Voltage

The output voltage is programmed with a FB resistor as shown in the Figure below. Choose the resistor value according to:

$$R_{FB} = \frac{249k\Omega}{\frac{V_{OUT}}{0.8V} - 1}$$

1% resistor is recommended to maintain output voltage accuracy.

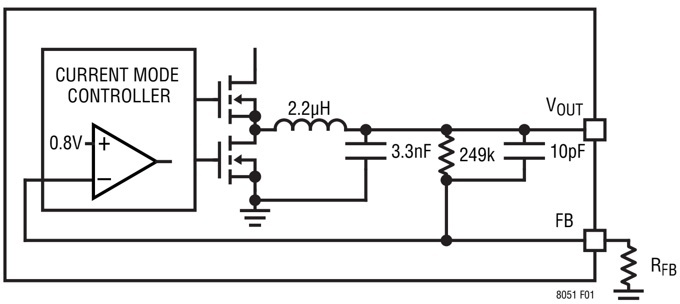


Figure 1. Set Output Voltage with a FB Resistor

For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{FB} and R_T values.
3. Connect BIAS as indicated.

When using the LTM8051 with different output voltages, the higher frequency recommended by Table 1 will usually result in the best operation. While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8051 should be allowed to switch is given in Table 1 in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

APPLICATIONS INFORMATION

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8051's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8051 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8051. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8051 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT} (V)	R_{FB} (kΩ)	C_{IN}[2]	C_{OUT}	BIAS	C_{FF}	f_{SW} (kHz)	R_T (kΩ)	MAX f_{SW} (kHz)	MIN_{RT} (kΩ)
3V to 40V[1]	0.8	Open	1µF 50V X5R 0805	2 x 100uF 4V X5R 0805	3.2V to 10V	47pF	450	75	1200	24.9
3V to 40V[1]	1	1000	1µF 50V X5R 0805	2 x 100uF 4V X5R 0805	3.2V to 10V	33pF	550	60.4	1400	21
3V to 40V[1]	1.2	499	1µF 50V X5R 0805	2 x 100uF 4V X5R 0805	3.2V to 10V	22pF	650	49.9	1400	21
3V to 40V[1]	1.5	287	1µF 50V X5R 0805	2 x 100uF 4V X5R 0805	3.2V to 10V	22pF	800	40.2	1400	21
3.2V to 40V[1]	1.8	200	1µF 50V X5R 0805	100uF 4V X5R 0805	3.2V to 10V	-	800	40.2	1800	15
3.5V to 40V[1]	2	165	1µF 50V X5R 0805	100uF 4V X5R 0805	3.2V to 10V	-	900	34.8	1800	15
4.2V to 40V[1]	2.5	118	1µF 50V X5R 0805	100uF 4V X5R 0805	3.2V to 10V	-	1100	27.4	2000	13.3
5V to 40V[1]	3.3	78.7	1µF 50V X5R 0805	100uF 4V X5R 0805	3.2V to 10V	-	1200	24.9	2800	8.06
7V to 40V[1]	5	47.5	1µF 50V X5R 0805	47uF 6.3V X5R 0805	3.2V to 10V	-	1300	22.1	3000	7.15
10.5V to 40V[1]	8	27.4	1µF 50V X5R 0805	22uF 10V X5R 0805	3.2V to 10V	-	1700	16.5	3000	7.15

Note 1: The LTM8051 may be capable of the operating at lower input voltages but may skip switching cycles.

Note 2: A bulk input capacitor is required.

APPLICATIONS INFORMATION

Frequency Selection

The LTM8051 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies. The resistors in the table are standard 1% E96 values.

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. When using the LTM8051 with different output voltages, the higher frequency recommended by Table 1 will usually result in the best operation. System level or other considerations, however, may necessitate another operating frequency. While the LTM8051 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8051 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Table 2. Switching Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	113
0.4	86.6
0.5	68.1
0.6	54.9
0.7	46.4
0.8	40.2
0.9	34.8
1.0	30.9
1.2	24.9
1.4	21.0
1.6	17.8
1.8	15.0
2.0	13.3
2.2	11.5
2.4	10.2
2.6	9.09
2.8	8.06
3.0	7.15

BIAS*n* Pin Considerations

The BIAS*n* pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 3.2V. If the output voltage is programmed to 3.2V or higher, BIAS*n* may be simply tied to V_{OUTn}. If V_{OUTn} is less than 3.2V, BIAS*n* can be tied to V_{INn} or some other voltage source. If the BIAS*n* pin voltage is too high, the efficiency of the LTM8051 may suffer. The optimum BIAS*n* voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency. In all cases, ensure that the maximum voltage at the BIAS*n* pin is less than 10V. If BIAS*n* power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin. A 1µF ceramic capacitor works well. The BIAS*n* pin may also be tied to GND at the cost of a small degradation in efficiency.

Maximum Load

The maximum practical continuous load that the LTM8051 can drive per channel, while rated at 1.2A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8051 in the case of overload or short-circuit. The internal temperature of the LTM8051 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat sinking capability of the system. For example, if V_{OUT1} of LTM8051 is configured to regulate at 1V, and the other 3 channels are turned off, V_{OUT1} may continuously deliver 3A from $24V_{IN}$ if the ambient temperature is controlled to less than 60°C. This is quite a bit higher than the 1.2A continuous rating. Please see graphs in the Typical Performance Characteristics section. Similarly, if all 4 channels of the LTM8051 are delivering $8V_{OUT}$ and the ambient temperature is 100°C, each channel will deliver at most 0.6A from $24V_{IN}$, which is less than the 1.2A continuous rating.

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APPLICATIONS INFORMATION

Power Derating

The $12V_{IN}$, $24V_{IN}$ and $36V_{IN}$ power loss curves can be used in coordination with the load current derating curves for calculating an approximate θ_{JA} thermal resistance for the LTM8051 with airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.35 to 1.4 multiplicative factor at 125°C. These factors come from the fact that the power loss of the regulator increases about 45% from 25°C to 150°C, thus a 45% spread over 125°C delta equates to ~0.35%/°C loss increase. A 125°C maximum junction minus 25°C room temperature equates to a 100°C increase. This 100°C increase multiplied by 0.35%/°C equals a 35% power loss increase at the 125°C junction, thus the 1.35 multiplier.

The derating curves are plotted with four V_{OUTn} at the same operating condition starting at 6A of total load current and low ambient temperature. The derating curves with airflow are measured at output voltages of 1.5V, 3.3V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal FEA modeling.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The derived thermal resistances in Tables 3 through 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the power loss curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with two-ounce copper (70µm) for all the layers.

Table 3. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Graph 37-39	12, 24, 36	Graph 04	0	None	16
Graph 37-39	12, 24, 36	Graph 04	200	None	13.5
Graph 37-39	12, 24, 36	Graph 04	400	None	12.5

Table 4. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Graph 40-42	12, 24, 36	Graph 08	0	None	16
Graph 40-42	12, 24, 36	Graph 08	200	None	13.5
Graph 40-42	12, 24, 36	Graph 08	400	None	12.5

Table 5. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Graph 43-45	12, 24, 36	Graph 10	0	None	16
Graph 43-45	12, 24, 36	Graph 10	200	None	13.5
Graph 43-45	12, 24, 36	Graph 10	400	None	12.5

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Load Sharing

The four LTM8051 channels may be paralleled to produce higher currents. To do this on two or more LTM8051, tie the V_{INn}, V_{OUTn}, FB*n* and SHARE*n* pins of all the paralleled channels/modules together (see Figure 7). To ensure that paralleled channels start up together, the TRSS*n* pins may be tied together, as well. If it is inconvenient to tie the TRSS*n* pins together, make sure that the same value soft-start capacitors are used for each µModule regulator. When load sharing among *n* units and using a single R_{FB} resistor, the value of the resistor is:

$$R_{FB} = \frac{199.2}{n(V_{OUT} - 0.8)}, \text{where } R_{FB} \text{ is in k}\Omega$$

Examples of load sharing applications are given in Figure 6 through Figure 8.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8051 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8051 delivers single cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off and energy is delivered to the load by the output capacitor. During the sleep time, V_{INn} and BIAS*n* quiescent currents are greatly reduced, so, as the load current decreases towards a no load condition, the percentage of time that the LTM8051 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

Burst Mode operation is enabled by tying SYNC to GND.

Minimum Input Voltage

The LTM8051 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3V may turn off the LTM8051.

V_{IN1} must be above 3V for channel 1 and channel 4 to operate. If V_{IN1} is above 3V, channel 4 will operate as long as V_{IN4} is above 2V.

V_{IN23} must be above 3V for channel 2 and channel 3 to operate.

Output Voltage Tracking and Soft-Start

The LTM8051 allows the user to adjust its output voltage ramp rate by means of the TRSS*n* pin. An internal 2µA pulls up the TRSS*n* pin to about 2.4V. Putting an external capacitor on TRSS*n* enables soft starting the output to reduce current surges on the input supply. During the soft-start ramp the output voltage will proportionally track the TRSS*n* pin voltage. For output tracking applications, TRSS*n* can be externally driven by another voltage source. From 0V to 0.8V, the TRSS*n* voltage will override the internal 0.8V reference input to the error amplifier, thus regulating the FB*n* pin voltage to that of the TRSS*n* pin. When TRSS*n* is above 0.8V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TRSS*n* pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TRSS*n* pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the RUN*n* pin transitioning low, V_{INn} voltage falling too low, or thermal shutdown.

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Pre-Biased Output

As discussed in the Output Voltage Tracking and Soft-Start section, the LTM8051 regulates the output to the FB*n* voltage determined by the TRSS*n* pin whenever TRSS*n* is less than 0.8V. If the LTM8051 output is higher than the target output voltage, and SYNC*n* is not held below 0.8V, the LTM8051 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If there is nothing loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8051. If SYNC is grounded, the LTM8051 will not return current to the input.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below about 0.8V (this can be ground or a logic low output). To synchronize the LTM8051 oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNC*n* pin. The square wave amplitude should have valleys that are below 0.8V and peaks above 1.5V.

The LTM8051 may be synchronized over a 300kHz to 3MHz range. The LTM8051 will not enter Burst Mode operation at light output loads while synchronized to an external clock. The R_T resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz or lower.

The LTM8051 features spread spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, apply between 2.8V and 4.2V to the SYNC pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to about 20% higher than that value. The modulation frequency is about 7kHz. For example, when the LTM8051 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 7kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part may run in discontinuous mode.

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8051 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR'ed with the LTM8051's output. If the V_{INn} pin is allowed to float and the RUN*n* pin is held high (either by a logic signal or because it is tied to V_{INn}), then the LTM8051's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN*n* pin, the internal current drops to essentially zero. However, if the V_{INn} pin is grounded while the output is held high, parasitic diodes inside the LTM8051 can pull large currents from the output through the V_{INn} pin. Figure 2 shows a circuit that runs only when the input voltage is present and that protects against a shorted or reversed input.

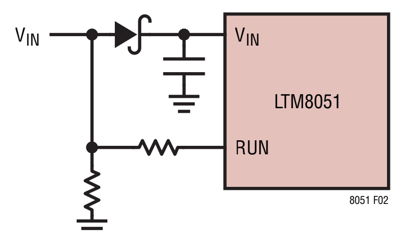

Figure 2. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8051 Runs Only When the Input Is Present

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8051. The LTM8051 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

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A few rules to keep in mind are:

1. Place the R_{FB} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8051.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8051.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM8051.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8051.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8051 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

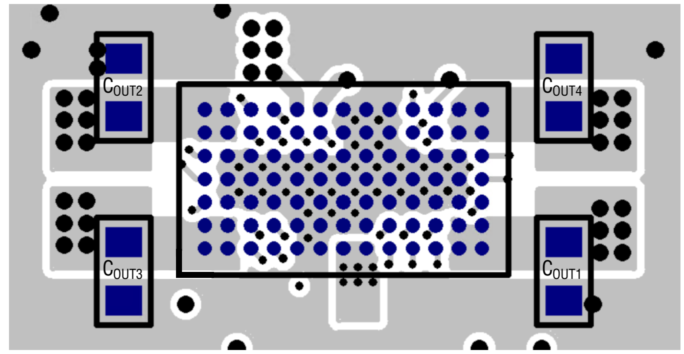


Figure 3. Layout Showing Suggested External Components, GND Plane and Vias

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8051. However, these capacitors can cause problems if the LTM8051 is plugged into a live supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8051 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8051's rating and damaging the part. If the input supply is poorly controlled or the LTM8051 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is add an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8051 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8051 mounted to

APPLICATIONS INFORMATION

a 74cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (Finite Element Analysis) or CFD (Computational Fluid Dynamics) to predict thermal performance. To that end, the Pin Configuration typically gives three dominant thermal coefficients:

1. θ_{JA} – Thermal resistance from junction to ambient
2. θ_{JCbot} – Thermal resistance from junction to the bottom of the product case
3. θ_{JCtop} – Thermal resistance from junction to top of the product case

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical approximation of these dominant thermal resistances is given in Figure 4. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard, and are not shown. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8051 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8051. The bulk of the heat flow out of the LTM8051 is through the bottom of the package and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

APPLICATIONS INFORMATION

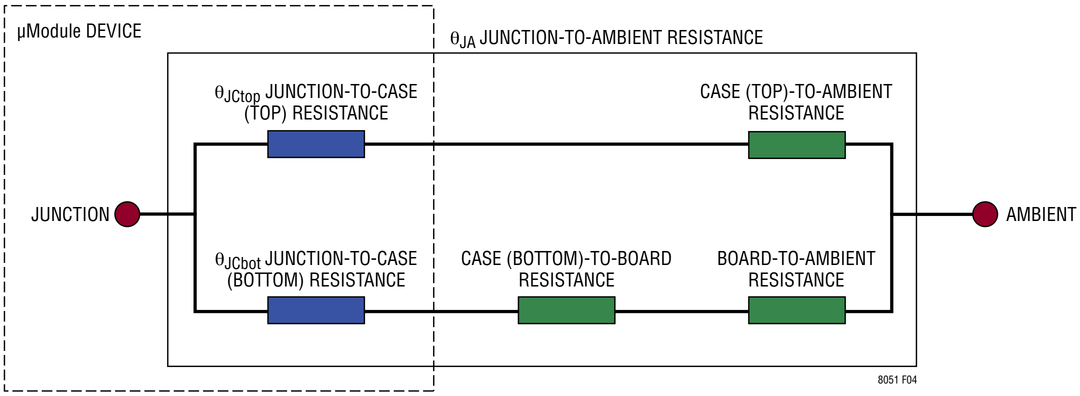


Figure 4. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

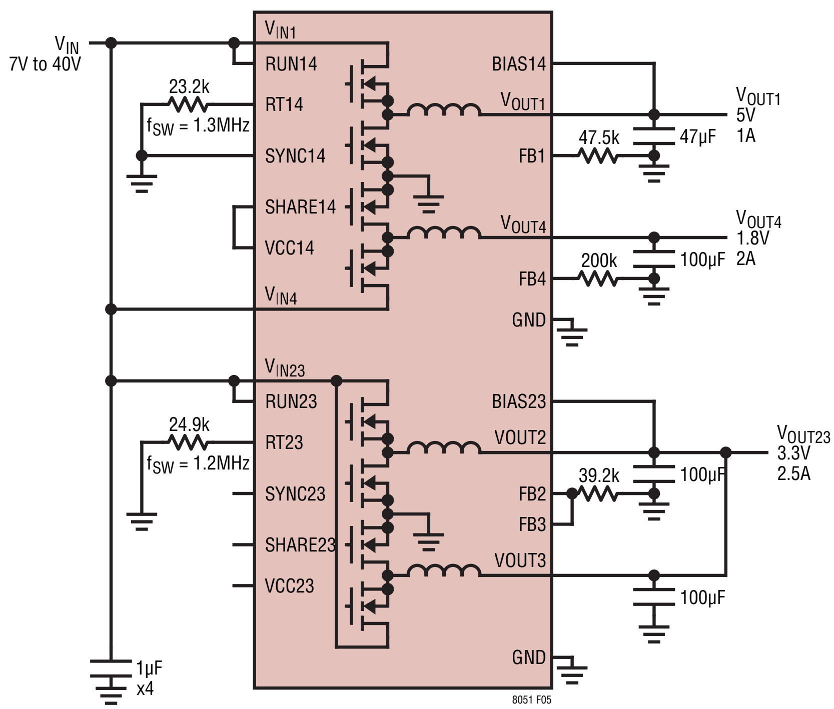
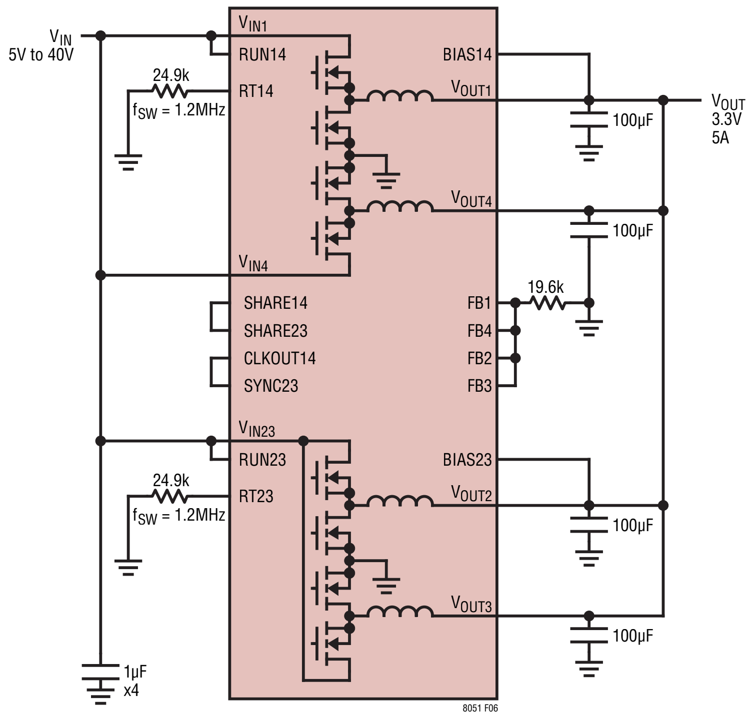


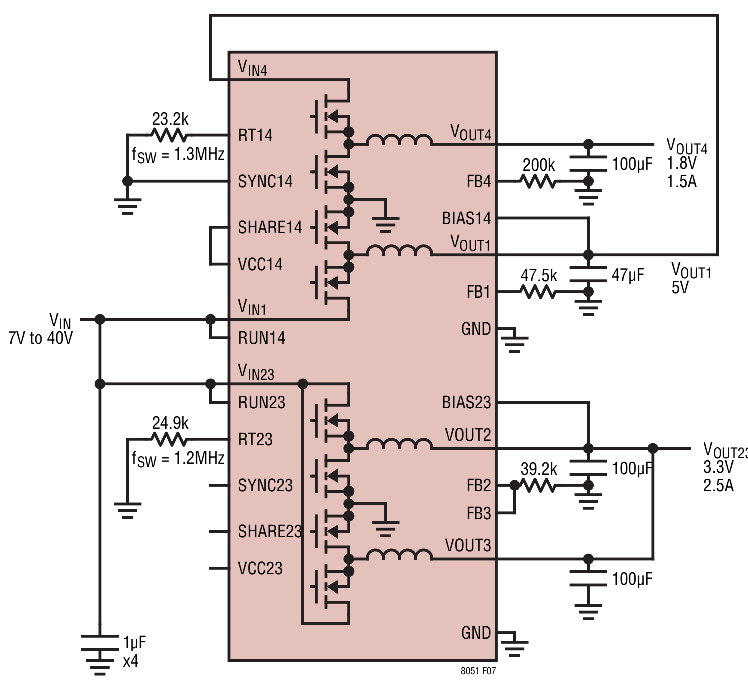
Figure 5. 7V to 40V Input to 5V at 1A, 1.8V at 2A, and Paralleled 3.3V at 2.5A

TYPICAL APPLICATIONS



PINS NOT USED: TRSS1, TRSS2, TRSS3, TRSS4, PG1, PG2, PG3, PG4, SYNC14, CLKOUT23, VCC14, VCC23

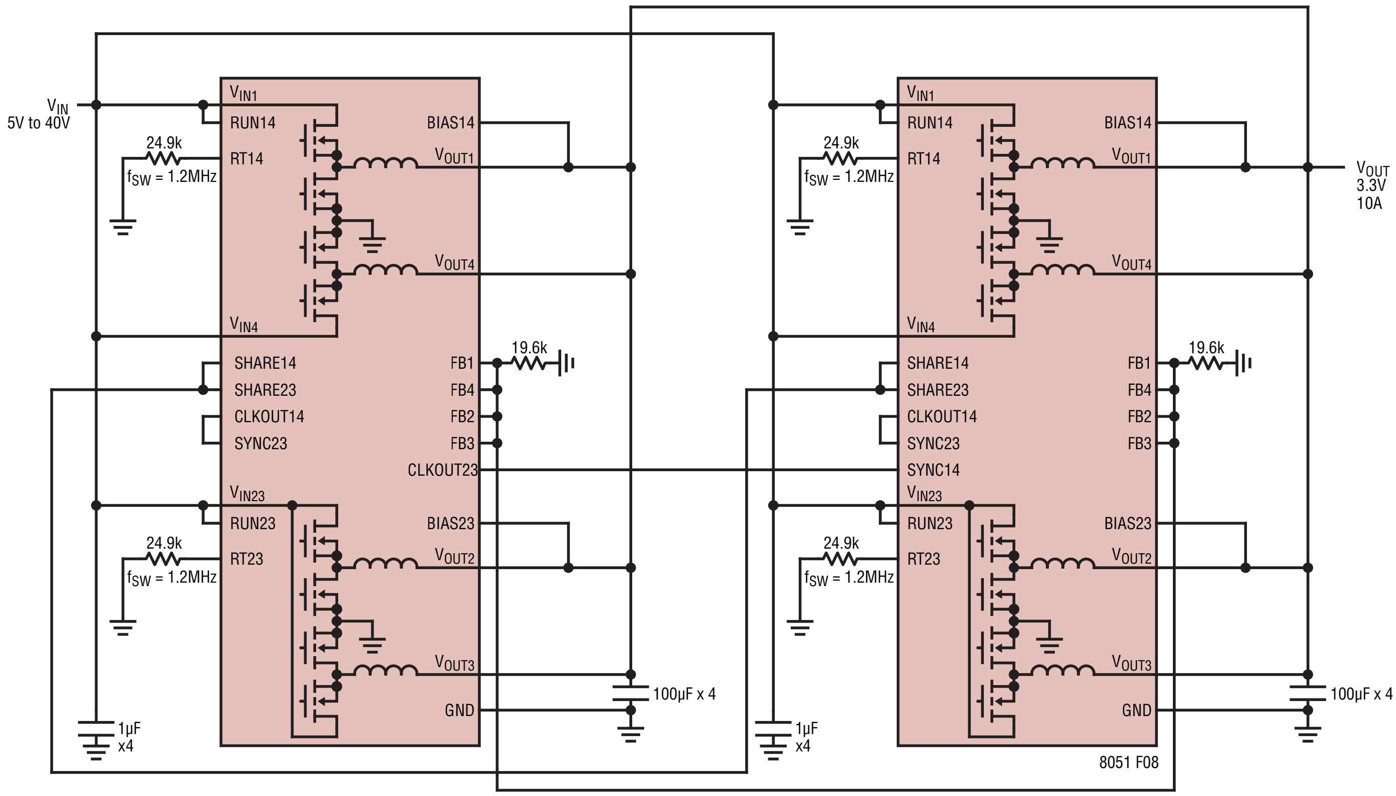
Figure 6. 5V to 40V Input to Paralleled 3.3V at 5A, frequency is synchronized.



PINS NOT USED: TRSS1, TRSS2, TRSS3, TRSS4, PG1, PG2, PG3, PG4, CLKOUT14, CLKOUT23

Figure 7. 7V to 40V Input to Cascaded 1.8V at 1.5A and Paralleled 3.3V at 2.5A

TYPICAL APPLICATIONS

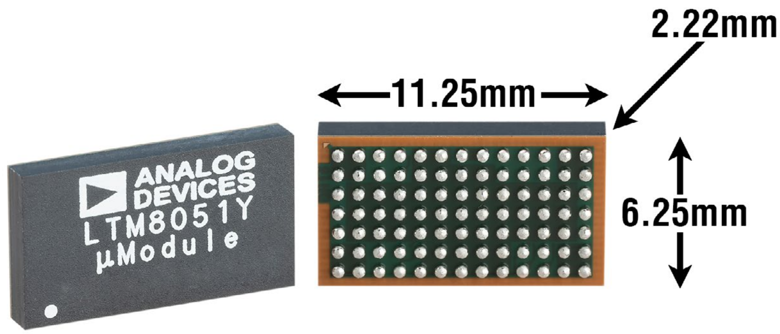


PINS NOT USED: TRSS1, TRSS2, TRSS3, TRSS4, PG1, PG2, PG3, PG4, VCC14, VCC23

Figure 8. Two LTM8051 are Paralleled to Supply 3.3V/10A

Rev. A

PACKAGE PHOTO



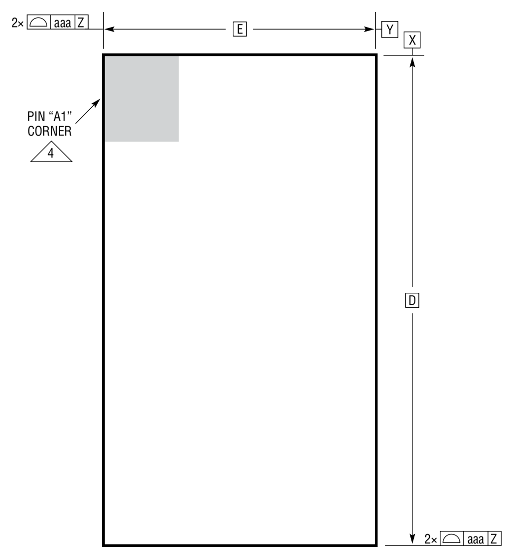
PACKAGE DESCRIPTION

Table 6. LTM8051 Pinout (Sorted by Pin Number)

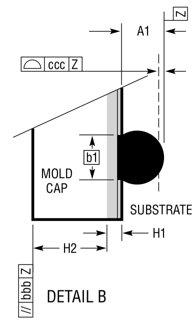
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
A1	V_{OUT3}	B1	V_{OUT3}	C1	TRSS3	D1	FB3	E1	GND	F1	GND	G1	V_{IN23}
A2	V_{OUT3}	B2	V_{OUT3}	C2	TRSS2	D2	FB2	E2	GND	F2	GND	G2	GND
A3	SHARE23	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND	G3	GND
A4	V_{CC23}	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND	G4	GND
A5	BIAS23	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND	G5	GND
A6	V_{OUT2}	B6	V_{OUT2}	C6	CLKOUT23	D6	CLKOUT14	E6	SYNC23	F6	SYNC14	G6	GND
A7	V_{OUT2}	B7	V_{OUT2}	C7	RUN23	D7	RUN14	E7	V_{IN1}	F7	V_{IN4}	G7	GND
Pin	**Pin Name**	**Pin**	**Pin Name**	**Pin**	**Pin Name**	**Pin**	**Pin Name**	**Pin**	**Pin Name**	**Pin**	**Pin Name**		
H1	V_{IN23}	J1	RT23	K1	RT14	L1	FB4	M1	V_{OUT1}	N1	V_{OUT1}		
H2	GND	J2	TRSS1	K2	TRSS4	L2	FB1	M2	V_{OUT1}	N2	V_{OUT1}		
H3	GND	J3	GND	K3	GND	L3	GND	M3	GND	N3	BIAS14		
H4	GND	J4	GND	K4	GND	L4	GND	M4	GND	N4	V_{CC14}		
H5	GND	J5	GND	K5	GND	L5	GND	M5	GND	N5	SHARE14		
H6	GND	J6	GND	K6	PG2	L6	PG1	M6	V_{OUT4}	N6	V_{OUT4}		
H7	GND	J7	GND	K7	PG3	L7	PG4	M7	V_{OUT4}	N7	V_{OUT4}		

PACKAGE DESCRIPTION

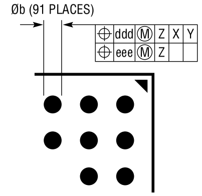
BGA Package
91-Lead (11.25mm × 6.25mm × 2.22mm)
(Reference LTC DWG# 05-08-1608 Rev Ø)



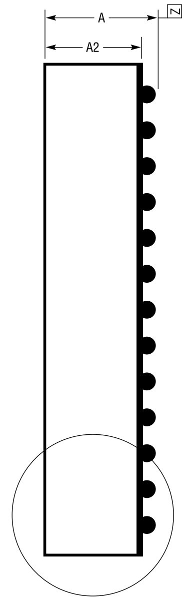
PACKAGE TOP VIEW



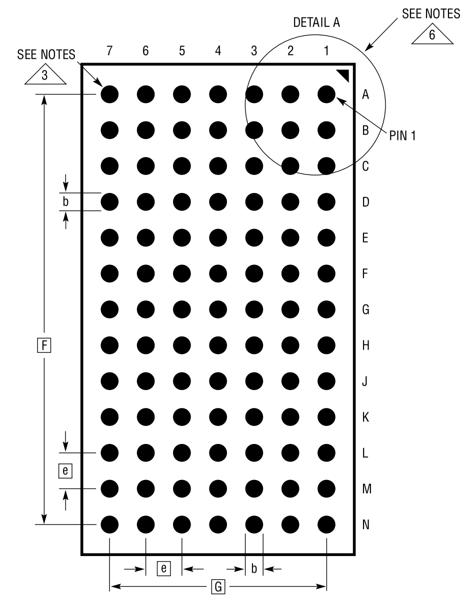
DETAIL B



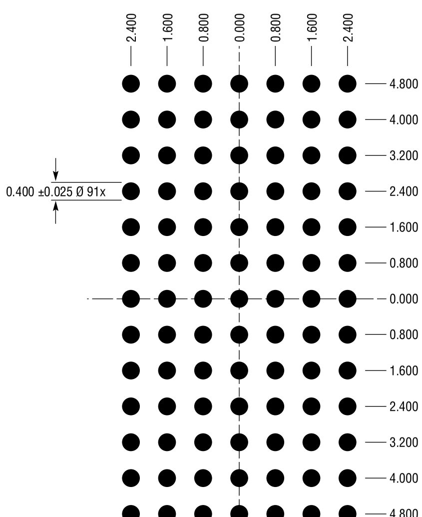
DETAIL A



DETAIL B
PACKAGE SIDE VIEW



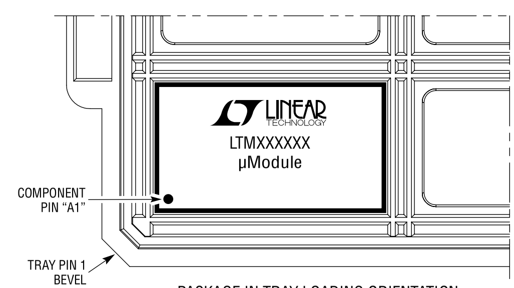
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTES
A	2.03	2.22	2.41	
A1	0.30	0.40	0.50	BALL HT
A2	1.73	1.82	1.91	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		11.25		
E		6.25		
e		0.80		
F		9.60		
G		4.80		
H1		0.32		SUBSTRATE THK
H2		1.50		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 91				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG μModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

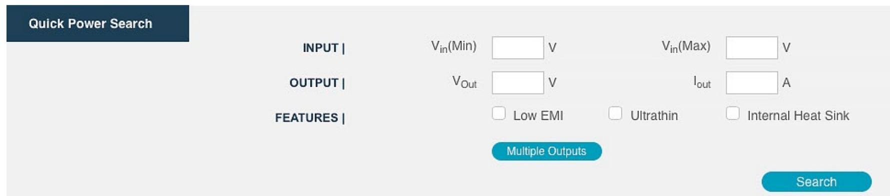
BGA 91 0118 REV Ø

Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/21	Changed V_{IN1n} to V_{INn}. Added V_{INn} = 6V.	3
		Removed Output Noise Spectrum graphs and added Output Noise Spectral Density graph.	11
		Fixed type error Figure 5 to Figure 2 in Shorted Input Protection section.	20

DESIGN RESOURCES

SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8074	40V, 1.2A Silent Switcher µModule Regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 12V$, 4mm × 4mm × 1.82mm BGA
LTM8063	40V, 2A Step-Down Silent Switcher µModule Regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 15V$, 4mm × 6.25mm × 2.22mm BGA Package
LTM8065	40V, 2.5A Step-Down Silent Switcher µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 18V$, 6.25mm × 6.25mm × 2.32mm BGA Package
LTM8053	40V, 3.5A Step-Down µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 15V$, 6.25mm × 9mm × 3.32mm BGA
LTM8003	40V, 3.5A, H-Grade, 150°C Operation, FMAE-Compliant Pinout	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 15V$, $I_{OUT} = 3.5A$, 6.25mm × 9mm × 3.32mm BGA
LTM8052	36V, 5A CVCC Step-Down µModule Regulator	$6V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 24V$, Constant Voltage Constant Current, 11.25mm × 15mm × 2.82mm LGA, 11.25mm × 15mm × 3.42mm BGA
LTM4613	36V, 8A Low EMI Step-Down µModule Regulator	$5V \le V_{IN} \le 36V$, $3.3V \le V_{OUT} \le 15V$, EN55022B Compliant, 15mm × 15mm × 4.32mm LGA, 15mm × 15mm × 4.92mm BGA.
LTM8073	60V, 3A Step-Down µModule Regulator	$3.4V \le V_{IN} \le 60V$, $0.85V \le V_{OUT} \le 15V$, 6.25mm × 9mm × 3.32mm BGA
LTM8071	60V, 5A Silent Switcher µModule Regulator	$3.6V \le V_{IN} \le 60V$, $0.97V \le V_{OUT} \le 15V$, 9mm × 11.25mm × 3.32mm BGA
LTM4622	Dual 2.5A, 20V Step-Down µModule Regulator	$3.6V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4642	Dual 4A, 20V Step-Down µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 9mm × 11.25mm × 4.92mm BGA
LTM4643	Quad 3A, 20V Step-Down µModule Regulator	$4V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 3.3V$, 9mm × 15mm × 1.82mm LGA, 9mm × 15mm × 2.42mm BGA
LTM4644	Quad 4A, 14V Step-Down µModule Regulator	$4V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, 9mm × 15mm × 5.01mm BGA

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