LTM8080

$40V_{IN}$, Dual 500mA or Single 1A Ultralow Noise, Ultrahigh PSRR µModule Regulator

FEATURES

- **Dual LDOs Powered by an Integrated Switching Step-Down Regulator**
- **Low Noise Silent Switcher® Architecture with an Integrated EMI Noise Shield**
- **CISPR22 Class B and CISPR25 Class 5 Compliant**
- **Ultralow Output RMS Noise: <1µV_{RMS} (10Hz to 100kHz)**
- **Ultralow Output Spot Noise: 2nV/$\sqrt{Hz}$ at 10kHz**
- **Ultrahigh PSRR: 80dB at 100kHz**
- **Wide Input Voltage: 3.5V to 40V**
- **Wide Output Voltage: 0V to 8V**
- **Dual 500mA Continuous Current at T_A = 85°C**
- **Voltage Tracking Function to Minimize Power Loss**
- **100µA SET Pin Current with ±1% Initial Accuracy**
- Selectable Switching Frequency: 200kHz to 2.2MHz
- External Synchronization
- Programmable Power Good
- Parallelable for Lower Noise and Higher Current
- 9mm × 6.25mm × 3.32mm BGA

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs
- Very Low Noise Instrumentation
- High Speed/High Precision Data Converters
- Medical Applications: Imaging, Diagnostics

DESCRIPTION

The LTM®8080 is a $40V_{IN}$, dual 500mA or single 1A ultralow noise, ultrahigh PSRR µModule® regulator. The LTM8080 has cascaded architecture, which contains a $40V_{IN}$ step-down Silent Switcher regulator with an integrated EMI noise shield followed by dual high-performance low dropout linear regulators. The dual LDOs feature ADI's ultralow noise and ultrahigh PSRR architecture for powering noise-sensitive applications. The LTM8080 is an integrated solution comprised of a switcher and LDOs, which offers both advantages while maintaining a small size and significantly reduced PCB layout sensitivity.

The package includes the controllers, power switches, inductors, and support components. In addition, the LTM8080 has a built-in voltage tracking function that automatically sets V_{BUS} to either 2.5V nominal or 1V higher than V_{OUT1}, whichever is greater, to achieve superior noise performance and minimize power dissipation.

The LTM8080 is packaged in a thermally enhanced, compact (9mm × 6.25mm × 3.32mm) over-molded Ball Grid Array (BGA) package suitable for automated assembly by standard surface mount equipment and is RoHS compliant.

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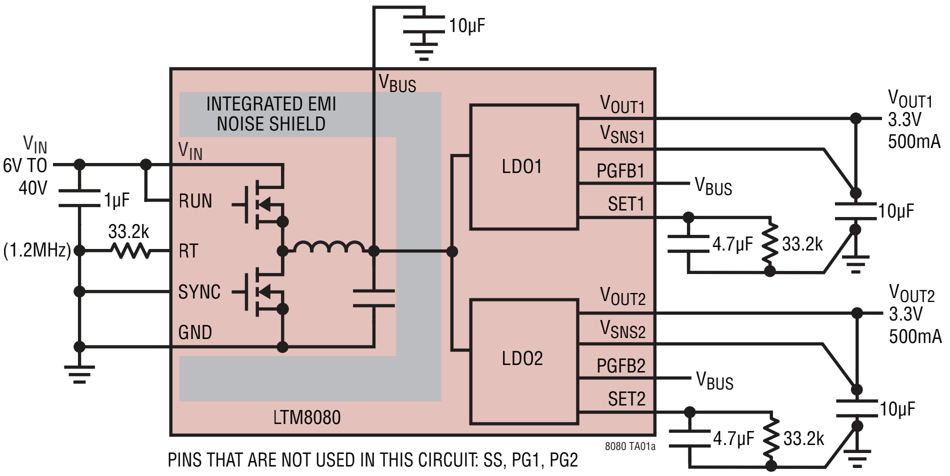
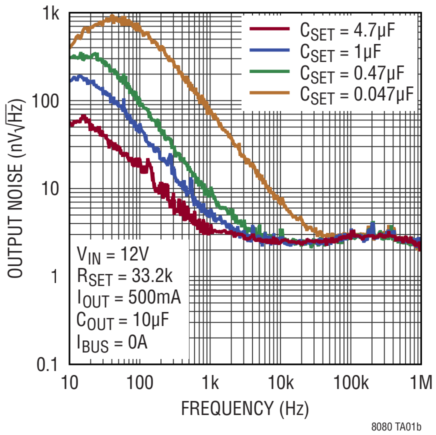
TYPICAL APPLICATION

Dual 3.3V/500mA from 6V to 40V Input



PINS THAT ARE NOT USED IN THIS CIRCUIT: SS, PG1, PG2

Noise Spectral Density

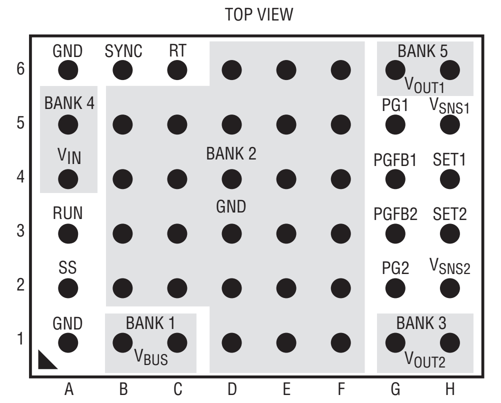


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN 42V
V_{BUS}, V_{OUTn}, V_{SNSn}, SET*n*, PG*n*, PGFB*n* 9V
SYNC 6V
SS 4V
Maximum Internal Temperature (Note 2) .... 125°C
Storage Temperature.............................. –55°C to 125°C
Peak Reflow Solder Body Temperature .... 250°C

PIN CONFIGURATION



BGA PACKAGE
48-PIN (9mm × 6.25mm × 3.32mm)
T_{JMAX} = 125°C, θ_{JA} = 22.6°C/W, θ_{JCtop} = 40°C/W,
θ_{JCbot} = 9.7°C/W, WEIGHT = 0.45g

NOTES:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) SEE THE TYPICAL PERFORMANCE CHARACTERISTICS SECTION FOR LAB-MEASURED DERATING CURVES.

ORDER INFORMATION

PART NUMBER	TERMINAL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM8080EY#PBF	SAC305 (RoHS)	LTM8080Y	e1	BGA	4	–40°C to 125°C
LTM8080IY#PBF	SAC305 (RoHS)	LTM8080Y	e1	BGA	4	–40°C to 125°C
LTM8080MPY#PBF	SAC305 (RoHS)	LTM8080Y	e1	BGA	4	–55°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended BGA PCB Assembly and Manufacturing Procedures.
- BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator						
Minimum Input Voltage		●			3.5	V
Quiescent Current into V_{IN}	RUN = 0V				8	µA
Maximum V_{BUS} Output Current	V_{BUS} = 2.5V, V_{OUT} = 1.3V, I_{OUT} = 1mA (Note 3)				1.5	A
Switching Frequency	R_T = 221k R_T = 40.2k R_T = 16.2k			200 1 2.2		kHz MHz MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RUN Threshold Voltage	Rising	●	0.9	1.0	1.2	V
RUN Current	RUN = 2V				1	µA
SYNC Threshold Voltage	Synchronization		0.4		1.5	V
SYNC Threshold Voltage	To Enable Spread Spectrum		2.9		4.2	V
SYNC Current	SYNC = 2V				1	µA
SS Current	SS = 0V			2		µA
SS Pull-Down	SS = 0.1V			300		Ω
LDO						
Output Voltage Range		●	0		8	V
SET Pin Current (I_{SET})	I_{OUT} = 1mA, V_{OUT} = 1.3V, 3.5V < V_{IN} < 40V, 0V < V_{OUT} < 8V, 1mA < I_{OUT} < 500mA	●	99	100	101	µA
Fast Start-Up SET Pin Current	V_{PGFB} = 289mV, V_{OUT} = 1.3V			2		mA
Output Current	(Note 3)				500	mA
Output Offset Voltage V_{OS} (V_{OUT} to V_{SET})	V_{IN} = 12V, I_{OUT} = 1mA, V_{OUT} = 1.3V		–1		1	mV
	3.5V < V_{IN} < 40V, 0V < V_{OUT} < 8V, 1mA < I_{OUT} < 500mA	●	–2		2	mV
Line Regulation: ΔI_{SET}	V_{IN} = 3.5V to 40V, I_{OUT} = 1mA, V_{OUT} = 1.3V	●		0.5	±2	nA/V
Line Regulation: ΔV_{OS}	V_{IN} = 3.5V to 40V, I_{OUT} = 1mA, V_{OUT} = 1.3V	●		0.5	±3	µV/V
Load Regulation: ΔI_{SET}	I_{OUT} = 1mA to 500mA, V_{OUT} = 1.3V, V_{IN} = 24V			0.15		µA
Load Regulation: ΔV_{OS}	I_{OUT} = 1mA to 500mA, V_{OUT} = 1.3V , V_{IN} = 24V	●		0.1	0.5	mV
Output Noise Spectral Density (Note 4)	I_{OUT} = 500mA, Frequency = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, 1.3V ≤ V_{OUT} ≤ 8V			2		nV/√Hz
	I_{OUT} = 500mA, Frequency = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, 0V ≤ V_{OUT} < 1.3V			5		nV/√Hz
Output RMS Noise (Note 4)	I_{OUT} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 8V			0.8		μV_{RMS}
	I_{OUT} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 0V ≤ V_{OUT} < 1.3V			1.8		μV_{RMS}
Internal Current Limit				700		mA
PGFB Threshold Voltage	Rising			300		mV
PG Leakage Current	V_{PG} = 8V				1	µA

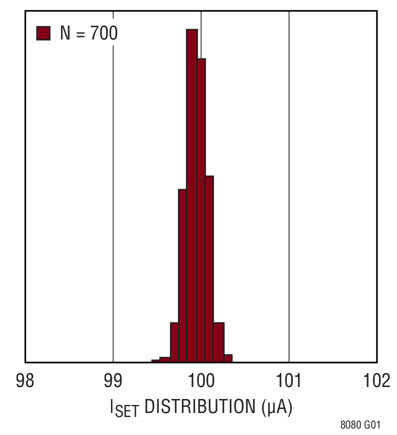
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

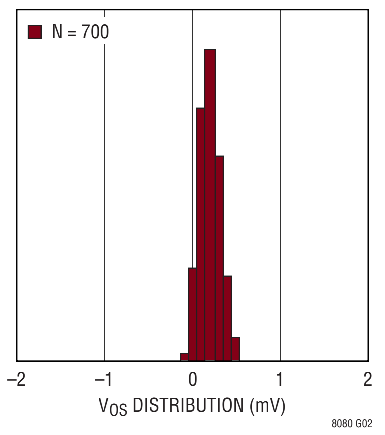
Note 2: The LTM8080E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM8080I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8080MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

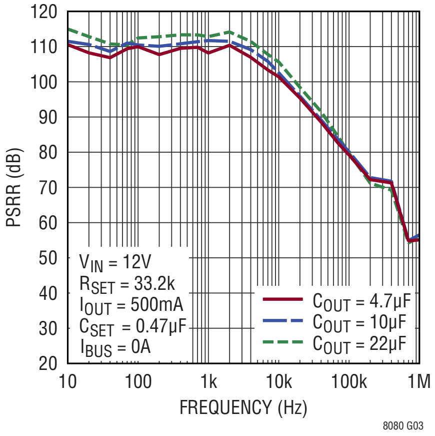
Note 3: The maximum current out of either channel may be limited by the internal temperature of the LTM8080.

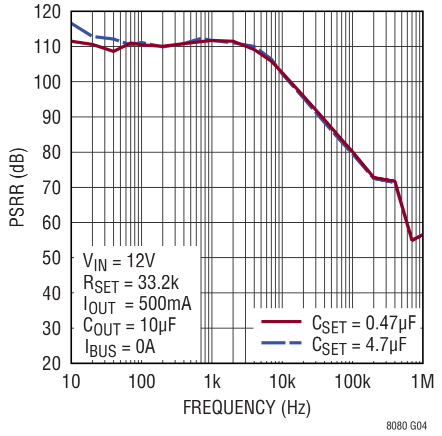
Note 4: Not tested in production.

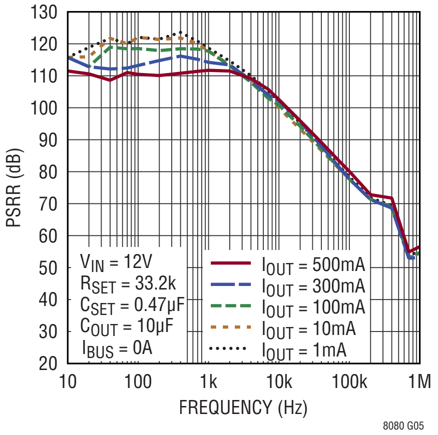
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, $V_{BUS} = V_{OUT1}$ + 1V, unless otherwise noted.

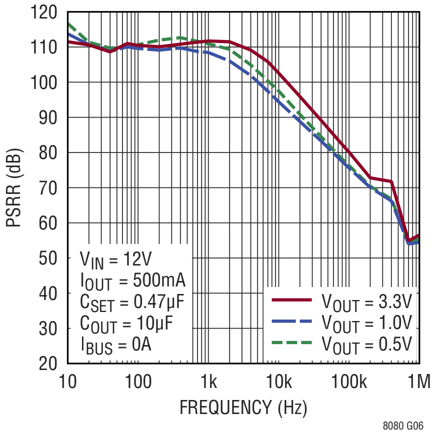

SET Pin Current Distribution

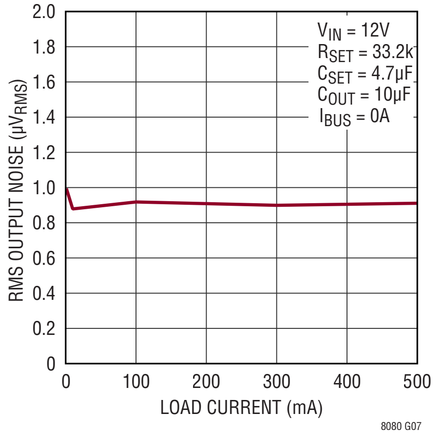

V_{OS} Distribution

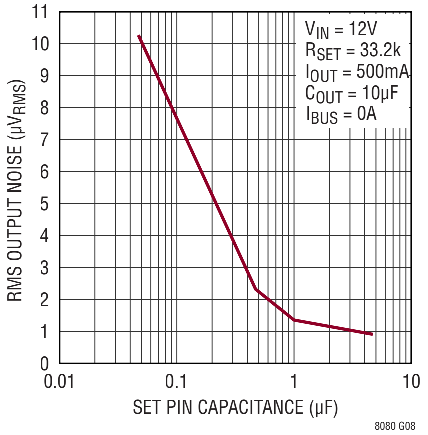

PSRR vs C_{OUT}

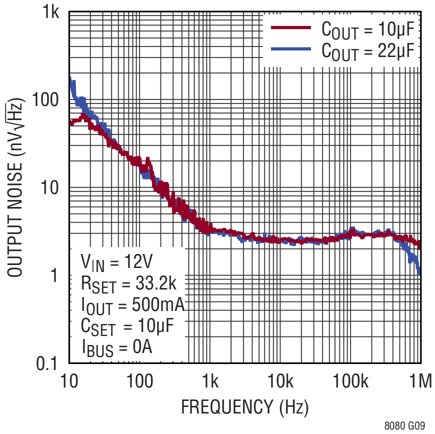

PSRR vs C_{SET}


PSRR vs I_{OUT}


PSRR vs V_{OUT}
V_{BUS} = 2.5V or (V_{OUT1} + 1V), whichever is Greater

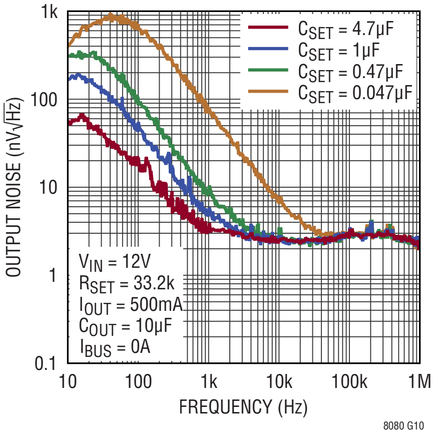

RMS Noise vs I_{OUT}


RMS Noise vs C_{SET}

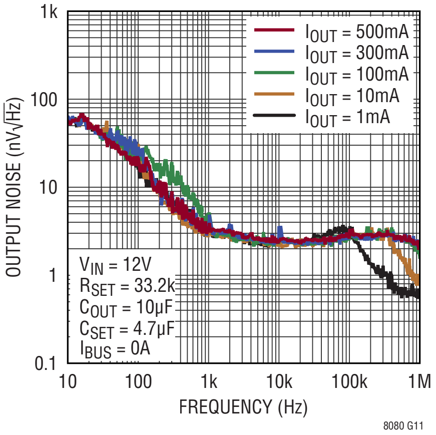

Noise Spectral Density vs C_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{BUS} = V_{OUT1} + 1V$, unless otherwise noted.

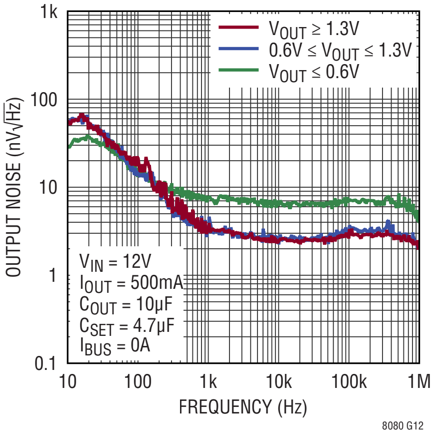
Noise Spectral Density vs C_{SET}



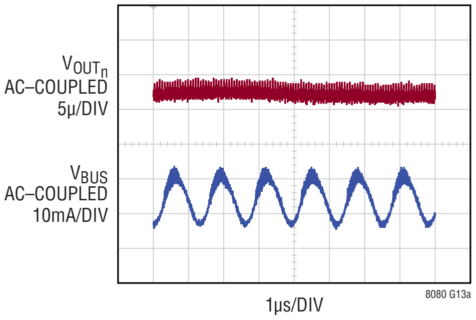
Noise Spectral Density vs I_{OUT}



Noise Spectral Density vs V_{OUT} V_{BUS} = 2.5V or (V_{OUT1} + 1V), whichever is Greater

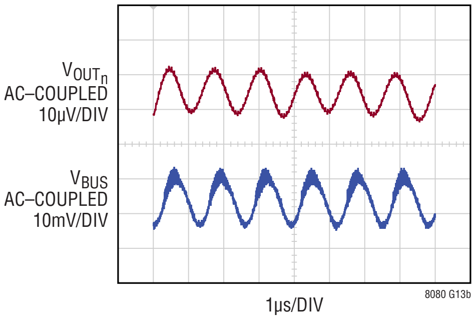


V_{OUTn} Noise Waveform V_{OUTn}: 10Hz to 100kHz BW V_{BUS}: Wideband



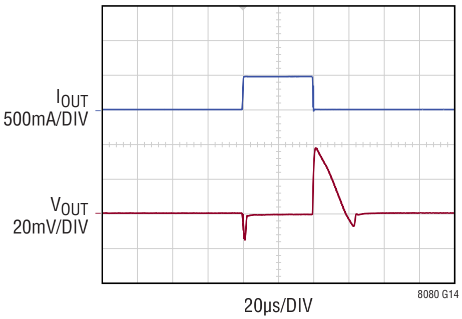
V_{IN} = 12V
R_{SET} = 33.2k
C_{SET} = 4.7µF
C_{OUT} = 10µF
I_{OUT} = 500mA
I_{BUS} = 0A
f_{SW} = 700kHz

V_{OUTn} Noise Waveform V_{OUTn}: 10Hz to 1MHz BW V_{BUS}: Wideband



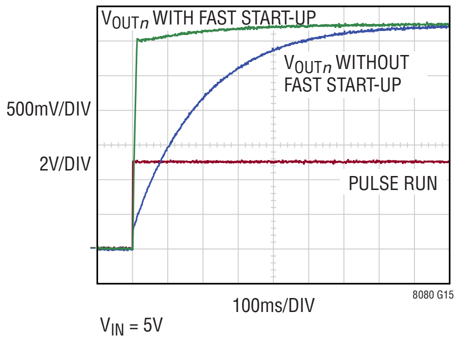
V_{IN} = 12V
R_{SET} = 33.2k
C_{SET} = 4.7µF
C_{OUT} = 10µF
I_{OUT} = 500mA
I_{BUS} = 0A
f_{SW} = 700kHz

Load Transient Response



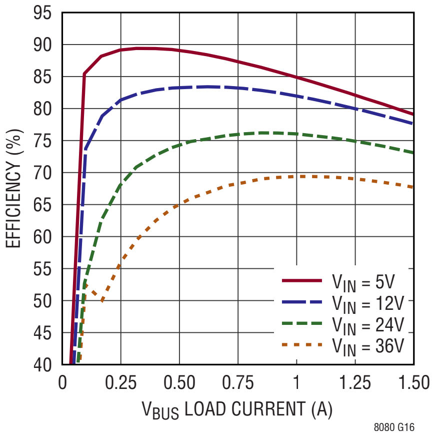
V_{IN} = 12V
R_{SET} = 33.2k
C_{OUT} = 10µF
C_{SET} = 0.47µF
LOAD STEP = 10mA TO 500mA
I_{BUS} = 0A

Start-Up Time with and without Fast Start-Up

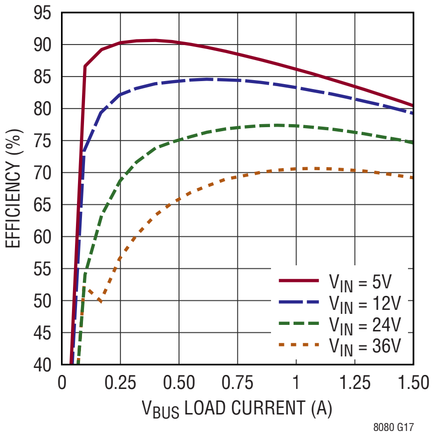


V_{IN} = 5V
R_{SET} = 33.2k
C_{OUT} = 10µF
C_{SET} = 4.7µF
R_{OUT} = 6.6Ω
I_{BUS} = 0A

V_{BUS} Efficiency vs Load, V_{BUS} = 2.5V Pulse-Skipping Mode, f_{SW} = 800kHz



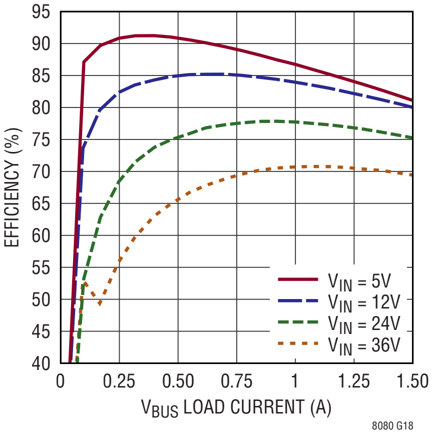
V_{BUS} Efficiency vs Load, V_{BUS} = 2.8V Pulse-Skipping Mode, f_{SW} = 900kHz



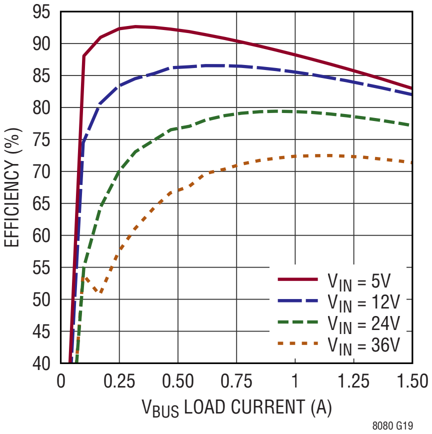
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{BUS} = V_{OUT1} + 1V$, unless otherwise noted.

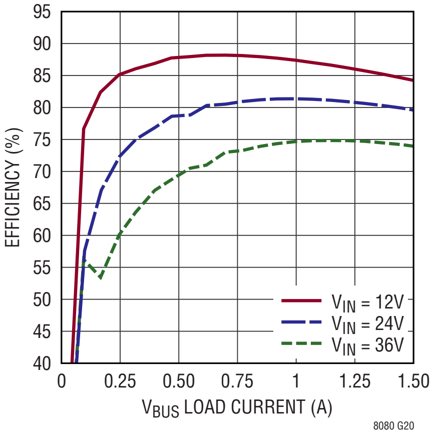
V_{BUS} Efficiency vs Load, V_{BUS} = 3V Pulse-Skipping Mode, f_{SW} = 1MHz



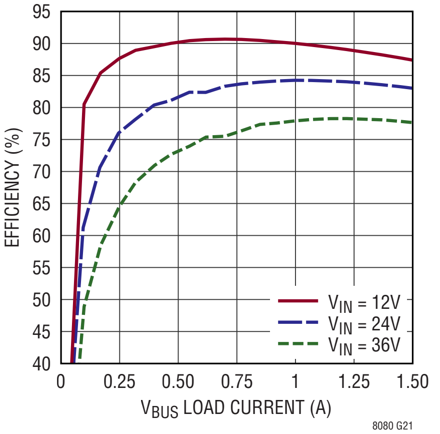
V_{BUS} Efficiency vs Load, V_{BUS} = 3.5V Pulse-Skipping Mode, f_{SW} = 1.1MHz



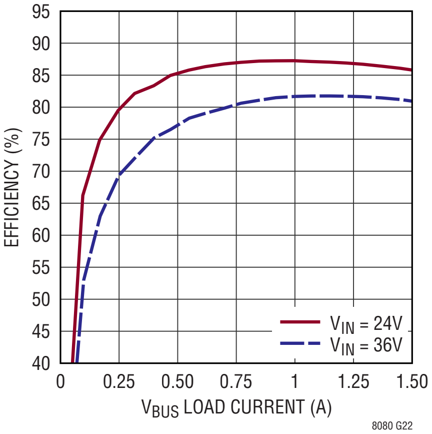
V_{BUS} Efficiency vs Load, V_{BUS} = 4.3V Pulse-Skipping Mode, f_{SW} = 1.2MHz



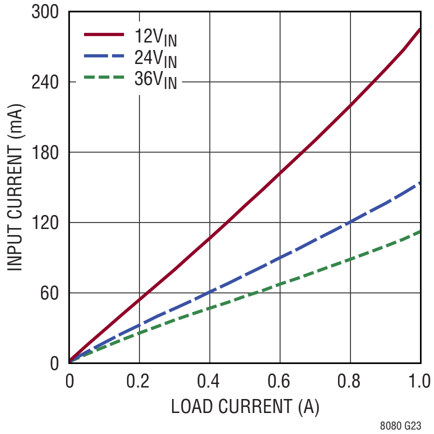
V_{BUS} Efficiency vs Load, V_{BUS} = 6V Pulse-Skipping Mode, f_{SW} = 1.3MHz



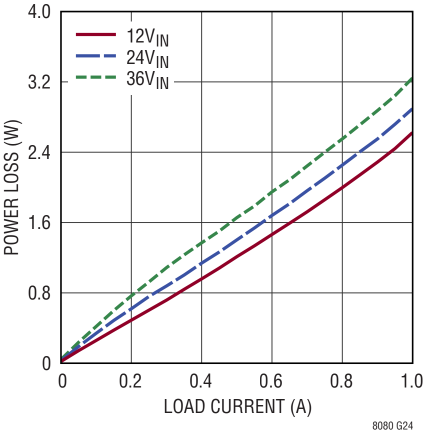
V_{BUS} Efficiency vs Load, V_{BUS} = 9V Pulse-Skipping Mode, f_{SW} = 1.4MHz



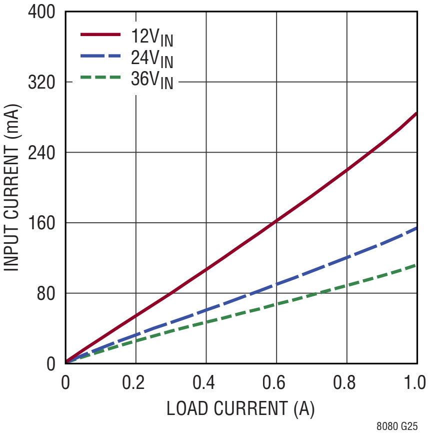
I_{IN} vs I_{OUT}, V_{OUT} = 0.8V, V_{BUS} = 2.5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



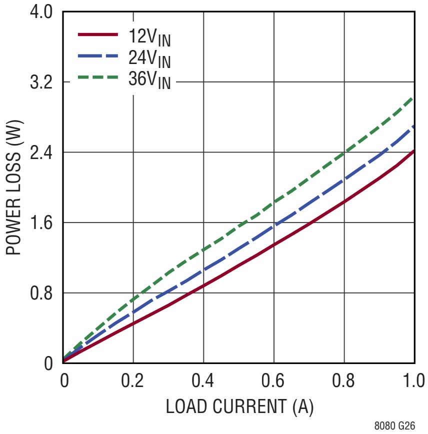
Power Loss, V_{OUT} = 0.8V, V_{BUS} = 2.5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



I_{IN} vs I_{OUT}, V_{OUT} = 1V, V_{BUS} = 2.5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation

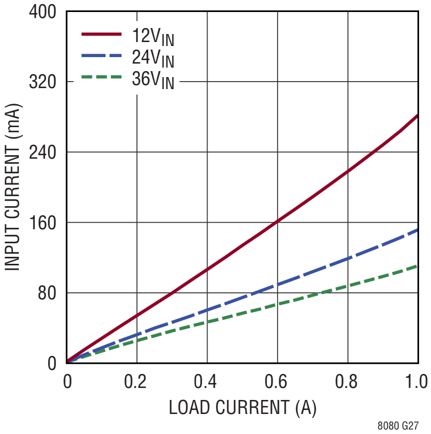


Power Loss, V_{OUT} = 1V, V_{BUS} = 2.5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation

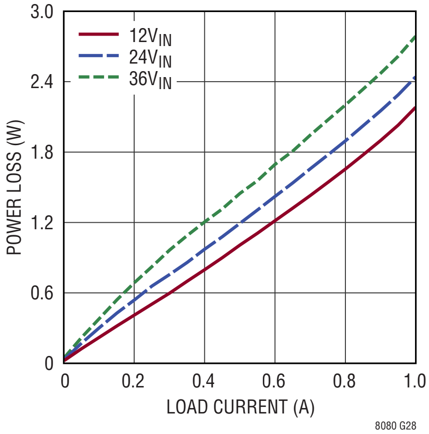


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{BUS} = V_{OUT1} + 1V$, unless otherwise noted.

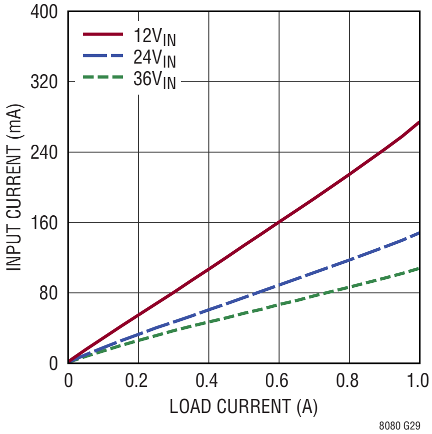
I_{IN} vs I_{OUT}, $V_{OUT} = 1.2V$, $V_{BUS} = 2.5V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



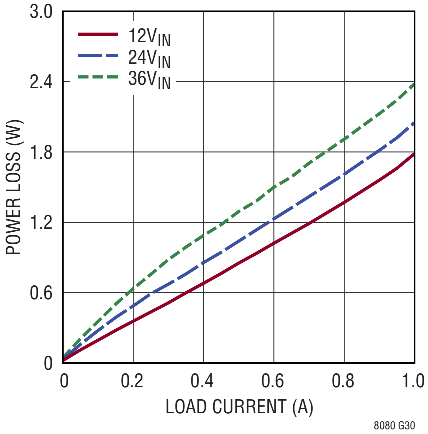
Power Loss, $V_{OUT} = 1.2V$, $V_{BUS} = 2.5V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



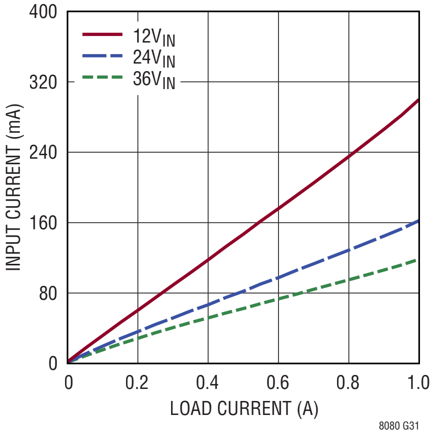
I_{IN} vs I_{OUT}, $V_{OUT} = 1.5V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



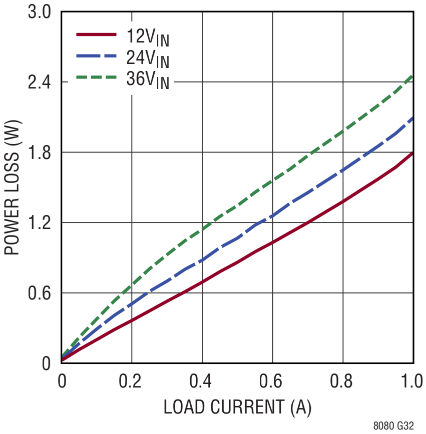
Power Loss, $V_{OUT} = 1.5V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



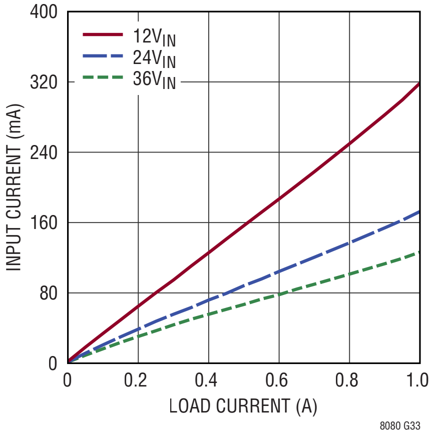
I_{IN} vs I_{OUT}, $V_{OUT} = 1.8V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



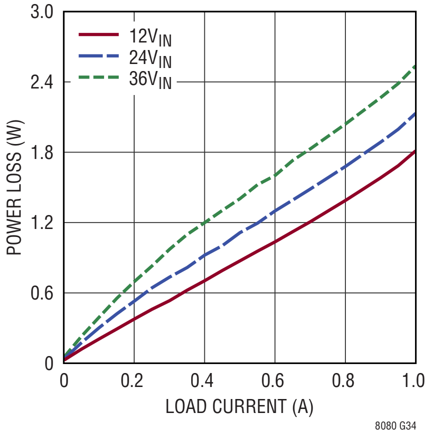
Power Loss, $V_{OUT} = 1.8V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



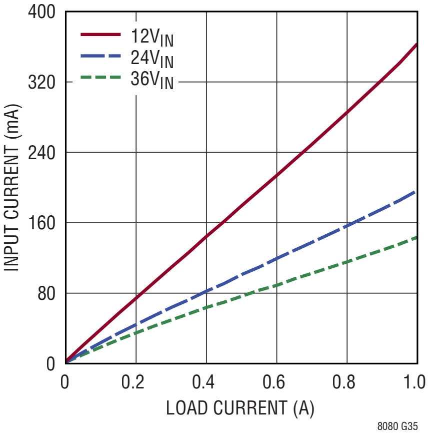
I_{IN} vs I_{OUT}, $V_{OUT} = 2V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



Power Loss, $V_{OUT} = 2V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



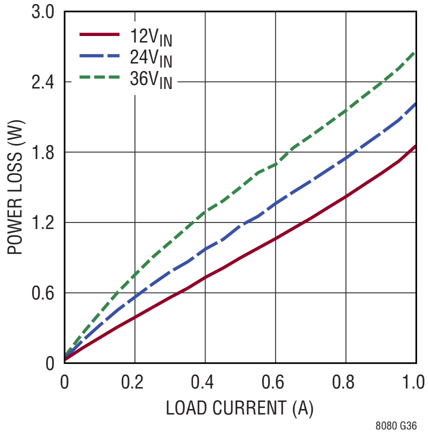
I_{IN} vs I_{OUT}, $V_{OUT} = 2.5V$, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



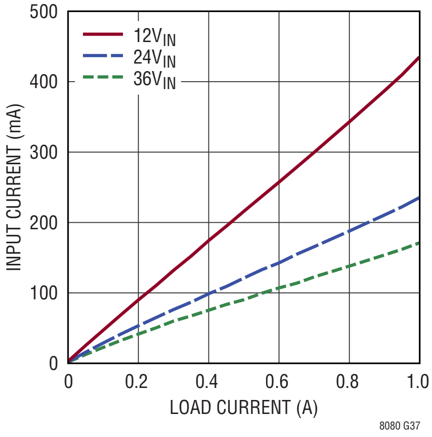
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{BUS} = V_{OUT1} + 1V, unless otherwise noted.

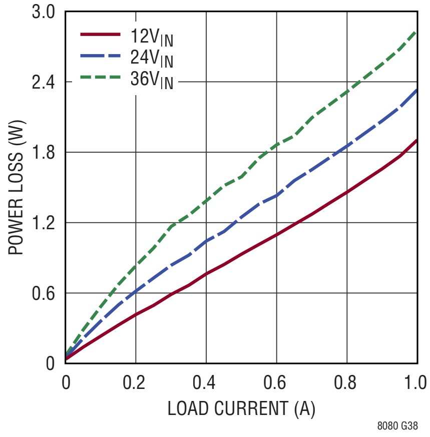
Power Loss, V_{OUT} = 2.5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



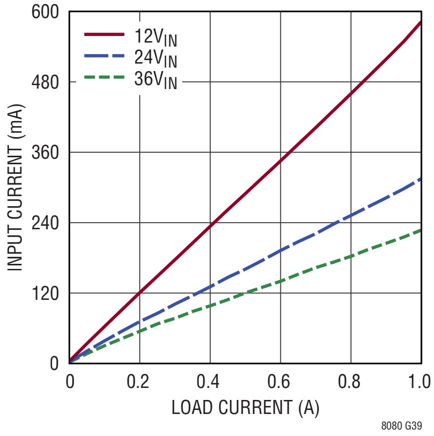
I_{IN} vs I_{OUT}, V_{OUT} = 3.3V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



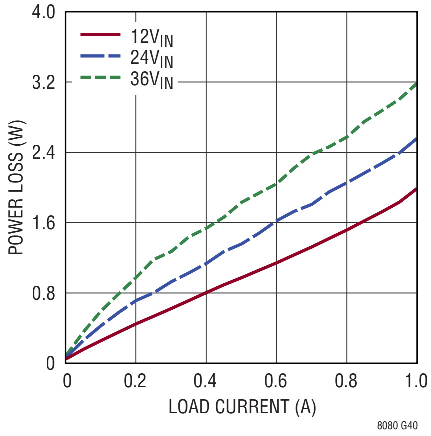
Power Loss, V_{OUT} = 3.3V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



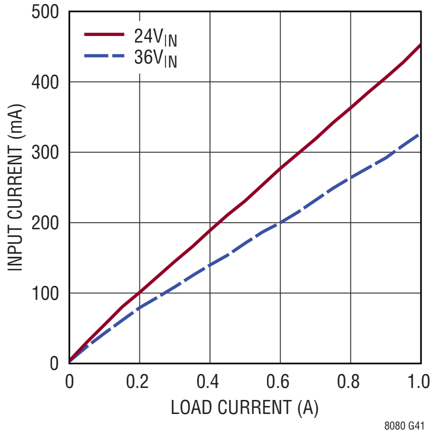
I_{IN} vs I_{OUT}, V_{OUT} = 5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



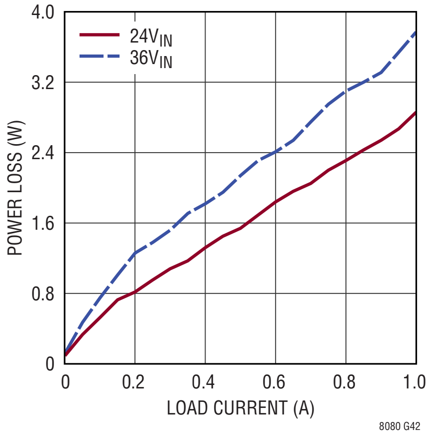
Power Loss, V_{OUT} = 5V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



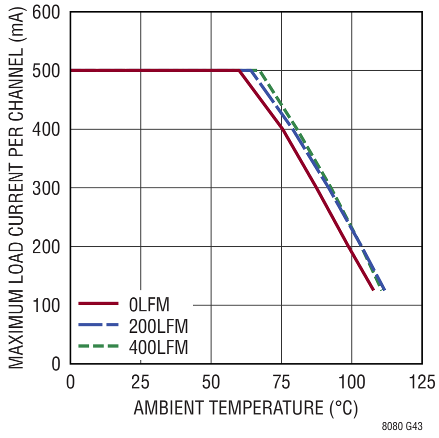
I_{IN} vs I_{OUT}, V_{OUT} = 8V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



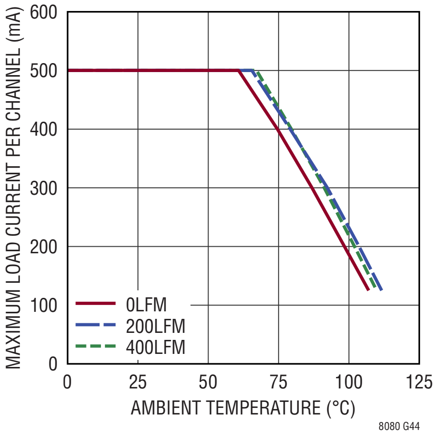
Power Loss, V_{OUT} = 8V, $V_{OUT1,2}$ in Parallel, Burst-Mode Operation



Thermal Derating 5V_{IN} to 1.2V_{OUT}, V_{BUS} = 2.5V, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board

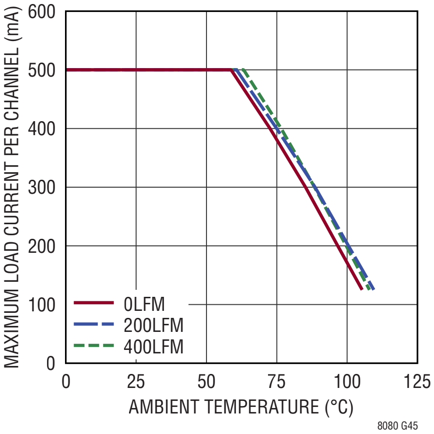


Thermal Derating 12V_{IN} to 1.2V_{OUT}, V_{BUS} = 2.5V, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board

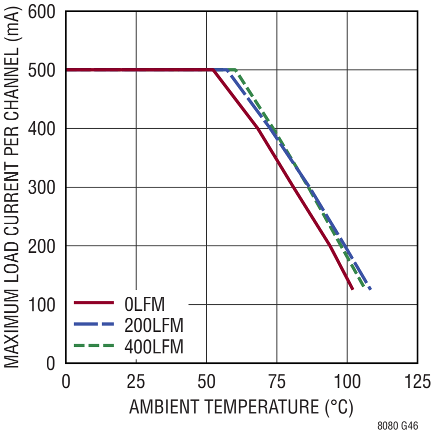


TYPICAL PERFORMANCE CHARACTERISTICS

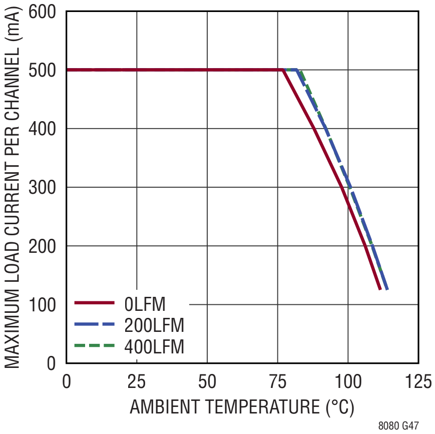
T_A = 25°C, V_{BUS} = V_{OUT1} + 1V, unless otherwise noted.



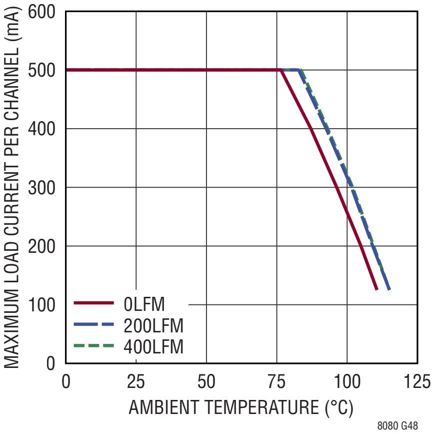
Thermal Derating 24V_{IN} to 1.2V_{OUT}, V_{BUS} = 2.5V, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



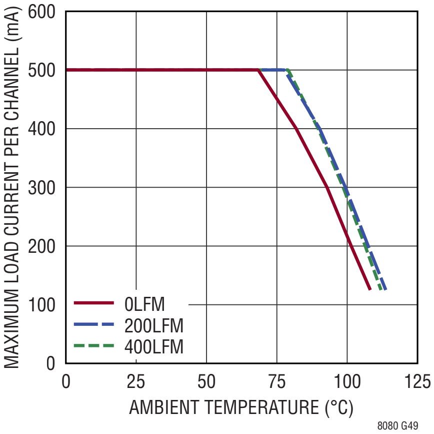
Thermal Derating 36V_{IN} to 1.2V_{OUT}, V_{BUS} = 2.5V, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



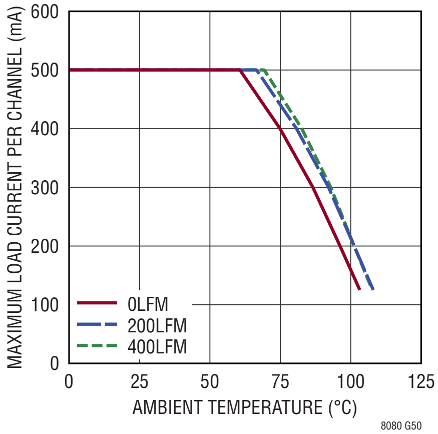
Thermal Derating 5V_{IN} to 1.8V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



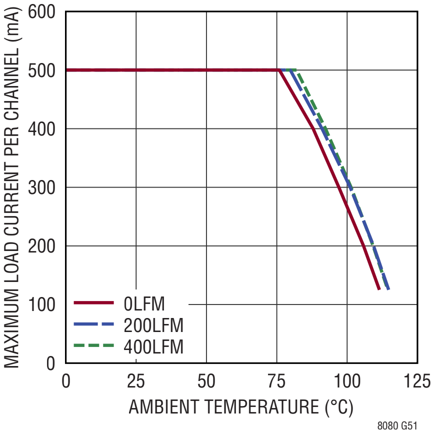
Thermal Derating 12V_{IN} to 1.8V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



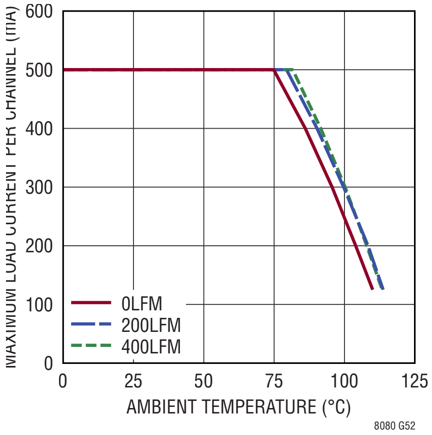
Thermal Derating 24V_{IN} to 1.8V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



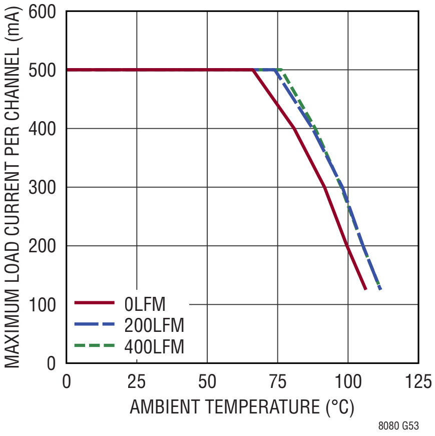
Thermal Derating 36V_{IN} to 1.8V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



Thermal Derating 5V_{IN} to 2.5V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



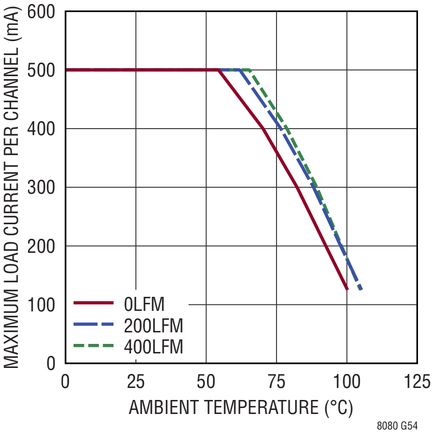
Thermal Derating 12V_{IN} to 2.5V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



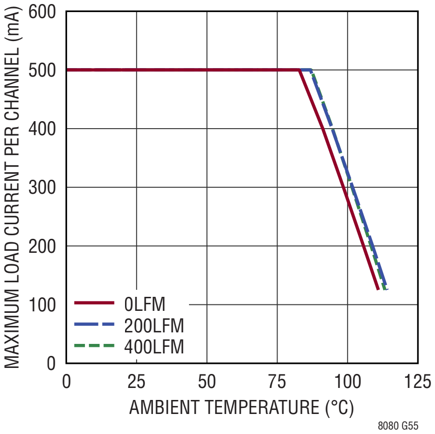
Thermal Derating 24V_{IN} to 2.5V_{OUT}, I_{BUS} = $I_{OUT1,2}$ = 0.5A DC3071A Demo Board

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{BUS} = V_{OUT1} + 1V$, unless otherwise noted.

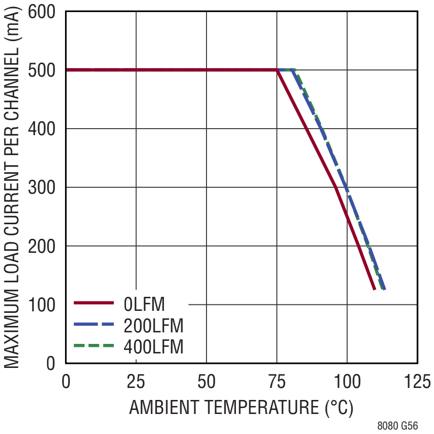
Thermal Derating 36V_{IN} to 2.5V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



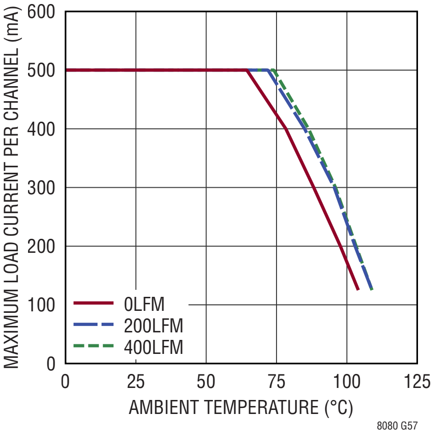
Thermal Derating 12V_{IN} to 3.3V_{OUT}, I_{BUS} = 0A, $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



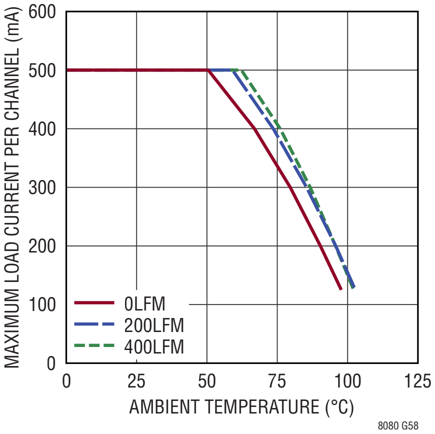
Thermal Derating 12V_{IN} to 3.3V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



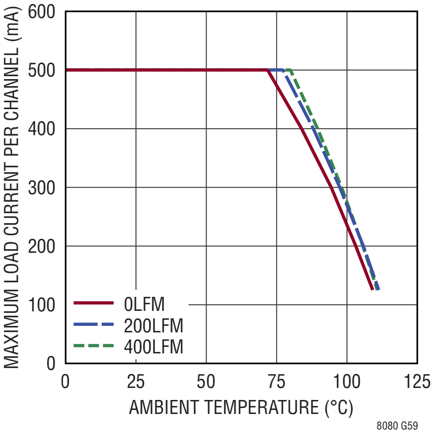
Thermal Derating 24V_{IN} to 3.3V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



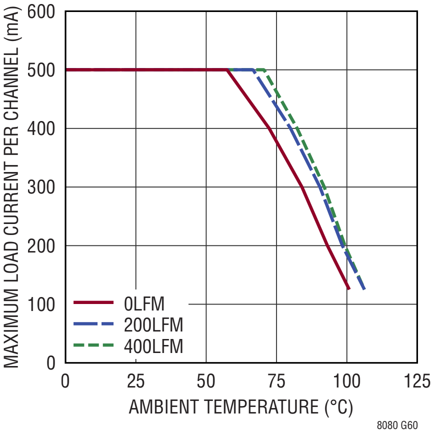
Thermal Derating 36V_{IN} to 3.3V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



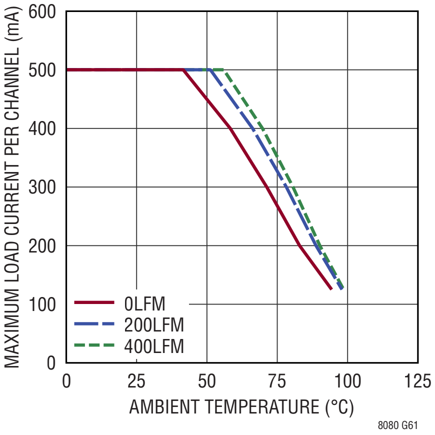
Thermal Derating 12V_{IN} to 5V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



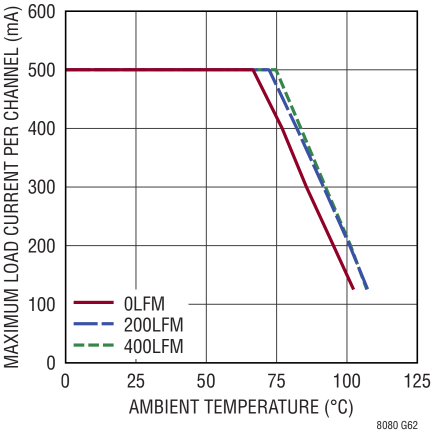
Thermal Derating 24V_{IN} to 5V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



Thermal Derating 36V_{IN} to 5V_{OUT}, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



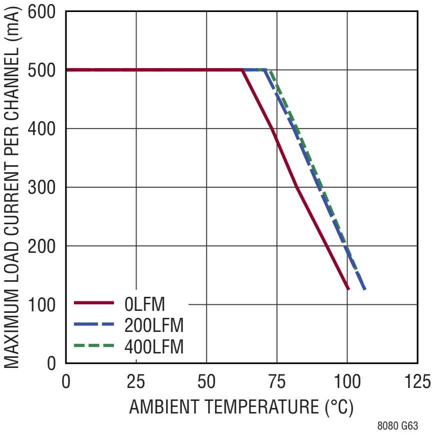
Thermal Derating 24V_{IN} to 8V_{OUT}, I_{BUS} = 0A, $I_{OUT1,2}$ = 0.5A DC3071A Demo Board



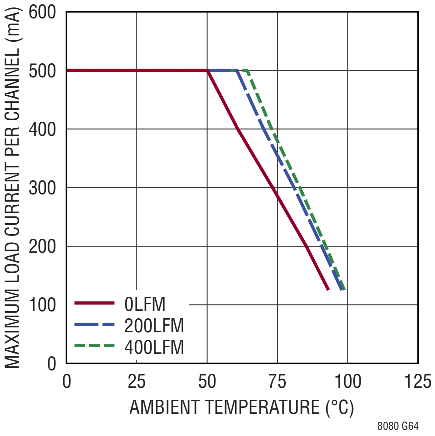
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{BUS} = V_{OUT1} + 1V$, unless otherwise noted.

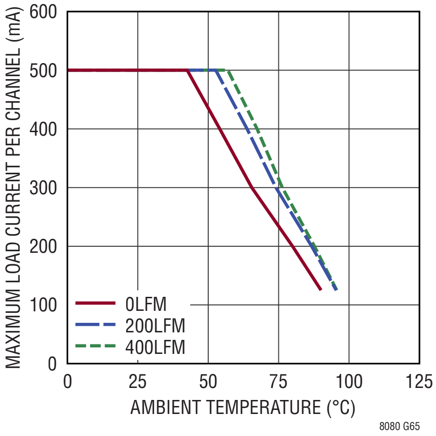
Thermal Derating $24V_{IN}$ to $8V_{OUT}$, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board



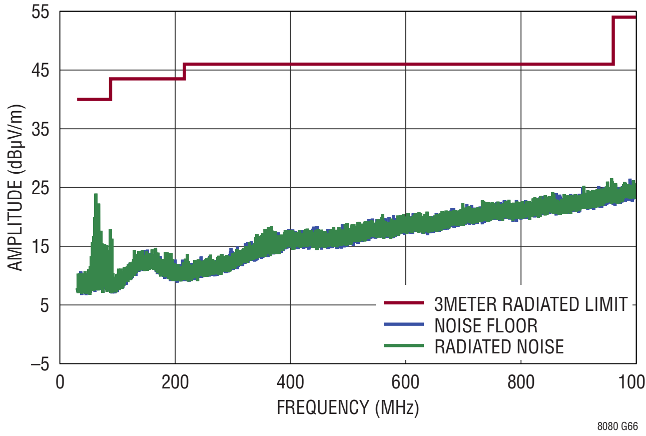
Thermal Derating $36V_{IN}$ to $8V_{OUT}$, $I_{BUS} = 0A$, $I_{OUT1,2} = 0.5A$ DC3071A Demo Board



Thermal Derating $36V_{IN}$ to $8V_{OUT}$, $I_{BUS} = I_{OUT1,2} = 0.5A$ DC3071A Demo Board

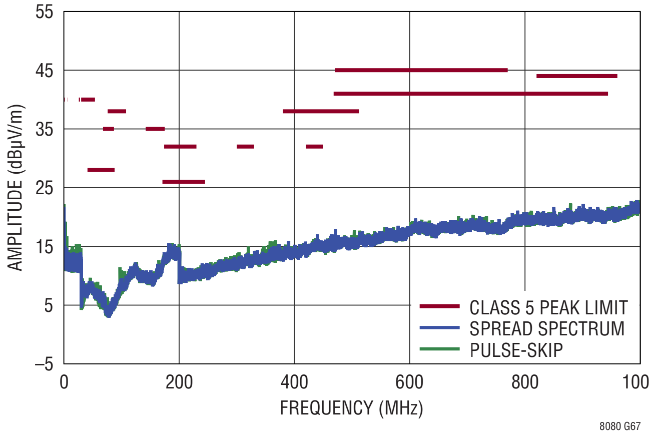


CISPR22 Class B Emissions



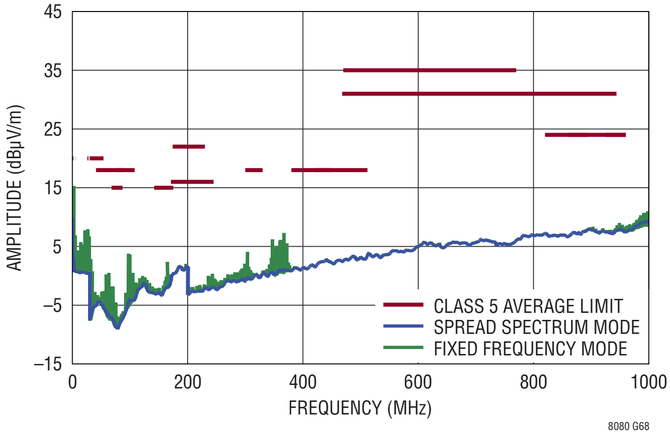
DC3071A DEMO BOARD
$V_{IN} = 24V$, $V_{OUT}1/2 = 3.3V$, $I_{OUT}1/2 = 500mA$

CISPR25 Radiated Emissions with Class 5 Peak Limits



DC3071A DEMO BOARD
$V_{IN} = 24V$, $V_{OUT}1/2 = 3.3V$, $I_{OUT}1/2 = 500mA$

CISPR25 Radiated Emissions with Class 5 Average Limits



DC3071A DEMO BOARD
$V_{IN} = 24V$, $V_{OUT}1/2 = 3.3V$, $I_{OUT}1/2 = 500mA$

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{BUS} (Bank 1): Output of the switching regulator and the inputs of LDOs. V_{BUS} = 2.5V or (V_{OUT1} + 1V), whichever is higher. V_{BUS} may deliver current based on the following formula: $I_{BUS(MAX)} = 1.5 – (I_{OUT1} + I_{OUT2})$, in amperes. Add more capacitors to these pins when necessary; see Table 1 for recommended values.

GND (Bank 2, Pins A1, A6): Tie these GND pins to a local ground plane below the LTM8080 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8080 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout sections for more details.

V_{OUTn} (Bank 3, Bank 5): Power Output Pins. These pins supply power to the load. For stability, use a minimum 10µF output capacitor with an ESR below 20mΩ and an ESL below 2nH. Large load transients require larger output capacitance to limit peak voltage transients. See the Applications Information section for more information on output capacitance. The V_{OUT2} voltage must be equal to or less than the V_{OUT1} voltage.

V_{IN} (Bank 4): V_{IN} supplies current to the LTM8080's internal regulator and to the internal power switches. These pins must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

SS (Pin A2): The SS pin is used to provide a soft-start from the switching regulator. The internal 2µA pull-up current, in combination with an external capacitor tied to this pin, creates a voltage ramp. The soft-start ramp time is approximated by the equation t = 0.39 • C where C is in µF. This pin is pulled to the ground with an internal MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating.

RUN (Pin A3): Pull the RUN pin below 0.9V to shut down the LTM8080. Tie to 1.2V or above for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin.

SYNC (Pin B6): External clock synchronization input and operational mode. This pin programs four different operating modes:

1. Burst Mode® Operation. Tie this pin to the ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current.
2. Pulse-skipping mode. Float this pin for pulse-skipping mode. This mode offers full-frequency operation down to low output loads before pulse skipping occurs.
3. Spread spectrum mode. Tie this pin high (between 2.9V and 4.2V) for pulse-skipping mode with spread spectrum modulation.
4. Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization, the part will operate in pulse-skipping mode.

RT (Pin C6): Use the RT pin to program the switching frequency of the LTM8080 by connecting a resistor from this pin to the ground. See Table 2 to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin. Do not drive this pin.

PG*n* (Pins G2, G5): Power Good. PG is an open-collector flag that indicates output voltage regulation. PG pulls low if PGFB is below 300mV. If the power good functionality is not needed, float the PG pin. A parasitic substrate diode exists between the PG and GND pins; do not drive PG more than 0.3V below GND during regular operation or a fault condition.

PIN FUNCTIONS

PGFB*n* (Pins G3, G4): Power Good Feedback. The PG pins pull high if PGFB increases beyond 300mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between V_{OUTn}, PGFB, and GND sets the programmable power good threshold with the following transfer function:

$V_{OUT(PG\_THRESHOLD)} = 0.3V \cdot (1 + R_{PG1,3}/R_{PG2,4})$

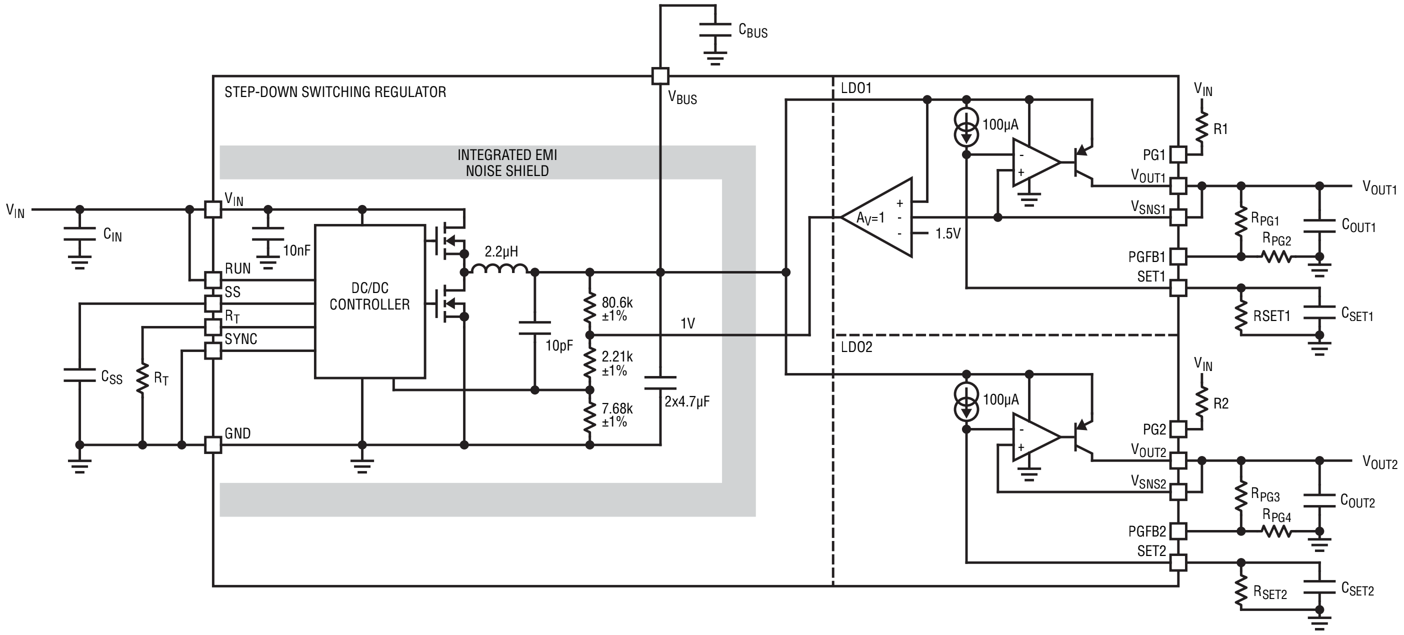
for $R_{PG2,4} \leq 30k\Omega$.

As discussed in the Applications Information section, PGFB activates fast start-up circuitry. Tie PGFB to V_{BUS} if power good and fast start-up functionalities are not needed. A parasitic substrate diode exists between the PGFB and GND pins; do not drive PGFB more than 0.3V below GND during normal operation or a fault condition.

V_{SNSn} (Pins H2, H5): Output Sense. These pins are the noninverting input to the error amplifier of the LDO. Kelvin connects V_{SNSn} directly to the output capacitor and the load for optimal transient performance and load regulation. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. A parasitic substrate diode exists between the V_{SNSn} and GND pins; do not drive V_{SNSn} more than 0.3V below GND during regular operation or a fault condition.

SET*n* (Pins H3, H4): These pins are the inverting input of the error amplifier and the regulation set-point for the LDOs. SET sources a precision 100µA current that flows through an external resistor connected between the SET and GND. $V_{SET} = I_{SET} \cdot R_{SET}$ determines the LDO's output voltage. The output voltage range is from zero to 8V. Adding a capacitor from SET to GND improves noise, PSRR, and transient response at the expense of increased start-up time. For optimum load regulation, Kelvin connects the ground side of the SET pin resistor directly to the load. A parasitic substrate diode exists between the SET and GND pins; do not drive SET more than 0.3V below GND during regular operation or a fault condition.

BLOCK DIAGRAM


C$_{BUS}$
STEP-DOWN SWITCHING REGULATOR
V$_{BUS}$
INTEGRATED EMI
NOISE SHIELD
V$_{IN}$
C$_{IN}$
V$_{IN}$
10nF
RUN
SS
R$_T$
SYNC
DC/DC
CONTROLLER
2.2µH
10pF
80.6k
±1%
2.21k
±1%
7.68k
±1%
1V
2x4.7µF
C$_{SS}$
R$_T$
GND
LDO1
100µA
A$_V$=1
1.5V
V$_{IN}$
R1
PG1
V$_{OUT1}$
V$_{SNS1}$
PGFB1
SET1
V$_{OUT1}$
R$_{PG1}$
R$_{PG2}$
C$_{OUT1}$
RSET1
C$_{SET1}$
LDO2
100µA
V$_{IN}$
R2
PG2
V$_{OUT2}$
V$_{SNS2}$
PGFB2
SET2
V$_{OUT2}$
R$_{PG3}$
R$_{PG4}$
C$_{OUT2}$
R$_{SET2}$
C$_{SET2}$

OPERATION

The LTM8080 is a $40V_{IN}$, dual 500mA or single 1A ultralow noise, ultrahigh PSRR µModule regulator. The LTM8080 has cascaded architecture with a $40V_{IN}$ step-down Silent Switcher regulator and dual high-performance low-dropout linear regulators. The dual LDOs feature ADI's ultralow noise and ultrahigh PSRR architecture for powering noise-sensitive applications. The LTM8080 is an integrated solution of a switching regulator and two LDOs, which offers both advantages while maintaining a small size and significantly reduced PCB layout sensitivity.

The package includes the controllers, power switches, inductors, and support components. Operating over a wide input voltage range, the LTM8080 supports a switching frequency range of 200kHz to 2.2MHz and a wide output voltage range of 0V to 8V.

The LTM8080 has a built-in voltage tracking function that automatically sets V_{BUS} to 1V higher than the V_{SNS1} or sets V_{BUS} to 2.5V, whichever is higher, to achieve the best noise performance and minimized power dissipation.

Switching Regulator

The front-end switching regulator is a nonisolated step-down switching DC/DC power supply that can deliver up to 1.5A continuous current. The internal operating temperature determines the continuous current. If V_{SNS1} is higher than 1.5V, V_{BUS} is regulated to be 1V higher than V_{SNS1}; if V_{SNS1} is lower than 1.5V, V_{BUS} is set to 2.5V. The input voltage range is 3.5V to 40V. Given that the switching regulator is a step-down converter, ensure that the input voltage is high enough to support the desired output voltage and load current. See the simplified Block Diagram.

The front-end switching regulator contains a current mode controller, power switching elements, a power inductor, and a modest input and output capacitance. The switching regulator is a fixed-frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

Use the RUN pin to place the switching regulator in shutdown, reducing the input current to a few microamps.

To enhance efficiency, tie the SYNC pin to GND so the switching regulator automatically switches to Burst Mode operation in light or no-load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to just a few microamps.

The oscillator reduces the switching regulator's operating frequency when the voltage at the internal FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

A soft-start is implemented by generating a voltage ramp at the SS pin using an external capacitor that is charged by a constant internal current.

The switching regulator is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with regular operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the device's reliability.

Linear Regulators

The back-end linear regulators are high-performance low dropout linear regulators featuring ADI's ultralow noise ($2nV/\sqrt{Hz}$ at 10kHz) and ultrahigh PSRR (76dB at 1MHz) architecture for powering noise-sensitive applications. Designed as a precision current source followed by a high-performance rail-to-rail voltage buffer, the LDO outputs can be easily paralleled to reduce noise further, increase output current, and spread heat on the PCB. The device additionally features fast start-up capability and programmable power good.

The LDOs are easy to use and incorporate all the protection features expected in high-performance regulators. Included are short-circuit protection, safe operating area protection, reverse-battery protection, reverse-current protection, and thermal shutdown with hysteresis.

The V_{OUT1} LDO incorporates a VIOC tracking function to control the front-end switching regulator to maintain a 1V constant voltage across the LDO V_{OUT1} and minimize power dissipation.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward, summarized as follows:

1. See Table 1 and find the row with the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{BUS}, C_{OUT}, C_{SET}, R_{SET}, and R_T values.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental conditions. Remember that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude, and other factors. See the graphs in the Typical Performance Characteristics section for more details.

The recommended frequency (and attendant R_T value) at which the LTM8080 is optimal for efficiency over the given input condition is shown in the f_{SW} column in Table 1. Additional conditions must be satisfied if the synchronization function is used. See the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those shown in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable and can yield improved dynamic response if necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental conditions.

Ceramic capacitors are small, robust, and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U, have very large temperature and voltage coefficients of capacitance. In an application circuit, they may have only a tiny fraction of their nominal capacitance resulting in a much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8080's switching frequency depends on the load current and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8080 operates at a lower current limit during Burst-Mode operation, the noise is typically very quiet to a casual ear. If this audible noise is unacceptable, use a high-performance electrolytic capacitor at V_{BUS}. It may also be a parallel combination of a ceramic capacitor and a low-cost electrolytic capacitor.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}* (V)	V_{OUT} (V)	V_{BUS} (V)	R_{SET} (kΩ)	C_{SET}	C_{IN}**	C_{BUS}	C_{OUT}	f_{SW}	R_T (kΩ)
3.5 to 40	0.8	2.5	8.06	4.7µF 4V	1µF 50V	22µF 6.3V	10µF 4V	800kHz	52.3
3.5 to 40	1	2.5	10	4.7µF 4V	1µF 50V	22µF 6.3V	10µF 4V	800kHz	52.3
3.5 to 40	1.2	2.5	12.1	4.7µF 4V	1µF 50V	22µF 6.3V	10µF 4V	800kHz	52.3
3.5 to 40	1.5	2.5	15	4.7µF 4V	1µF 50V	22µF 6.3V	10µF 4V	800kHz	52.3
3.5 to 40	1.8	2.8	18.2	4.7µF 4V	1µF 50V	22µF 6.3V	10µF 4V	900kHz	46.4
4.5 to 40	2	3	20	4.7µF 4V	1µF 50V	22µF 6.3V	10µF 4V	1MHz	40.2
5 to 40	2.5	3.5	24.9	4.7µF 6.3V	1µF 50V	10µF 10V	10µF 6.3V	1.1MHz	36.5
6 to 40	3.3	4.3	33.2	4.7µF 6.3V	1µF 50V	10µF 10V	10µF 6.3V	1.2MHz	33.2
9 to 40	5	6	49.9	4.7µF 10V	1µF 50V	10µF 16V	10µF 10V	1.3MHz	30.1
15 to 40	8	9	80.6	4.7µF 16V	1µF 50V	10µF 16V	10µF 16V	1.5MHz	24.3

*The LTM8080 may be capable of lower input voltages but may skip switching cycles or reduce its operating frequency.

**An input bulk capacitor is required.

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A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8080. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8080 circuit is plugged into a live supply, the input voltage can ring twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8080 uses a constant-frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	221
0.3	143
0.4	110
0.5	86.6
0.6	71.5
0.7	60.4
0.8	52.3
0.9	46.4
1.0	40.2
1.2	33.2
1.4	27.4
1.6	23.7
1.8	20.5
2	18.2
2.2	16.2

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value shown in Table 1 for the input and output operating conditions. System level or other considerations, however, may necessitate another operating frequency. While the LTM8080 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM8080 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much V_{BUS} ripple or too large of a V_{BUS} capacitor.

Maximum Load

The maximum practical continuous load that the LTM8080 can drive, while rated at 500mA per channel, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8080 in the case of overload or short-circuit. The internal temperature of the LTM8080 depends upon operating conditions such as the ambient temperature, the power delivered, and the system's heat-sinking capability. For example, if the output voltage is 8V and the ambient temperature is 85°C, the LTM8080 will provide at most 200mA from $36V_{IN}$, less than the 500mA continuous rating. See the derating curves in the Typical Performance Characteristics section.

Load Sharing

The two LTM8080 channels may be paralleled to produce a higher current. To do this, tie the V_{OUTn}, V_{SNSn}, and V_{SETn} pins of all the paralleled channels together. Connect the V_{OUTn} pins using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LTM8080 outputs. PCB trace resistance in milliohms/inch is shown in Table 3.

Table 3. PC Board Trace Resistance*

WEIGHT (oz)	WIDTH (10mil)	WIDTH (20mil)
1	54.3	27.1
2	27.1	13.6

*Trace resistance is measured in mΩ/in.

The slight worst-case offset of 2mV for each output minimizes the required ballast resistor value. Figure 1 shows that LTM8080 two outputs, each using a 20mΩ PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 20mΩ external resistors only add 10mV of output regulation drop with a 1A maximum current. A 3.3V output, only adds 0.3% to the regulation accuracy. Tie the V_{SNSn} pin directly to each output capacitor, respectively. The Typical Applications

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section gives an example of both channels of the LTM8080 configured for load sharing. When load sharing among n channels and using a single R_{SET} resistor, the value of the resistor is shown in Equation 1.

$$R_{SET} = \frac{V_{OUT}}{n \bullet 100\mu A} \quad (1)$$

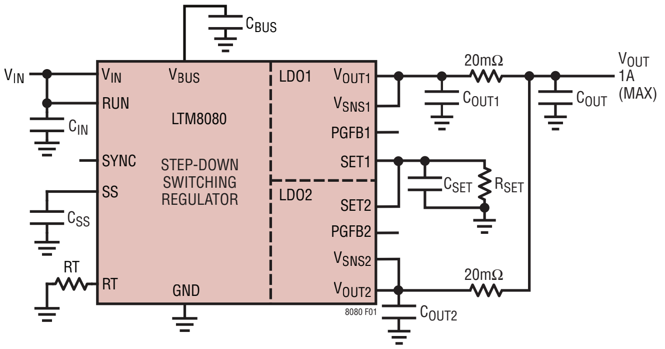


Figure 1. Paralleling Two Channels of LTM8080

Burst-Mode Operation

To enhance efficiency at light loads, the LTM8080 can be configured to Burst Mode operation, which keeps the V_{BUS} capacitor charged to the proper voltage while minimizing the quiescent input current. During Burst Mode operation, the LTM8080 delivers single-cycle bursts of current to the V_{BUS} capacitor, followed by sleep periods where most of the internal circuitry is powered off, and energy is provided to the LDOs by the V_{BUS} capacitor. During sleep time, V_{IN} quiescent current is significantly reduced, so as the load current decreases towards a no-load condition, the percentage of time that the LTM8080 operates in sleep mode increases, and the average input current are significantly reduced, resulting in higher light load efficiency. Burst Mode operation is enabled by tying SYNC to GND.

Minimum Input Voltage

The LTM8080's front end is a step-down converter, so a minimum headroom is required to keep the output in regulation. Keep the input above 3.5V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3.5V may turn off the LTM8080.

V_{BUS} Soft-Start

The LTM8080 allows the user to program its V_{BUS} voltage ramp rate using the SS pin. An internal 2µA pulls up the SS pin to about 3.1V. Putting an external capacitor on SS enables soft-starting the V_{BUS} to reduce current surges on the input supply. The V_{BUS} voltage will proportionally track the SS pin voltage during the soft-start ramp. When the SS voltage exceeds 0.778V, the internal feedback voltage will take over and regulate the internal reference voltage. The SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the SS pin, which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the RUN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

See the Set PIN (Bypass) Capacitance: Noise, PSRR, Transient Response, and V_{OUT} Soft-Start section for the output soft-start function.

Prebiased Output

As the LTM8080 regulates the V_{OUT} to V_{SET}, if the LTM8080 output is higher than the target output voltage, the LTM8080 cannot regulate the output to target output voltage.

V_{BUS} can be used as an auxiliary supply, so care should be taken if the V_{BUS} voltage is higher than the target V_{BUS} voltage. The LTM8080 front-end switching regulator will attempt to regulate the V_{BUS} voltage to the target V_{BUS} voltage by returning a small amount of energy back to the input supply. If nothing is loading the input supply, its voltage may rise. Take care that it stays high enough that the input voltage is, at most, the absolute maximum rating of the LTM8080.

Frequency Foldback

The LTM8080 is equipped with frequency foldback, which reduces the thermal and energy stress on the internal power elements during a short-circuit or output overload condition. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially

APPLICATIONS INFORMATION

large output capacitance of the load. However, when a clock is applied to the SYNC pin, the frequency foldback is disabled.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). Then, to synchronize the LTM8080 oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys below 0.4V and peaks above 1.5V.

The LTM8080 may be synchronized over a 200kHz to 2.2MHz range. The LTM8080 will not enter Burst Mode operation at light output loads while synchronized to an external clock but instead will pulse-skip to maintain regulation. The R_T resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal is 500kHz and higher, the R_T should be selected for 500kHz or lower frequency.

The LTM8080 features spread-spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, apply between 2.9V and 4.2V to the SYNC pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to about 20% higher than that value. The modulation frequency is about 3kHz. When the spread-spectrum operation is selected, the Burst-Mode operation is disabled, and the part may run in pulse-skipping mode.

PSRR

While the high-level integration of the LTM8080 solves most headache routing to achieve ultrahigh PSRR, ADI still recommends using the LTM8080 demo board layout and the input/output capacitances shown in Table 1 for achieving the best possible PSRR performance.

Output Noise

LTM8080 back-end linear regulator uses a 100µA current reference to define output voltage. This current reference operates with a typical noise current level of $20\text{pA}/\sqrt{\text{Hz}}$ (6nA_{RMS} over a 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor value, which in turn is RMS summed with the error amplifier's noise and the resistor's noise of $\sqrt{4kTR}$, where by k = Boltzmann's constant $1.38 \cdot 10^{-23}$J/K and T is the absolute temperature.

Conventional linear regulators use a resistor divider to set the output voltage. This method gains the reference noise and injects that noise onto the output. The LTM8080 uses the ADI patented unity-gain follower architecture to set the output voltage. This unique architecture does not gain any noise present at the SET pin, thereby minimizing noise injected into the output. Therefore, if a capacitor bypasses the SET pin resistor, the output noise is independent of the programmed output voltage. The resultant output noise is set just by the error amplifier's noise—typically $2\text{nV}/\sqrt{\text{Hz}}$ from 10kHz to 1MHz and $0.8\mu\text{V}_{\text{RMS}}$ in a 10Hz to 100kHz bandwidth using a 4.7µF SET pin capacitor. Therefore, paralleling multiple LTM8080 outputs will reduce noise by $\sqrt{N}$ for N outputs.

See the Typical Performance Characteristics section for noise spectral density, and RMS-integrated noise over various load current and SET pin capacitances.

Set PIN (Bypass) Capacitance: Noise, PSRR, Transient Response, and V_{OUT} Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor improves PSRR and transient performance. Note that any bypass capacitor leakage deteriorates the LTM8080 output DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, ADI recommends using a good quality low leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. The RC time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Ramp-up rate from 0 to 90% of nominal V_{OUT} is shown in Equation 2.

$$t_{SS} \approx 2.3 \cdot R_{SET} \cdot C_{SET} \text{ (Fast Start-Up Disabled)} \quad (2)$$

APPLICATIONS INFORMATION

V_{OUT} Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. While this would typically significantly increase the regulator's start-up time, the LTM8080 incorporates fast start-up circuitry that increases the SET pin current to about 2mA during start-up.

A 2mA current source remains engaged to charge the SET pin while the respective PGFB is below 300mV unless the regulator is in current limit, dropout, thermal shutdown, or the input voltage is below minimum V_{IN}.

If fast start-up capability is not used, tie PGFB*n* to V_{BUS} or V_{OUT} for output voltages above 300mV. Note that doing so also disables power good functionality.

Programmable Power Good

The power good threshold is user-programmable using the ratio of two external resistors, $R_{PG1,3}$ and $R_{PG2,4}$ (see the Block Diagram and Equation 3).

$$V_{OUT(PG\_THRESHOLD)} = 0.3V \bullet \left(1+\frac{R_{PG1,3}}{R_{PG2,4}}\right) - I_{PGFB} \bullet R_{PG1,3} \quad (3)$$

If the PGFB pin increases above 300mV, the respective open-collector PG pin de-asserts and becomes high impedance. The power good comparator has 7mV hysteresis and 5µs of deglitching. Therefore, the PGFB pin current (I_{PGFB} = 25nA, typically) must be considered when determining the resistor divider network. The PGFB pin current (I_{PGFB}) can be ignored if $R_{PG2,4}$ is less than 30k. If power good functionality is not used, float the PG pin. Note that programmable power good and fast start-up capabilities are disabled for output voltages below 300mV.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8080. The LTM8080 is, nevertheless, a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with a high level of integration, you may fail to achieve specified operations with a haphazard or poor layout. See Figure 2 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place C_{SET}, R_{SET}, C_{OUT}, C_{BUS}, and R_T as close to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8080.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8080.
4. Place the C_{IN} and C_{BUS} capacitors so that their ground current flows directly adjacent to or underneath the LTM8080.
5. Connect all the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8080.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias, as shown in Figure 2. The LTM8080 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use tiny holes. Therefore, it should employ more thermal vias than a board that uses larger holes.

APPLICATIONS INFORMATION

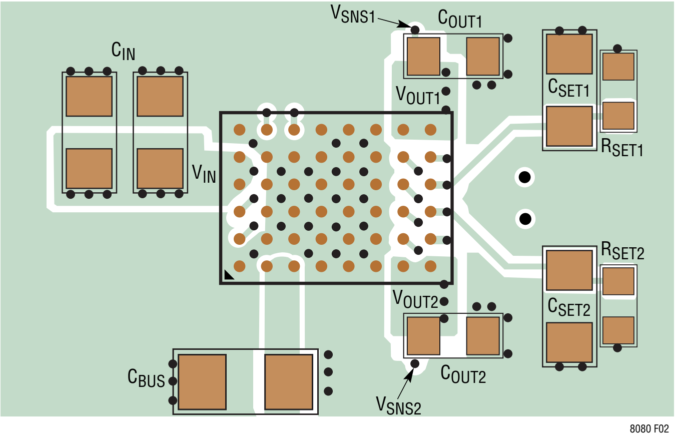


Figure 2. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM8080. However, these capacitors can cause problems if the LTM8080 is plugged into a live supply (Refer to ADI Application Note 88 for a complete discussion). The low-loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pins of the LTM8080 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8080's rating and damaging the part. The input network should be designed to prevent this overshoot if the input supply is poorly controlled or the LTM8080 is hot-plugged into an energized supply. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low-frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the most significant component in the circuit.

Thermal Considerations

The LTM8080 output current may need to be derated if it is required to operate at a high ambient temperature. The amount of current derating depends upon the input voltage, output power, and ambient temperature. The derating curves in the Typical Performance Characteristics section can be used as a guide. The LTM8080 generated these curves mounted to a 65.8cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer counts can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental operating conditions.

Many designers use FEA (finite element analysis) to predict thermal performance for increased accuracy and fidelity to the actual application. The data sheet typically gives three thermal coefficients:

1. θ_{JA} – Thermal resistance from junction to ambient.
2. θ_{JCbot} – Thermal resistance from the junction to the bottom of the product case.
3. θ_{JCtop} – Thermal resistance from junction to the top of the product case.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12 and are as follows:

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as "still air," although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.

APPLICATIONS INFORMATION

3. θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions don't generally match the user's application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none can be individually used to predict the product's thermal performance accurately. Likewise, it would be inappropriate to attempt to use anyone coefficient to correlate to the junction temperature vs load graphs given in the product's datasheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all thermal resistances simultaneously.

A graphical approximation of these dominant thermal resistances is shown in Figure 3. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard and are not shown. The blue resistances are contained within the µModule regulator, and the green is outside.

The die temperature of the LTM8080 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8080. The bulk of the heat flow out of the LTM8080 is through the bottom of the package and the pads into the printed circuit board. Consequently, a poorly printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. See the PCB Layout section for printed circuit board design suggestions.

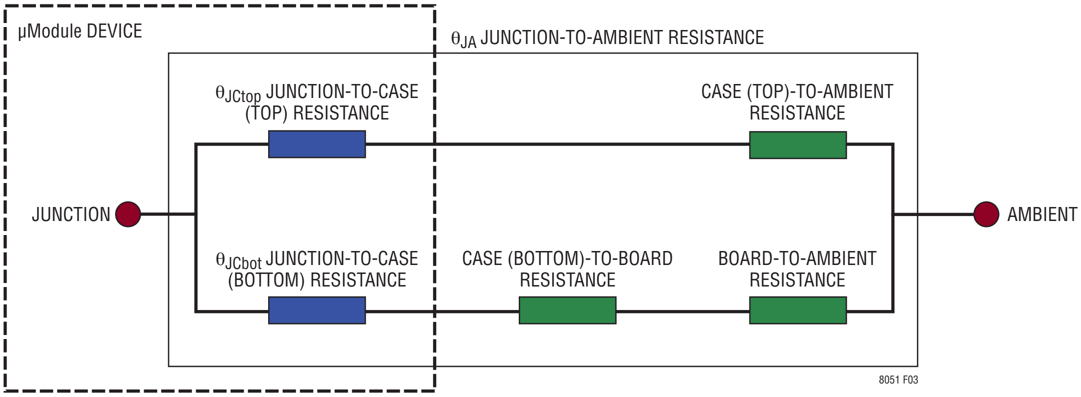
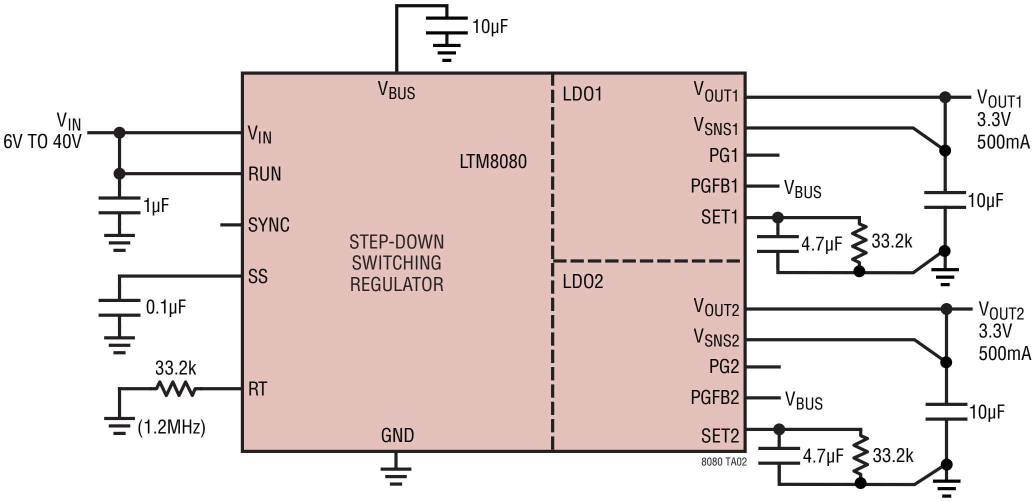

µModule DEVICE
θJA JUNCTION-TO-AMBIENT RESISTANCE
θJCtop JUNCTION-TO-CASE (TOP) RESISTANCE
CASE (TOP)-TO-AMBIENT RESISTANCE
JUNCTION
AMBIENT
θJCbot JUNCTION-TO-CASE (BOTTOM) RESISTANCE
CASE (BOTTOM)-TO-BOARD RESISTANCE
BOARD-TO-AMBIENT RESISTANCE
8051 F03

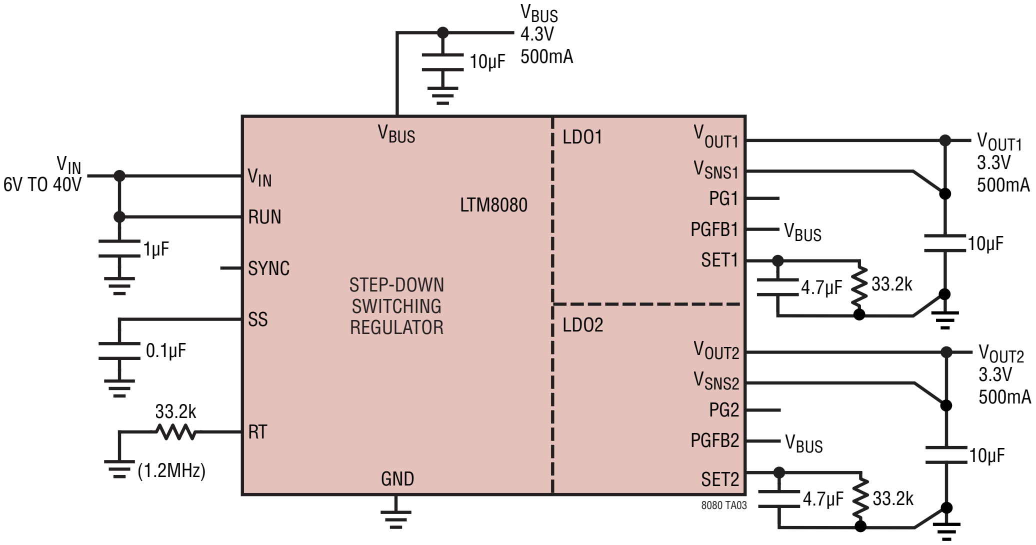
Figure 3. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

TYPICAL APPLICATIONS

Dual 3.3V LDO Outputs from 6V to 40V Input

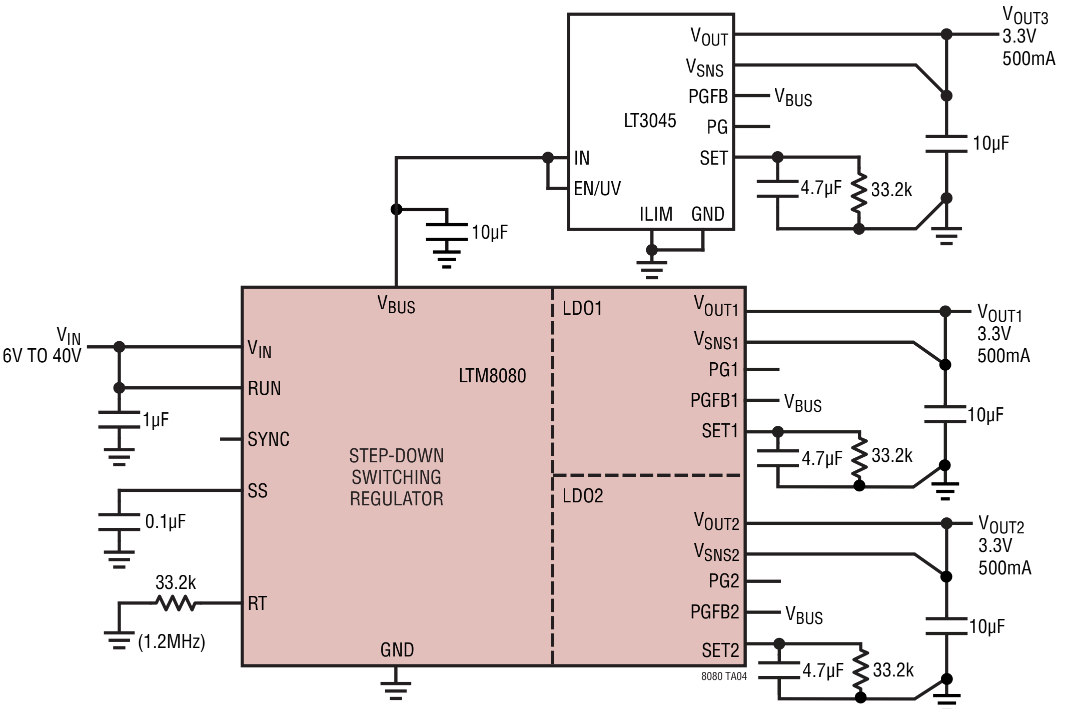

10µF
VBUS
LTM8080
STEP-DOWN
SWITCHING
REGULATOR
VIN
6V TO 40V
VIN
RUN
1µF
SYNC
SS
0.1µF
33.2k
RT
(1.2MHz)
GND
LDO1
VOUT1
VSNS1
PG1
PGFB1
SET1
VBUS
4.7µF
33.2k
VOUT1
3.3V
500mA
10µF
LDO2
VOUT2
VSNS2
PG2
PGFB2
SET2
VBUS
4.7µF
33.2k
VOUT2
3.3V
500mA
10µF
8080 TA02

4.3V Switcher Output and Dual 3.3V LDO Outputs from 6V to 40V Input


VBUS
4.3V
500mA
10µF
VBUS
LTM8080
STEP-DOWN
SWITCHING
REGULATOR
VIN
6V TO 40V
VIN
RUN
1µF
SYNC
SS
0.1µF
33.2k
RT
(1.2MHz)
GND
LDO1
VOUT1
VSNS1
PG1
PGFB1
SET1
VBUS
4.7µF
33.2k
VOUT1
3.3V
500mA
10µF
LDO2
VOUT2
VSNS2
PG2
PGFB2
SET2
VBUS
4.7µF
33.2k
VOUT2
3.3V
500mA
10µF
8080 TA03

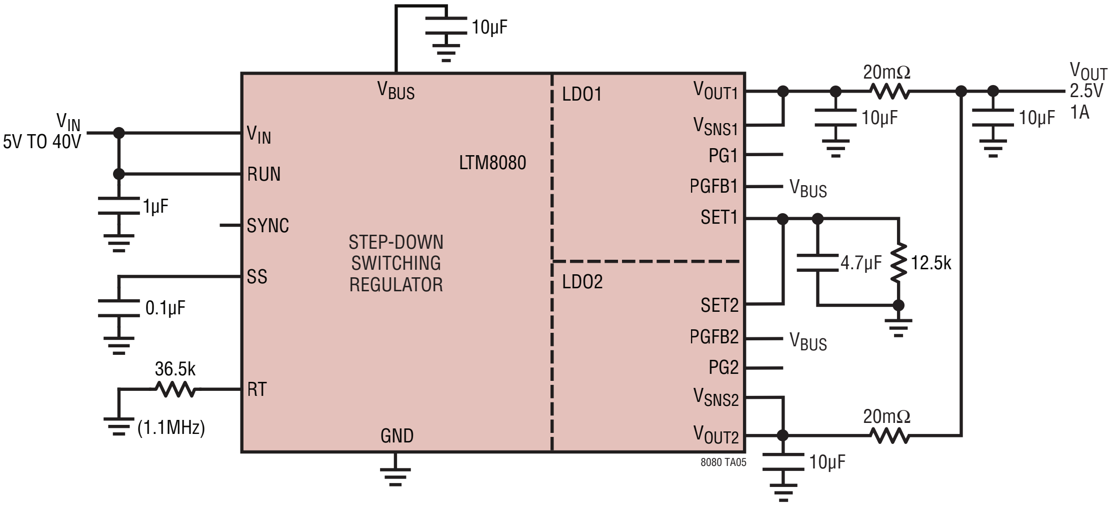
TYPICAL APPLICATIONS

Triple 3.3V LDO Outputs from 6V to 40V Input



LT3045
VOUT
VSNS
PGFB
PG
SET
IN
EN/UV
ILIM
GND
VBUS
VOUT3
3.3V
500mA
10µF
4.7µF
33.2k
10µF
LTM8080
STEP-DOWN
SWITCHING
REGULATOR
LDO1
LDO2
VIN
6V TO 40V
VIN
RUN
SYNC
SS
RT
GND
1µF
0.1µF
33.2k
(1.2MHz)
VOUT1
VSNS1
PG1
PGFB1
SET1
VOUT1
3.3V
500mA
VOUT2
VSNS2
PG2
PGFB2
SET2
VOUT2
3.3V
500mA
8080 TA04

Paralleled LDOs for a Single 2.5V, 1A Output



10µF
VBUS
LTM8080
STEP-DOWN
SWITCHING
REGULATOR
LDO1
LDO2
VIN
5V TO 40V
VIN
RUN
SYNC
SS
RT
GND
1µF
0.1µF
36.5k
(1.1MHz)
VOUT1
VSNS1
PG1
PGFB1
SET1
SET2
PGFB2
PG2
VSNS2
VOUT2
20mΩ
20mΩ
4.7µF
12.5k
VOUT
2.5V
1A
8080 TA05

PACKAGE DESCRIPTION

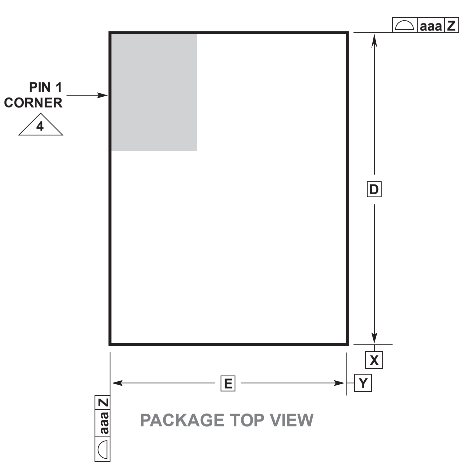
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

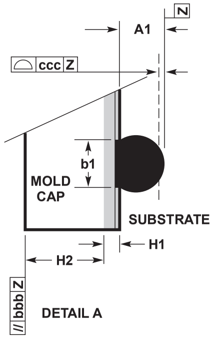
Table 4. LTM8080 Pinout (Sorted by Pin Number)

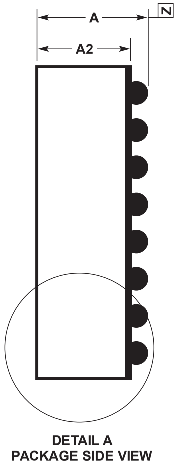
PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
A6	GND	B6	SYNC	C6	RT	D6	GND	E6	GND	F6	GND	G6	V_{OUT1}	H6	V_{OUT1}
A5	V_{IN}	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND	G5	PG1	H5	V_{SNS1}
A4	V_{IN}	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND	G4	PGFB1	H4	SET1
A3	RUN	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND	G3	PGFB2	H3	SET2
A2	SS	B2	GND	C2	GND	D2	GND	E2	GND	F2	GND	G2	PG2	H2	V_{SNS2}
A1	GND	B1	V_{BUS}	C1	V_{BUS}	D1	GND	E1	GND	F1	GND	G1	V_{OUT2}	H1	V_{OUT2}

PACKAGE DESCRIPTION

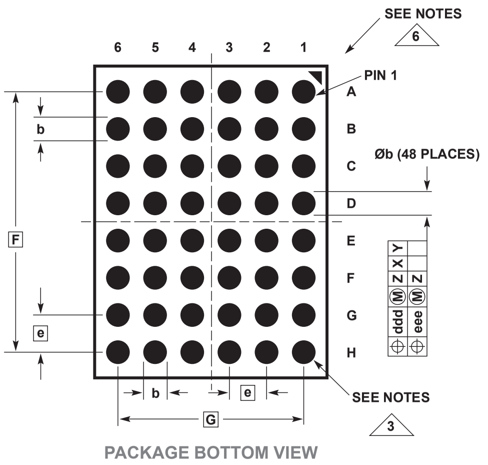
48-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
9mm × 6.25mm × 3.32mm
(Reference DWG # 05-08-1999)

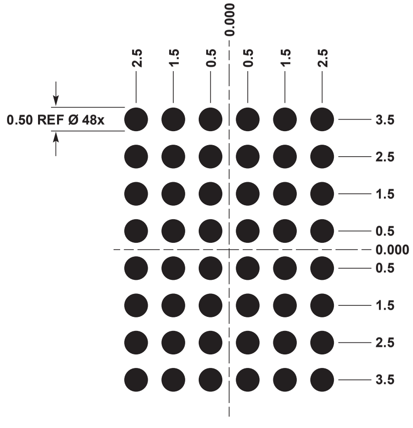

aaa Z
PIN 1
CORNER
4
D
X
E
Y
aaa Z
PACKAGE TOP VIEW


A1
Z
ccc Z
b1
MOLD
CAP
SUBSTRATE
H1
H2
// bbb Z
DETAIL A



DETAIL A
PACKAGE SIDE VIEW


SEE NOTES
6
6 5 4 3 2 1
PIN 1
A
B
C
D
E
F
G
H
Øb (48 PLACES)
ddd M Z X Y
eee M Z
b
F
e
b
e
G
SEE NOTES
3
PACKAGE BOTTOM VIEW


2.5
1.5
0.5
0.000
0.5
1.5
2.5
0.50 REF Ø 48x
3.5
2.5
1.5
0.5
0.000
0.5
1.5
2.5
3.5
SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTES
A	3.12	3.32	3.52	
A1	0.40	0.50	0.60	BALL HT
A2	2.72	2.82	2.92	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		9.00		
E		6.25		
e		1.00		
F		7.00		
G		5.00		
H1		0.32 REF		SUBSTRATE THK
H2		2.50 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.25	
eee			0.10	
TOTAL NUMBER OF BALLS: 48				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

3 BALL DESIGNATION PER JEP95

4 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

5. PRIMARY DATUM -Z- IS SEATING PLANE

6 ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

08-10-2022-C

Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	11/22	Initial Release	—
A	5/23	Corrected maximum V_{OUT} for noise measurements Corrected V_{OUTn} noise waveforms Updated efficiency curve labels Updated PGFBn pin description equation Updated block diagram	3, 5, 6, 13, 14

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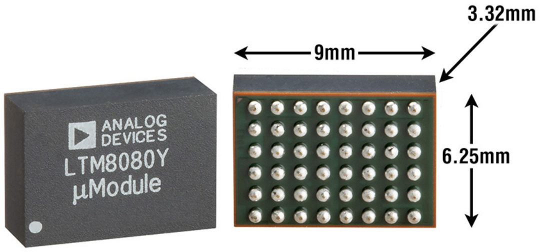
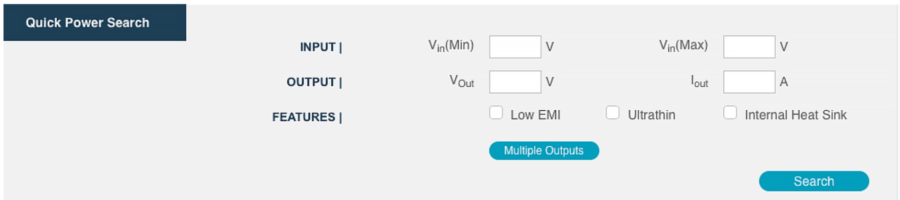
PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table.  Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | ☐ Low EMI ☐ Ultrathin ☐ Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8063	40V, 2A Step-Down Silent Switcher µModule Regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 15V, 4mm × 6.25mm × 2.22mm BGA Package
LTM8065	40V, 2.5A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA Package
LTM8053	40V, 3.5A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA
LTM8078	40V, Dual 1.4A Step-Down Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 10V, 6.25mm × 6.25mm × 2.32mm BGA Package
LTM8024	40V, Dual 3.5A Step-Down Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 9mm × 11.25mm × 3.32mm BGA Package
LTM8051	40V, Quad 1.2A Step-Down Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 6.25mm × 11.25mm × 2.32mm BGA Package
LTM8060	40V, Quad 3A Step-Down Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 11.9mm × 16mm × 3.32mm BGA Package

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