Click here for production status of specific part numbers.

MAX16602

VR13.HC and AI Cores Dual-Output Voltage Regulator Chipset

General Description

The MAX16602 IC provides a high-density, flexible and scalable solution to power AI cores or Intel® VR13.HC server CPUs. This Maxim controller IC employs coupled inductors and smart power-stage ICs to implement high-efficiency core regulators with enhanced transient response and low-quiescent current. An additional single-phase output generates the VSA rail in the system using a single-phase smart power stage. The complete circuit is a highly efficient (8+1) multiphase synchronous buck converter with extensive status and parameter-measurement features. The controller also supports PWM paralleling to control up to 16 phases. A single, scalable PCB design with appropriate smart power-stage IC selection can be used to produce regulators with a wide range of current ratings.

The IC's architecture simplifies design, reduces component count, enables advanced power management and telemetry, and increases energy savings over the full load range. Autonomous phase-shedding is implemented to maintain high efficiency across the entire load range.

Regulator parameters for protection and shutdown can be set and monitored through the serial interface using the PMBus™ protocol. Power-stage faults, input and output voltage, input and output current, input power, and the temperature of each smart power-stage IC are readable over the serial interface. The critical fault retention feature prevents exothermic events after a power-device fault. The smart power-stage ICs communicate with the controller IC through analog and digital signals that are also readable through the registers in the controller IC. Preset and user configurations are programmed in nonvolatile memory (NVM). MTP-programmable NVM circuits allow for seven field modifications.

An integrated 3.3V to 1.8V regulator supports both MAX16602 and power-stage ICs with 1.8V bias supplies. SNS_PS_BIAS monitoring also allows for flexible bias and sequencing.

The MAX16602 is available in a 56-pin, 7mm x 7mm QFN package.

***Ordering Information* appears at end of data sheet.**

Intel is a registered trademark of Intel Corporation.

PMBus is a trademark of SMIF, Inc.

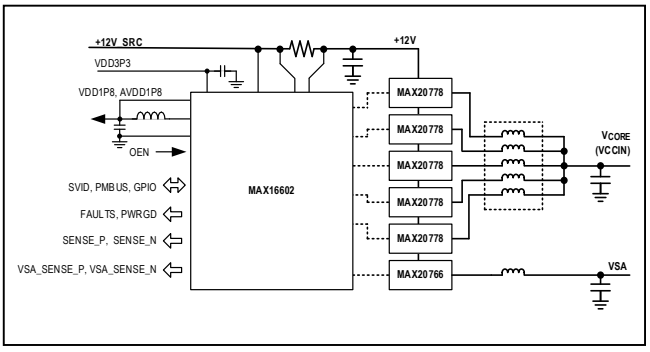
Benefits and Features

- High Power Density and Efficiency
  - Smart Power-Stage Support: MAX20778/A, MAX20779/A/B/C, MAX20780, MAX20790, MAX16604
  - Top-Tier Efficiency (95.6% Peak Efficiency at $1.8V_{OUT}$)
  - Integrated Input Power Monitor
- Telemetry Through PMBus
  - Digitally Programmable Configuration
  - Input Voltage, Current, and Power Monitoring
  - Power-Stage Temperature Monitoring and Reporting
- Advanced Power Management
  - Autonomous Phase-Shedding
  - Orthogonal Current Rebalance for Phase-Current Balance During Transients
  - Low-Quiescent Current—Improves Light-Load and Standby Efficiency
- Protection Features
  - Input and Bias Supply Undervoltage Protection
  - Overcurrent Protection
  - Critical Fault-Flag Output Pin

Applications

- High-Current Multiphase Voltage Regulators
  - AI Cores and XPUs
  - VR13.HC CPUs and Memory
  - Graphics Processors
  - Networking ASICs
- Servers and Workstations
- Enterprise Storage
- Communications and Networking Equipment Supply

Typical Operating Circuit



19-100634; Rev 1; 4/20

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Absolute Maximum Ratings

AV_{DD1P8} to AGND .....-0.3V to +2.4V
DVDD1P8 to DGND .....-0.3V to +2.4V
V_{DD3P3} to DGND .....-0.3V to +4V
SNS_PS_BIAS to DGND ..... -0.3V to V_{DD3P3} + 0.3V
CORE_SENSE_P to AGND ..... -0.3V to AV_{DD1P8} + 0.3V
PMBUS_A, PMBUS_D,
PMBUS_C to DGND ..... -0.3V to V_{DD3P3} + 0.3V
SVID_A, SVID_D to DGND..... -0.3V to AV_{DD1P8} + 0.3V
SVID_C to DGND.....-0.3V to + 2.4V
GPIO_0, GPIO_1,
GPIO_2 to DGND (Note 1)..... -0.3V to V_{DD3P3} + 0.3V
IC to DGND .....-0.3V to +7.5V
OEN, OVP, VR_HOT, FAULT to DGND.....-0.3V to +4V
PWRGD_CORE, VSA_PWRGD to DGND .....
.....-0.3V to V_{DD3P3} + 0.3V
PIN_ALERT to DGND ..... -0.3V to V_{DD3P3} + 0.3V
CORE_SENSE_N to AGND..... -0.3V to AV_{DD1P8} + 0.3V
VSA_SENSE_P, VSA_SENSE_N to AGND
..... -0.3V to AV_{DD1P8} + 0.3V
ADDR, PROG to AGND ..... -0.3V to AV_{DD1P8} + 0.3V
PWM_<7:0>, PWM_VSA, TSENSE_<3:0>,
TSENSE_VSA to DGND.....-0.3V to $V_{DVDD1P8}$ + 0.3V
ISENSE_<7:0>, ISENSE_VSA
to AGND ..... -0.3V to AV_{DD1P8} + 0.3V
VX to PGND ..... -0.3V to V_{DD3P3} + 0.3V
V_{IN}, SNS_IN_P, SNS_IN_N to AGND.....-0.3V to +13.7V
AGND to DGND .....-0.3V to +0.3V
PGND to DGND .....-0.3V to +0.3V
Junction Temperature (T_J).....+150°C
Storage Temperature Range..... -65°C to +150°C
Peak Reflow Temperature Lead-Free .....+260°C

Note 1: *Not higher than +2.4V if used for analog input functions.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56 QFN	
Package Code	G5677+2
Outline Number	**21-100073**
Land Pattern Number	**90-0455**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	29.5°C/W
Junction to Case (θ_{JC})	2.6°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES AND SUPPLY CURRENT							
Bias Supply Voltage Range	$V_{AVDD1P8}$, $V_{DVDD1P8}$			1.7		1.9	V
	V_{DD3P3}			3.0		3.6	V
1.8V Bias Supply Current	$I_{AVDD1P8}$ + $I_{DVDD1P8}$	System operational				52	mA
V_{DD3P3} Bias Supply Current	I_{VDD3P3}	1.8V switcher off (VX = 3.3V)				500	µA
OUTPUT-VOLTAGE RANGE AND ACCURACY							
Output-Voltage Range		5mV mode	CORE and VSA	0.25		1.52	V
		10mV mode	CORE only	0.5		2.3	V
DC Set-Point Tolerance	V_{OUT_VSA}	T_A = 0°C to +85°C	1.0V to 1.52V	-0.5		+0.5	%
			0.8V to 0.995V	-5		+5	mV
			0.25V to 0.795V	-8		+8	mV
	V_{OUT_CORE}	T_A = 0°C to +85°C	1.5V to 2.3V	-0.5		+0.5	%
			1V to 1.49V	-0.52		+0.52	%
			0.7V to 0.995V	-5		+5	mV
			0.5V to 0.695V	-8		+8	mV
			0.25V to 0.495V	-9		+9	mV
DC Load Line	$R_{LOADLINE}$ Range 1	Range	0xD8[5] = 0, 0xD8[1] = 1, 0xD3[7] = 0, R_{DES} = 92Ω, LSB = 7.48µΩ	0.516		0.98	mΩ
		Accuracy	T_A = 0°C to +85°C	-2.3		+2.3	%
	$R_{LOADLINE}$ Range 2	Range	0xD8[5] = 0, 0xD8[1] = 0, 0xD3[7] = 0, R_{DES} = 92Ω, LSB = 5.75µΩ	0.397		0.753	mΩ
		Accuracy	T_A = 0°C to +85°C	-2.3		+2.3	%
	$R_{LOADLINE}$ Range 3	Range	0xD8[5] = 0, 0xD8[1] = 0, 0xD3[7] = 1, R_{DES} = 73.25Ω, LSB = 4.58µΩ	0.316		0.600	mΩ
		Accuracy	T_A = 0°C to +85°C	-2.3		+2.3	%
	$R_{LOADLINE}$ Range 4	Range	0xD8[5] = 1, 0xD8[1] = 1, 0xD3[7] = 0, R_{DES} = 92Ω, LSB = 2.44µΩ	0.1735		0.325	mΩ
		Accuracy	T_A = 0°C to +85°C	-3		+3	%
	$R_{LOADLINE}$ Range 5	Range	0xD8[5] = 1, 0xD8[1] = 0, 0xD3[7] = 1, R_{DES} = 73.25Ω, LSB = 1.43µΩ	0.108		0.197	mΩ
		Accuracy	T_A = 0°C to +85°C	-5		+5	%

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CORE_SENSE_P, VSA_SENSE_P Leakage Current	$I_{CORE\_SENSE\_P}$, $I_{VSA\_SENSE\_P}$	CORE_SENSE_P = 2.3V, CORE_SENSE_N = 0V, VSA_SENSE_P = 1.52V, VSA_SENSE_N = 0V, OEN = 0			90	µA
VID TRANSITION SLEW RATE						
CORE Slew-Rate Accuracy	CORE_SR (Note 2)	Slow, including soft-start ($CORE\_SR_{SLW}$ = $CORE\_SR_{FST}$/4)	-5		+5	%
		Fast ($CORE\_SR_{FST}$ = 27mV/µs)	-5		+5	%
VSA Slew-Rate Accuracy	VSA_SR (Note 2)	Slow, including soft-start (VSA_SR_{SLW} = VSA_SR_{FST}/4)	-5		+5	%
		Fast (VSA_SR_{FST} = 10.7mV/µs)	-5		+5	%
SWITCHING FREQUENCY						
CORE Switching Frequency	f_{SW_CORE}	CORE switching-frequency range, 0.1667µs switching period step	300		857	kHz
		CORE switching-frequency accuracy	-10		+10	%
VSA Switching Frequency	f_{SW_VSA}	Low-switching frequency	599	667	735	kHz
		High-switching frequency	720	800	880	kHz
SUPPLY UVLO						
V_{DD1P8} UVLO	V_{DD1P8_UVLO}	V_{DD1P8} rising, 50mV (typ) hysteresis	1.62	1.64	1.66	V
V_{DD3P3} UVLO	V_{DD3P3_UVLO}	V_{DD3P3} rising, 50mV (typ) hysteresis	2.87	2.91	2.95	V
12V Input UVLO	V_{IN_UVLO}	V_{IN} rising, 1V (typ) hysteresis, 0xD9[5] = 0, 0xD9[3:0] = 0	9.6	10.1	10.5	V
		V_{IN} rising, 1V (typ) hysteresis 0xD9[5] = 1, 0xD9[3:0] = 0 V_{IN} divider RV_{IN_TOP} = 4.75kΩ, RV_{IN_BOT} = 19.6kΩ	9.7	10.2	10.6	V
SNS_PS_BIAS Undervoltage	$V_{PS\_BIAS\_UV}$	Power-stage supply undervoltage threshold rising; 60mV (typ) hysteresis	1.52	1.55	1.58	V
VIN_UVLO Delay to Shutdown	td_{VIN_UVLO}			5		µs
SNS_PS_BIAS Undervoltage Delay to Shutdown	$td_{SNS\_PS\_BIAS}$			5		µs

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP_CORE}, V_{OVP_VSA}	Referred to VID setting, 10mV (typ) hysteresis	5mV mode	180	200	220	mV
			10mV mode, CORE only	230	250	270	mV
Fixed Umbrella Overvoltage-Protection Threshold	$V_{UM\_OVP\_CORE}$, $V_{UM\_OVP\_VSA}$	Referred to CORE_SENSE_P, VSA_SENSE_P, 7mV (typ) hysteresis	5mV mode	2.41	2.50	2.59	V
			10mV mode, CORE only	2.41	2.50	2.59	V
Overvoltage to $\overline{OVP}$ Delay	t_{OV_DELAY}	Delay from V_{OUT} > V_{TH} to $\overline{OVP}$ asserted			700		ns
OVERCURRENT PROTECTION							
OCP Timeout and Hiccup Mode On-Time	t_{OCP}				5		ms
Hiccup Mode Off-Time	t_{HICCUP_OFF}				45		ms
CORE Positive OCP Current-Limit Range per Phase	$I_{POCP\_CORE\_PH}$	0xD8[0] = 0, LSB = 2.76A ocp_code (0xD3[3:0]) from 0 to 11		27.58		57.94	A
		0xD8[0] = 1, LSB = 5.52A ocp_code (0xD3[3:0]) from 0 to 11		55.16		115.18	A
CORE Positive OCP System Current-Limit Range	I_{POCP_CORE}	0xD8[0] = 0, I_{POCP_C} = (27.58A + 2.76A x ocp_code) x n_ph 7 and 8 phase systems with ocp_code > 5 will be clamped at n_ph = 6		27.58		347.64	A
		0xD8[0] = 1, I_{POCP_C} = (55.16A + 5.52A x ocp_code) x n_ph 7 and 8 phase systems with ocp_code > 5 will be clamped at n_ph = 6		55.16		695.28	A
CORE Positive OCP Accuracy		Range 27.58A to 38.62A		-25		+25	%
		Range 41.38A to 46.90A		-20		+20	
		Range 49.66A to 52.42A		-17		+17	
		Range 55.18A to 60.68A		-15		+15	
		Range 66.20A to 82.76A		-12.5		+12.5	
		Range 88.28A to 107.58A		-10		+10	
		Range 110.36A to 151.7A		-8		+8	
		Range 154.48A to 187.60A		-6		+6	
		Range 193.10A to 695.28A		-5		+5	
CORE Negative OCP Current-Limit Ratio to CORE Positive OCP Current Limit		0xD3[4] = 0, wrt POCP 0xD8[0] = 1			-33		%
		0xD3[4] = 1, wrt POCP 0xD8[0] = 1			-16.66		

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CORE Negative OCP Accuracy		Range -9.18A to -11.94A		-35		+35	%
		Range -12.86A to -16.54A		-30		+30	
		Range -17.46A to -20.21A		-22		+22	
		Range -22.04A to -25.72A		-20		+20	
		Range -27.56A to -31.24A		-15		+15	
		Range -33.07A to -47.77A		-12.5		+12.5	
		Range -51.44A to -231.53A		-10		+10	
VSA Positive OCP Current-Limit Range	I_{POCP_VSA}	Four typical selections: 23.5A, 28A, 35A, 40A		23.5		40	A
VSA Negative OCP Current Limit to VSA Positive OCP Current Limit	I_{NOCP_VSA}	(Note 3)			-100		%
VSA OCP Current-Limit Accuracy		POCP and NOCP		-20		+20	%
APS THRESHOLD							
Fast Threshold Accuracy		APS threshold range: 8A to 70A		-12.5		+12.5	%
POWER GOOD (CORE and VSA)							
Power-Good Threshold, Deasserting	V_{PWRGD_CORE}, V_{PWRGD_VSA}	Referred to VID, 9mV (typ) hysteresis	5mV mode (CORE)	-240	-218	-196	mV
			5mV mode (VSA)	-257	-234	-211	mV
			10mV mode, CORE only	-330	-296	-270	mV
FAULT DETECTION							
Power-Stage Fault-Detector Threshold	V_{TS_TH}	TSENSE_ pin to GND			300		mV
Power-Stage Fault-Detector Propagation Delay	$t_{TS/\overline{FAULT}}$	Delay from TSENSE to $\overline{FAULT}$			2		µs
OUTPUT PINS (PWM_, $\overline{OVP}$, $\overline{FAULT}$, PWRGD_CORE, PWRGD_VSA)							
PWM_ Output	$V_{PWM\_}$	Logic-high voltage, I_{LOAD} = 2mA		1.5			V
		Logic-low voltage, I_{LOAD} = 2mA				0.13	V
Output-Low Voltage	V_{OL}	$\overline{OVP}$, $\overline{FAULT}$, PWRGD_CORE, PWRGD_VSA, I_{LOAD} = 4mA				0.4	V
Output-High Leakage Current	I_{LK}	$\overline{OVP}$, $\overline{FAULT}$, PWRGD_CORE, PWRGD_VSA; conditions = output in Hi-Z; pulled up to 3.6V				1	µA

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT ENABLE (OEN)						
OEN Thresholds	V_{IH}	Input logic-high	0.9			V
	V_{IL}	Input logic-low			0.6	V
OEN Filter	t_{FILTER}	Valid enable-signal pulse width		0.2		µs
		Valid shutdown-signal pulse width		0.2		µs
		Digital OEN toggle filtering		200		µs
PMBus INTERFACE						
PMBus Input Logic	V_{IH}	Input logic-high, PMBUS_C, PMBUS_D	2.1			V
	V_{IL}	Input logic-low, PMBUS_C, PMBUS_D			0.8	V
PMBus Output Logic	V_{PMBUS_OL}	Output low voltage, PMBUS_D, $\overline{PMBUS\_A}$, I_{LOAD} = 4mA			0.4	V
Maximum PMBus Operating Frequency	f_{PMBUS}			400		kHz
$\overline{VR\_HOT}$						
$\overline{VR\_HOT}$ Accuracy		$V_{TSENSE\_}$ = 1.145V ($\overline{VR\_HOT}$ threshold at 105°C)	-3		+3	°C
Temperature Zone Hysteresis				3		%
Output-Low Voltage	V_{OL}	$\overline{VR\_HOT}$, I_{LOAD} = 24mA			0.3	V
3.3V to 1.8V SWITCHING REGULATOR						
Set-Point Output Voltage	V_{DD1P8}	Switcher output voltage	1.8	1.85	1.9	V
Maximum Output Current	I_{VX_AVE}	L = 1.5µH, VX_{ON_TIME} = 1.15µs		500		mA
Switcher VX On-Time Accuracy	VX_{ON_TIME}	4 typical selections: 0.70µs, 1.15µs, 1.70µs, 2.26µs	-10		+10	%
TELEMETRY						
INPUT CURRENT SENSE						
ADC Resolution				10		bit
Differential Input Voltage Range	ΔV_{SNS_IN}	External current-sense mode			200	mV
		R_{SENSE} mode			57.5	mV
		R_{SENSE} mode, extended range			115	mV
Update Rate				64		µs

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Accuracy		External current-sense mode	Gain	-0.8		+0.8	%
			Offset, LSB = 259.4µV	-4		+4	LSB
		R_{SENSE} mode	Gain	-0.6		+0.6	%
			Offset, LSB = 68.66µV	-4		+4	LSB
		R_{SENSE} mode, extended range	Gain	-0.6		0.6	%
			Offset, LSB = 129.7µV	-4		+4	LSB
$\overline{PIN\_ALERT}$ Delay					32		µs
$\overline{PIN\_ALERT}$ Output Low Voltage	V_{OL}	I_{LOAD} = 24mA				0.3	V
SYSTEM ADC							
Update Rate		Input voltage (Note 4)			16		ms
		Input current, phase-input current			16		ms
		CORE output voltage			8		ms
		CORE phase-output current			16		ms
		Temperature			16		ms
Resolution					10		bits
Accuracy		Temperature, T_A = 0°C to +85°C	Gain	-0.8		+0.8	%
			Offset	-4		+4	LSB
		Input voltage, T_A = 0°C to +85°C V_{IN} = 7V to 13V 0xD9[4] = 0	Gain	-0.9		+0.9	%
			Offset	-5		+5	LSB
		CORE output voltage, T_A = 0°C to +85°C	Gain	-0.9		+0.9	%
			Offset	-6		+6	LSB
		CORE phase-output current, T_A = 0°C to +85°C	Gain	-1.5		+1.5	%
			Offset	-4		+4	LSB
		PWM duty-cycle measurement T_A = 0°C to +85°C PWM duty cycle = 0% to 50%	Gain	-1		+1	%
			Offset	-4		+4	LSB

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VIN_ADC							
Resolution					10		bits
Accuracy		Input voltage, T_A = 0°C to +85°C, V_{IN} = 7V to 13V, 0xD9[4] = 1 (Note 4)	Gain, SNS_VIN tied to V_{IN}	-0.9		+0.9	%
			Gain, SNS_VIN tied to external divider R_{VIN_TOP} = 4.75kΩ, R_{VIN_BOT} = 19.6kΩ	-0.9		+0.9	%
			Offset LSB = 15.625mV Referred to V_{IN}	-5		+5	LSB
I_{OUT} ADC CORE							
Intel 0x15 Update Rate					64		µs
Resolution					9		bits
Accuracy		0xE7[2:0] = 000, Range 0 to 603A, T_A = 0°C to +85°C	LSB		1.27		A
			Gain	-1.0		+1.0	%
			Offset	-5.7		+5.7	A
		0xE7[2:0] = 001, Range 0 to 301A, T_A = 0°C to +85°C	LSB		637		mA
			Gain	-1.35		+1.35	%
			Offset	-4		+4	A
		0xE7[2:0] = 010, Range 0 to 201A, T_A = 0°C to +85°C	LSB		425		mA
			Gain	-1.35		+1.35	%
			Offset	-3.6		+3.6	A
		0xE7[2:0] = 011, Range 0 to 150A, T_A = 0°C to +85°C	LSB		318		mA
			Gain	-1.35		+1.35	%
			Offset	-3.5		+3.5	A
		0xE7[2:0] = 100, Range 0 to 120A, T_A = 0°C to +85°C	LSB		255		mA
			Gain	-1.35		+1.35	%
			Offset	-3.4		+3.4	A
I_{OUT} ADC VSA							
Intel 0x15 Update Rate					64		µs
Resolution					9		bits
Accuracy		0xD1[4:3] = 01, Range 0 to 37.1A, T_A = 0°C to +85°C	Gain		78.125		mA
			Offset	-1.0		+1.0	%
			Offset	-4.5		+4.5	LSB

Electrical Characteristics (continued)

(Circuit of *Typical Application Circuit*, $V_{AVDD1P8}$ = $V_{DVDD1P8}$ = 1.8V, V_{DD3P3} = 3.3V, V_{IN} = 12V, ISENSE_ input = 10µA/A , T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

Note 2: Slew rate specification is guaranteed for the internal DAC. Performance of the output voltage of the regulator depends on the compensation and might be limited from the maximum bandwidth possible for the specific application.

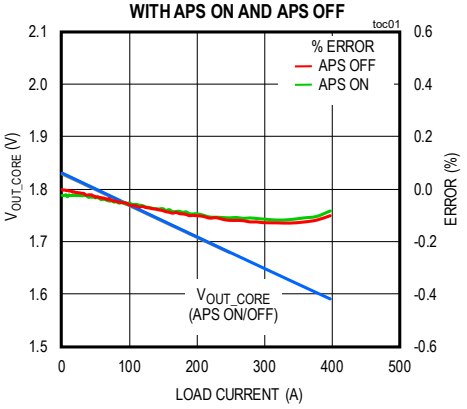
Note 3: See the *VSA Overcurrent Protection* section to calculate actual threshold based on design parameters.

Note 4: The input voltage can be acquired by the system ADC if the PMBus command 0xD9[4] = 0. it Is otherwise acquired from a faster and dedicated VIN_ADC.

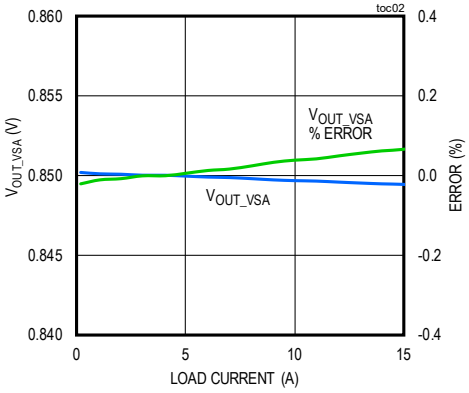
Typical Operating Characteristics

(V_{IN} = 12V, 6 + 1 phase configuration, f_{SW} (CORE) = 500kHz, inductor (CORE) = 100nH CL1208-6, inductor (VSA) = 180nH, f_{SW} (VSA) = 660kHz, V_{VID} (CORE) = 1.8V, V_{VID} (VSA) = 0.85V, T_A = +25°C, unless otherwise noted.)

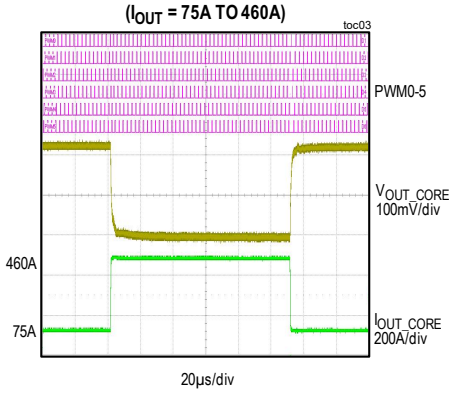
CORE VOLTAGE vs. LOAD CURRENT WITH APS ON AND APS OFF



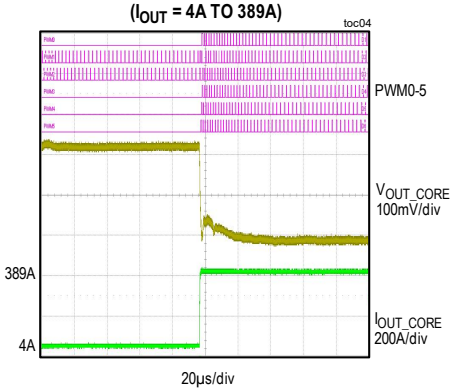
VSA VOLTAGE vs. LOAD CURRENT



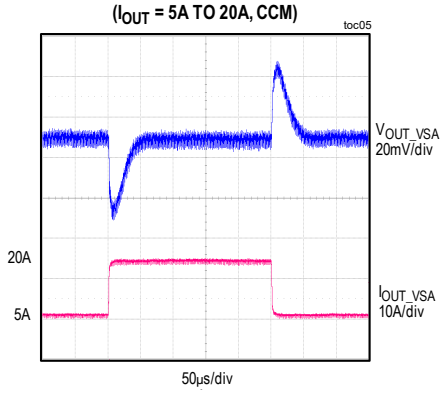
CORE OUTPUT LOAD TRANSIENT (I_{OUT} = 75A TO 460A)



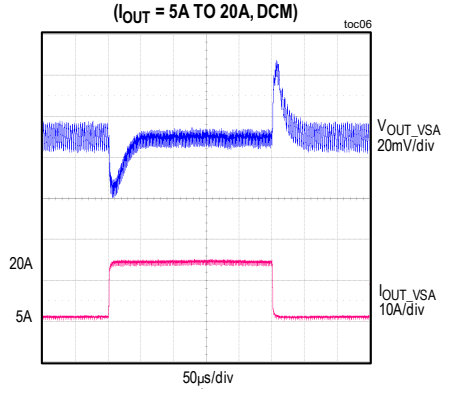
CORE OUTPUT LOAD TRANSIENT (I_{OUT} = 4A TO 389A)



VSA LOAD TRANSIENT (I_{OUT} = 5A TO 20A, CCM)



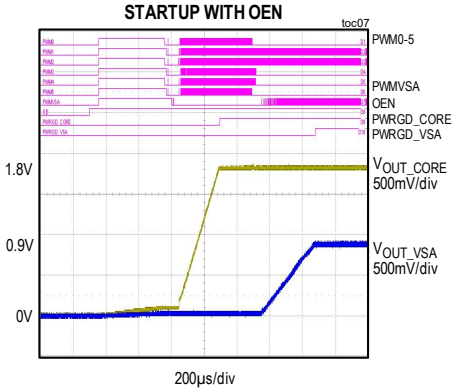
VSA LOAD TRANSIENT (I_{OUT} = 5A TO 20A, DCM)



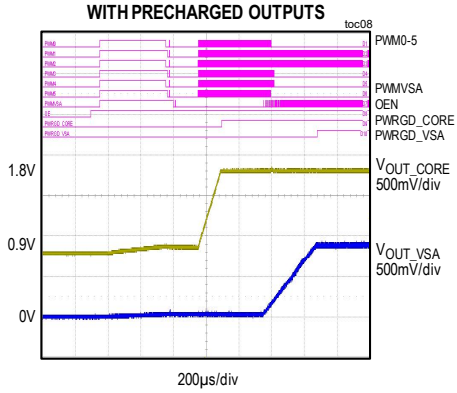
Typical Operating Characteristics (continued)

(V_{IN} = 12V, 6 + 1 phase configuration, f_{SW} (CORE) = 500kHz, inductor (CORE) = 100nH CL1208-6, inductor (VSA) = 180nH, f_{SW} (VSA) = 660kHz, V_{VID} (CORE) = 1.8V, V_{VID} (VSA) = 0.85V, T_A = +25°C, unless otherwise noted.)

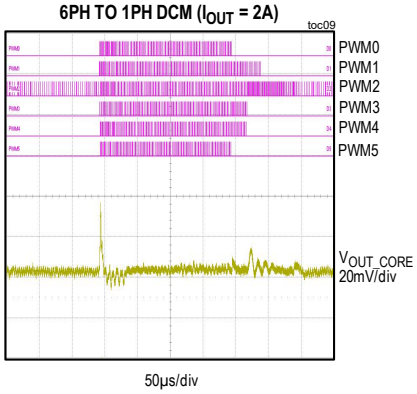
STARTUP WITH OEN



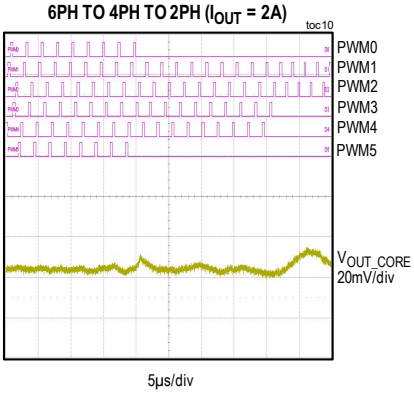
STARTUP WITH OEN
WITH PRECHARGED OUTPUTS



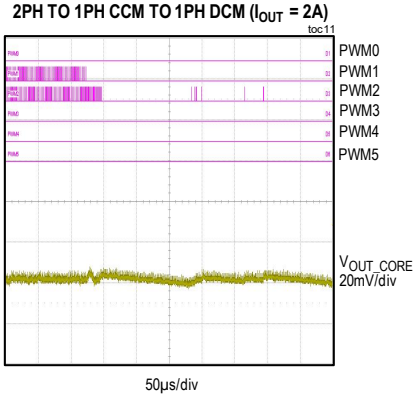
CORE APS TRANSITION
6PH TO 1PH DCM (I_{OUT} = 2A)



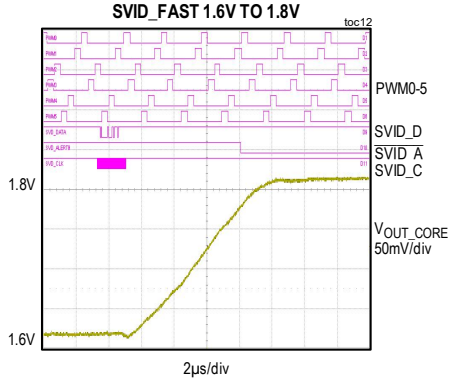
CORE APS TRANSITION
6PH TO 4PH TO 2PH (I_{OUT} = 2A)



CORE APS TRANSITION
2PH TO 1PH CCM TO 1PH DCM (I_{OUT} = 2A)



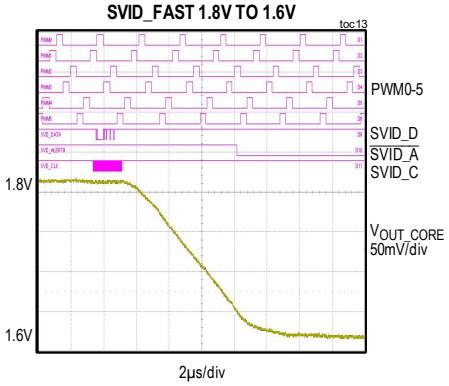
SVID_FAST 1.6V TO 1.8V



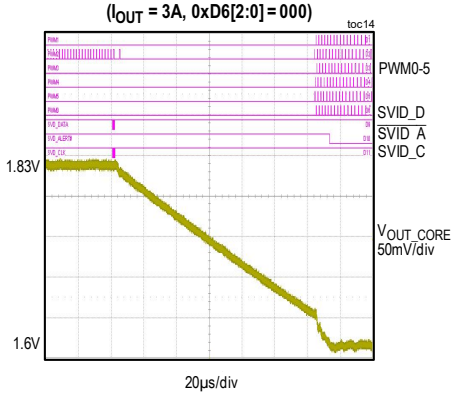
Typical Operating Characteristics (continued)

(V_{IN} = 12V, 6 + 1 phase configuration, f_{SW} (CORE) = 500kHz, inductor (CORE) = 100nH CL1208-6, inductor (VSA) = 180nH, f_{SW} (VSA) = 660kHz, V_{VID} (CORE) = 1.8V, V_{VID} (VSA) = 0.85V, T_A = +25°C, unless otherwise noted.)

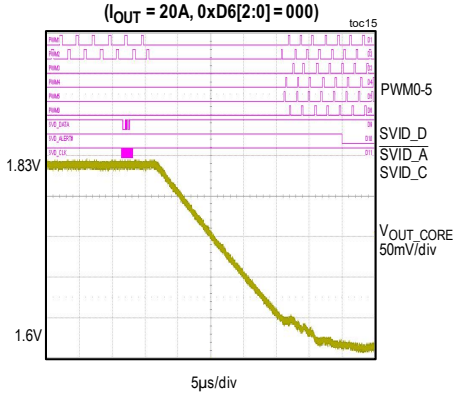
SVID_FAST 1.8V TO 1.6V



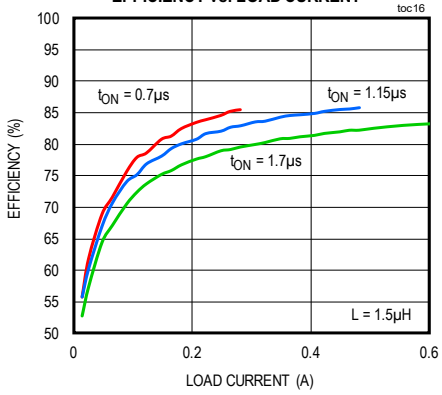
SVID_DECAY 1.83V to 1.6V
(I_{OUT} = 3A, 0xD6[2:0] = 000)



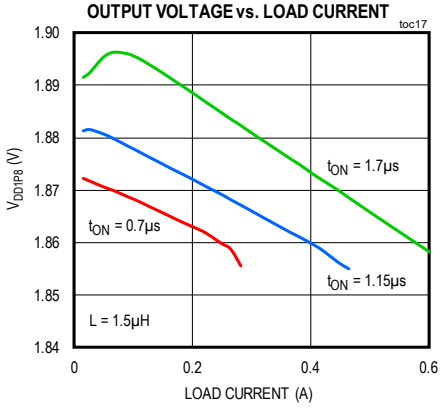
SVID_DECAY 1.83V to 1.6V
(I_{OUT} = 20A, 0xD6[2:0] = 000)



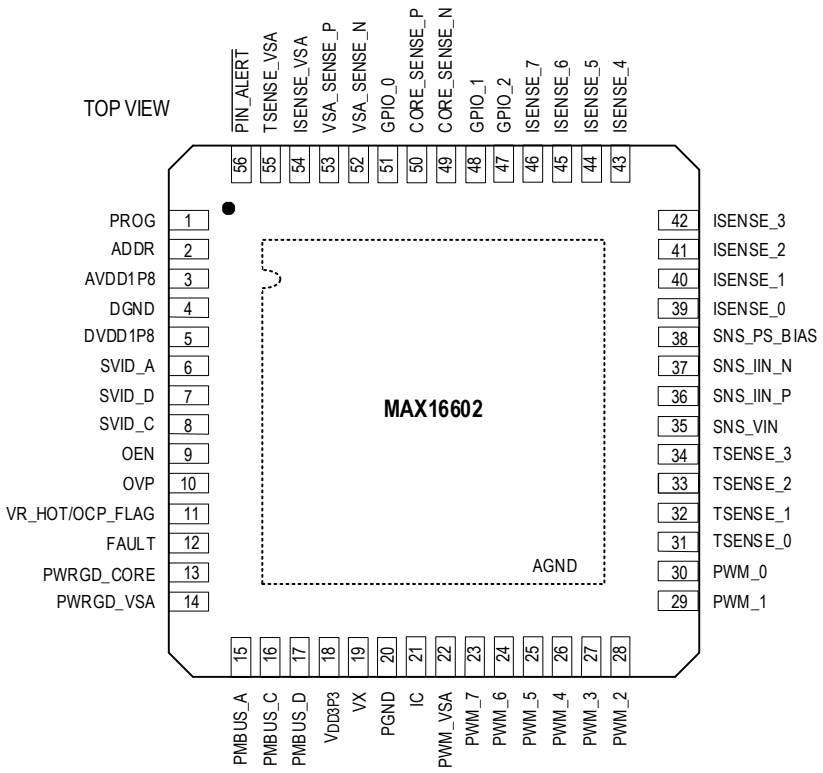
INTERNAL SWITCHER
EFFICIENCY vs. LOAD CURRENT



INTERNAL SWITCHER
OUTPUT VOLTAGE vs. LOAD CURRENT



Pin Configuration



QFN (7mm x 7mm)

Pin Description

PIN	NAME	FUNCTION
1	PROG	Configuration Programming Resistor. Connect a 1% accurate resistor to ground to program the application scenario (see Table 5) and the PMBus MSB address, unless overwritten using the PMBus MSB_PMBus bit.
2	ADDR	Address Programming Resistor. Connect a 1% accurate resistor to ground to set the SVID address and PMBus LSB address (see Table 5).
3	AV_{DD1P8}	Bias Supply Pin. Connect to DVDD1P8 or external power supply through a 4.7Ω resistor. Decouple with a minimum of 2.2µF and 0.1µF to the exposed GND pad.
4	DGND	Digital Ground. Connect to the ground plane using a single via placed in close proximity to the IC.
5	DVDD1P8	Digital Bias Supply Pin. Connect to the output of the chip inductor when using the internal 1.8V switching regulator; otherwise, connect to an external 1.8V supply. Decouple with a minimum of 1µF and 0.1µF to GND.
6	$\overline{SVID\_A}$	SVID Alert# Output

Pin Description (continued)

PIN	NAME	FUNCTION
7	SVID_D	SVID Data I/O
8	SVID_C	SVID Clock Input
9	OEN	Voltage Regulator Output-Voltage Enable. When OEN is pulled high, both outputs are enabled and start up to the programmed boot voltage. When OEN is pulled low, both outputs are ramped down to 0.5V at the slow slew rate before the power stages are set to the IDDQ state. The PMBus interface remains active when OEN is low.
10	$\overline{OVP}$	Output Overvoltage Indicator. This active-low open-drain output indicates that one or both of the outputs have exceeded the OVP threshold.
11	$\overline{VR\_HOT/OCP\_FLAG}$	Overtemperature-Warning Indicator. This active-low open-drain output indicates that one of the power-stage temperatures has exceeded the threshold programmed in the application scenario and reported in the SVID register Temp_Max (22h). Depending on scenario programming, the controller can also indicate when the controller OCP clamp is engaged on this pin.
12	$\overline{FAULT}$	Voltage Regulator Fault Indicator. This active-low open-drain output indicates that a VR fault occurred (see Table 2 and Table 3).
13	PWRGD_CORE	CORE Power-Good Signal. This open-drain output indicates when the V_{CORE} output is within regulation.
14	PWRGD_VSA	VSA Power-Good Signal. This open-drain output indicates when the VSA output is within regulation.
15	$\overline{PMBUS\_A}$	PMBus Alert# Output
16	PMBUS_C	PMBus Clock Input
17	PMBUS_D	PMBus Data I/O
18	V_{DD3P3}	3.3V Supply Pin. V_{DD3P3} is the input for the internal 1.8V switching regulator. Bypass this input with a 2 x 10µF and 0.1µF ceramic capacitor. V_{DD3P3} must be connected to a 3.3V bias supply with a 0.1µF bypass capacitor even when the internal 1.8V switching regulator is disabled.
19	VX	Switching Node for the Internal 1.8V Switching Regulator. Connect a chip inductor between VX and DVDD1P8, with a minimum of 2 x 22µF ceramic capacitors for the output of the regulator. Connect VX to V_{DD3P3} using a 100Ω resistor to disable the 1.8V switching regulator when using an external 1.8V bias supply.
20	PGND	Power Ground. Return path for the internal 1.8V switching regulator.
21	IC	Internally Connected Pin. Leave this pin unconnected.
22	PWM_VSA	Phase Control Output for the VSA Regulator. Connect PWM_VSA to the input pin of the VSA power stage. Connect PWM_VSA to GND to disable the VSA regulator.

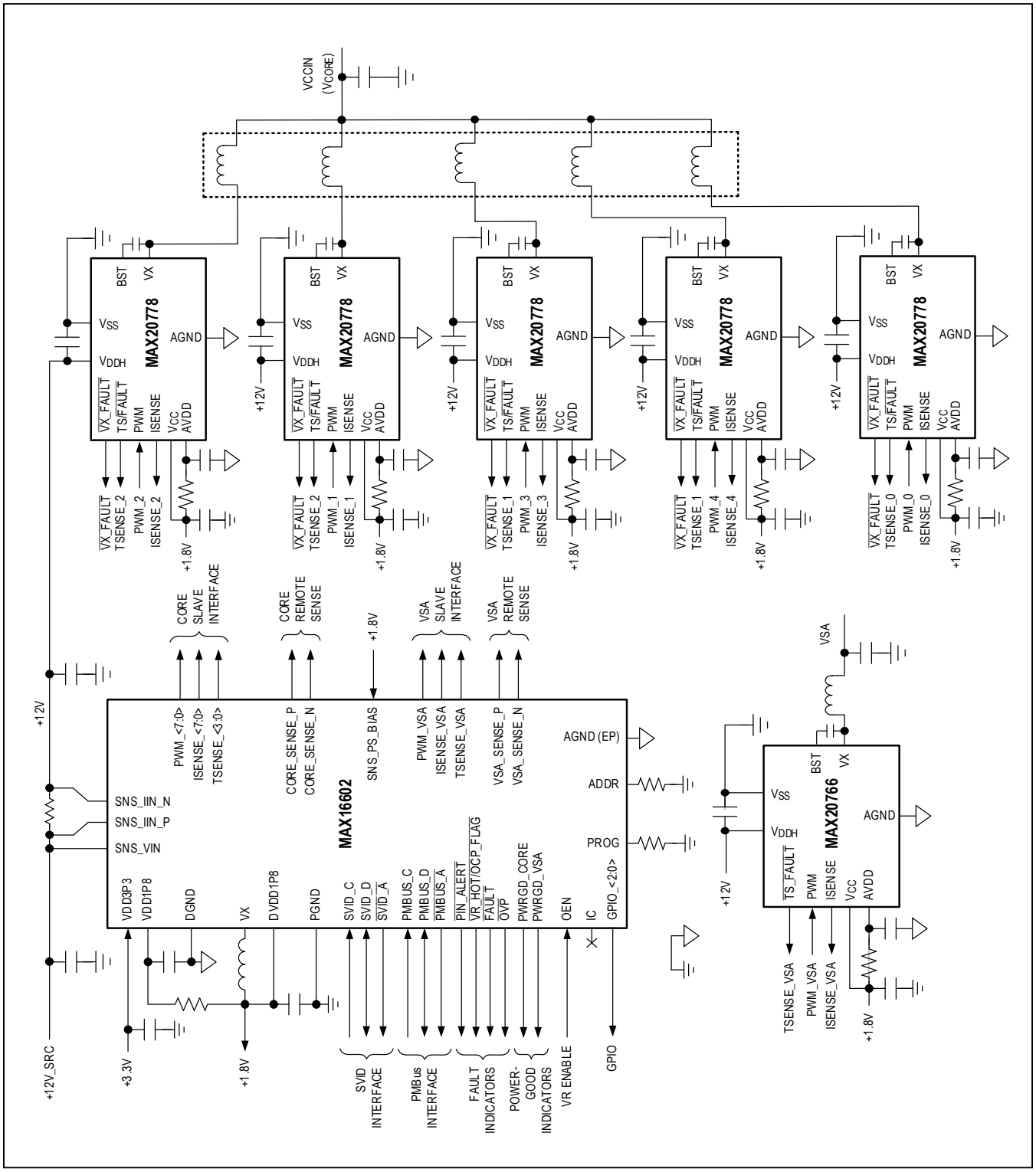
Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="10">23-30</td><td rowspan="10">PWM_<7:0></td><td>Phase-Control Outputs for the V_{CORE} Regulator. Connect PWM_<7:0> to the respective input pins of the V_{CORE} power stages. Connect PWM_ to GND for unused power-stage pairs.</td></tr>
<tr><td><table>
<tr><th>PIN</th><th>NAME</th></tr>
<tr><td>23</td><td>PWM_7</td></tr>
<tr><td>24</td><td>PWM_6</td></tr>
<tr><td>25</td><td>PWM_5</td></tr>
<tr><td>26</td><td>PWM_4</td></tr>
<tr><td>27</td><td>PWM_3</td></tr>
<tr><td>28</td><td>PWM_2</td></tr>
<tr><td>29</td><td>PWM_1</td></tr>
<tr><td>30</td><td>PWM_0</td></tr>
</table></td></tr>
<tr><td rowspan="6">31-34</td><td rowspan="6">TSENSE_<3:0></td><td>Temperature Sensor and Fault Input from the V_{CORE} Regulator Power Stages. Connect these pins to the TS/$\overline{FAULT}$ outputs of the power-stage ICs through an appropriate filter network. $V_{TSENSE\_}$ is an analog representation of the junction temperature of each power stage or power-stage pair of the V_{CORE} regulator during normal operation. TSENSE_ is pulled low by a power stage in case of a serious fault. Leave TSENSE_ unconnected for unused power stages.</td></tr>
<tr><td><table>
<tr><th>PIN</th><th>NAME</th><th>PHASE CONNECTION</th></tr>
<tr><td>31</td><td>TSENSE_0</td><td>0, 5</td></tr>
<tr><td>32</td><td>TSENSE_1</td><td>3, 4</td></tr>
<tr><td>33</td><td>TSENSE_2</td><td>1, 2</td></tr>
<tr><td>34</td><td>TSENSE_3</td><td>6, 7</td></tr>
</table></td></tr>
<tr><td>35</td><td>SNS_VIN</td><td>Input Voltage Sense. The SNS_VIN pin is used for input-voltage sensing and V_{IN_UVLO} protection. For applications above 13.7V and below 17V, set 0xD9[5] = 1, and connect SNS_VIN to the input using a resistive divider with RVIN_TOP = 4.75kΩ, RVIN_BOT = 19.6kΩ.</td></tr>
<tr><td>36</td><td>SNS_IIN_P</td><td>Positive Input for the Input Power Sensor. Connect SNS_IIN_P to the positive terminal of the input sense resistor or input current-monitor signal using a Kelvin connection. Connect to V_{IN} or PGND if unused.</td></tr>
<tr><td>37</td><td>SNS_IIN_N</td><td>Negative Input for the Input Power Sensor. Connect SNS_IIN_N to the negative terminal of the input sense resistor or input current-monitor signal using a Kelvin connection. Connect to SNS_IIN_P if unused.</td></tr>
<tr><td>38</td><td>SNS_PS_BIAS</td><td>Power-Stage Bias Monitor. Connect the power-stage bias supply to SNS_PS_BIAS to allow the controller to monitor power-stage bias for undervoltage faults.</td></tr>
</table>

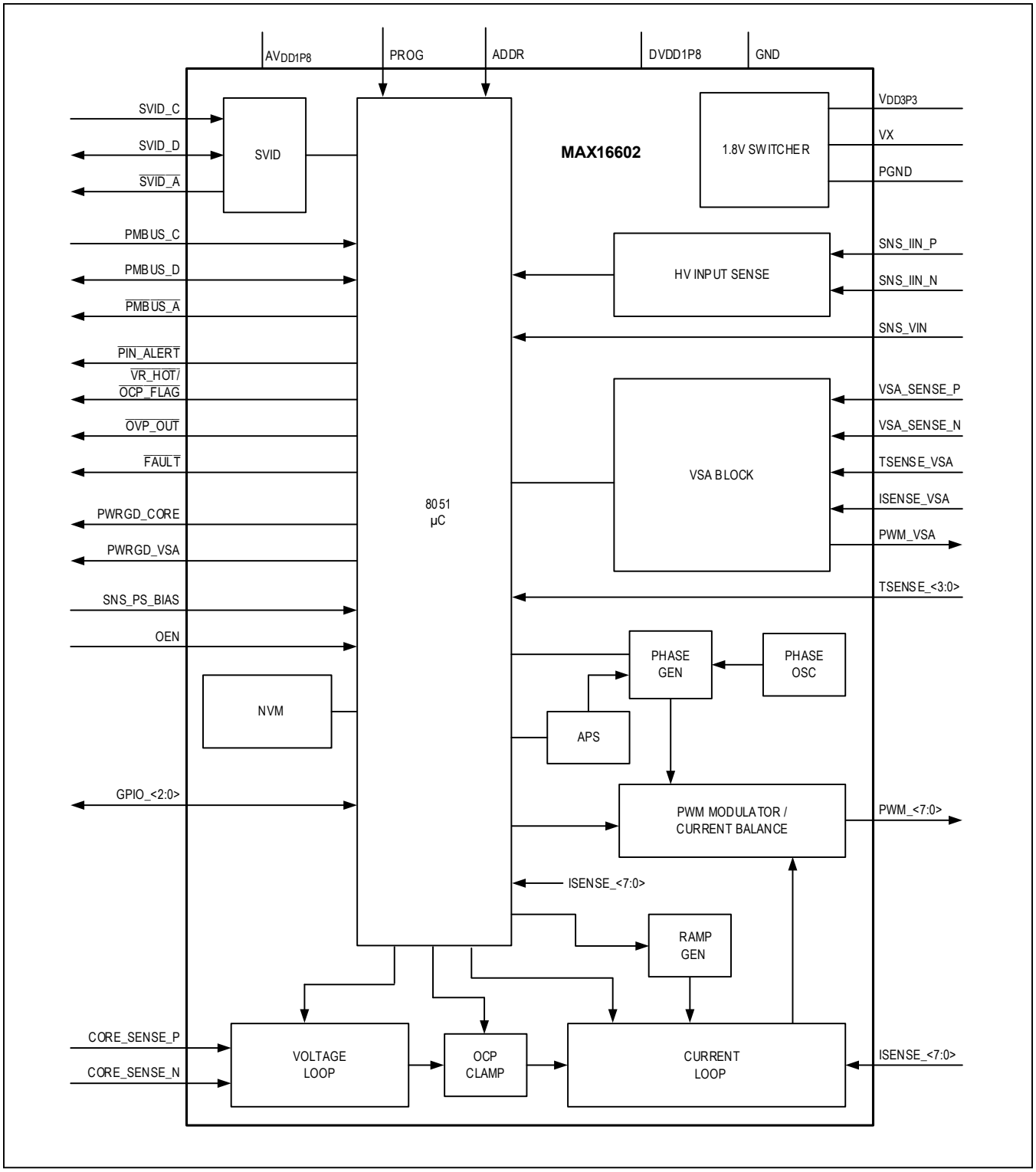
Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="10">39-46</td><td rowspan="10">ISENSE_<7:0></td><td colspan="2">Current-Sense Inputs for V_{CORE} Regulator Power Stages. Connect to the ISENSE_ outputs of the V_{CORE} regulator power-stage ICs. Leave ISENSE_ unconnected for unused power stages.</td></tr>
<tr><td>PIN</td><td>NAME</td></tr>
<tr><td>39</td><td>ISENSE_0</td></tr>
<tr><td>40</td><td>ISENSE_1</td></tr>
<tr><td>41</td><td>ISENSE_2</td></tr>
<tr><td>42</td><td>ISENSE_3</td></tr>
<tr><td>43</td><td>ISENSE_4</td></tr>
<tr><td>44</td><td>ISENSE_5</td></tr>
<tr><td>45</td><td>ISENSE_6</td></tr>
<tr><td>46</td><td>ISENSE_7</td></tr>
<tr><td rowspan="5">47-48, 51</td><td rowspan="5">GPIO_2, GPIO_1, GPIO_0</td><td colspan="2">General-Purpose I/O. The function for each pin depends on the scenario selected.</td></tr>
<tr><td>PIN</td><td>NAME</td></tr>
<tr><td>47</td><td>GPIO_2</td></tr>
<tr><td>48</td><td>GPIO_1</td></tr>
<tr><td>51</td><td>GPIO_0</td></tr>
<tr><td>49</td><td>CORE_SENSE_N</td><td colspan="2">Negative Differential Remote-Sense Input (V_{CORE}). Connect CORE_SENSE_N to ground at the load using a Kelvin connection.</td></tr>
<tr><td>50</td><td>CORE_SENSE_P</td><td colspan="2">Positive Differential Remote-Sense Input (V_{CORE}). Connect CORE_SENSE_P to V_{CORE} at the load using a Kelvin connection.</td></tr>
<tr><td>52</td><td>VSA_SENSE_N</td><td colspan="2">Negative Differential Remote-Sense Input (VSA). Connect to ground at the load using a Kelvin connection. Connect to GND if VSA is not used.</td></tr>
<tr><td>53</td><td>VSA_SENSE_P</td><td colspan="2">Positive Differential Remote-Sense Input (VSA). Connect to V_{VSA} at the load using a Kelvin connection. Connect to GND if VSA is not used.</td></tr>
<tr><td>54</td><td>ISENSE_VSA</td><td colspan="2">Current-Sense Input for VSA Regulator Power-Stage IC. Connect to the ISENSE output of the VSA regulator power-stage IC. If the power stage is not populated, the ISENSE pin should be left unconnected.</td></tr>
<tr><td>55</td><td>TSENSE_VSA</td><td colspan="2">Temperature Sensor and Fault Input from the VSA Regulator Power Stage. Connect to the TS/$\overline{FAULT}$ output of the power-stage IC through the appropriate filter network. The voltage on TSENSE_ is an analog representation of the junction temperature of the VSA power stage during normal operation. TSENSE_VSA is pulled low by the power stage in case of a serious fault.</td></tr>
<tr><td>56</td><td>$\overline{PIN\_ALERT}$</td><td colspan="2">Input Power Alert. This active-low, open-drain output indicates that PMAX has been exceeded.</td></tr>
<tr><td>57</td><td>AGND (EP)</td><td colspan="2">Exposed Ground Pad. Internally connected to the controller’s ground plane and substrate. Connect to the board ground near the DGND pin.</td></tr>
</table>

Typical Application Circuit



Functional Block Diagram



Detailed Description

The MAX16602 controller IC and up to eight MAX20778/A, MAX20779/A, MAX20780, or MAX20790 smart power-stage ICs, provide a highly integrated, high-performance multiphase V_{CORE} power conversion solution for AI cores or Intel VR13.HC platforms. The controller also supports PWM paralleling to control up to 16 phases. The controller IC contains the PWM and phase control circuits, a PMBus interface for reporting and control, and the SVID interface. The associated smart power-stage ICs contain the top and bottom power switches, drive logic, and temperature and current monitoring.

The *Typical Application Circuit* shows the schematic for the MAX16602 controller with the MAX20778 single-phase smart power-stage ICs for V_{CORE}, and a MAX20766 smart power stage for VSA. This control architecture uses the power-stage IC's lossless current sensing to provide a superior control loop with simple design parameters, precise load-line programming, high-accuracy current reporting, and fast-fault protection. The power stage's integrated power switches facilitate low-switching losses for a wide range of output currents.

The controller IC's V_{CORE} regulator can be configured for up to 8 phases (16 phases with paralleling). Unused phases can be disabled (see Table 4), allowing a single electrical design to be used for multiple applications with different output currents. A common PCB layout can be used with phases left unpopulated for lower output currents. TSENSE and ISENSE pins for unused phases must be left unconnected. The same applies when disabling VSA.

Key system parameters are set by the PROG configuration resistor, which allows a quick selection of one of the preset application configurations. The configuration parameters and other features such as autonomous phase-shedding, OCP mode, etc., can be adjusted from the default settings using the PMBus interface. In addition, the PMBus interface offers advanced monitoring and reporting capabilities. See the *PMBus Interface Overview* section for more details.

The IC features an integrated 1.8V regulator that requires only a small external inductor and reduces the total number of external bias supplies required, yet allows for lower operating power consumption. The integrated and accurate input-power sensor simplifies the overall implementation, making the chipset a completely integrated VR13.HC solution.

V_{CORE} Operation

Control Architecture

The controller IC contains multiple amplifier stages and modulator circuits that control each phase based on its current. Figure 1 shows the internal amplifier stages of the controller and how phase-current information is used to generate the phase-control signals. The first amplifier stage (A1) in Figure 1 is a differential amplifier, which provides an output equal to 1.6 times the error between the reference voltage and the differential remote-sense voltage. This difference is then scaled by appropriate selection of R1 and R2 and fed to the error amplifier (A3) through R_{DES}.

Phase resistors (shown as R_{PH1}, R_{PH2}, etc., in Figure 1) are used to sum the ISENSE current feedback signals from all the power stages to the inverting input of the error amplifier (A3). This current represents the total load current. In steady state, the current flowing through the internal R_{DES} resistor equals the sum of the ISENSE signals. This circuit creates a voltage drop across R_{DES} that sets the active load-line in conjunction with the DC gain of A1 and A2. The current through R_{DES} is defined to be the commanded current (1mA = 100A I_{OUT}) and the control loop forces the sum of the ISENSE signals to match this value. Since this architecture is fundamentally current mode, a provision is available for programming a zero for current-loop compensation purposes. This zero is usually used to compensate the double pole that is inherent in the LC filter of the power stage. This is achieved by proper programming of the current-loop amplifier parameters (R_P, F_{ZI}). Various values of ramp rate (modRamp_opt) can be set to facilitate control-loop stability. Calculation of the applicable resistor value is shown in the *Design Procedure* section.

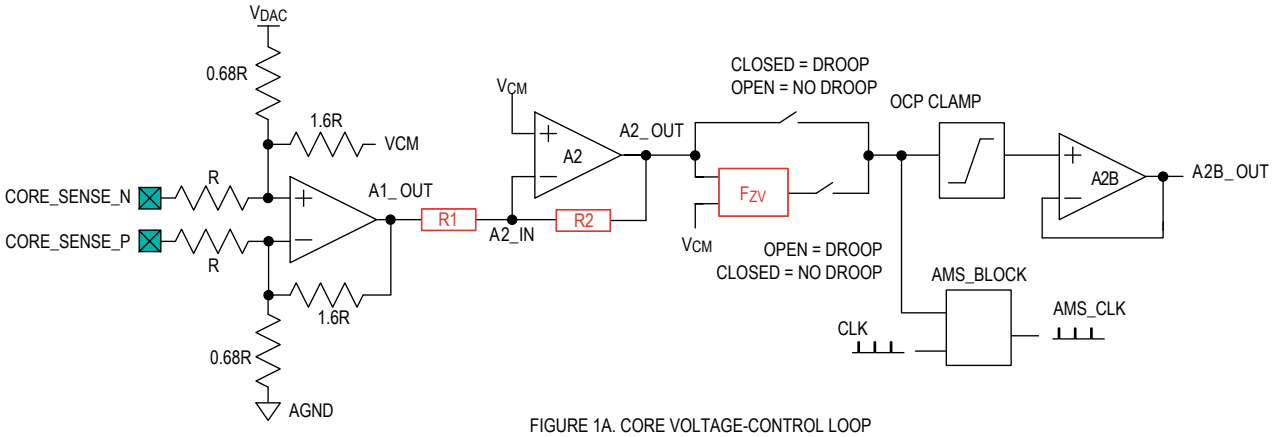


FIGURE 1A. CORE VOLTAGE-CONTROL LOOP

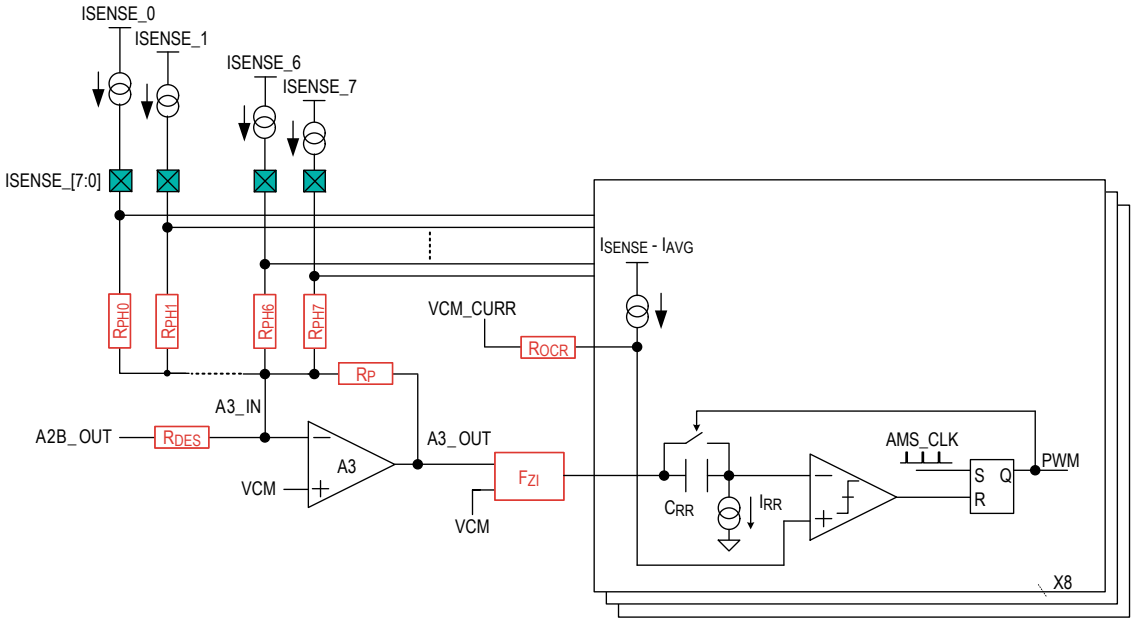


FIGURE 1B. CORE CURRENT-CONTROL LOOP

Figure 1. CORE Control Loop

Lossless Current Sensing and Load-Line Control

The MAX16602 provides accurate output load-line control over the entire range of output currents. As described in the *Control Architecture* section, the output-voltage positioning is performed using the lossless current-sense signals from the Maxim smart power stages, which are fed back to the controller. This current sensing is superior to methods using the inductor's DC resistance and does not require any temperature compensation or filtering to obtain the current signal. The signal is sent back by each individual power stage as a current proportional to the current flowing through the power device. This arrangement results in a tightly controlled load-line that is accurate even at low currents where sensing current using the DC resistance is known to be inaccurate. The load-line is set by digitally programming the DC gain of the voltage control-loop-error amplifier (A2). This gain, in conjunction with the fixed gain of A1 and the internal R_{DES} resistor value, determines the commanded current to the current loop for a given output-voltage error (VID - V_{OUT}). By adding an integrator after the A2 amplifier, load-line droop is disabled.

Integrated 1.8V Regulator

The controller device features an integrated 1.8V switching regulator that provides the bias current to the controller and the smart power-stage devices. This regulator enables efficient power conversion from the 3.3V supply at both high-load and low-load currents by operating in DCM mode and using constant on-time control with input and output feed forward.

When V_{DD1P8} is lower than the 1.8V reference, a fixed high-side PWM-on signal is initiated to turn on the high-side FET. This allows current to flow from the input through the inductor to the output-filter capacitor and load. When the fixed-on-time ends, the high-side FET is turned off, and the low-side FET is turned on briefly to ramp the inductor current to zero. Both high- and low-side FETs then remain off until V_{DD1P8} drops below 1.8V. In order to achieve a simple average output current limiting protection, this regulator only allows the high-side FET to turn on when the inductor current has reached zero. The maximum average current can be calculated using the Equation 1. Soft-start is also guaranteed by the fixed on-time topology and inherent current limiting, while peak current limit is modulated by input and output feed-forward.

Equation 1

$$I_{VX\_MAX(DC)} = \frac{(V_{DD3P3} - V_{DD1P8}) \times t_{ON}}{2L}$$

The fixed on-time is preconfigured by the PROG scenario, but can be adjusted through PMBus register 0xD6[7:6]. The recommended fixed on-time setting is 1.15µs, while the recommended inductor value is 1.5µH.

The 1.8V regulator requires minimum external components: only an output inductor, two 22µF MLCC output capacitors and two input capacitors. No external compensation network or semiconductors are needed. To use an external 1.8V bias, the 1.8V regulator can be disabled by connecting VX to V_{DD3P3} through a 100Ω resistor.

Input-Power Sensor

The MAX16602 features an integrated input-power sensor that simplifies the VR13.HC solution. A low-resistance external current-sense resistor reduces power loss while providing good current-sense accuracy. Alternatively, a current-monitor signal from a current-sense amplifier can be used. The input voltage is sensed at the V_{IN} input (pin 35). Input current and input-voltage telemetry can be read back through PMBus. Input-power telemetry can be read back using PMBus or SVID.

Input-Current Sensor

Figure 2 shows the difference in configuration when using an input-sense resistor or an integrated protection IC with a current-sense amplifier.

Using an Input-Sense Resistor

Calculate the input-sense resistor value using the desired maximum input current and the maximum full-scale voltage.

Equation 2:

$$IIN\_RSENSE = \Delta V_{PROT\_IN\_MAX} / I_{IN\_MAX}$$

Select the IIN_RSENSE value using the GUI or PMBus register 0xD4[15:13]. $\Delta V_{PROT\_IN\_MAX}$ is 50mV or 100mV based on the IIN_RSENSE selection.

Using an Input Current-Sense Amplifier

Select the input current-sense amp option under the IIN_RSENSE selection in the GUI or at PMBus register 0xD4[15:13]. Program IIN_MAX_FS at 0xDE[6:0] with the full-scale input-current value. Select the external components to give a full-scale voltage of 200mV across the SNS_IIN_P to SNS_IIN_N inputs at the IIN_MAX_FS current level.

Equation 3:

$$IIN\_MAX\_FS \times R_{SENSE} = 200mV / Current\_Sense\_Gain$$

where Current_Sense_Gain is the product of current-sense amplifier gain (e.g., 12.5V/V for MAX40010L) and resistor-divider gain. The input R_{SENSE} is determined based on the maximum input current, and the input current signal recommended by the selected current-sense amplifier. This maximizes the full load accuracy.

System Startup

When AV_{DD1P8} (pin 3), DVDD1P8 (pin 5), and V_{DD3P3} (pin 18) rise above their respective undervoltage-lockout thresholds, the MAX16602 is enabled and begins the initialization procedure, which is completed in ~800µs. Programming and configuration resistors are checked for valid values and decoded, and CORE_SENSE_P and VSA_SENSE_P pins are checked for opens. If no controller faults are found, when V_{IN} (pin 35) and SNS_P_BIAS (pin 38) are above their respective undervoltage lockout thresholds, the system is ready to respond to the hardware enable (OEN) signal. After OEN goes high, the device begins the phase-detection sequence. If no other faults are detected, the output ramp begins after the power-stage detection is completed.

Once the hardware enable is received, the SVID bus is made active, and the regulator ramps the V_{CORE} and VSA rails, with the slow ramp rate, to the boot voltage that has been preprogrammed through PROG.

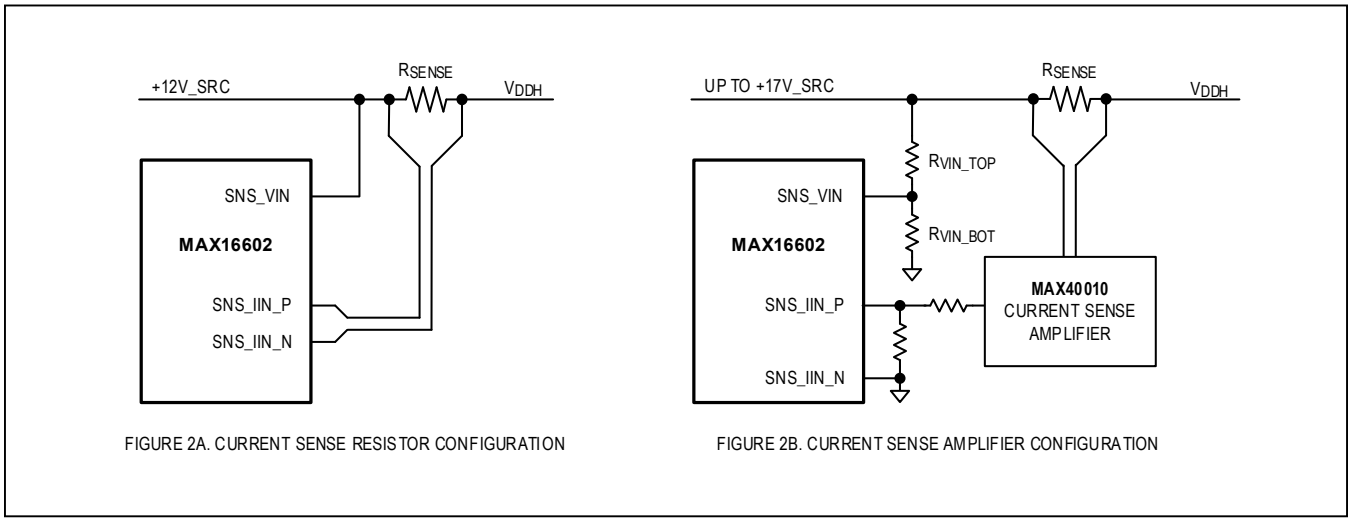


FIGURE 2A. CURRENT SENSE RESISTOR CONFIGURATION

FIGURE 2B. CURRENT SENSE AMPLIFIER CONFIGURATION

Figure 2. Input Current-Sense Option

PWRGD_CORE and PWRGD_VSA signals are asserted after the respective outputs have reached the target VID voltages. If an output is set for no boot voltage, the regulation begins only after a valid SetVID command is received. See Figure 3 for a non-zero V_{BOOT} power-up sequence.

After the regulator is disabled by pulling the OEN pin low, the device does not restart for at least 200µs (typ) to guarantee normal startup. In addition, regulation does not begin until ($V_{CORE\_SENSE\_P}$ - $V_{CORE\_SENSE\_N}$) < 0.5V for the CORE to start, and ($V_{VSA\_SENSE\_P}$ - $V_{VSA\_SENSE\_N}$) < 0.5V for the VSA to start to ensure there is sufficient boost supply for the smart power stages to operate properly.

Constraints for Startup and Shutdown

The following power-sequencing constraints apply for the MAX16602 controller and supported Maxim smart power stages.

Power-Up

There is no sequencing order required between OEN, V_{DD1P8}, V_{DD3P3}, V_{IN} and SNS_PS_BIAS. The device starts up only when all conditions are satisfied, the minimum OFF time has elapsed, and ($V_{CORE\_SENSE\_P}$ - $V_{CORE\_SENSE\_N}$) < 0.5V and ($V_{VSA\_SENSE\_P}$ - $V_{VSA\_SENSE\_N}$) < 0.5V for CORE and VSA, respectively and independently.

Power-Down

OEN has a 200ns (typ) deglitch filter, and does not respond to OEN-low signals shorter than that time. OEN must first go low before any other supply starts to ramp down in order to have a controlled ramp-down of the outputs. Once a valid OEN-low signal has been recorded, the regulator does not restart for at least 200µs (typ).

Switching Modes

The controller device can operate in continuous conduction mode (CCM) with a programmable number of active phases, and also in single-phase discontinuous conduction mode (DCM) according to the power-management settings (e.g., APS) and the SVID commands issued by the CPU.

When DCM is enabled, the switching frequency is directly proportional to the load current. The DCM-offset voltage can be selected by PMBus (dcm_offset_core, 0xB3[6]). A lower DCM-offset voltage results in a lower output-voltage ripple, but a higher switching frequency. Typically, lower switching frequency improves efficiency.

VID and Ramp Rates

The MAX16602 complies with the VR13.HC specifications for VID values and ramp rates, and provides all required SVID commands, including decay mode. Slow and fast ramp rates are specified in the *Electrical Characteristics* table.

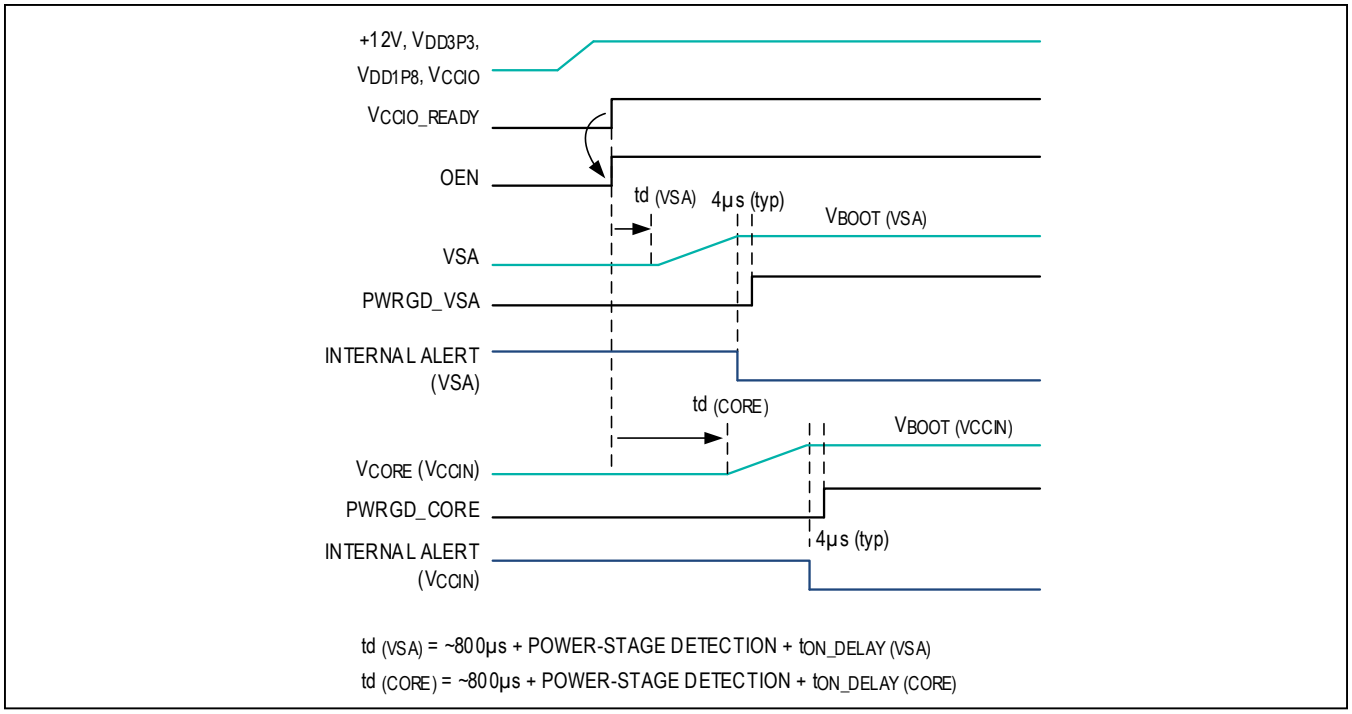


Figure 3. V_{CORE} and V_{SA} Startup Sequence

Power States

The device supports PS0, PS1, PS2, and PS3 commands for CORE and VSA.

Autonomous Phase Shedding (APS)

The MAX16602 allows autonomous phase-shedding (APS) control of the number of active phases to maximize the efficiency of the regulator. With APS_PS0 enabled, the number of active phases is controlled by the load current with no external commands, and can be as low as the minimum allowed by the APS_PS1 and Auto_DCM settings. If APS_PS1 is disabled, the regulator operates in CCM with at least two phases, unless a SetPS2 command is issued by the CPU. If Auto_DCM is enabled, the regulator operates in single-phase DCM at light loads if the APS settings or SetPS issued by the CPU allow single-phase operation.

The APS feature uses two sets of thresholds:

- APS_Slow thresholds are used to make phase-shedding decisions.
- APS_Fast thresholds are used to make phase-adding decisions.

The device rapidly enables all phases when the increasing load current crosses the APS_Fast threshold. The controller sheds phases if the digitized output current remains below the APS_Slow threshold for at least 200µs for the initial phase-count change. Subsequent phase-shedding decisions occur with a 20µs delay. The APS_Fast and APS_Slow thresholds are preset according to the PROG scenario, but can be adjusted using PMBus.

Switching frequency is increased during each phase transition, and a positive offset is added during phase addition to keep the output voltage within specifications.

Table 1. Operation Modes in Applicable Power States

APS MODE SETTING	STATE	OPERATING MODE
APS_PS0	Enabled	Phase shed down according to the load conditions and to the APS_PS1 setting.
	Disabled	Multiphase CCM operation.
APS_PS1	Enabled	Phase shed down according to the load conditions and to the Auto_DCM setting.
	Disabled	2-phase CCM operation.
Auto_DCM	Enabled	1-phase DCM operation at light loads.
	Disabled	1-phase CCM operation at light loads.

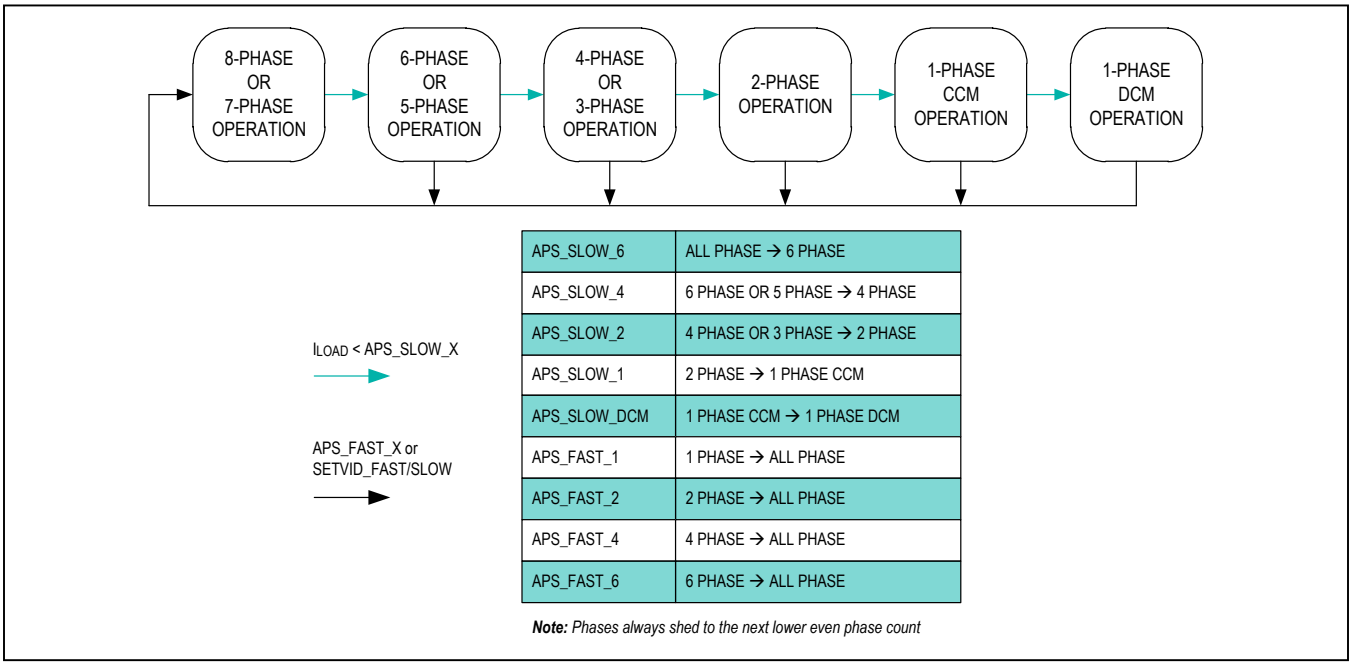


Figure 4. APS State Diagram (8-Phase Configuration Example)

Advanced Modulation Scheme (AMS)

The MAX16602 includes an advanced modulation scheme (AMS) to provide improved transient response. AMS provides significant advantage over conventional PWM schemes. Enabling the AMS feature allows for modulation at both leading and trailing edges. Figure 5 shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off of phases with minimal delay. Depending on load demand, multiple phases can turn on simultaneously when load increases or turned off immediately when load releases. Since the total inductor current increases very quickly, satisfying the load demand, the current drawn from output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty.

Current Steering

The controller IC architecture includes a current-steering feature that can be used to compensate for different thermal properties of smart power-stage devices. This feature allows the use of differently scaled smart power-stage ICs. Current steering is the method by which a percentage of current can be steered away from any phase, allowing that phase to operate in steady state at a current level different from the other phases. This functionality is configured by changing the phase-current steering percentage (100%, 95%, 90%, or 85%) of each phase in PMBus register 0xB4. The control architecture forces the scaled individual phase-current feedback voltages ($\%I_{PH} \times R_{PH}$) to be equal in steady state. This allows a precise derating of current in any or multiple power stages to achieve better thermal balance by trading off current balance. Equation 4 shows the DC current flowing into a given phase according to the total output current and the steering percentage set for each phase.

Equation 4

$$I_i = \frac{\frac{1}{Steering\%_i}}{\sum_{}^{N_{PH}} \frac{1}{Steering\%_k}} \times I_{OUT}$$

Orthogonal Current Rebalancing (OCR)

The controller device implements an orthogonal current-rebalancing (OCR) feature for enhanced dynamic current sharing, or balancing, between different phase currents. This feature maintains current balance during load transients, even at load frequencies close to VR switching frequency and its harmonics.

Each duty-cycle modulator reference voltage is conditioned by the OCR block to minimize phase imbalance without affecting the total current. OCR operates by including average current information, as well as individual phase currents in the current command for each phase. This prevents each phase current from diverging from the average. R_{OCR} is the adjustable OCR gain set through PMBus register 0xB4.

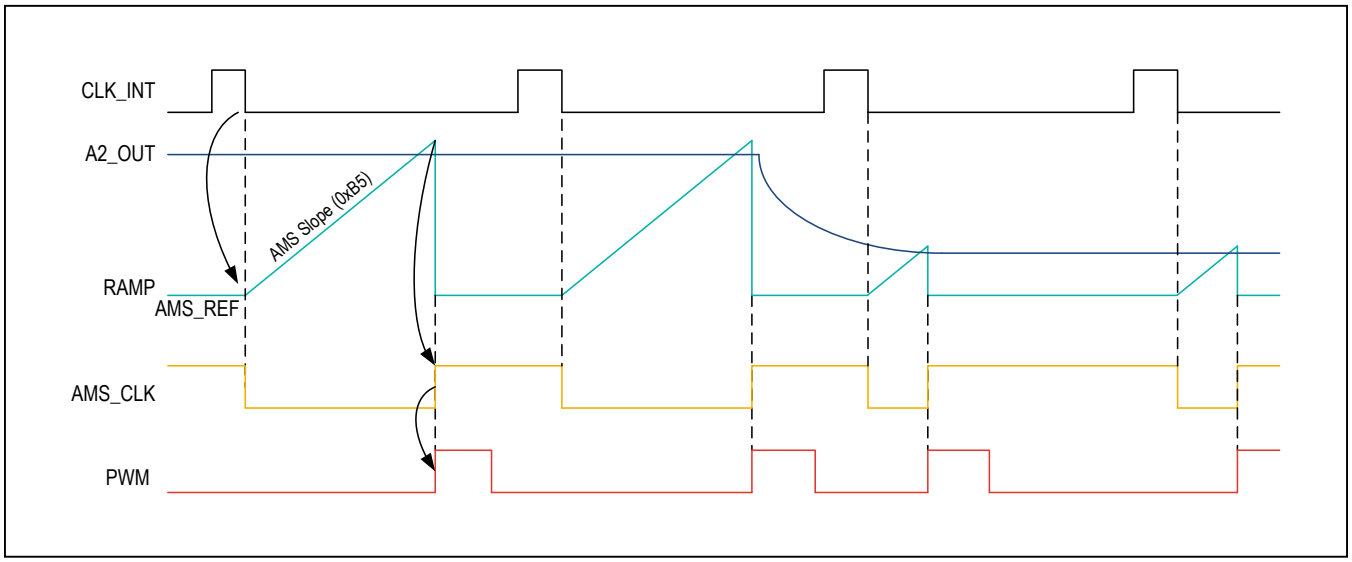


Figure 5. AMS Operation

V_{CORE} Protection and Monitoring

The controller IC includes multiple circuits to protect the regulator and monitor the output voltage.

Fault Detection at Startup

The MAX16602 performs various fault detections upon exiting V_{DD1P8} UVLO and after OEN rises.

After exiting V_{DD1P8} UVLO, the device performs the following fault checks:

- ISENSE pins short to power-stage AVDD
- Valid ADDR and PROG resistor values
- Positive sense lines open (CORE_SENSE_P and VSA_SENSE_P)

After OEN rises, the device performs these additional fault checks:

- TSENSE unconnected for populated power stages
- Power-stage phase-control outputs (PWM pins for power-stage detection, population order, and PWM pins shorted on the same power-stage device)
- Power-stage faults

An error is flagged and the regulator does not start if any of the faults are detected. The faults are logged in the STATUS_MONITORING register 0xF9.

V_{CORE} Power Good (PWRGD_CORE)

The V_{CORE} power-good (PWRGD_CORE) signal is an active-high, open-drain output used to show that V_{CORE} has settled at the boot voltage or the last specified SVID command. PWRGD_CORE goes high after a fixed delay after the end of the startup VID transition (see the *Electrical Characteristics* table). PWRGD_CORE is not deasserted during VID transitions, but is deasserted if any of the following occur:

- The output voltage drops below the tolerance-band threshold relative to the nominal voltage for any reason.
- Any latching fault is detected.

Overcurrent Protection (OCP)

The overcurrent-protection (OCP) default level is loaded by the scenario selected by PROG. The overcurrent threshold can be overwritten using PMBus register 0xD3[3:0] by selecting 1 of 10 values. The system overcurrent condition is detected by comparing the voltage across the internal R_{DES} resistor with the voltage equivalent to the selected OCP threshold. Negative (sinking) overcurrent protection (NOCP) is either 33% or 16.66% of the positive value with 0xD8[0] = 1, regardless the actual setting of 0xD8[0]. NOCP is set by the selected scenario and can be overwritten through PMBus register 0xD3[4].

The overcurrent protection is based on the instantaneous voltage drop across the internal R_{DES}, and a small ripple voltage reflecting the output-voltage ripple can be present. An overcurrent fault is a nonlatching fault and is registered in the fault log if clamping continues for more than 5ms to ensure only periods of continuous overloads are recorded as faults. Depending on scenario programming, the controller can also indicate when the controller OCP clamp is engaged on the $\overline{OCP\_FLAG}$ pin. An additional warning flag is made available through the SVID Status register, indicating that ICCMAX has been exceeded.

"CCM" and "Hiccup" modes are available for positive OCP. In Hiccup OCP mode, when the OCP threshold is exceeded, the system delivers the programmed OCP current for a 5ms period before shutting down and waits for 45ms before restarting. This cycle continues until the load current drops below the programmed value. In CCM OCP mode, the system delivers the programmed OCP current until the load current drops below the OCP value.

The OCP mode is preconfigured by the PROG scenario, but can be adjusted using PMBus register 0xD2[7].

Overvoltage Protection

The controller IC includes two separate overvoltage-protection circuits. One compares the delta between the output voltage and the programmed nominal output with the output-OVP threshold (see the *Electrical Characteristics* table). The other compares the output voltage with the umbrella OVP threshold (see the *Electrical Characteristics* table). If either is tripped, an OVP fault is registered, $\overline{OVP}$ is asserted (not $\overline{FAULT}$), and PWRGD_CORE and PWRGD_VSA are deasserted and regulation halted. OVP faults can only be cleared by toggling the 1.8V or 3.3V supply rails.

Undervoltage Lockout (UVLO)

The device also includes undervoltage-lockout (UVLO) circuits on the 1.8V, 3.3V, and V_{IN} (i.e., V_{DDH}). The UVLO thresholds are defined in the *Electrical Characteristics* table. V_{IN} is monitored directly. If a UVLO event is detected on any supply, the system stops regulating.

If the UVLO event is due to the 1.8V or 3.3V rails falling below the undervoltage threshold, then when the respective supply voltage rises above the respective undervoltage threshold, the IC reloads the default settings from PROG or the last user scenario, and restarts if OEN is still high. If the UVLO event is due to the V_{IN} falling undervoltage threshold, then configuration is not reset, and the IC restarts when V_{IN} is valid again as long as OEN is still high.

Power-Stage Temperature Warning ($\overline{\text{VR\_HOT}}$)

Power-stage temperature warning (VR_HOT) is an open-drain, active-low output that asserts when the temperature of any power stage reaches the threshold programmed in the scenario. VR_HOT is intended as a warning for the CPU to take action, and the system continues to regulate normally. The VR_HOT threshold is fixed at +105°C.

Smart power stages have additional thermal protection designed to protect the power device. These protection features are designed not to interfere with the warning and protection features in the controller. See the respective power-stage data sheet for details.

Fault Indicator Output ($\overline{\text{FAULT}}$)

The fault indicator output ($\overline{\text{FAULT}}$) is an open-drain, active-low output that asserts when a major fault is detected. During initialization, it is asserted if a resistor or node is found out of range or open, as described in the *Fault Detection at Startup* section. When the system is regulating, the smart power-stage faults are monitored continuously and are reported using the controller $\overline{\text{FAULT}}$. See Table 2 and Table 3.

The IC shuts down and pulls $\overline{\text{FAULT}}$ low immediately when any V_{CORE} TSENSE or TSENSE_VSA pin goes low during regulation. $\overline{\text{FAULT}}$ remains latched low and can be cleared only by cycling V_{DD1P8} or V_{DD3P3}.

Table 2. Effects of Controller Faults During Regulation or Startup

PROTECTION FEATURE	OUTPUT SIGNAL(S) SHOWING FAULT	SYSTEM SHUTDOWN	SYSTEM LATCHED OFF	LOGGED IN FAULT LOG
Configuration Resistors Out of Range Detected at Startup	$\overline{\text{FAULT}}$	System does not start	N/A	Yes
V_{CORE} Average-Output OCP (Hiccup)	PWRGD_CORE (if output drops below threshold) $\overline{\text{OCP\_FLAG}}$ (if enabled)	Yes. Restart after 45ms	No	Yes (after 5ms)
V_{CORE} Average-Output OCP (CCM)	PWRGD_CORE (if output drops below threshold) $\overline{\text{OCP\_FLAG}}$ (if enabled)	No	No	Yes (after 5ms)
VSA Average-Output OCP	PWRGD_VSA (if output drops below threshold)	Yes	Yes	Yes, if PWRGD_VSA deasserts
12V UVLO	PWRGD (when output drops below threshold)	Yes	No	Yes
Umbrella OVP, V_{CORE}, and VSA Rails	$\overline{\text{OVP}}$, PWRGD_CORE, PWRGD_VSA	Yes	Yes	Yes
Output OVP, V_{CORE}, and VSA Rails	$\overline{\text{OVP}}$, PWRGD_CORE, PWRGD_VSA	Yes	Yes	Yes
Output Undervoltage	PWRGD_CORE or PWRGD_VSA	No	No	No
V_{DD1P8} UVLO (1.8V)		Yes	No	No
V_{DD3P3} UVLO (3.3V)		Yes	No	No
Overtemperature Warning	$\overline{\text{VR\_HOT}}$	No	No	No
Overtemperature Fault	$\overline{\text{FAULT}}$	Yes	Yes	Yes
SNS_PS_BIAS Undervoltage		Yes	No	No

Table 3. Effects of Power-Stage Faults During Regulation or Startup

POWER-STAGE FAULT	OUTPUT SIGNAL SHOWING FAULT	SYSTEM SHUTDOWN	SYSTEM LATCHED OFF	LOGGED IN FAULT LOG
Power-Stage Detection Faults at Startup (Power-Stage Population: PWM Open; PWM Shorted on Same Power-Stage; ISENSE Shorted to V_{DD}; TSENSE Unconnected on Populated Power Stage)	$\overline{FAULT}$ (active-low)	System does not start	N/A	Yes
Power-Stage Faults at Startup	$\overline{FAULT}$ (active-low)	System does not start	N/A	Yes
Power-Stage Cycle-by-Cycle Clamp OCP (Sinking or Sourcing Current)	None	No	No	No
Power-Stage Cycle-by-Cycle Shutdown OCP (Sinking or Sourcing Current)	$\overline{FAULT}$ (active-low)	Yes	Yes	Yes
Power-Stage OTP Shutdown	$\overline{FAULT}$ (active-low)	Yes	Yes	Yes
Power-Stage Boost UVLO (Undervoltage Lockout on Boost Supply)	$\overline{FAULT}$ (active-low)	Yes	Yes	Yes
Power-Stage VX Short-to-Ground or V_{DDH}	$\overline{FAULT}$ (active-low)	Yes	Yes	Yes
Power-Stage V_{DDH} OVLO	$\overline{FAULT}$ (active-low)	Yes	Yes	Yes
Power-Stage V_{DDH} UVLO	None	Yes	No	Yes
Power-Stage V_{DD} UVLO	None	Yes	No	Yes

VSA Operation

VSA Control Architecture

The VSA control architecture is a simplified version of that used for V_{CORE} without droop, as shown in Figure 6. Sixteen options for the ramp rate and two switching frequency settings are provided; these are preconfigured by the PROG scenario, but can be adjusted using PMBus registers.

VSA Output Operation

VSA Startup

VSA startup operation is described in the V_{CORE} section.

VSA Power States

The VSA rail supports the PS0, PS2, PS3, and decay power states.

DCM Operation

A programmable control-loop offset is included in the VSA circuit that functions in the same manner as the VCORE. The offset is preconfigured by the PROG scenario, but can be adjusted using PMBus register 0xB3[6].

VSA Scenario Programmable Parameters

Switching frequency and boot voltage are some of the parameters that are preconfigured by the PROG scenario.

VSA Protection and Monitoring

VSA Power Good

The VSA output has an independent power-good signal that operates in the same manner as that for V_{CORE}.

VSA Overcurrent Protection

The VSA overcurrent protection employs a peak current cycle-by-cycle clamp. The clamp is activated by comparing the voltage across R_{PH_VSA} with a reference threshold. When a positive, or sourcing, OCP is detected, PWM_VSA is held low until the next switching cycle (assuming the OCP condition has disappeared). Negative, or sinking, overcurrent protection is also provided. When negative OCP is detected, PWM_VSA is driven high for a constant on-time.

Equation 5:

$$I_{LPK} = \frac{(V_{IN} - V_{OUT}) x (t_{D\_COMP} + t_{D\_PS})}{L} + I_{POCP\_VSA}$$

where:

t_{D_COMP} is the current comparator delay

t_{D_PS} is the power-stage PWM-to-VX delay

and I_{POCP_VSA} is from *Electrical Characteristics*

The negative OCP threshold is typically lower (in absolute value) than the programmed setting. See Equation 6 to calculate the expected OCP threshold according to the design parameters.

Equation 6:

$$NOCP = \frac{-25mV - Mod_{RR} \times \left(\frac{V_{OUT}}{V_{IN}} \times t_{SW} - t_1\right)}{R_{PH}} \times K_I - \frac{V_{IN} - V_{OUT}}{L} \times \left(\frac{V_{OUT}}{V_{IN}} \times t_{SW} - t_2\right) + \frac{V_{IN} - V_{OUT}}{2L} \times \frac{V_{IN} - V_{OUT}}{V_{IN}} \times t_{SW}$$

where:

Mod_{RR} = Modulator ramp rate of the VSA regulator

R_{PH} = 1500Ω (typ)

K_I = Current-sense gain, 10µA/A (typ)

t_1 = 10ns (typ)

t_2 = 60ns (typ)

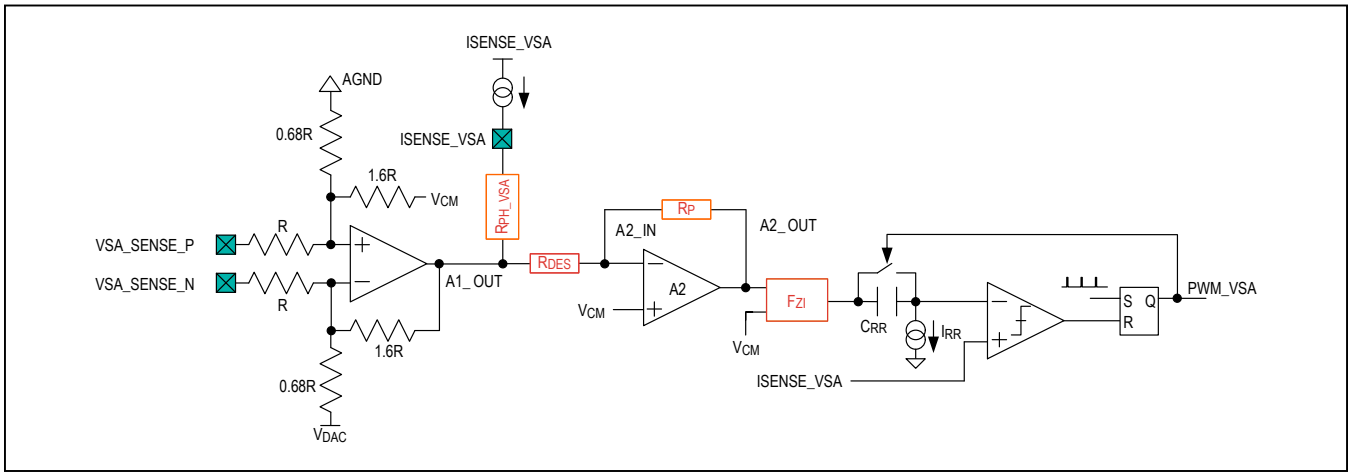


Figure 6. VSA Control Loop

VSA Overvoltage Protection

The VSA output has two OVP circuits, one that tracks the nominal voltage and another that uses a fixed umbrella OVP. The OVP operation is the same as described for V_{CORE}.

Design Procedure

Determining the Optimum Number of Phases

The value of ICCMAX is selected based on the choice of CPU. The ICCMAX and OCP registers are programmed by the scenario. OCP is generally set 20% higher than ICCMAX. Based on the load-current requirements and the area available, the smart power stage to be used and the desired performance versus cost determines the number of phases required. Efficiency curves and current ratings shown on the smart power-stage data sheets can be used for this purpose.

Phase Population Order

Care must be taken when configuring the MAX16602 for a particular phase count. For a given phase count, specific phase positions must be populated while the others must be deactivated. Phases are deactivated by connecting a 1kΩ resistor between the device's phase-control (PWM) pins of the inactive phases and ground. The TSENSE and ISENSE pins for unused phases must be left unconnected. Table 4 defines the population positions and the respective firing sequence.

Output Capacitance Calculation

One criterion for determining the value of the output capacitance (C_{OUT}) is based on the maximum allowable overshoot (V_{OV_MAX}) during unloading transients. Equation 7 provides the minimum value of output capacitance required to meet a given overshoot specification.

Equation 7:

$$\Delta Q_{OFF\_LOAD} = \frac{I_{STEP}^2}{2} \times \left(\frac{L_{OUT}}{V_{OUT}} \frac{1}{N_{PH}} - \frac{1}{SLEW\_RATE} \right)$$

$$\Rightarrow C_{OUT} > \frac{\Delta Q_{OFF\_LOAD}}{I_{STEP} \times R_{LL} + V_{OV\_MAX}}$$

In other cases the minimum C_{OUT} requirement can be driven by the maximum bandwidth achievable by the voltage regulator (see Equation 8).

Equation 8:

$$F_{C\_VOLTAGE\_LOOP} = \frac{1}{2 \times \pi \times R_{LL} \times C_{OUT}}$$

$$\Rightarrow C_{OUT} > \frac{1}{2 \times \pi \times R_{LL} \times (0.4 \times f_{SW})}$$

Consider a 6-phase design example in which the allowable overshoot is the limiting factor. If the system has 100nH of inductance per phase, a 1.7V output, a maximum current step of 200A, and the maximum allowable overshoot of 50mV, then the minimum C_{OUT} theoretically required is ~750µF. The $F_{C\_VOLTAGE\_LOOP}$ condition requires ~900µF. and is the determining factor. Selecting a slightly higher value gives a good design margin against component variation and effective capacitance loss due to bias voltage.

Table 4. Phase Population and PWM* Firing Sequence

NUMBER OF POPULATED PHASES	POWER-STAGE PAIR POSITIONS TO BE POPULATED BY LAYOUT	FIRING SEQUENCE
2	2, 1	2, 1
3	3, 1, 2	2, 1, 3
4	3, 4, 2, 1	2, 4, 1, 3
5	3, 4, 2, 1, 0	2, 4, 1, 0, 3
6	3, 4, 2, 1, 5, 0	2, 5, 4, 1, 0, 3
7	3, 4, 2, 1, 0, 5, 6	2, 5, 4, 6, 1, 0, 3
8	3, 4, 2, 1, 5, 0, 6, 7	2, 5, 4, 6, 1, 0, 3, 7

**Defined by PWMx pin name (e.g., position 2 driven by PWM2).*

Configuration Resistor-Value Selection

System operating parameters are set using configuration resistors. ADDR selects the SVID and PMBus address, while PROG selects the preconfigured scenario. The correct resistor value and parameters programmed by each resistor are shown in Table 5. Configuration parameters can be programmed over PMBus while OEN is low. These settings are not reset on any subsequent OEN toggle.

Design Procedure for Digital Parameters

Unlike previous-generation controllers, the MAX16602 integrates all the control-loop components that were previously externally mounted. The following parameters are now digitally selected:

V_{CORE} Regulator

- Switching frequency (300kHz to 857kHz)
- Load-line (0.105mΩ to 0.979mΩ). See Table 6 for details on range and steps.
- System OCP (30A to 695A). See Table 7 for details.
- APS fast and slow thresholds
- Modulator ramp rate (0.4V/µs to 1.9V/µs, 0.1V/µs LSB)
- AMS ramp rate (0.125V/µs to 1.0625V/µs, 0.0625V/µs LSB)
- Current-loop zero (8.4kHz to 45.5kHz)
- Voltage-loop zero (9.6kHz to 159.2kHz (No-droop configuration only)
- R_P (195Ω to 3770Ω, 65Ω LSB lower range to 162.5Ω LSB upper range)
- R_{OCR} (1.5kΩ to 17kΩ, 500Ω LSB)

VSA Regulator

- Switching frequency (660kHz or 800kHz)
- Modulator ramp rate (0.4V/µs to 1.9V/µs, 0.1V/µs LSB)
- Control-loop zero (8.4kHz to 45.5kHz)
- R_P (1.04kΩ to 5.07kΩ, 130Ω LSB)

The parameters listed above are preconfigured by the PROG scenario, but can be adjusted through the PMBus interface. The default scenarios contain the optimized settings for several standard CPUs, and should work as is, or only with minor adjustments.

Table 5. ADDR and PROG Tables

ADDR 1% RESISTOR (kΩ)	CODE	SVID ADDRESS (CORE/VSA)	PMBus LSB ADDRESS (CORE/VSA)
1.78	0	0/1	0/1
2.37	1	0/1	1/2
3.16	2	0/1	2/3
4.22	3	0/1	3/4
5.62	4	0/1	4/5
7.5	5	0/1	5/6
9.76	6	0/1	6/7
13	7	0/1	7/8
17.4	8	2/3	8/9
23.2	9	2/3	9/10
30.9	10	2/3	10/11
41.2	11	2/3	11/12
54.9	12	2/3	12/13
73.2	13	2/3	13/14
97.6	14	2/3	14/15
127	15	2/3	0/1

PROG 1% RESISTOR (kΩ)	CODE	SCENARIO
1.78	0	0
2.37	1	1
3.16	2	2
4.22	3	3
5.62	4	4
7.5	5	5
9.76	6	6
13	7	7
17.4	8	8
23.2	9	9
30.9	10	10
41.2	11	11
54.9	12	12
73.2	13	13
97.6	14	14
127	15	15

Note: *The PMBus MSB address is either 110 or 101 depending on the scenario setting. The MSB_PMBus bit (0xDE[7]) can be used to override and select an MSB of 110 or 101.*

Table 6. Load-Line Range and Resolution

LOW_RDES 0xD3[7]	VR13_LL 0xD8[1]	A2_HI_GAIN 0xD8[5]	R_{DES} (Ω)	DCLL_LSB (µΩ)	DCLL_MIN (mΩ)	DCLL_MAX (mΩ)
0	0	0	92	5.750	0.397	0.753
0	0	1	92	1.917	0.132	0.251
0	1	0	92	7.475	0.516	0.979
0	1	1	92	2.492	0.172	0.326
1	0	0	73.25	4.578	0.316	0.600
1	0	1	73.25	1.526	0.105	0.200
1	1	0	73.25	5.952	0.411	0.780
1	1	1	73.25	1.984	0.137	0.260

Note: *low_rdes should be kept at 0. For applications that require low_rdes = 1, consider using the MAX16601.*

Table 7. System Overcurrent Limit

ocp_hc 0xD8[0]	ocp_th 0xD3[3:0]	1-PH CONFIG	2-PH CONFIG	3-PH CONFIG	4-PH CONFIG	5-PH CONFIG	6-PH CONFIG	7-PH CONFIG	8-PH CONFIG
0	0000	28	55	83	110	138	165	193	221
0	0001	30	61	91	121	152	182	212	243
0	0010	33	66	99	132	166	199	232	265
0	0011	36	72	108	143	179	215	251	287
0	0100	39	77	116	154	193	232	270	309
0	0101	41	83	124	166	207	248	290	331
0	0110	44	88	132	177	221	265	265	265
0	0111	47	94	141	188	235	281	281	281
0	1000	50	99	149	199	248	298	298	298
0	1001	52	105	157	210	262	315	315	315
0	1010	55	110	166	221	276	331	331	331
0	1011	58	116	174	232	290	348	348	348
1	0000	55	110	165	221	276	331	386	441
1	0001	61	121	182	243	303	364	425	485
1	0010	66	132	199	265	331	397	463	530
1	0011	72	143	215	287	359	430	502	574
1	0100	77	154	232	309	386	463	541	618
1	0101	83	166	248	331	414	497	579	662
1	0110	88	177	265	353	441	530	530	530
1	0111	94	188	281	375	469	563	563	563
1	1000	99	199	298	397	497	596	596	596
1	1001	105	210	315	419	524	629	629	629
1	1010	110	221	331	441	552	662	662	662
1	1011	116	232	348	464	579	695	695	695

Note: *Setting PMBus Command 200K_C_REPORT (0xD9[7]) to 1 doubles the supported current in the above table. This requires having two power stages in parallel with 5µA/A current-sense gain.*

Table 8. System Overcurrent Limit, R_{DES} = 73Ω

ocp_hc D8[0]	ocp_th D3[3:0]	1-PH CONFIG	2-PH CONFIG	3-PH CONFIG	4-PH CONFIG	5-PH CONFIG	6-PH CONFIG	7-PH CONFIG	8-PH CONFIG
0	0000	28	55	83	110	138	165	193	221
0	0001	30	61	91	121	152	182	212	243
0	0010	33	66	99	132	166	199	232	265
0	0011	36	72	108	143	179	215	251	N/S
0	0100	39	77	116	154	193	232	270	N/S
0	0101	41	83	124	166	207	248	N/S	N/S
0	0110	44	88	132	177	221	265	265	265
0	0111	47	94	141	188	235	N/S	N/S	N/S
0	1000	50	99	149	199	248	N/S	N/S	N/S
0	1001	52	105	157	210	262	N/S	N/S	N/S
0	1010	55	110	166	221	276	N/S	N/S	N/S
0	1011	58	116	174	232	N/S	N/S	N/S	N/S
1	0000	55	110	165	221	276	331	386	441
1	0001	61	121	182	243	303	364	425	485
1	0010	66	132	199	265	331	397	463	530
1	0011	72	143	215	287	359	430	502	N/S
1	0100	77	154	232	309	386	463	541	N/S
1	0101	83	166	248	331	414	497	N/S	N/S
1	0110	88	177	265	353	441	530	530	530
1	0111	94	188	281	375	469	N/S	N/S	N/S
1	1000	99	199	298	397	497	N/S	N/S	N/S
1	1001	105	210	315	419	524	N/S	N/S	N/S
1	1010	110	221	331	441	552	N/S	N/S	N/S
1	1011	116	232	348	464	N/S	N/S	N/S	N/S

N/S: Not Supported. Current limit exceeds common-mode range.

Note: *Setting PMBus Command 200K_C_REPORT (0xD9[7]) to 1 doubles the supported current in the above table. This requires using two power stages in parallel with 5µA/A current-sense gain.*

Table 9. MAX16602x Application Scenarios

SCENARIO #	PROJECT	IC REVISION
0	Test Scenario	MAX16602
1	Xilinx® Versal, 8 x MAX20778, 200A_{MAX}	—
2	Reserved	MAX16602
3	Reserved	MAX16602
4	Reserved	MAX16602
5	Reserved	MAX16602
6	—	—
7	—	—
8	8 x MAX20780, 0.85V, 320A_{MAX}	MAX16602
9	Broadcom®, 12 x MAX20780, 529A_{MAX}	MAX16602
10	12 x MAX20779, 460A_{MAX} Project	MAX16602
11	—	—
12	Reserved	MAX16602
13	8 x MAX20778, 0.9V, 320A_{MAX}	MAX16602
14	3 x MAX20778, 0.9V Project	MAX16602
15	8 x MAX20778, 0.9V Project	MAX16602

Note: *Newer revisions are backwards compatible—include previous scenarios.*

PMBus Interface Overview

The MAX16602 controller IC includes a serial bus (PMBus) that supports advanced regulator monitoring and control capabilities. The PMBus interface supports a subset of the SMBus 3.1 specification. More information about this specification can be found at **www.smbus.org**. The following SMBus 3.1 features are supported (appropriate specification section numbers in parenthesis):

- Static SMBus address programming with one external resistor
- Compliant with high-power SMBus DC specifications (3.1.3)
- Supports SMBus protocols:
  - Write byte/word (5.5.4)
  - Read byte/word (5.5.5)
  - Send byte (5.5.2)
  - Receive byte (5.5.3)
  - Packet-error checking mechanism support (5.4)
  - PMBALERT# signal through $\overline{\text{PMBUS\_A}}$ pin
- No support for Address Resolution Protocol (5.6)
- PMBus power-stage support only (different from Maxim smart power stages, such as the MAX20778)

Monitoring Functions

The following monitoring information is available using the MAX16602 PMBus interface.

System Level

- System fault log (saves up to five system faults in chronological order; fault log must be cleared before other faults are logged)
- SVID log (saves the last five SVID commands and payload in chronological order and an elapsed time counter)
- Parameters programmed using PROG configuration resistors
- Overtemperature threshold
- Manufacturer module ID
- Manufacturer module part number
- Device ID
- Device revision
- Input voltage

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V_{CORE} Regulator

- Fault status for each individual power stage
- Regulator status
- Number of Maxim smart power-stage devices
- VID code (set through SVID or PMBus)
- Single-byte peak current
- Dual-byte output current
- Dual-byte output voltage
- Phase output current
- Phase input current
- Input current
- Input power
- Temperature of the hottest power stage
- Phase temperature
- Maximum voltage code (set through SVID or PMBus)
- VID offset (set through SVID or PMBus)

VSA Regulator

- VSA regulator status
- VID code (set through SVID or PMBus)
- Maximum voltage code (set through SVID or PMBus)
- VID offset (set through SVID or PMBus)
- VSA power-stage fault status
- Temperature monitoring

Storing User Configuration

User configurations are programmed in nonvolatile memory (NVM). MTP-programmable NVM allows for 8 field modifications. NVM programming should be done at room temperature to guarantee proper programming of the memory. Follow the steps below when programming the NVM:

1) Apply bias voltage and keep OEN low.
2) Set all registers to the desired values.
3) Disable WRITE_PROTECT.
4) Execute STORE_USER_ALL.
5) Enable WRITE_PROTECT if required.

The STORE_USER_ALL command instructs the MAX16602 to copy the entire contents of the configuration registers to the matching locations in the nonvolatile User Store memory. Once User Store has been written, the MAX16602 powers up to the latest User Store value. This covers both CORE and VSA registers.

STORE_USER_ALL is limited to seven writes. If this command reaches the max count, then the part REJECTs the command.

Loading Saved Configurations

Configurations may be saved to a text file using the Maxim GUI or any equivalent method. The configuration text file can be edited to make required changes, and then loaded into back into the same IC or to different ICs. Follow the steps below when loading a configuration text file:

1) Apply bias voltage and keep OEN low.
2) Disable WRITE_PROTECT.
3) Click the Load from File button in the Maxim GUI.
4) Enable WRITE_PROTECT if required.

Loaded configurations are not permanently saved to NVM until a STORE_USER_ALL command is executed.

Control Functions

The following control functions can be overridden using the PMBus interface:

- Parameters programmed using PROG and ADDR configuration resistors except SVID address and PMBus LSB address.

V_{CORE} Regulator

- Output voltage (DAC code setting to program the V_{CORE} reference voltage directly or VID code)
- Overclock output voltage
- OEN signal to shut down the V_{CORE} regulator. Can also be used to restart the regulator
- Set point setting
- VR_HOT (power-stage temperature) threshold
- Maximum output voltage
- OCP mode

VSA Regulator

- Output voltage (DAC code setting to program the VSA reference voltage directly or VID code)
- Overclock output voltage
- OEN signal to shutdown the VSA regulator (can also be used to restart the regulator)
- Set point setting
- Maximum output voltage

Relevant Specifications

The MAX16602 meets the following specifications:

- Intel VR13.HC PWM specification, rev 1.7
- Intel SVID protocol specification, rev 1.91
- PMBus specification, rev 1.2

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16602GGN+	-40°C to +105°C	56 QFN-EP*
MAX16602GGN+T	-40°C to +105°C	56 QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/19	Initial release	—
1	4/20	Updated Benefits and Features, Pin Configuration, Pin Description, Typical Application Circuit, VCORE Operation, Figure 3, VCORE Protection and Monitoring; fixed typos and errors in Electrical Characteristics; updated tables 2, 3, 6, 7, and 8; added table before Table 8	1, 3, 4, 5, 7, 14, 16, 18, 23, 24, 28, 29, 33, 34

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