Click here for production status of specific part numbers.

MAX16990/MAX16992

36V, 2.5MHz Automotive Boost/ SEPIC Controllers

General Description

The MAX16990/MAX16992 are high-performance, current-mode PWM controllers with 4µA (typ) shutdown current for wide input voltage range boost/SEPIC converters. The 4.5V to 36V input operating voltage range makes these devices ideal in automotive applications, such as front-end “preboost” or “SEPIC” power supplies and for the first boost stage in high-power LED lighting applications. An internal low-dropout regulator (PVL regulator) with a 5V output voltage enables the MAX16990/MAX16992 to operate directly from an automotive battery input. The input operating range can be extended to as low as 2.5V when the converter output is applied to the SUP input.

There are multiple versions of the devices offering one or more of the following functions: a synchronization output (SYNCO) for two-phase operation, an overvoltage protection function using a separate input pin (OVP), and a reference input pin (REFIN) to allow on-the-fly output voltage adjustment.

The MAX16990 and MAX16992 operate in different frequency ranges. All versions can be synchronized to an external master clock using the FSET/SYNC input.

In addition, the MAX16990/MAX16992 have a factory-programmable spread-spectrum option. Both devices are available in compact 12-pin TQFN and 10-pin µMAX® packages.

Applications

- Automotive LED Lighting
- Automotive Audio/Navigation Systems
- Dashboards

***Ordering Information* appears at end of data sheet.**

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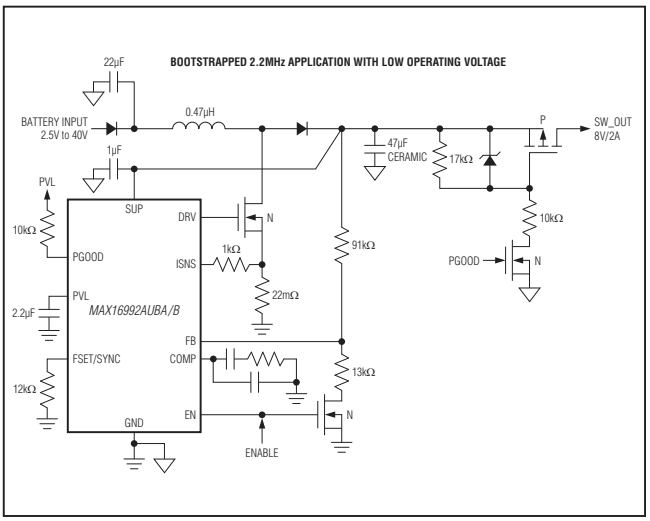
Benefits and Features

- Minimized Radio Interference with 2.5MHz Switching Frequency Above the AM Radio Band
- Space-Efficient Solution Design with Minimized External Components
  - 100kHz to 1MHz (MAX16990) and 1MHz to 2.5MHz (MAX16992) Switching-Frequency Ranges
  - 12-Pin TQFN (3mm x 3mm) and 10-Pin µMAX Packages
- Spread Spectrum Simplifies EMI Management Design
- Flexibility with Available Configurations for Boost, SEPIC, and Multiphase Applications
  - Adjustable Slope Compensation
  - Current-Mode Control
  - Internal Soft-Start (9ms)
- Protection Features Support Robust Automotive Applications
  - Operating Voltage Range Down to 4.5V (2.5V or Lower in Bootstrapped Mode), Immune to Load-Dump Transient Voltages Up to 42V
  - PGOOD Output and Hiccup Mode for Enhanced System Protection
  - Overtemperature Shutdown
  - -40°C to +125°C Operation

Typical Application Circuit



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Absolute Maximum Ratings

EN, SUP, OVP, FB to GND .....-0.3V to +42V
DRV, SYNCO, FSET/SYNC, COMP,
PGOOD, ISNS, REFIN to GND.....-0.3V to (V_{PVL} + 0.3V)
PVL to GND.....-0.3V to 6V
Continuous Power Dissipation (T_A = +70°C)
µMAX on SLB (derate 10.3mW/°C above +70°C) 825mW
µMAX on MLB (derate 12.9mW/°C above +70°C)....1031mW
TQFN 12 on SLB (derate 13.2mW/°C above +70°C)...1053mW
TQFN 12 on MLB (derate 21.32mW/°C above +70°C)...705mW
TQFN 16 on SLB (derate 14.7mW/°C above +70°C)... 1176mW
TQFN 16 on MLB (derate 23.1mW/°C above +70°C)...1847mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

µMAX (Single-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....97°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5°C/W
µMAX (Four-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....78°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5°C/W
TQFN-12 (Single-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....76°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... 11°C/W
TQFN-12 (Four-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....46.9°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5.27°C/W
TQFN-16 (Single-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....68°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....10°C/W
TQFN-16 (Four-Layer Board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....43.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....4.0°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = 14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
SUP Operating Supply Range	V_{SUP}			4.5		36	V
SUP Supply Current in Operation	I_{CC}	V_{FB} = 1.1V, no switching	MAX16990		0.75	1.3	mA
			MAX16992		1.25	2	
SUP Supply Current in Shutdown	I_{SHDN}	V_{EN} = 0V			4	7	µA
OVP Threshold Voltage	V_{OVP}	OVP rising (REFIN = PVL)		105	110	115	% of V_{FB}
OVP Threshold Voltage Hysteresis	V_{OVPH}				2.5		% of V_{FB}
OVP Input Current	I_{OVP}			-1		+1	µA
PVL REGULATOR							
PVL Output Voltage	V_{PVL}			4.7	5	5.3	V
		MAX16990/MAX16992 16-pin QFN			5		
PVL Undervoltage Lockout	V_{UV}	SUP rising		3.8	4	4.3	V
		MAX16990/MAX16992 16-pin QFN		3.7	4	4.4	
PVL Undervoltage-Lockout Hysteresis	V_{UVH}				0.4		V

Electrical Characteristics (continued)

(V_{SUP} = 14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR							
Switching Frequency	f_{SW}	R_{FSET} = 69kΩ		360	400	440	kHz
		R_{FSET} = 12kΩ		2000	2200	2400	
Spread-Spectrum Spreading Factor	SS	B, D, and F versions			Q6		% of f_{SW}
Switching Frequency Range	f_{SWR}	When set with resistor on pin	MAX16990	100		1000	kHz
			MAX16992	1000		2500	
FSET/SYNC Frequency Range	f_{SYNC}	Using external SYNC signal	MAX16990	220		1000	kHz
			MAX16992	1000		2500	
FSET Regulation Voltage	V_{FSET}	12kΩ < R_{FSET} < 69kΩ			0.9		V
Soft-Start Time	t_{SS}	Internally set		6	9	12	ms
Hiccup Period	t_{HICCUP}				55		ms
Maximum Duty Cycle	DC_{MAX}	MAX16990, R_{FSET} = 69kΩ		93			%
		MAX16992, R_{FSET} = 12kΩ		85			
Minimum On-Time	t_{ON}			50	80	110	ns
THERMAL SHUTDOWN							
Thermal-Shutdown Temperature	T_S	Temperature rising			165		°C
Thermal-Shutdown Hysteresis	T_H				10		°C
GATE DRIVERS							
DRV Pullup Resistance	R_{DRVH}	I_{DRV} = 100mA			3	5.5	Ω
DRV Pulldown Resistance	R_{DRVL}	I_{DRV} = -100mA			1.4	2.5	Ω
DRV Output Peak Current	I_{DRV}	Sourcing, C_{DRV} = 10nF			0.75		A
		Sinking, C_{DRV} = 10nF			1		
REGULATION/CURRENT SENSE							
FB Regulation Voltage	V_{FB}	V_{REFIN} = VPVL	Across full line, load, and temperature range	0.99	1	1.01	V
		V_{REFIN} = 2V		1.98	2	2.02	
		V_{REFIN} = 0.5V		0.495	0.5	0.505	
		V_{REFIN} = External	MAX16990/ MAX16992 16-pin QFN	-1.5		1.5	%
		V_{REFIN} = V_{PVL}		0.985	1	1.015	V
FB Input Current	I_{FB}			-0.5		+0.5	µA
ISNS Threshold				212	250	288	mV
ISNS Leading-Edge Blanking Time	t_{BLANK}	MAX16990			60		ns
		MAX16992			40		
Current-Sense Gain	A_{VI}				8		V/V
Peak Slope Compensation Current-Ramp Magnitude		Added to ISNS input		40	50	60	µA
PGOOD Threshold	V_{PG}	Percentage of final value (REFIN = PVL)	Rising	85	90	95	%
			Falling	80	85	90	

Electrical Characteristics (continued)

(V_{SUP} = 14V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Note 2)

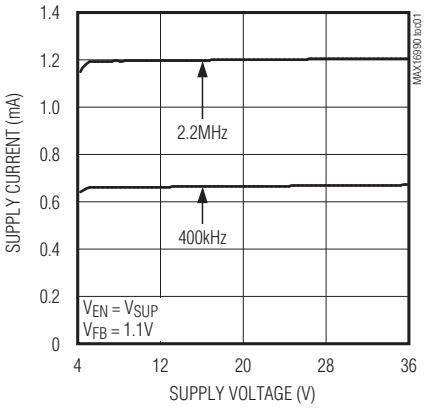
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
REFIN Input Voltage Range			0.5		2	V
REFIN Threshold for 1V FB Regulation			V_{PVL} - 0.8	V_{PVL} - 0.4	V_{PVL} - 0.1	V
Error-Amplifier gm	A_{VEA}			700		µS
Error-Amplifier Output Impedance	R_{OEA}			50		MΩ
COMP Output Current	I_{COMP}			140		µA
COMP Clamp Voltage			2.7	3	3.3	V
LOGIC-LEVEL INPUTS/OUTPUTS						
PGOOD/SYNCO Output Leakage Current		V_{PGOOD}/V_{SYNCO} = 5V		0.5		µA
PGOOD/SYNCO Output Low Level		Sinking 1mA			0.4	V
EN High Input Threshold		EN rising	1.7			V
EN Low Input Threshold					1.2	V
FSET/SYNC High Input Threshold			2.5			V
FSET/SYNC Low Input Threshold					1	V
EN and REFIN Input Current			-1		+1	µA

Note 2: All devices 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

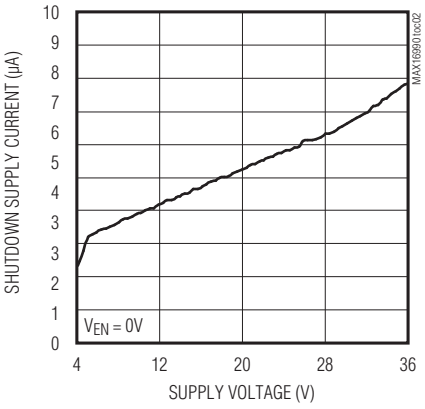
Typical Operating Characteristics

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted.)

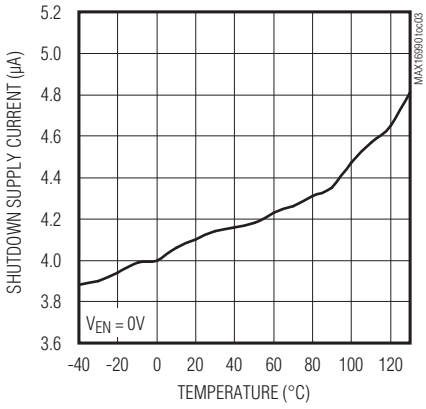
SUPPLY CURRENT vs. SUPPLY VOLTAGE



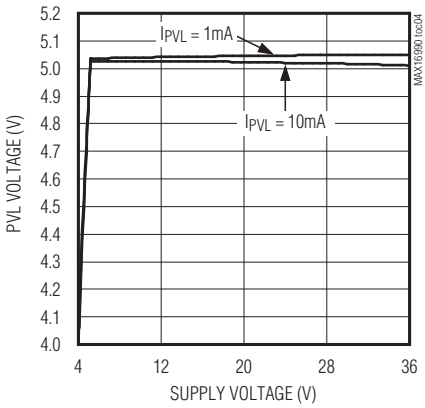
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



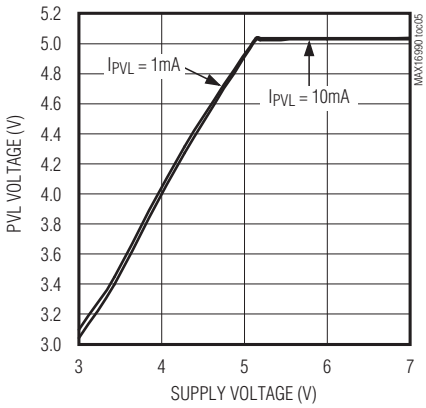
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



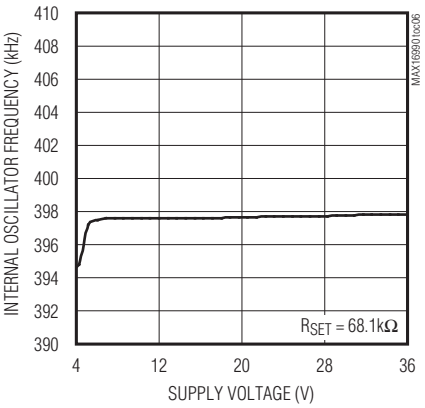
PVL VOLTAGE vs. SUPPLY VOLTAGE



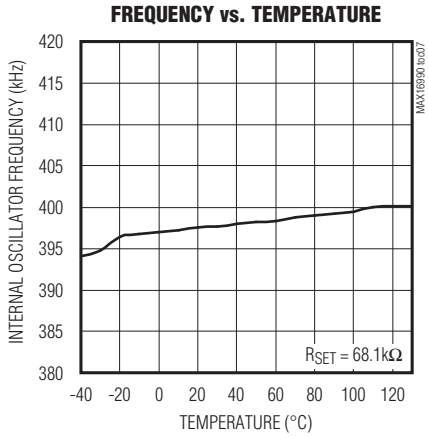
PVL VOLTAGE vs. SUPPLY VOLTAGE



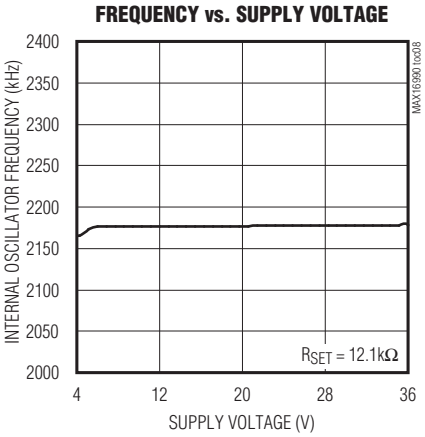
MAX16990 INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



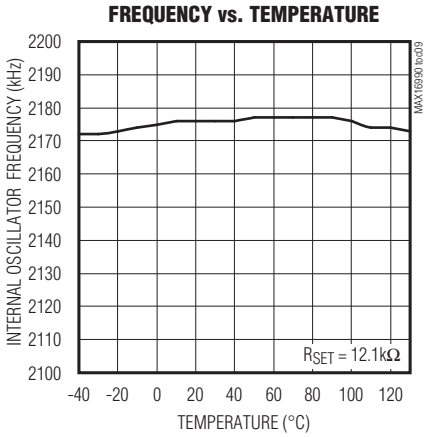
MAX16990 INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



MAX16992 INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



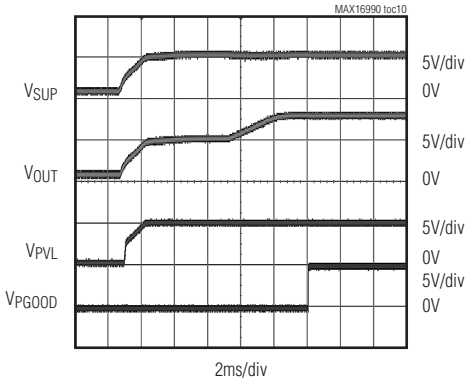
MAX16992 INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



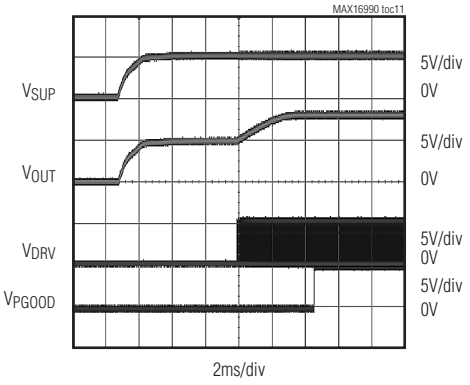
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted.)

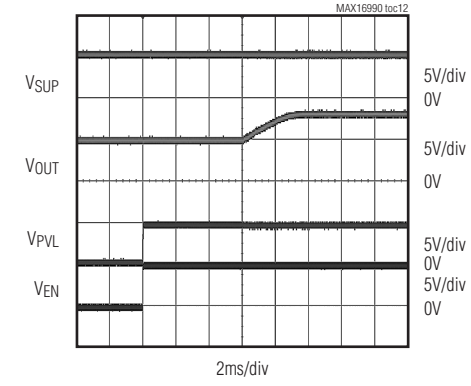
POWER-UP RESPONSE



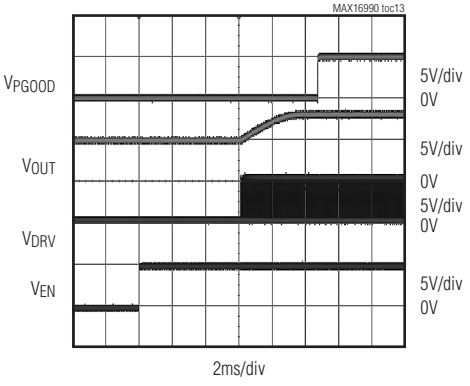
POWER-UP RESPONSE



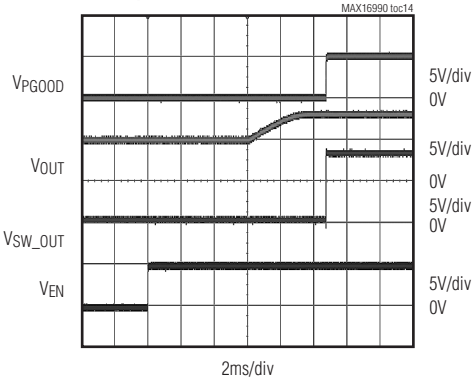
STARTUP RESPONSE



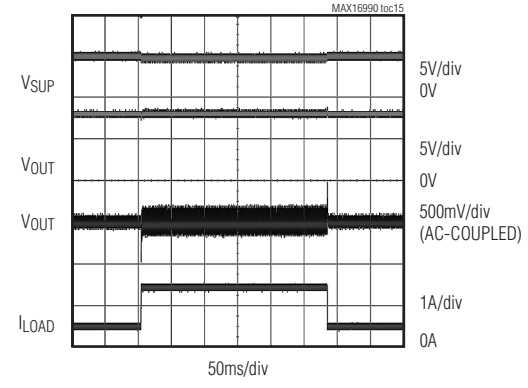
STARTUP RESPONSE



STARTUP RESPONSE (WITH SWITCHED OUTPUT)



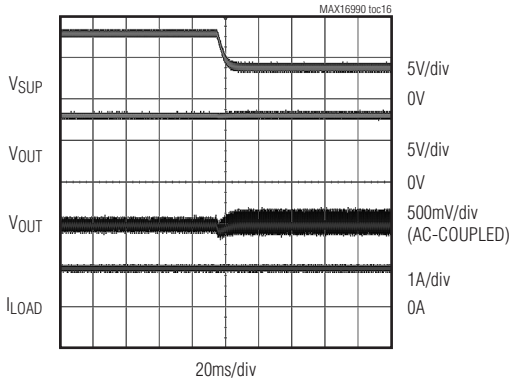
OUTPUT LOAD TRANSIENT



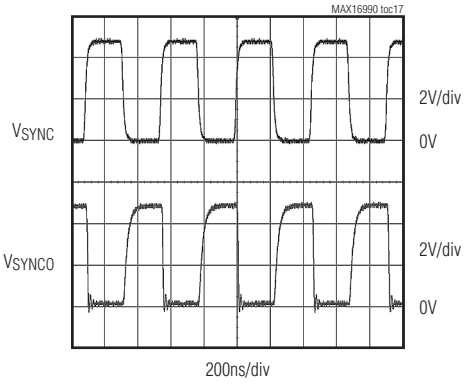
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted.)

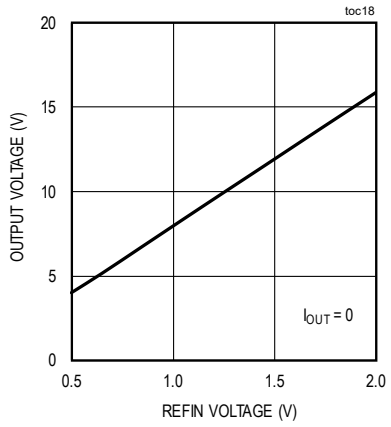
LINE TRANSIENT



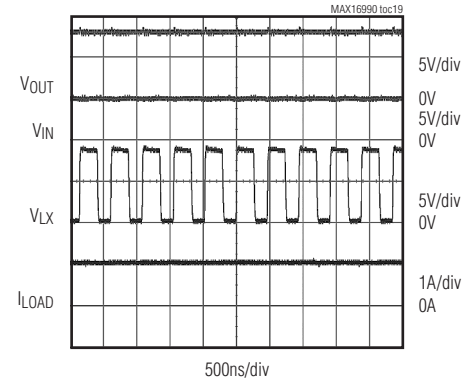
MAX16992 VSYNC vs. VSYNCO



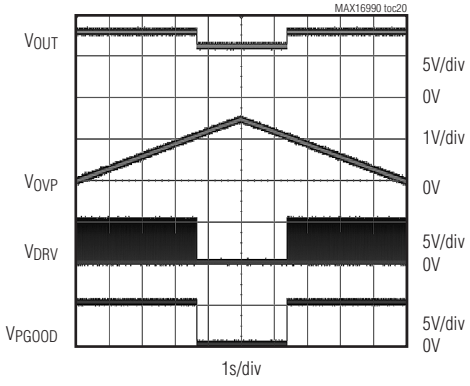
OUTPUT VOLTAGE vs. REFIN VOLTAGE



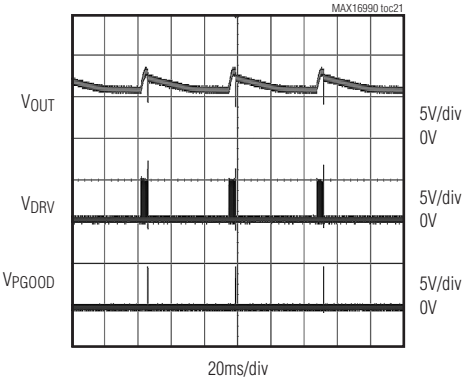
SWITCHING WAVEFORM



OVP SHUTDOWN



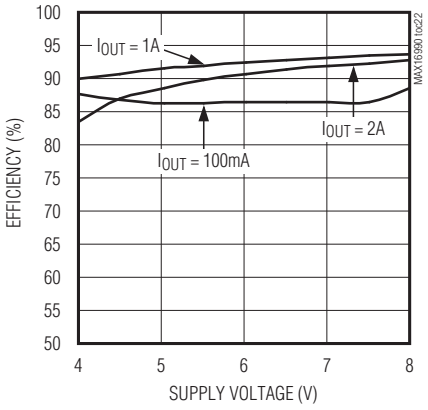
HICCUP MODE



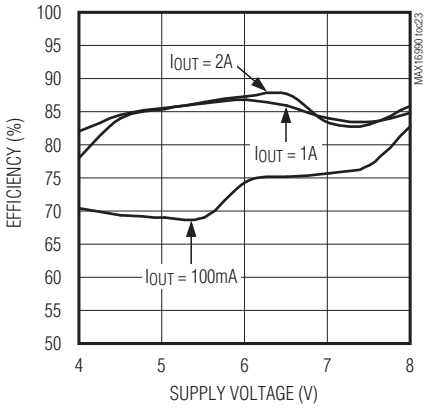
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = +25°C, unless otherwise noted.)

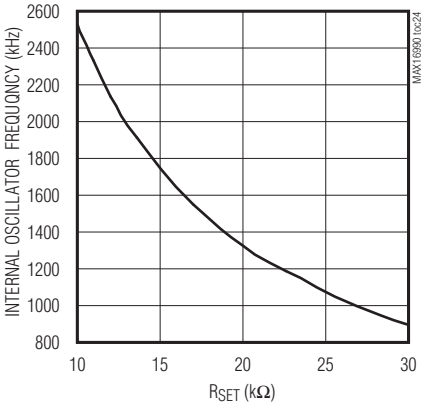
MAX16990 EFFICIENCY



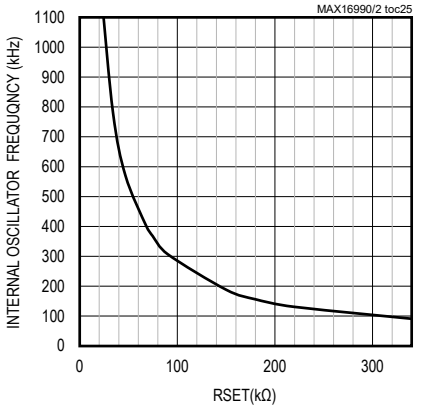
MAX16992 EFFICIENCY



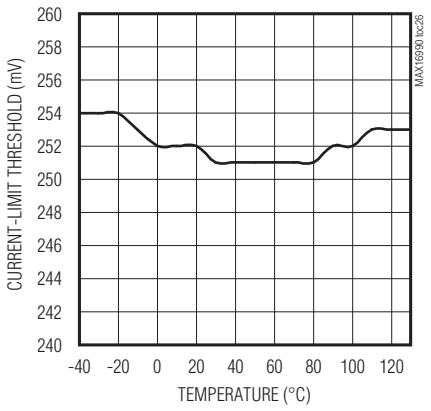
MAX16992 INTERNAL OSCILLATOR FREQUENCY vs. R_{SET}



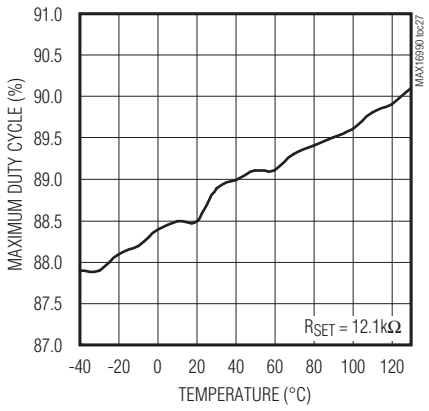
MAX16990 INTERNAL OSCILLATOR FREQUENCY vs. R_{SET}



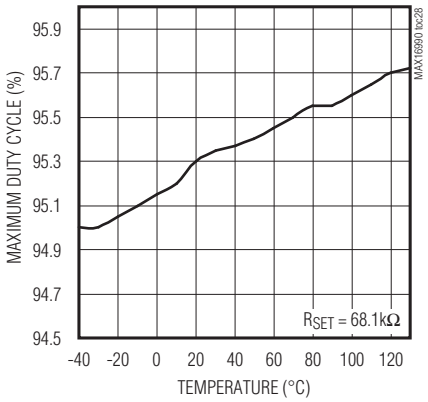
CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



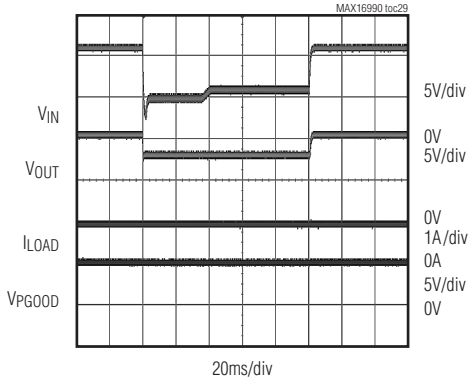
MAX16992 MAXIMUM DUTY CYCLE vs. TEMPERATURE



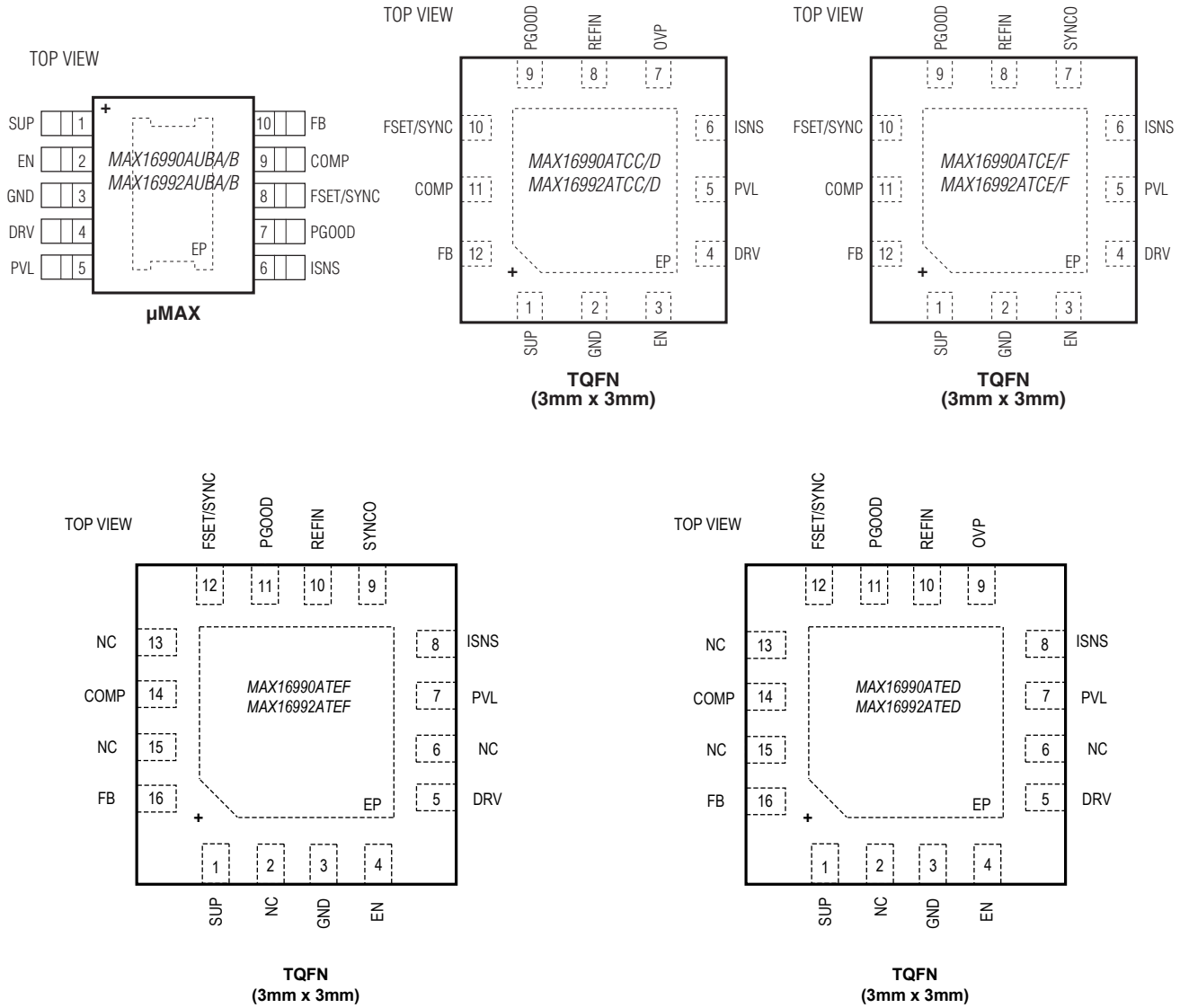
MAX16990 MAXIMUM DUTY CYCLE vs. TEMPERATURE



COLD-CRANK INPUT VOLTAGE TRANSIENT



Pin Configurations



Pin Descriptions

MAX16990AUBA/B, MAX16992AUBA/B	MAX16990ATCC/D, MAX16992ATCC/D	MAX16990ATCE/F, MAX16992ATCE/F	MAX16990ATEF/V+, MAX16992ATEF/V+	MAX16990ATED/V+, MAX16992ATED/V+	NAME	FUNCTION
µMAX-EP	TQFN-EP	TQFN-EP	TQFN-EP	TQFN-EP		
1	1	1	1	1	SUP	Power-Supply Input. Place a bypass capacitor of at least 1µF between this pin and ground.
2	3	3	4	4	EN	Active-High Enable Input. This input is high-voltage-capable or can alternatively be driven from a logic-level signal.
3	2	2	3	3	GND	Ground Connection
4	4	4	5	5	DRV	Drive Output for Gate of nMOS Boost Switch. The nominal voltage swing of this output is between PVL and GND.
5	5	5	7	7	PVL	Output of 5V Internal Regulator. Connect a ceramic capacitor of at least 2.2µF from this pin to ground, placing it as close as possible to the pin.
6	6	6	8	8	ISNS	Current-Sense Input to Regulator. Connect a sense resistor between the source of the external switching FET and GND. Then connect another resistor between ISNS and the source of the FET for slope compensation adjustment.
—	—	7	9	—	SYNCO	Open-Drain Synchronization Output. SYNCO outputs a square-wave signal which is 180° out-of-phase with the device's operational clock. Connect a pullup resistor from this pin to PVL or to a 5V or lower supply when used.
—	7	—	—	9	OVP	Overvoltage Protection Input. When this pin goes above 110% of the FB regulation voltage, all switching is disabled. Operation resumes normally when OVP drops below 107.5% of the FB regulation point. Connect a resistor divider between the output, OVP, and GND to set the overvoltage protection level.

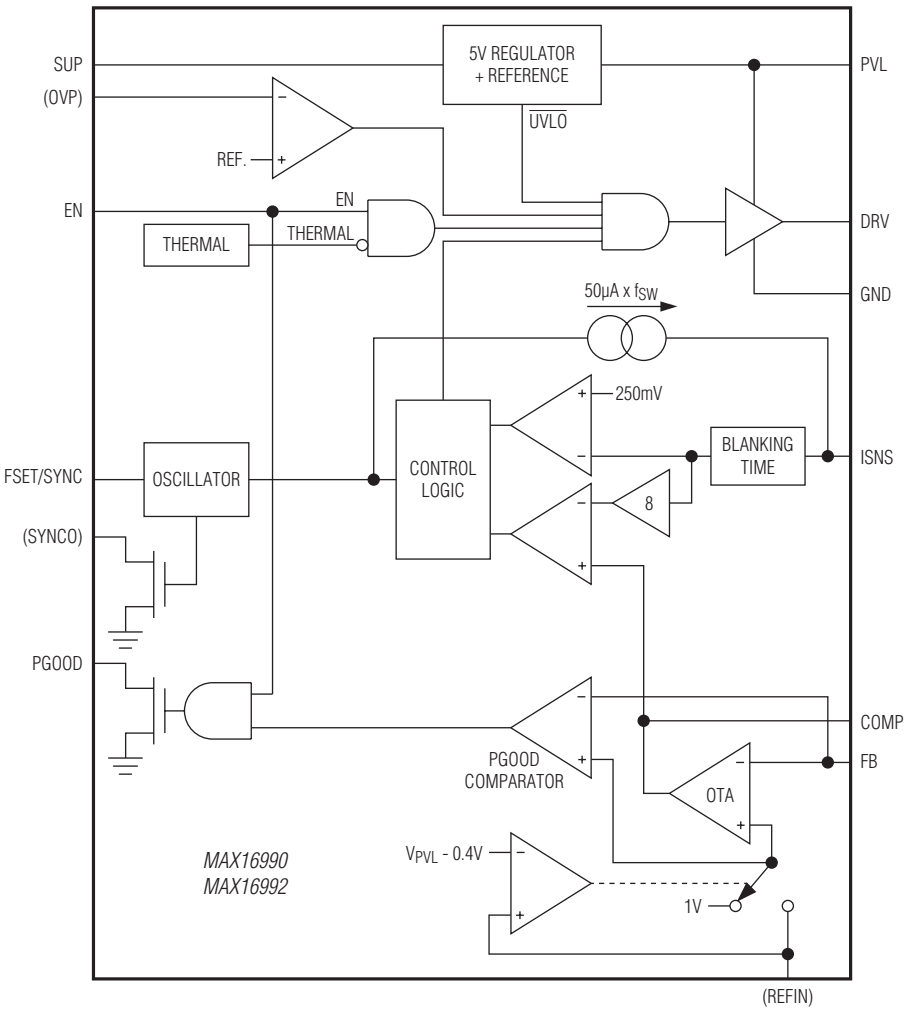
Pin Descriptions (continued)

MAX16990AUBA/B, MAX16992AUBA/B	MAX16990ATCC/D, MAX16992ATCC/D	MAX16990ATCE/F, MAX16992ATCE/F	MAX16990ATEF/V+, MAX16992ATEF/V+	MAX16990ATED/V+, MAX16992ATED/V+	NAME	FUNCTION
µMAX-EP	TQFN-EP	TQFN-EP	TQFN-EP	TQFN-EP		
—	8	8	10	10	REFIN	Reference Input. When using the internal reference, connect REFIN to PVL. Otherwise, drive this pin with an external voltage between 0.5V and 2V to set the boost output voltage.
7	9	9	11	11	PGOOD	Open-Drain Power-Good Output. Connect a resistor from this pin to PVL or to another voltage less than or equal to 5V. PGOOD goes high after soft-start when the output exceeds 90% of its final value. When EN is low, PGOOD is also low. After soft-start is complete, if PGOOD goes low and 16 consecutive current-limit cycles occur, the devices enter hiccup mode and a new soft-start is initiated after a delay of 44ms.
8	10	10	12	12	FSET/ SYNC	Frequency Set/Synchronization. To set a switching frequency between 100kHz and 1000kHz (MAX16990) or between 1000kHz and 2500kHz (MAX16992), connect a resistor from this pin to GND. To synchronize the converter, connect a logic signal in the range 220kHz to 1000kHz (MAX16990) or 1000kHz to 2500kHz (MAX16992) to this input. The external n-channel MOSFET is turned on (i.e., DRV goes high) after a short delay (60ns for 2.2MHz operation, 125ns for 400kHz) when SYNC transitions low.
9	11	11	14	14	COMP	Output of Error Amplifier. Connect the compensation network between COMP and GND.

Pin Descriptions (continued)

MAX16990AUBA/B, MAX16992AUBA/B	MAX16990ATCC/D, MAX16992ATCC/D	MAX16990ATCE/F, MAX16992ATCE/F	MAX16990ATEF/V+, MAX16992ATEF/V+	MAX16990ATED/V+, MAX16992ATED/V+	NAME	FUNCTION
µMAX-EP	TQFN-EP	TQFN-EP	TQFN-EP	TQFN-EP		
10	12	12	16	16	FB	Boost Converter Feedback. This pin is regulated to 1V when REFIN is tied to PVL or otherwise regulated to REFIN during boost operation. Connect a resistor divider between the boost output, the FB pin, and GND to set the boost output voltage. In a two-phase converter, connect the FB pin of the slave IC to PVL.
—	—	—	2	2	NC	No Connect
—	—	—	6	6	NC	No Connect
—	—	—	13	13	NC	No Connect
—	—	—	15	15	NC	No Connect
—	—	—	—	—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram



Detailed Description

The MAX16990/MAX16992 are high-performance, current-mode PWM controllers for wide input voltage range boost/SEPIC converters. The input operating voltage range of 4.5V to 36V makes these devices ideal in automotive applications such as for front-end “preboost” or “SEPIC” power supplies and for the first boost stage in high-power LED lighting applications. An internal low-dropout regulator (PVL regulator) with an output voltage of 5V enables the devices to operate directly from an automotive battery input. The input operating range can be as low as 2.5V when the converter output supplies the SUP input.

The input undervoltage lockout (UVLO) circuit monitors the PVL voltage and turns off the converter when the voltage drops below 3.6V (typ). An external resistor programs the switching frequency in two ranges from 100kHz to 1000kHz (MAX16990) or between 1000kHz and 2500kHz (MAX16992). The FSET/SYNC input can also be used for synchronization to an external clock. The SYNC pulse width should be greater than 70ns.

Inductor current information is obtained by means of an external sense resistor connected from the source of the external n-channel MOSFET to GND.

The devices include an internal transconductance error amplifier with 1% accurate reference. At startup, the internal reference is ramped in a time of 9ms to obtain soft-start.

The devices also include protection features such as hiccup mode and thermal shutdown, as well as an optional overvoltage-detection circuit (OVP pin, C and D versions).

Current-Mode Control Loop

The MAX16990/MAX16992 offers peak current-mode control operation for best load-step performance and simpler compensation. The inherent feed-forward characteristic is especially useful in automotive applications where the input voltage changes quickly during cold-crank and load-dump conditions. While the current-mode architecture offers many advantages, there are some shortcomings. In high duty-cycle operation, subharmonic oscillations can occur. To avoid this, the device offers programmable slope compensation using a single resistor between the ISNS pin and the current-sense resistor. To avoid premature turn-off at the beginning of the on-cycle, the current-limit and PWM comparator inputs have leading-edge blanking.

Startup Operation/UVLO/EN

The devices feature undervoltage lockout on the PVL-regulator and turn on the converter once PVL rises above 4V. The internal UVLO circuit has about 400mV hysteresis to avoid chattering during turn-on. Once the converter is operating and if SUP is fed from the output, the converter input voltage can drop below 4.5V. This feature allows operation at cold-crank voltages as low as 2.5V or even lower with careful selection of external components. The EN input can be used to disable the device and reduce the standby current to less than 4µA (typ).

Soft-Start

The devices are provided with an internal soft-start time of 9ms. At startup, after voltage is applied and the UVLO threshold is reached, the device enters soft-start. During soft-start, the reference voltage ramps linearly to its final value in 9ms.

Oscillator Frequency/External Synchronization/ Spread Spectrum

Use an external resistor at FSET/SYNC to program the MAX16990 internal oscillator frequency from 100kHz to 1MHz and the MAX16992 frequency between 1MHz and 2.5MHz. See TOCs 24 and 25 in the *Typical Operating Characteristics* section for resistor selection.

The SYNCO output is a 180° phase-shifted version of the internal clock, and can be used to synchronize other converters in the system or to implement a two-phase boost converter with a second MAX16990/MAX16992. The advantages of a two-phase boost topology are lower input and output ripple and simpler thermal management as the power dissipation is spread over more components. See the *Multiphase Operation* section for further details.

The devices can be synchronized using an external clock at the FSET/SYNC input. A falling clock edge on FSET/SYNC turns on the external MOSFET by driving DRV high after a short delay.

The B, D, and F versions of the devices have spread-spectrum oscillators. In these parts, the internal oscillator frequency is varied dynamically ±6% around the switching frequency. Spread spectrum can improve system EMI performance by reducing the height of peaks due to the switching frequency and its harmonics in the spectrum. The SYNCO output includes spread-spectrum modulation when the internal oscillator is used on the B, D, and F versions. Spread spectrum is not active when an external clock is applied to the FSET/SYNC pin.

n-Channel MOSFET Driver

DRV drives the gate of an external n-channel MOSFET. The driver is powered by the internal regulator (PVL), which provides approximately 5V. This makes both the devices suitable for use with logic-level MOSFETs. DRV can source 750mA and sink 1000mA peak current. The average current sourced by DRV depends on the switching frequency and total gate charge of the external MOSFET (see the *Power Dissipation* section).

Error Amplifier

The devices include an internal transconductance error amplifier. The noninverting input of the error amplifier is connected to the internal 1V reference and feedback is provided at the inverting input. High 700µS open-loop transconductance and 50MΩ output impedance allow good closed-loop bandwidth and transient response. Moreover, the source and sink current capability of 140µA provides fast error correction during output load transients.

Slope Compensation

The devices use an internal current-ramp generator for slope compensation. The internal ramp signal resets at the beginning of each cycle and slews at a typical rate of 50µA x f_{SW}. The amount of slope compensation needed depends on the slope of the current ramp in the inductor. See the *Current-Sense Resistor Selection and Setting Slope Compensation* section for further information.

Current Limit

The current-sense resistor (R_{CS}) connected between the source of the MOSFET and ground sets the current limit. The ISNS input has a voltage trip level (V_{CS}) of 250mV. When the voltage produced by the current in the inductor exceeds the current-limit comparator threshold, the MOSFET driver (DRV) quickly terminates the on-cycle. In some cases, a short time-constant RC filter could be required to filter out the leading-edge spike on the sense waveform in addition to the internal blanking time. The amplitude and width of the leading edge spike depends on the gate capacitance, drain capacitance, and switching speed (MOSFET turn-on time).

Hiccup Operation

The devices incorporate a hiccup mode to protect the external power components when there is an output short-circuit. If PGOOD is low (i.e., the output voltage is less than 85% of its set value) and there are 16 consecutive current-limit events, switching is stopped. There is then a waiting period of 44ms before the device tries to restart by initiating a soft-start. Note that a short-circuit on the output places considerable stress on all the power components even with hiccup mode, so that careful component selection is important if this condition is encountered. For more complete protection against output short-circuits, a series pMOS switch driven from PGOOD through a level-shifter can be employed (see Figure 1).

Applications Information

Inductor Selection

Using the following equation, calculate the minimum inductor value so that the converter remains in continuous mode operation at minimum output current (I_{OMIN}):

$$L_{MIN} = (V_{IN}^2 \times D \times \eta)/(2 \times f_{SW} \times V_{OUT} \times I_{OMIN})$$

where:

$$D = (V_{OUT} + V_D - V_{IN})/(V_{OUT} + V_D - V_{DS})$$

and:

$$I_{OMIN} \text{ is between 10\% and 25\% of } I_{OUT}$$

A higher value of I_{OMIN} reduces the required inductance, but it increases the peak and RMS currents in the switching MOSFET and inductor. Select I_{OMIN} between 10% to 25% of the full load current. V_D is the forward voltage drop of the external Schottky diode, D is the duty cycle, and V_{DS} is the voltage drop across the external switch. Select an inductor with low DC resistance and with a saturation current (I_{SAT}) rating higher than the peak switch current limit of the converter.

Input and Output Capacitors

The input current to a boost converter is almost continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and maximum ESR using the following equations:

$$C_{IN} = DI_L \times D/(4 \times f_{SW} \times DV_Q)$$

$$ESR_{MAX} = DV_{ESR}/DI_L$$

where $DI_L = ((V_{IN} - V_{DS}) \times D)/(L \times f_{SW})$.

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. DI_L is peak-to-peak inductor ripple current as calculated above. DV_Q is the portion of input ripple due to the capacitor discharge and DV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (DV_{ESR}) and capacitor discharge (DV_Q) are equal when using a combination of ceramic and aluminium capacitors. During the converter turn-on, a large current is drawn from the input source,

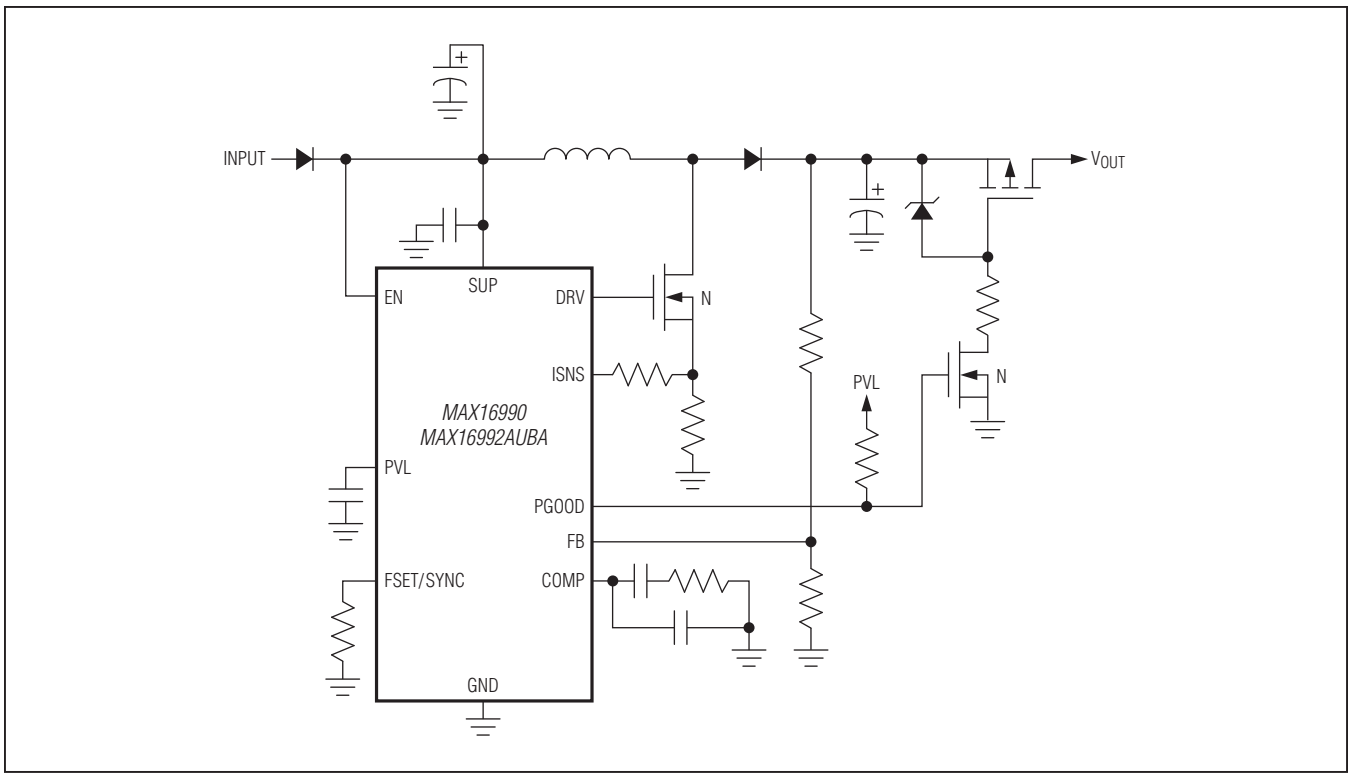


Figure 1. Application with Output Short-Circuit Protection

especially at high output-to-input differential. The devices have an internal soft-start, but a larger input capacitor than calculated above could be necessary to avoid chattering due to finite hysteresis during turn-on.

In a boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at lower duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to ESR while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak.

$$ESR = DV_{ESR}/I_{OUT}$$

$$C_{OUT} = (I_{OUT} \times D_{MAX})/(DV_Q \times f_{SW})$$

where I_{OUT} is the output current, DV_Q is the portion of the ripple due to the capacitor discharge, and DV_{ESR} is the ripple contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle (i.e., the duty cycle at the minimum input voltage). Use a combination of low-ESR ceramic and high-value, low-cost aluminium capacitors for lower output ripple and noise.

Current-Sense Resistor Selection and Setting Slope Compensation

Set the current-limit threshold 20% higher than the peak switch current at the rated output power and minimum input voltage. Use the following equation to calculate an initial value for R_{CS}:

$$R_{CS} = 0.2/\{1.2 \times [((V_{OUT} \times I_{OUT})/\eta)/V_{INMIN} + 0.5 \times ((V_{OUT} - V_{INMIN})/V_{OUT}) \times (V_{INMIN}/(f_{SW} \times L))]\}$$

where η is the estimated efficiency of the converter (use 0.85 as an initial value or consult the graph in the *Typical Operating Characteristics* section); V_{OUT} and I_{OUT} are the output voltage and current, respectively; V_{INMIN} is the minimum value of the input voltage; f_{SW} is the switching frequency; and L is the minimum value of the chosen inductor.

The devices use an internal ramp generator for slope compensation to stabilize the current loop when operating at duty cycles above 50%. The amount of slope

compensation required depends on the down-slope of the inductor current when the main switch is off. The inductor down-slope in turn depends on the input to output voltage differential of the converter and the inductor value. Theoretically, the compensation slope should be equal to 50% of the inductor downslope; however, a little higher than 50% slope is advised. Use the following equation to calculate the required compensating slope (mc) for the boost converter:

$$mc = 0.5 \times (V_{OUT} - V_{IN})/L \text{ A/s}$$

The internal ramp signal resets at the beginning of each cycle and slews at the rate of 50µA x f_{SW}. Adjust the amount of slope compensation by choosing R_{SCOMP} to satisfy the following equation:

$$R_{SCOMP} = (mc \times R_{CS})/(50e\text{-}6 \times f_{SW})$$

In some applications, a filter could be needed between the current-sense resistor and the ISNS pin to augment the internal blanking time. Set the RC time constant just long enough to suppress the leading edge spike of the MOSFET current. For a given design, measure the leading spike at the lowest input and rated output load to determine the value of the RC filter which can be formed from the slope-compensation resistor and an added capacitor from ISNS to GND.

MOSFET Selection

The devices drive a wide variety of logic-level n-channel power MOSFETs. The best performance is achieved with low-threshold n-channel MOSFETs that specify on-resistance with a gate-source voltage (V_{GS}) of 5V or less. When selecting the MOSFET, key parameters can include:

1) Total gate charge (Q_g).
2) Reverse-transfer capacitance or charge (C_{RSS}).
3) On-resistance ($R_{DS(ON)}$).
4) Maximum drain-to-source voltage ($V_{DS(MAX)}$).
5) Maximum gate frequencies threshold voltage ($V_{TH(MAX)}$).

At high switching frequencies, dynamic characteristics (parameters 1 and 2 of the above list) that predict switching losses have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Qg includes all capacitances associated with charging the gate. The $V_{DS(MAX)}$ of the selected MOSFET must be greater than the maximum output voltage setting plus a diode drop (or the maximum input voltage if greater) plus an additional margin to allow for spikes at the MOSFET drain due to the inductance in the rectifier diode and output capacitor path. In addition, Q_g determines the current needed to drive the gate at the selected operating frequency using the PVL linear regulator and therefore determines the power dissipation of the IC (see the *Power Dissipation* section).

Low-Voltage Operation

The devices operate down to a voltage of 4.5V or less on their SUP pins. If the system input voltage is lower than this, the circuit can be operated from its own output as shown in the *Typical Application Circuit*. At very low input voltages, it is important to remember that input current will be high and the power components (inductor, MOSFET and diode) must be specified for this higher input current. In addition, the current limit of the devices must be set high enough so that the limit is not reached during the on-time of the MOSFET, which would result in output-power limitation and eventually, entering hiccup mode. Estimate the maximum input current using the following equation:

$$I_{INMAX} = ((V_{OUT} \times I_{OUT})/\eta)/V_{INMIN} + 0.5 \times ((V_{OUT} - V_{INMIN})/V_{OUT}) \times (V_{INMIN}/(f_{SW} \times L))$$

where I_{INMAX} is the maximum input current; V_{OUT} and I_{OUT} are the output voltage and current, respectively; η is the estimated efficiency (which is lower at low input voltages due to higher resistive losses); V_{INMIN} is the minimum value of the input voltage; f_{SW} is the switching frequency; and L is the minimum value of the chosen inductor.

Boost Converter Compensation

Refer to Application Note 5587: *Selecting External Components and Compensation for Automotive Step-Up DC-DC Regulator with Preboost Reference Design*.

SEPIC Operation

For a reference example of using the devices in SEPIC mode, see Figure 2.

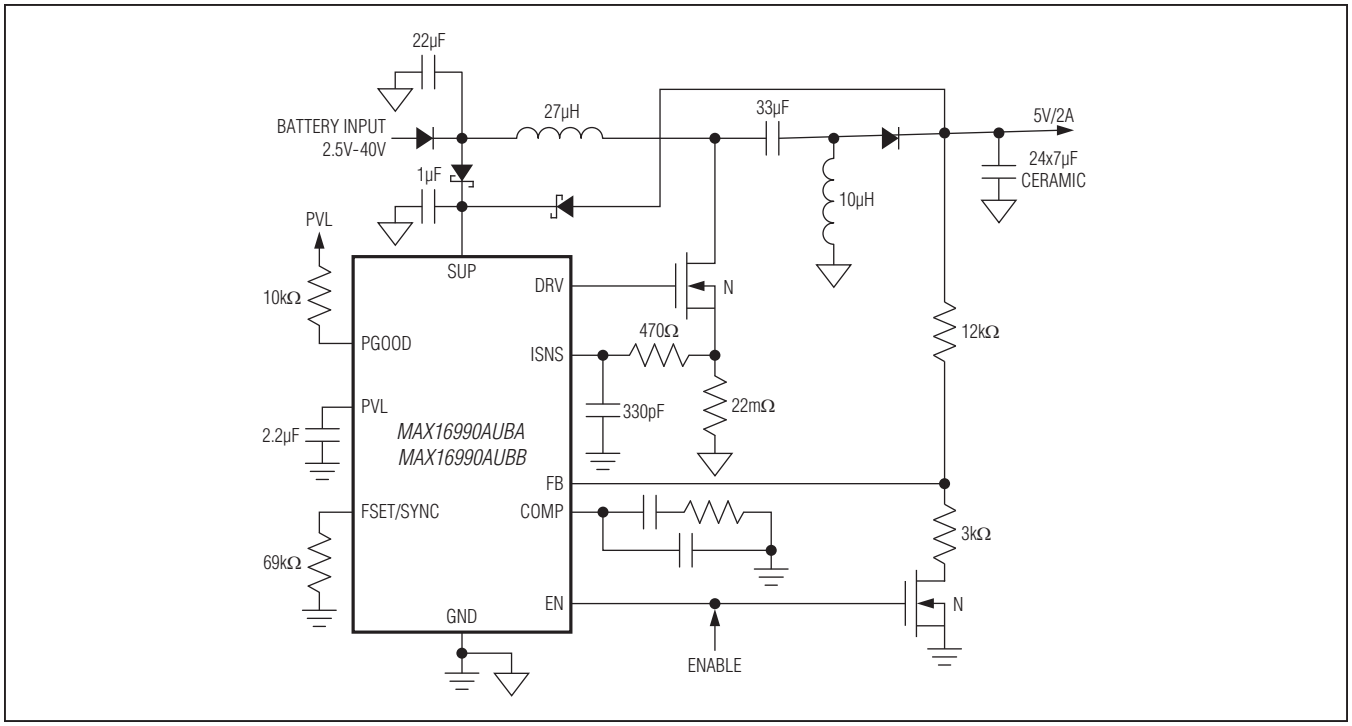


Figure 2. SEPIC Bootstrapped 400kHz Application with Low Operating Voltage

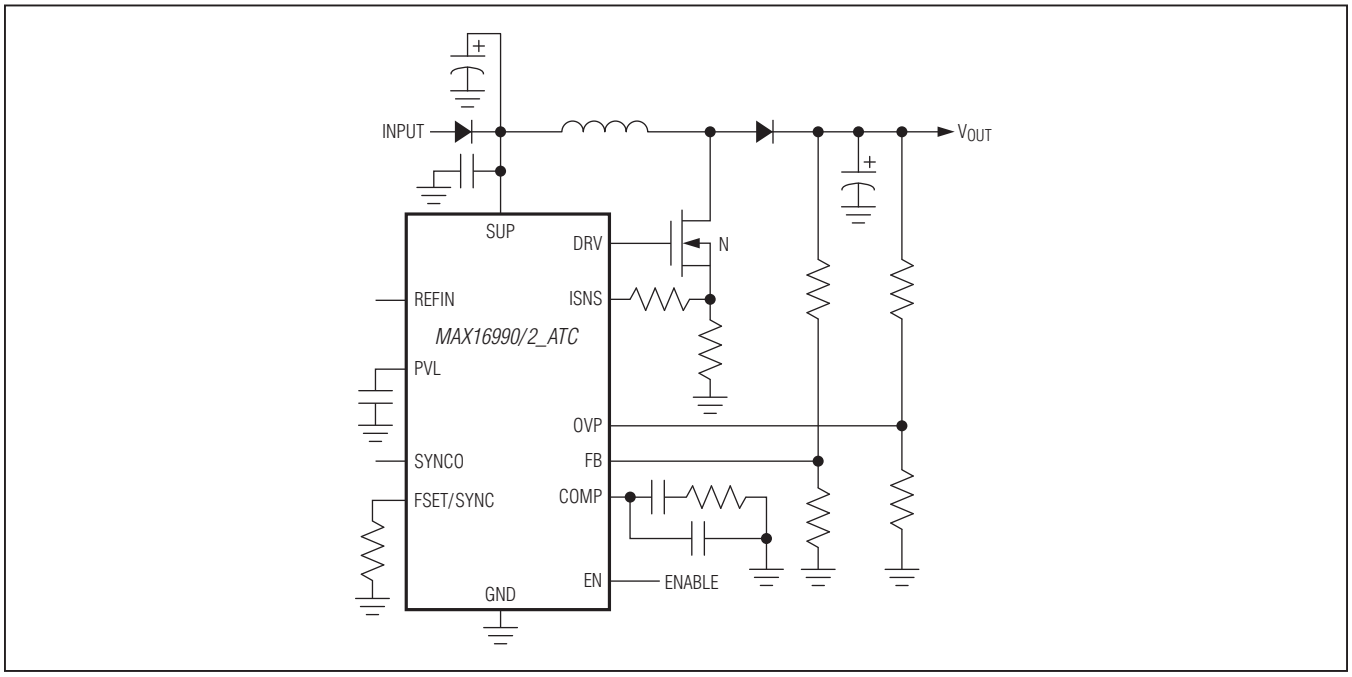


Figure 3. Application with Independent Output Overvoltage Protection

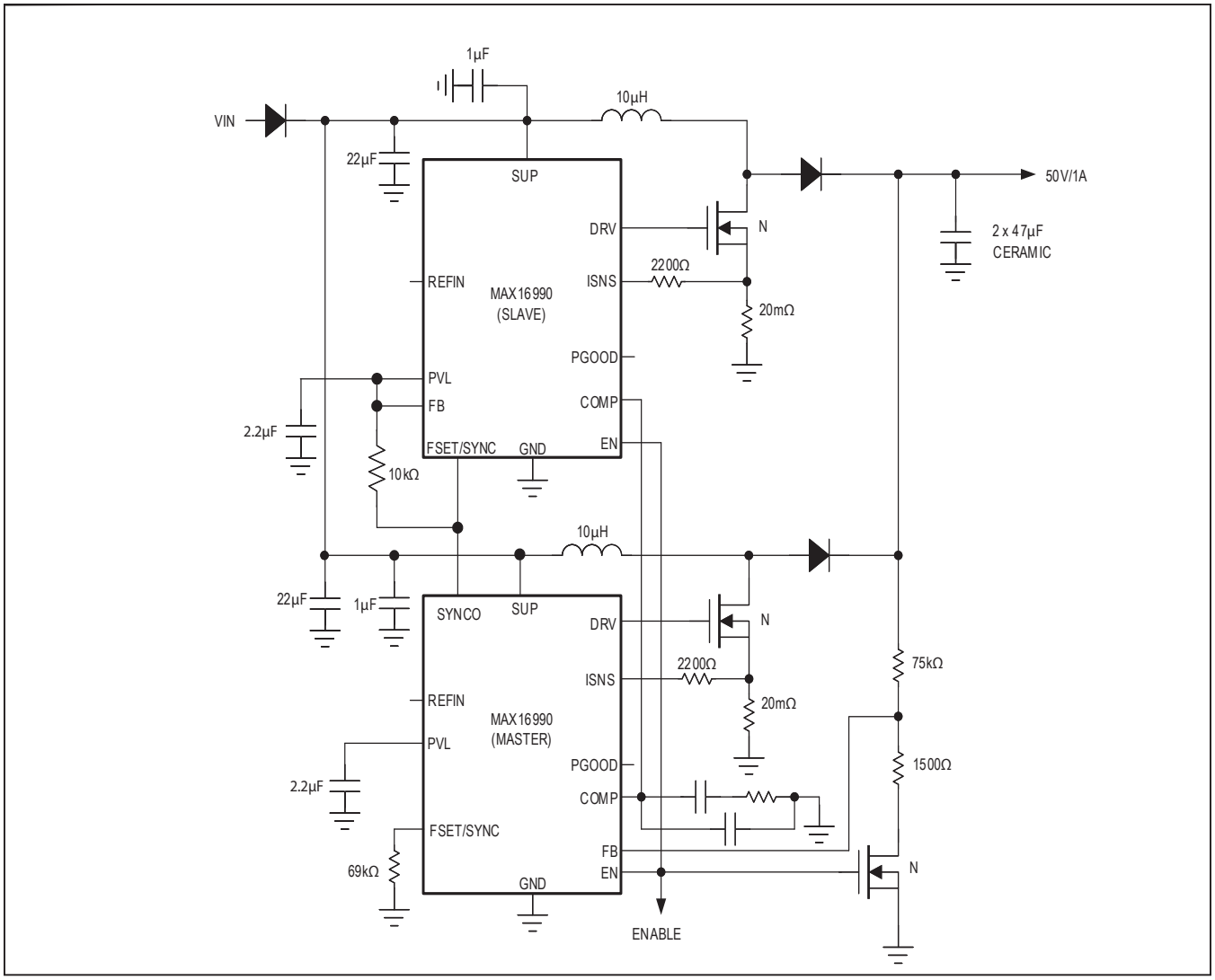


Figure 4. Two-Phase 400kHz Boost Application with Minimum Component Count

Overvoltage Protection

The “C” and “D” variants of the devices include the overvoltage protection input. When the OVP pin goes above 110% of the FB regulation voltage, all switching is disabled. For an example application circuit, see Figure 3.

Multiphase Operation

Two boost phases can be implemented with no extra components, using two ICs as shown in Figure 4. In this circuit, the SYNCO output of the master device drives the SYNC input of the slave, forcing it to operate 180° out of phase. The FB pin of the slave device is connected to PVL, thus disabling its error amplifier. In this way, the error amplifier of the master controls both devices by means of the COMP signal, and good current-sharing is attained between the two phases. When designing the PCB for a multiphase converter, it is important to protect the COMP trace in the layout from noisy signals by placing it on an inner layer and surrounding it with ground traces.

Using REFIN to Adjust the Output Voltage

The REFIN pin can be used to directly adjust the reference voltage of the boost converter, thus altering the output voltage. When not used, REFIN should be connected to PVL. Because REFIN is a high-impedance pin, it is simple to drive it by means of an external digital-to-analog converter (DAC) or a filtered PWM signal.

Power Dissipation

The power dissipation of the IC comes from two sources: the current consumption of the IC itself and the current required to drive the external MOSFET, of which the latter is usually dominant. The total power dissipation can be estimated using the following equation:

$$P_{IC} = V_{SUP} \times I_{CC} + (V_{SUP} - 5) \times (Q_g \times f_{SW})$$

where V_{SUP} is the voltage at the SUP pin of the IC, I_{CC} is the IC quiescent current consumption or typically 0.75mA (MAX16990) or 1.25mA (MAX16992), Q_g is the total gate charge of the chosen MOSFET at 5V, and f_{SW} is the switching frequency. P_{IC} reaches its maximum at maximum V_{SUP}.

Ordering Information

PART	FREQUENCY RANGE	OVP/ SYNCO	SPREAD SPECTRUM	TEMP RANGE	PIN-PACKAGE
MAX16990AUBA/V+	220kHz to 1MHz	None	Off	-40°C to +125°C	10 µMAX-EP*
MAX16990AUBB/V+	220kHz to 1MHz	None	On	-40°C to +125°C	10 µMAX-EP*
MAX16990ATCC/V+	220kHz to 1MHz	OVP	Off	-40°C to +125°C	12 TQFN-EP*
MAX16990ATCD/V+	220kHz to 1MHz	OVP	On	-40°C to +125°C	12 TQFN-EP*
MAX16990ATCD/VY+	220kHz to 1MHz	OVP	On	-40°C to +125°C	12 SWTQFN-EP*
MAX16990ATCE/V+	220kHz to 1MHz	SYNCO	Off	-40°C to +125°C	12 TQFN-EP*
MAX16990ATCF/V+	220kHz to 1MHz	SYNCO	On	-40°C to +125°C	12 TQFN-EP*
MAX16990ATED/V+	220kHz to 1MHz	OVP	On	-40°C to +125°C	16 TQFN-EP*
MAX16990ATEF/V+	220Hz to 1MHz	SYNCO	On	-40°C to +125°C	16 TQFN-EP*
MAX16992AUBA/V+	1MHz to 2.5MHz	None	Off	-40°C to +125°C	10 µMAX-EP*
MAX16992AUBB/V+	1MHz to 2.5MHz	None	On	-40°C to +125°C	10 µMAX-EP*
MAX16992ATCC/V+	1MHz to 2.5MHz	OVP	Off	-40°C to +125°C	12 TQFN-EP*
MAX16992ATCD/V+	1MHz to 2.5MHz	OVP	On	-40°C to +125°C	12 TQFN-EP*
MAX16992ATCD/VY+	1MHz to 2.5MHz	OVP	On	-40°C to +125°C	12 SWTQFN-EP*
MAX16992ATCE/V+	1MHz to 2.5MHz	SYNCO	Off	-40°C to +125°C	12 TQFN-EP*
MAX16992ATCF/VY+	1MHz to 2.5MHz	SYNCO	On	-40°C to +125°C	12 SWTQFN-EP*
MAX16992ATED/V+	1MHz to 2.5MHz	OVP	On	-40°C to +125°C	16 TQFN-EP*
MAX16992ATEF/V+	1MHz to 2.5MHz	SYNCO	On	-40°C to +125°C	16 TQFN-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product - contact factory for availability*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PKG CODE	OUTLINE NO.	LAND PATTERN NO.
12 SWTQFN-EP	T1233Y+4	21-100171	90-100060
12 TQFN-EP	T1233+4	21-0136	90-0019
10 µMAX-EP	U10E+3	21-0109	90-0148
16 TQFN-EP	T1633+5	21-0136	90-0032

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—
1	4/13	Added EP to µMAX package in *Pin Descriptions*	9–11
2	4/13	Corrected errors in TOCs 21 and 29	7, 8
3	7/13	Removed future product asterisks from *Ordering Information*	18
4	2/15	Update the *Benefits and Features* section	1
5	7/15	Corrected value in Figure 2, changing inductor value from 22µF to 22µH	16
6	8/15	Corrected part number in *Typical Application Circuit*	1
7	2/17	Replaced toc18 in *Typical Operating Characteristics*, added MAX16992ATCF/VY+ in Ordering Information as a future product, and added SWTQFN-EP (package code T1233Y+4) in *Package Information* sections	7, 18
8	7/17	Added Note 3 to SUP Operating Supply Range in the *Electrical Characteristics* table	2
9	9/17	Deleted Note 3 in and after the *Electrical Characteristics* table	2, 4
10	5/18	Replaced Figure 4 and added MAX16990ATCD/VY+** to *Ordering Information*	17,18
11	8/18	Added MAX16992ATCD/VY+ to *Ordering Information* as a future product	18
12	10/18	Removed future product status from MAX16990ATCD/VY+ in *Ordering Information*	18
13	4/19	Removed future product status from MAX16992ATCF/VY+ and future product-contact factory for availability note *Ordering Information* section	18
14	6/19	Updated *Absolute Maximum Ratings* and *Package Thermal Characteristics*	2
14.1		Corrected broken links in *Package Information* section	18
15	7/20	Updated *Absolute Maximum Ratings* and *Package Thermal Characteristics* sections, added TQFN-16 pin configurations, added two new columns to *Pin Descriptions* table, updated *Ordering Information* and *Package Information* tables	2, 9, 10, 18
16	9/20	Updated *Electrical Characteristics* and *Ordering Information* to add future-product notation	2, 3, 20
17	2/21	Updated *Ordering Information* to remove all future-product notation	20

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