MAX17693A/MAX17693B

4.2V–60V No-Opto Isolated Flyback Converter with Integrated FET

General Description

Maxim's Rainier family of isolated power devices enable cooler, smaller, and simpler power-supply solutions. The MAX17693A/B are high efficiency No-Opto integrated nMOSFET flyback converters that use fixed frequency peak current mode control. The device senses the isolated output voltage directly from the primary-side flyback waveform during the secondary-side rectifier conduction. No secondary-side error amplifier and optocoupler are required to provide an accurate, isolated, regulated output voltage, saving up to 20% of PCB space normally required for a traditional flyback converter.

The MAX17693A/B feature a low R_{DSON}, 76V, 245mΩ integrated nMOSFET primary switch and are designed to operate over a wide supply range from 4.2V to 60V. The switching frequency of the device is programmable from 100kHz to 350kHz. An EN/UVLO feature allows the user to turn ON/OFF the power converter precisely at the desired input voltage. Input overvoltage protection can be implemented using the OVI pin (MAX17693A only). Soft-start limits inrush current at startup. The MAX17693A/B support external clock synchronization to avoid low-frequency “beats” on the input bus in systems with multiple converters. The devices also have programmable frequency dithering for low-EMI, spread-spectrum operation.

The MAX17693A/B allow temperature compensation for variations in the output rectifier diode forward voltage drop. The MAX17693A is internally compensated for loop stability, while the MAX17693B offers external loop compensation flexibility. The MAX17693A/B have robust hiccup-protection and thermal protection schemes, and are available in space-saving 12-pin, 3mm x 3mm TDFN packages with a temperature range from -40°C to +125°C.

Applications

- Isolated Power Supplies
- PLC I/O Modules
- IGBT Gate Drive Supplies
- Industrial and Telecom Applications

Benefits and Features

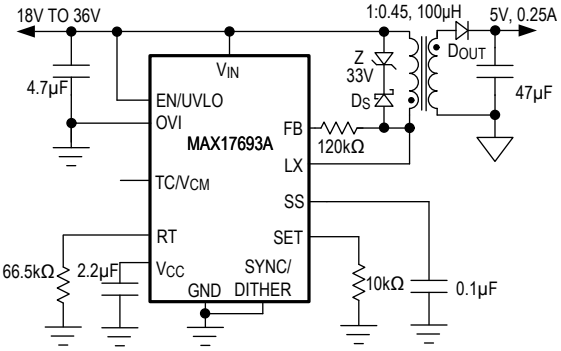
- Reduces External Components and Total Cost
  - Eliminates the Optocoupler and Secondary-Side Error Amplifier
  - Up to 20% Space Savings
  - 76V, Low R_{DSON} Integrated nMOSFET
  - Internal Loop Compensation (MAX17693A)
  - Built-In Soft-Start
- Reduces Power Dissipation
  - Delivers up to 1.4W Output Power
  - Frequency Fold-Back Enables Enhanced Light-Load Efficiency
  - 2.5µA Shutdown Current
- Supports Key System-Level Design Requirements
  - Frequency Dithering Supports Low-EMI, Spread-Spectrum Operation
  - Switching Frequency Synchronization to External Clock
- Operates Reliably in Adverse Environments
  - Output Diode Forward Voltage Temperature Compensation
  - Hiccup Current-Limit Protection
  - Programmable EN/UVLO Threshold
  - Input Overvoltage (OVI) Protection (MAX17693A)
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/ -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

19-101081; Rev 0; 4/21

maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

V_{IN}, EN/UVLO to GND ..... -0.3V to +70V
LX to GND ..... -0.3V to +80V
V_{IN} to FB ..... -0.3V to +0.3V
V_{CC} to GND..... -0.3V to +16V
OVI (MAX17693A)..... -0.3V to +6V
COMP (MAX17693B) ..... -0.3V to +6V
RT, SYNC/DITHER, SS, SET, and TC/V_{CM} to GND -0.3V to +6V
LX RMS Current ..... +1.72A

Continuous Power Dissipation (Single-Layer Board) (T_A = +70ºC, Derate 15.9mW/ºC above +70ºC).....1269.80mW
Continuous Power Dissipation (Multilayer Board) (T_A = +70ºC, derate 24.4mW/ºC above +70ºC) 1951.20mW
Operating Temperature Range (Note 1).....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN

Package Code	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	63°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = V_{FB} = $V_{EN/UVLO}$ = 24V, V_{OVI} = 0V (MAX17693A), COMP = OPEN (MAX17693B), C_{VCC} = 2.2µF to GND; V_{GND} = $V_{TC/VCM}$ = $V_{SYNC/DITHER}$ = 0V, RT, LX, SS = OPEN, R_{SET} = 10kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
Input-Voltage Range	V_{IN}		4.2		60	V
Input-Supply Shutdown Current	I_{IN_SHDN}	EN/UVLO = GND		2.5		µA
Input-Supply Current	I_Q	No Load		0.95		mA

Electrical Characteristics (continued)

(V_{IN} = V_{FB} = $V_{EN/UVLO}$ = 24V, V_{OVI} = 0V (MAX17693A), COMP = OPEN (MAX17693B), C_{VCC} = 2.2µF to GND; V_{GND} = $V_{TC/VCM}$ = $V_{SYNC/DITHER}$ = 0V, RT, LX, SS = OPEN, R_{SET} = 10kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN/UVLO						
EN/UVLO Threshold	V_{ENR}	V_{EN} Rising	1.19	1.215	1.24	V
	V_{ENF}	V_{EN} Falling	1.07	1.1	1.12	
True Shutdown EN/ UVLO Threshold	V_{ENSHDN}			0.8		V
EN/UVLO Input Leakage Current	I_{ENLKG}	V_{EN} = 2V, T_A = T_J = +25ºC	-100		+100	nA
V_{CC}						
V_{CC} Regulation Voltage	V_{CC}	V_{IN} = 7V, 100µA ≤ I_{VCC} ≤ 5mA	5.56	5.77	5.9	V
		7V ≤ V_{IN} ≤ 60V, I_{VCC} = 100µA	5.56	5.77	5.9	
V_{CC} Current Limit	I_{VCC_MAX}	V_{IN} = 7V, V_{VCC} = 4.3V	9.5	15	30	mA
V_{CC} Dropout	V_{DO}	V_{IN} = 4.5V, I_{VCC} = 3.5mA		120	260	mV
V_{CC} UVLO	$V_{VCC-UVR}$	Rising	3.9	4.0	4.1	V
	$V_{VCC-UVF}$	Falling	3.7	3.8	3.9	
OVI (MAX17693A)						
OVI Threshold	V_{OVI_R}	OVI Rising	1.19	1.215	1.24	V
	V_{OVI_F}	OVI Falling	1.07	1.1	1.12	
OVI Response Time		V_{OVI} step from 1V to 1.245V (30mV Overdrive)		2		µs
OVI Input-Leakage Current	I_{OVI}	V_{OVI} = 2V, T_A = T_J = 25ºC	-100		+100	nA
RT						
Switching-Frequency Range	f_{SWRT}		100		350	kHz
Switching-Frequency Accuracy		f_{SWRT} = 100kHz to 350kHz	-6		+6	%
Default Switching Frequency		RT = OPEN		200		kHz
SYNC/DITHER						
Synchronization Logic-High Input	V_{IH}		2.1			V
Synchronization Logic-Low Input	V_{IL}				0.8	V
Synchronization Pulse-Width			100			ns
Dithering Ramp Charging Current				21		µA
Dithering Ramp Discharging Current				21		µA

Electrical Characteristics (continued)

(V_{IN} = V_{FB} = $V_{EN/UVLO}$ = 24V, V_{OVI} = 0V (MAX17693A), COMP = OPEN (MAX17693B), C_{VCC} = 2.2µF to GND; V_{GND} = $V_{TC/VCM}$ = $V_{SYNC/DITHER}$ = 0V, RT, LX, SS = OPEN, R_{SET} = 10kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dithering Ramp–High Trip Point				2		V
Dithering Ramp–Low Trip Point				0.4		V
SS						
Soft-Start Charging Current	I_{SS}		4.75	5	5.25	µA
Default Soft-Start Time	t_{SS}		3.8	5.0	6.5	ms
LX						
Maximum Duty Cycle	D_{MAXOSC}	(Note 3)	65	68	71	%
Minimum LX On-Time	t_{ON_MIN}		150	180	210	ns
Minimum LX Off-Time To Sample Output Voltage	t_{OFF_MIN}		300	340	380	ns
Internal nMOSFET On Resistance	R_{DSON}	I_{LX} = 300mA		245	400	mΩ
CURRENT LIMIT (I_{LIM})						
Peak Current Limit	$I_{LX-PEAK-MAX}$	MAX17693A/B	0.495	0.543	0.600	A
Runaway Current Limit	$I_{LX-RUNAWAY}$	MAX17693A/B	0.6	0.666	0.74	A
Overcurrent Hiccup Timeout				16384		CYCLE
Minimum Peak Current	$I_{LX-PEAK-MIN}$	MAX17693A/B	0.07	0.091	0.117	A
SET						
SET Regulation Voltage	V_{SET}		0.988	1	1.012	V
TC/V_{CM}						
TC/V_{CM} Pin Bias Voltage	$V_{TC-BIAS}$	T_A = T_J = 25ºC		0.55		V
Temperature Compensation Coefficient	$\frac{\partial V_{TC/VCM}}{\partial T}$			+1.85		mV/ºC
COMP (MAX17693B)						
Error Amplifier Transconductance	Gm			660		µS
COMP Source Current	I_{COMP_SOURCE}	V_{COMP} = 2V, V_{SET} = 0.8V	33	55	90	µA
COMP Sink Current	I_{COMP_SINK}	V_{COMP} = 2V, V_{SET} = 1.2V	33	55	90	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SH}			160		ºC

Electrical Characteristics (continued)

(V_{IN} = V_{FB} = $V_{EN/UVLO}$ = 24V, V_{OVI} = 0V (MAX17693A), COMP = OPEN (MAX17693B), C_{VCC} = 2.2µF to GND; V_{GND} = $V_{TC/VCM}$ = $V_{SYNC/DITHER}$ = 0V, RT, LX, SS = OPEN, R_{SET} = 10kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Hysteresis				10		ºC

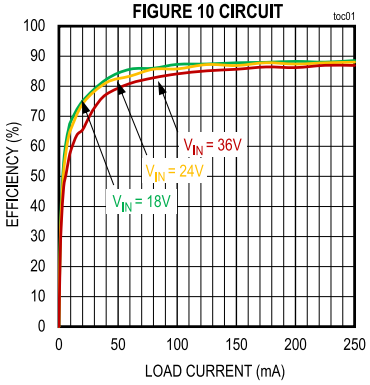
Note 2: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 3: Maximum duty cycle (D_{MAXOSC}) is not valid when an external clock is applied to the SYNC/DITHER pin. During external clock synchronization the minimum off-time on LX is decided by the internal oscillator frequency, which is set by R_{RT}. Refer to the *External Clock Synchronization and Switching Frequency Dithering (SYNC/DITHER)* section for more details.

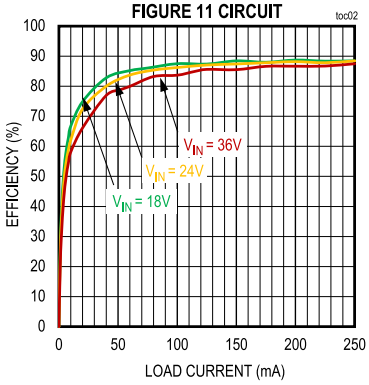
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{OVI} = V_{GND} = 0V, C_{IN} = 4.7µF, C_{VCC} = 2.2µF, T_A = +25°C unless otherwise noted.)

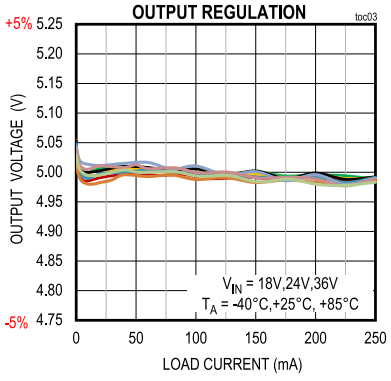
MAX17693A, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 10 CIRCUIT



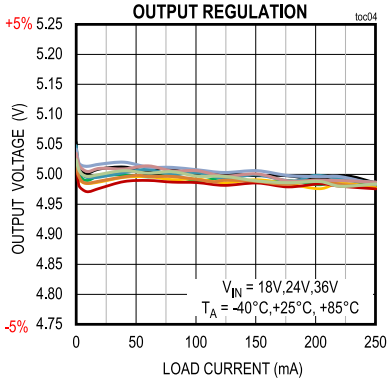
MAX17693B, 5V OUTPUT EFFICIENCY vs. LOAD CURRENT FIGURE 11 CIRCUIT



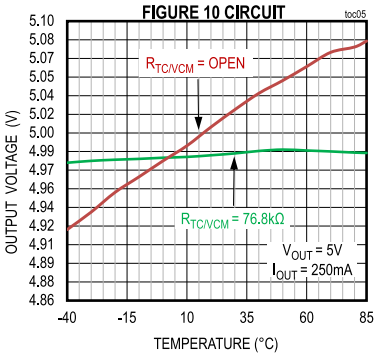
MAX17693A, 5V OUTPUT OUTPUT REGULATION



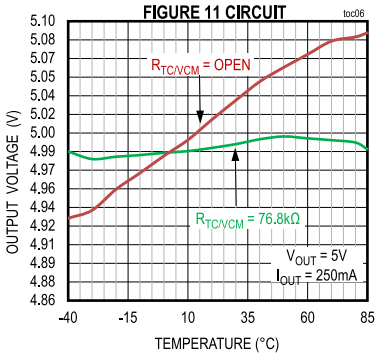
MAX17693B, 5V OUTPUT OUTPUT REGULATION



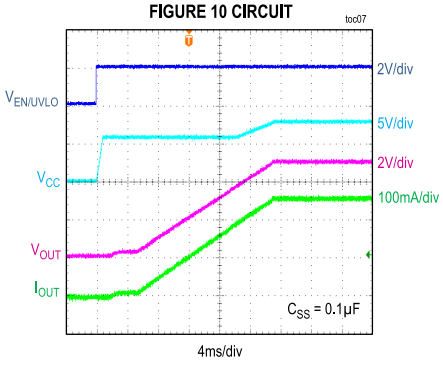
MAX17693A OUTPUT VOLTAGE vs. TEMPERATURE FIGURE 10 CIRCUIT



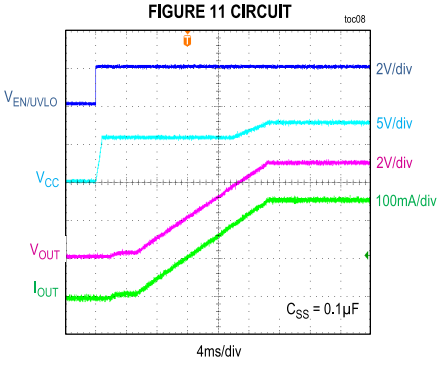
MAX17693B OUTPUT VOLTAGE vs. TEMPERATURE FIGURE 11 CIRCUIT



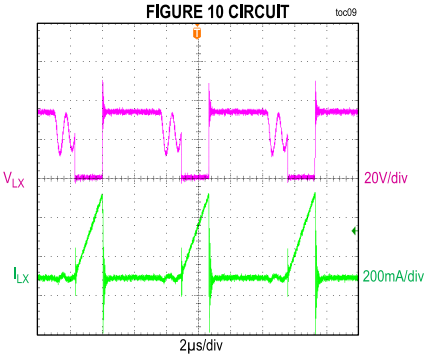
MAX17693A, SOFT-START 5V OUTPUT, 0.25A LOAD, FIGURE 10 CIRCUIT



MAX17693B, SOFT-START 5V OUTPUT, 0.25A LOAD, FIGURE 11 CIRCUIT



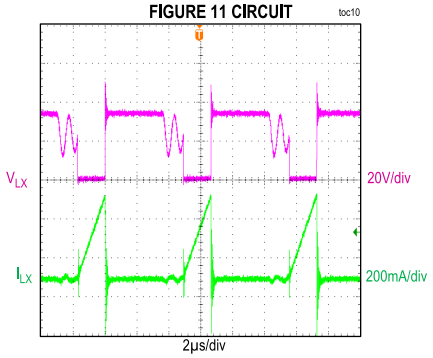
MAX17693A, STEADY-STATE SWITCHING WAVEFORMS 5V OUTPUT, 0.25A LOAD CURRENT, FIGURE 10 CIRCUIT



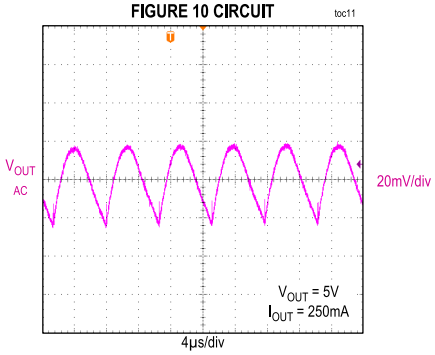
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{OVI} = V_{GND} = 0V, C_{IN} = 4.7µF, C_{VCC} = 2.2µF, T_A = +25°C unless otherwise noted.)

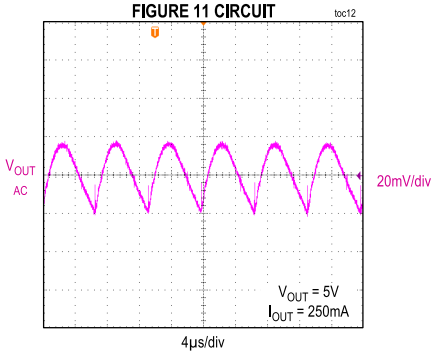
MAX17693B, STEADY-STATE SWITCHING WAVEFORMS
5V OUTPUT, 0.25A LOAD CURRENT,
FIGURE 11 CIRCUIT



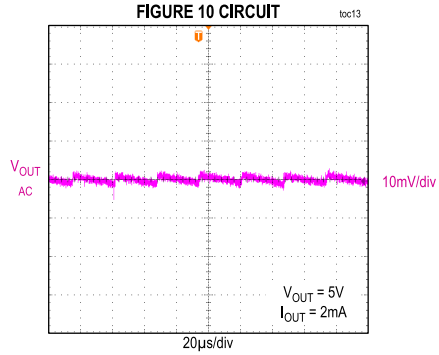
MAX17693A
OUTPUT-VOLTAGE RIPPLE
FIGURE 10 CIRCUIT



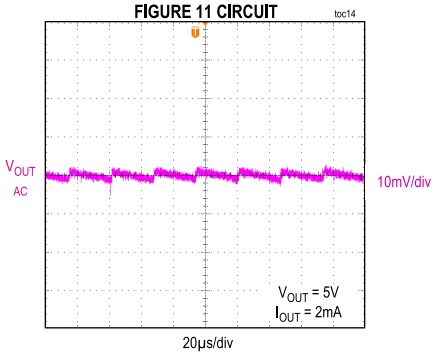
MAX17693B
OUTPUT-VOLTAGE RIPPLE
FIGURE 11 CIRCUIT



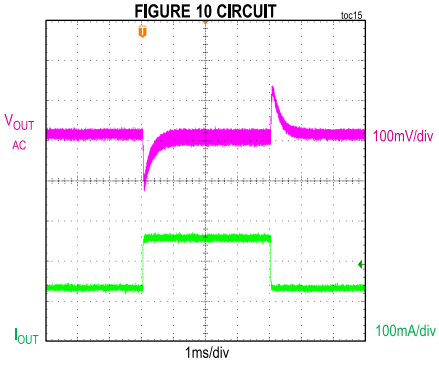
MAX17693A
OUTPUT-VOLTAGE RIPPLE
FIGURE 10 CIRCUIT



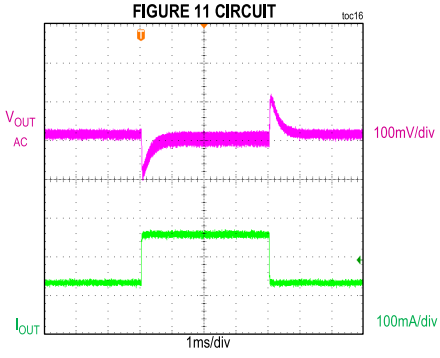
MAX17693B
OUTPUT VOLTAGE RIPPLE
FIGURE 11 CIRCUIT



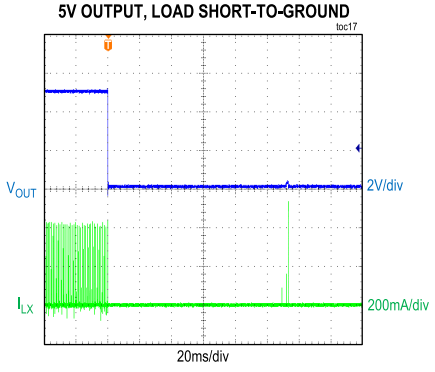
MAX17693A, LOAD TRANSIENT RESPONSE
LOAD CURRENT STEPPED FROM 0.125A TO 0.25A
FIGURE 10 CIRCUIT



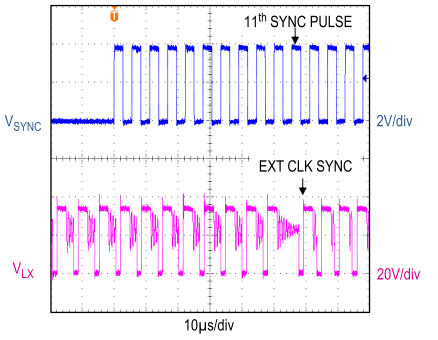
MAX17693B, LOAD TRANSIENT RESPONSE
LOAD CURRENT STEPPED FROM 0.125A TO 0.25A
FIGURE 11 CIRCUIT



SHORT-CIRCUIT PROTECTION
5V OUTPUT, LOAD SHORT-TO-GROUND

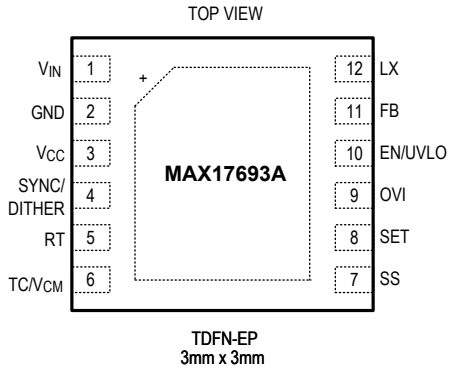


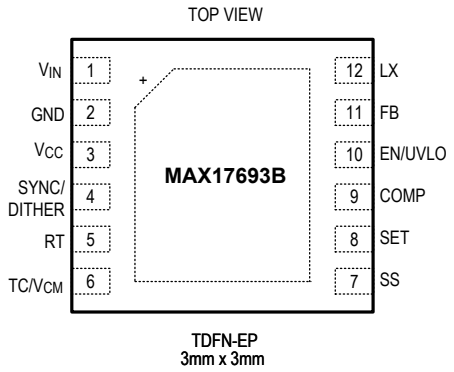
APPLICATION OF EXTERNAL CLOCK
AT 180kHz, 5V OUTPUT, 0.15A LOAD



Pin Configuration

MAX17693A/MAX17693B





Pin Description

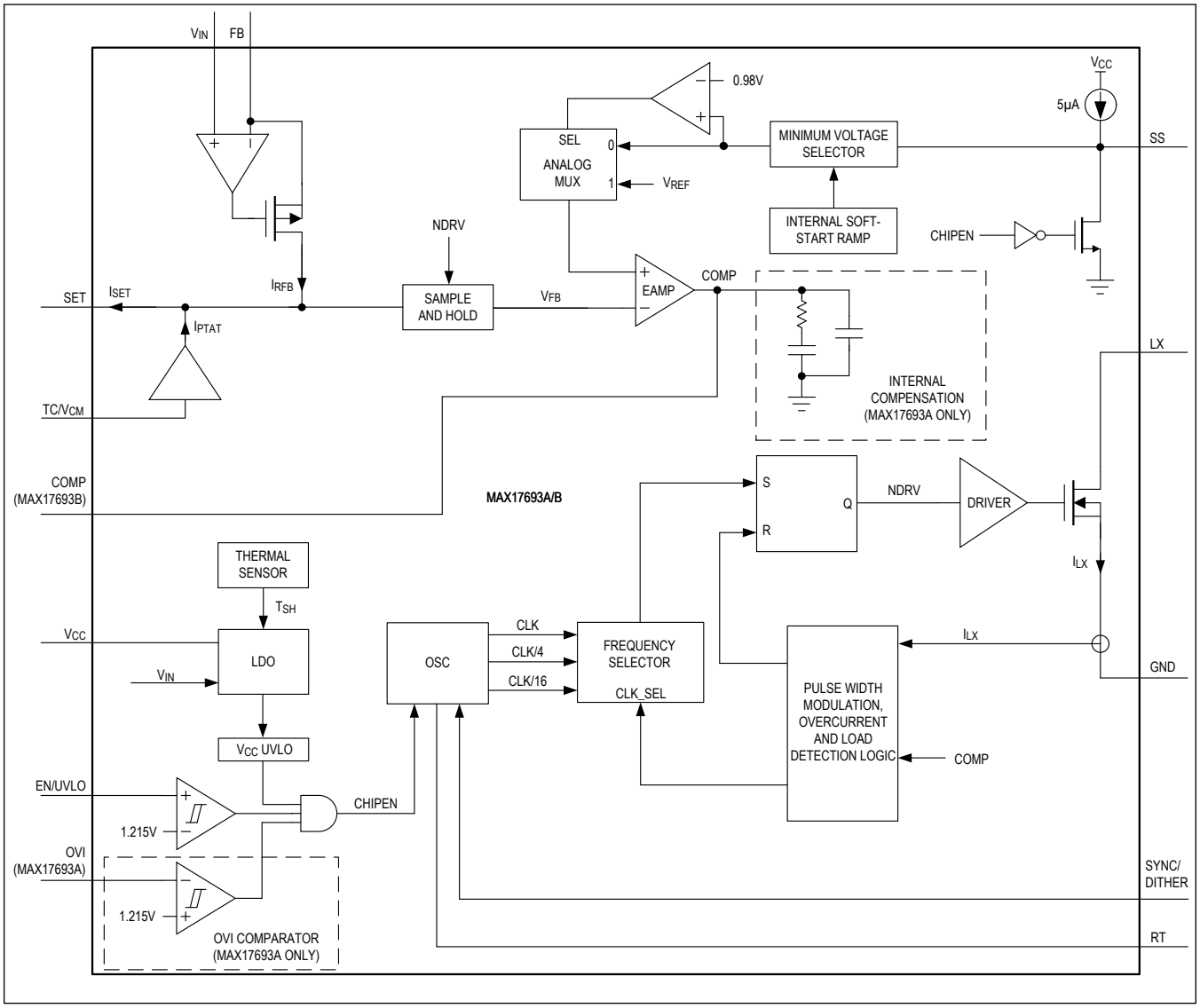
PIN	NAME	FUNCTION
1	V_{IN}	Input-Supply Voltage Pin. The input-supply voltage range is 4.2V to 60V. This pin acts as a reference pin for the feedback resistor connected to the FB pin. Connect a minimum of 1µF ceramic capacitor between the V_{IN} pin and GND.
2	GND	Ground Pin. Connect GND to the primary-side ground plane. See the MAX17693A/MAX17693B EV kit for a sample PCB layout.
3	V_{CC}	Linear Regulator Output Pin. Connect a 2.2µF (min) bypass capacitor from the V_{CC} pin to GND and place as close as possible to the MAX17693A/MAX17693B.
4	SYNC/ DITHER	Frequency Dithering or External Clock Synchronization Pin. For spread-spectrum frequency dithering from this pin, connect a capacitor to GND and a resistor to RT. Connect SYNC/DITHER to an external clock source for synchronization. When the SYNC/DITHER function is not used, this pin should be connected to ground for proper operation. See the *External Clock Synchronization and Switching Frequency Dithering(SYNC/DITHER)* section for more details.
5	RT	Switching Frequency Programming Pin. Connect a resistor (R_{RT}) from the RT pin to GND to set the converter switching frequency. Leave this pin open to select 200kHz as a default switching frequency. See the *Switching Frequency* section for appropriate R_{RT} resistor selection.

Pin Description (continued)

PIN	NAME	FUNCTION
6	TC/V_{CM}	Dual Function Pin. The TC/V_{CM} pin is used for programming the output-diode forward-voltage temperature compensation and selecting an appropriate common-mode voltage setting. See the *Selection of Temperature Compensation Resistor ($R_{TC/VCM}$)* section to select an appropriate resistor for this pin.
7	SS	Soft-Start Pin. Connect a capacitor C_{SS} from the SS pin to GND to program the soft-start time above 5ms. Leave the SS pin open for a 5ms default soft-start time.
8	SET	SET Pin. Connect a 10kΩ resistor with 1% or better tolerance from this pin to GND and place as close as possible to MAX17693A/B.
9	OVI MAX17693A	Input Overvoltage Protection Pin. Connect a resistor-divider between the input supply, OVI, and GND to set the input overvoltage threshold. The MAX17693A stops switching when the voltage at the OVI pin exceeds 1.215V and resumes switching when the voltage at the OVI pin falls below 1.1V.
9	COMP MAX17693B	Error Amplifier Output Pin. Connect a frequency compensation network between the COMP pin and GND. See the *Loop Compensation (MAX17693B only)* section for more details.
10	EN/UVLO	Enable/Undervoltage Lockout Pin. Connect a resistor-divider between the input supply, EN/UVLO, and GND to set the input turn-on threshold. The MAX17693A/B start switching when the voltage at the EN/UVLO pin exceeds 1.215V and stop switching when the voltage at the EN/UVLO pin falls below 1.1V
11	FB	Feedback Input Pin. The FB pin is used for sensing the reflected output voltage during a flyback period. A resistor connected between this pin and the LX node is used to program the output voltage. See the *Selection of SET and FB Resistors* section for more details.
12	LX	Switching Node. This node is connected to the drain of the integrated nMOSFET. Connect LX to the primary-side switching node of the flyback transformer.
—	EP	Exposed Pad. Connect EP to the primary side GND plane with thermal vias. Refer to the MAX17693A and MAX17693B EV kits for an example layout.

Functional Diagrams

MAX17693A/MAX17693B



Detailed Description

For low- and medium-power applications, the flyback converter is the preferred choice due to its simplicity and low cost. However, in isolated applications, the use of an optocoupler with secondary-side error amplifiers or auxiliary winding for voltage feedback across the isolation boundary increases the number of components and design complexity. The MAX17693A/MAX17693B eliminate these components and implement an innovative algorithm to sample and regulate the output voltage by primary-side sensing. During the flyback period, the reflected voltage across the primary winding is proportional to the sum of the output voltage, diode forward voltage, and the drop across transformer parasitic elements. By sampling and regulating this reflected voltage when the secondary current is close to zero, the algorithm minimizes the effect of transformer parasitic elements and the diode forward voltage on the output voltage regulation. The MAX17693A/MAX17693B also integrate the nMOSFET, further simplifying the converter design and layout.

Supply Voltage

The MAX17693A/MAX17693B support a wide operating input-voltage range from 4.2V to 60V. Using an internal amplifier, the MAX17693A/B maintain the FB pin voltage close to the V_{IN} pin voltage of the IC such that the current through R_{FB} is proportional to the reflected secondary winding voltage during the flyback period. Therefore, the V_{IN} pin should be directly connected to the power-supply connection of the primary winding.

LDO Output (V_{CC})

The regulated output of the internal LDO is available at the V_{CC} pin. The LDO output voltage is 5.77V (typ). Connect a 2.2µF (min) ceramic capacitor between the V_{CC} and GND pins for stable operation over the full temperature range. Ceramic capacitors have a DC-bias derating effect that should be considered. The derated capacitance should be higher than 1µF over temperature. Place this capacitor as close as possible to the IC.

In case of high input voltage applications, overall system efficiency can be improved by overdriving V_{CC} using an additional auxiliary winding on the power transformer. While the converter is enabled, the winding output voltage on C_{VCC} should be higher than maximum V_{CC} regulation voltage (5.9V) to disable the internal LDO. Also, to avoid the conduction of the internal LDO body diode between V_{IN} and V_{CC}, the overdrive voltage on C_{VCC} should be less than the input-supply voltage. Typically, the auxiliary winding should be designed to output a voltage between 6.5V and 14V to ensure that the internal LDO turns off and the IC is supplied from the auxiliary winding output. The typical circuit for overdriving the V_{CC} is shown in Figure 1.

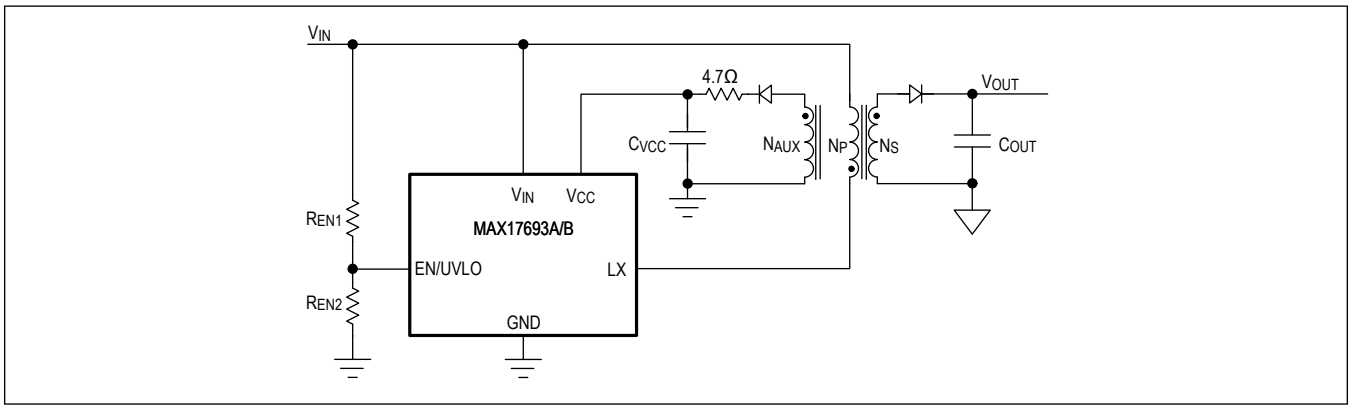


Figure 1. V_{CC} Pin Overdrive Configuration

Enable/Undervoltage Lockout (EN/UVLO) and Overvoltage Protection (OVI)

The EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input under-voltage lockout threshold (UVLO) pin. The MAX17693A/B do not commence switching operation until the EN/UVLO pin voltage exceeds

1.215V (typ). The MAX17693A/B turn off if the EN/UVLO pin voltage falls below 1.1V (typ). A resistor-divider from V_{IN} to GND can be used to divide and apply a fraction of the input voltage (V_{IN}) to the EN/UVLO pin as shown in Figure 2. The values of the resistor-divider can be selected such that the EN/UVLO pin voltage exceeds the EN/UVLO turn-on threshold at the desired input-supply voltage.

For the MAX17693B, choose R_{EN1} to be 3.3MΩ (max) and then calculate R_{EN2} as follows:

$$R_{EN2} = \frac{1.215 \times R_{EN1}}{V_{START} - 1.215}$$

where,

V_{START} = Minimum input voltage at which the device is required to turn on.

R_{EN1} = Top resistor of EV/UVLO voltage divider.

R_{EN2} = Bottom resistor of EV/UVLO voltage divider.

For the MAX17693A, the resistor-divider is modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to EN/UVLO function as shown in Figure 3. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching only if the voltage at the OVI pin falls below 1.1V (typ). For given values of minimum input voltage for startup (V_{START}) and input overvoltage protection voltage (V_{OVI}) in MAX17693A, choose R_{OVI} to be 10kΩ and then calculate R_{ENB} and R_{ENU} using these equations:

$$R_{ENB} = R_{OVI} \times \left[\frac{V_{OVI}}{V_{START}} - 1\right]$$

$$R_{ENU} = \left[R_{OVI} + R_{ENB}\right] \times \left[\frac{V_{START}}{1.215} - 1\right]$$

where, V_{OVI} is the maximum input voltage at which the device is required to turn-off.

If the OVI feature is not used, R_{ENB} and R_{ENU} should be calculated using a procedure similar to that outlined in the MAX17693B equation above, and OVI should be connected to GND.

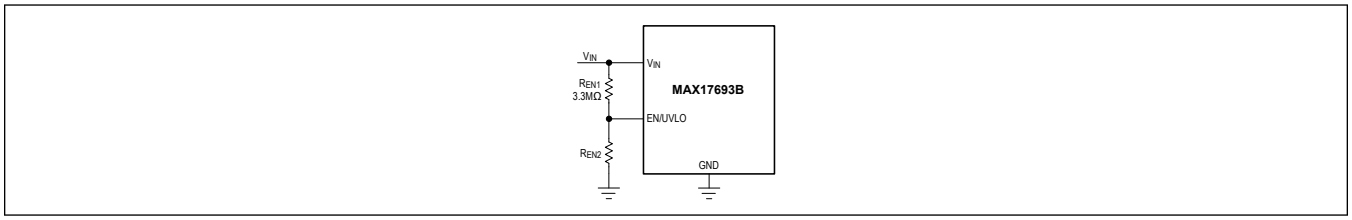


Figure 2. Programming EN/UVLO in MAX17693B

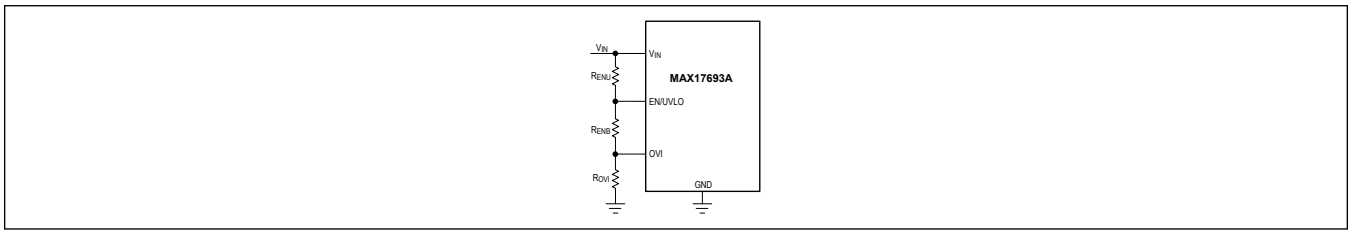


Figure 3. Programming EN/UVLO and OVI in MAX17693A

Soft-Start Time

The soft-start feature reduces input inrush current during startup. During the soft-start time, the soft-start ramp on the reference input of the error amplifier increases the output voltage at the desired rate and limits current into the output

capacitor. With SS open, the MAX17693A/B offer a default 5ms (typ) soft-start time. The soft-start time can also be programmed to more than 5ms by placing a capacitor C_{SS} from SS to GND.

C_{SS} can be calculated using following equation.

$$C_{SS} = 5 \times t_{SS}$$

where,

C_{SS} = Soft-start capacitor in nF.

t_{SS} = Soft-start time in ms.

Switching Frequency

The switching frequency of the MAX17693A/B is programmable between 100kHz to 350kHz using a resistor R_{RT} connected between RT and GND. Also, the MAX17693A/B offer a default 200kHz switching frequency when the RT pin is left open.

Use the following equation to determine the appropriate value of R_{RT} needed to generate the desired switching frequency (f_{SWRT}):

$$R_{RT} = \frac{10^7}{f_{SWRT}}$$

where, R_{RT} is the RT pin resistor in kΩ.

External Clock Synchronization and Switching Frequency Dithering (SYNC/DITHER)

The SYNC/DITHER pin of the MAX17693A/B can be used for either external clock synchronization or switching frequency dithering. Connect a resistor, R_{DITHER} from the RT pin to SYNC/DITHER, and a capacitor C_{DITHER} from SYNC/DITHER to GND as shown in Figure 4 for switching frequency dithering.

When the dithering function is not used, an external clock can be directly connected to the SYNC/DITHER pin as shown in Figure 5 to synchronize the internal oscillator frequency to an external clock frequency. When both external clock synchronization and switching frequency dithering is not used, SYNC/DITHER should be connected to GND for proper converter operation.

Frequency dithering spreads the energy at the switching frequency and its harmonics over a wider frequency band; thus, reducing their peaks and helping to meet stringent EMI goals. The MAX17693A/B offer spread-spectrum frequency dithering in the range of ±4% to ±12% of the switching frequency. A 21µA current source from V_{CC} charges the C_{DITHER} capacitor to 2V (typ). Upon reaching 2V, a sink current of 21µA to GND discharges C_{DITHER} to 0.4V (typ). The charging and discharging of the C_{DITHER} capacitor generates a triangular waveform of frequency (f_{TRI}) on the SYNC/DITHER pin with magnitude levels at 2V and 0.4V, respectively. Since the RT pin is regulated to 1.215V (typ) internally, a resistor R_{DITHER} connected from SYNC/DITHER to RT linearly modulates the nominal switching frequency due to the triangular waveform generated on the SYNC/DITHER pin.

For the desired dithering, calculate the appropriate values for C_{DITHER} and R_{DITHER} using this procedure.

$$C_{DITHER} = \frac{21 \times 10^{-6}}{3.2 \times f_{TRI}}$$

where, f_{TRI} is the frequency of the triangular waveform on the SYNC/DITHER pin. The programmable range for f_{TRI} is 100Hz to 1kHz.

$$R_{DITHER} = \frac{66 \times R_{RT}}{\%\,DITHER}$$

where,

R_{RT} = Switching frequency programmable resistor.

%DITHER = Amount of dither expressed as a percentage of nominal switching frequency.

For example, setting R_{DITHER} to 10 times of R_{RT} generates ±6.6% dithering.

The internal oscillator can be synchronized to an external clock(f_{SYNC}) by applying the external clock to the SYNC/

DITHER pin directly. The external clock is detected at the rising edge of the 9th consecutive clock cycle. Depending on the timing of 9th pulse rising edge during one time period of the internal oscillator, the switching is synchronized to the external clock frequency either on the 10th or 11th pulse of the external clock. Refer to the *Electrical Characteristics* table for recommended magnitude and pulse-width of the external clock.

The allowable external clock frequency range is from 1.10 x f_{SWRT} to 1.32 x f_{SWRT}. Note that any tolerance on the external clock should be included while complying with the given SYNC frequency range.

With external clock synchronization, the minimum off-time on LX is decided by the internal oscillator frequency, set by R_{RT}. Hence, during synchronization, the allowable maximum duty cycle ($D_{MAXSYNC}$) that can be used in an application is reduced and is given by:

$$D_{MAXSYNC} = 1 - \frac{f_{SYNC}(max)}{f_{SWRT}} \times (1 - D_{MAXOSC})$$

where,

D_{MAXOSC} = Oscillator maximum duty cycle.

$f_{SYNC}(max)$ = Maximum external clock frequency.

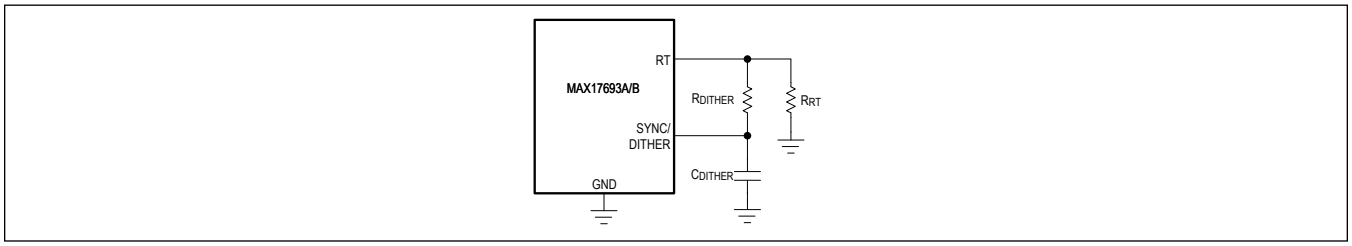


Figure 4. Switching Frequency Dithering Configuration

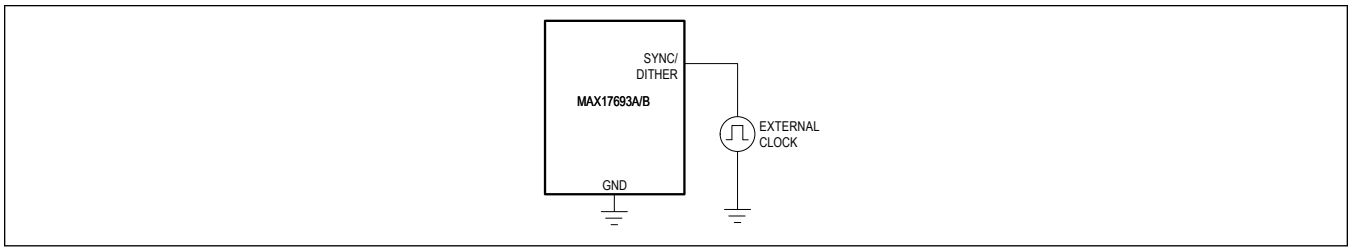


Figure 5. External Clock Synchronization Configuration

Theory of No-Opto Flyback Operation (SET and FB)

The MAX17693A/B sense the LX pin voltage while the secondary diode (D_{OUT}) is conducting. During this sensing period, the LX voltage is the sum of input voltage and reflected secondary winding voltage. Using an internal differential amplifier, the MAX17693A/B generate a current (I_{RFB}) in the feedback resistor (R_{FB}), which is proportional to secondary winding voltage. This current through the R_{FB} resistor also flows through the R_{SET} resistor placed between SET and GND, and produces a ground referenced feedback voltage on the SET pin as shown in Figure 6.

The MAX17693A/B use a built-in algorithm to sample the SET pin voltage when the secondary winding current is close to zero; hence, the resistive drops in the voltage across the secondary winding can be neglected. The sampled voltage on the SET pin is proportional to the sum of output voltage and secondary diode forward voltage drop. This sampled voltage feeds the inverting input of the internal error amplifier, whereas the internal reference voltage feeds the non-inverting input of the error amplifier. The control loop regulates the sampled SET pin voltage to the internal reference voltage. The above description applies to a case where the TC/V_{CM} pin is programmed for no temperature compensation. This

operation can be expressed mathematically:

$$\frac{V_{OUT} + V_D}{K} \times \frac{R_{SET}}{R_{FB}} = V_{SET}$$

where,

V_{OUT} = Output voltage.

V_D = Output diode forward voltage drop.

K = Transformer secondary-to-primary turns-ratio (N_S/N_P).

V_{SET} = SET regulation voltage.

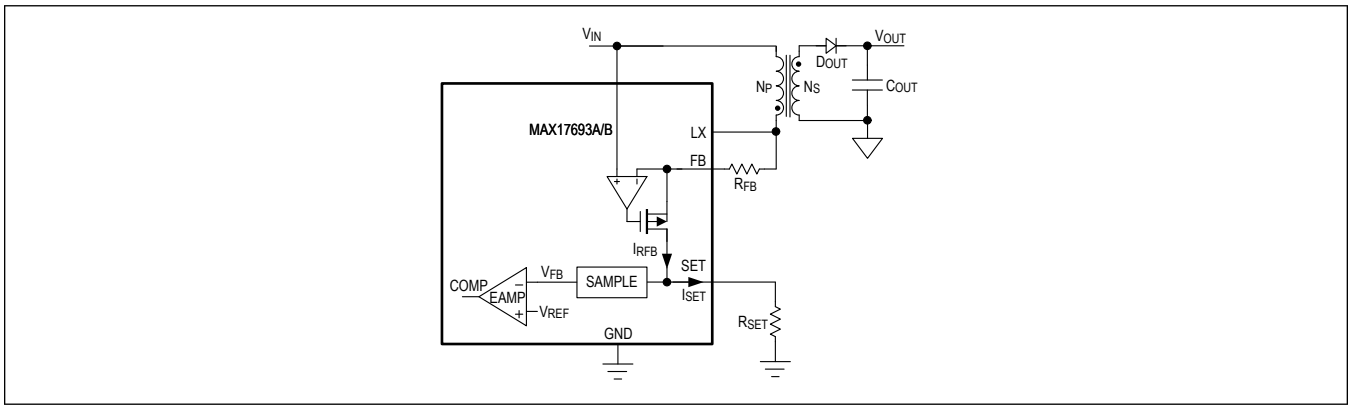


Figure 6. Simplified diagram of No-Opto Flyback Operation

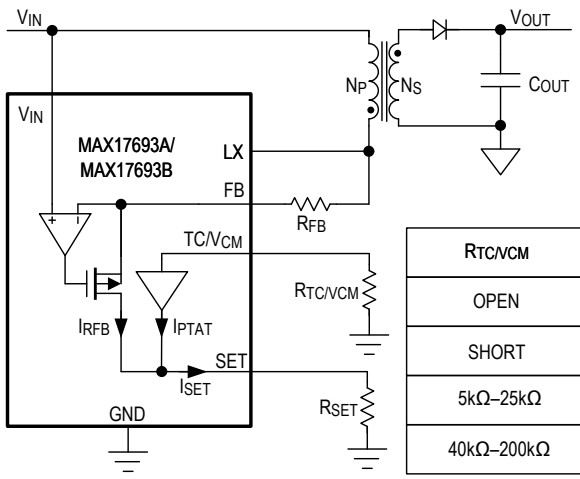
Temperature Compensation and Common-Mode Voltage Setting (TC/V_{CM})

TC/V_{CM} is a dual function pin. This pin is used to select an appropriate common-mode voltage range for proper operation of internal blocks based on the operating conditions of the converter as well as to implement temperature compensation for the output diode. The setting on the TC/V_{CM} pin is detected during power-up and latched. The TC/V_{CM} pin can be used to implement any one of two common-mode voltage settings (K_{VCM}), with or without temperature compensation (Figure 7). The temperature compensation for the output diode can be programmed in the range of -1mV/°C to -2mV/°C. The TC/V_{CM} pin voltage ($V_{TC/VCM}$) is regulated at 0.55V at room temperature and has a +1.85mV/°C positive temperature coefficient. A current (I_{PTAT}) that depends on the resistor ($R_{TC/VCM}$) connected to the TC/V_{CM} pin is applied at the SET pin to provide temperature compensation for changes in the MAX17693A/B junction temperature. This scheme assumes that the output diode temperature change tracks the MAX17693A/B junction temperature. Resistor values outside of those indicated in Figure 7 are not allowed on the TC/V_{CM} Pin.

The above operation can be expressed mathematically as:

$$\left[\frac{(V_{OUT} + V_D)}{K} \times \frac{1}{R_{FB}} + I_{PTAT}\right] \times R_{SET} = V_{SET}$$

Based on required temperature compensation, the I_{PTAT} current can be programmed by selecting an appropriate $R_{TC/VCM}$ resistor. The *Selection of Temperature Compensation Resistor ($R_{TC/VCM}$)* section details the design procedure for the K_{VCM} and $R_{TC/VCM}$ resistor selection.



RTC/VCM	VCM SETTING	IPTAT	TEMPERATURE COMPENSATION
OPEN	$K_{VCM} \geq 2.5$	0	NO
SHORT	$K_{VCM} < 2.5$	0	NO
5kΩ–25kΩ	$K_{VCM} < 2.5$	$0.15 \times \frac{V_{TC/VCM}}{R_{TC/VCM}}$	YES
40kΩ–200kΩ	$K_{VCM} \geq 2.5$	$1.2 \times \frac{V_{TC/VCM}}{R_{TC/VCM}}$	YES

Figure 7. TC/V_{CM} Pin Configuration

Overcurrent Protection/Hiccup Mode

The MAX17693A/B provide a robust overcurrent protection scheme that protects the device in overload and output short-circuit conditions. A cycle-by-cycle current limit turns the power nMOSFET off whenever the LX current exceeds an internal peak current limit. Either one occurrence of the runaway current limit event or 16 consecutive peak current limit events triggers a hiccup mode that protects the converter by immediately suspending switching for a period of 16,384 clock cycles. Once the hiccup time-out expires, soft-start is attempted again. Refer to the *Electrical Characteristics* table for peak current and runaway current-limit values of MAX17693A/B.

Applications Information

Transformer Design Considerations

The MAX17693A/B are optimized for implementing discontinuous mode (DCM) flyback converters. The transformer design involves selecting a proper magnetizing inductance and transformer turns ratio along with the target switching frequency to meet the internal sampling algorithm requirements of the MAX17693A/B. Consider a design specification of minimum input voltage (V_{INMIN}), typical input voltage (V_{INTYP}), maximum input voltage (V_{INMAX}), output voltage (V_{OUT}), and output current (I_{OUT}). The transformer design procedure described in this section ensures the DCM operation for an input voltage of V_{INMIN} and above while delivering the full-load output power (V_{OUT} x I_{OUT}). Based on design requirements, either the minimum operating input voltage or part start-up voltage (V_{START}) set by the EN/UVLO divider can be selected as V_{INMIN}.

The first step in the transformer design is to arrive at the secondary to primary turns ratio K (N_S/N_P). The minimum turns ratio K_{MIN} is constrained by the maximum operating voltage rating of the integrated nMOSFET (76V). The maximum voltage stress is experienced at the LX node (drain of integrated nMOSFET) when the integrated nMOSFET turns-off and energy is transferred to the output. The voltage stress at LX is the sum of the maximum operating input voltage (V_{INMAX}), the reflected output voltage and the voltage spike due to energy stored in the leakage inductance (V_{LKG}) of the transformer, given by the following equation:

$$V_{LX} = V_{INMAX} + \frac{(V_{OUT} + V_D)}{K} + V_{LKG}$$

where, V_D is the output diode forward voltage at full load.

The leakage inductance voltage spike is limited using an external clamp circuit. Choosing a small value of clamp voltage for the V_{LKG} spike results in a higher power loss in the clamp circuit. Typically, V_{LKG} is clamped to a factor (K_S), 1x to 1.5x of the reflected output voltage to limit the clamp circuit loss. Refer to the *Voltage Clamp Design* section for an appropriate clamp design.

$$V_{LXMAX} = V_{INMAX} + \frac{\left(V_{OUT} + V_D\right)}{K_{MIN}} + \frac{K_S \times \left(V_{OUT} + V_D\right)}{K_{MIN}} \le 76V$$

$$K_{MIN} = \frac{\left(1 + K_S\right) \times \left(V_{OUT} + V_D\right)}{76 - V_{INMAX}}$$

The maximum duty cycle of a flyback converter to maintain DCM operation at minimum input voltage is given by,

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + (K_{MIN} \times V_{INMIN})}$$

For the MAX17693A/B, the maximum duty cycle should be limited to D_{MAXOSC} = 0.65. If the calculated D_{MAX} for K_{MIN} in the above equation is less than the maximum duty-cycle limit (D_{MAXOSC}), then $K = K_{MIN}$.

If the calculated D_{MAX} for K_{MIN} in the above equation exceeds the maximum duty-cycle limit (D_{MAXOSC}), then the turns ratio should be recalculated using D_{MAXOSC} = 0.65 in the following equation:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{MAXOSC})}{D_{MAXOSC} \times V_{INMIN}} = \frac{(V_{OUT} + V_D) \times 0.538}{V_{INMIN}}$$

Note that when an external clock synchronization is used, D_{MAXOSC} should be replaced with $D_{MAXSYNC}$ while calculating the turns ratio K.

Once the turns ratio K is determined, the maximum operating duty cycle of the converter D_{VINMIN} is given by:

$$D_{VINMIN} = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + (K \times V_{INMIN})}$$

The next step is to calculate the required primary magnetizing inductance (L_{MAG}) of the transformer. The MAX17693A/B obtain output voltage information from the reflected output voltage on the LX node during the secondary rectifier

conduction period. To ensure proper sampling, the secondary winding needs to conduct current for the minimum off-time (t_{OFF_MIN}, 380ns) specified in the *Electrical Characteristics* table. The following equation gives the minimum required magnetizing inductance that satisfies the minimum off-time with additional 100ns of design margin.

$$L_{MAG\_TOFF} = 480 \times 10^{-9} \times \frac{\left(V_{OUT} + V_D\right)}{0.07 \times K}$$

where, L_{MAG_TOFF} is the minimum magnetizing inductance that satisfies the minimum off-time requirements of sampling.

The MAX17693A/B implement a minimum on time (t_{ON_MIN}) of 210ns (max) to blank the leading-edge current spike that occurs when the integrated nMOSFET turns on. The following equation gives the minimum required magnetizing inductance that satisfies the minimum on-time.

$$L_{MAG\_TON} = \frac{210 \times 10^{-9}}{0.117} \times V_{INMAX}$$

where, L_{MAG_TON} is the minimum magnetizing inductance that satisfies the minimum on-time requirements.

The selected magnetizing inductance (L_{MAGSEL}) should be higher than both L_{MAG_TOFF} and L_{MAG_TON}. The manufacturer tolerance for the magnetizing inductance can be in the range of ±10% to ±20%. This variation should be considered in the following equation to specify the proper nominal magnetizing inductance to ensure correct output-voltage sampling.

$$L_{MAG} = \frac{L_{MAGSEL}}{(1 - TOL)}$$

where, TOL is 0.1 for 10% tolerance and 0.2 for 20% tolerance in the magnetizing inductance.

Leakage inductance should be specified and minimized to within 1% to 2% of the primary magnetizing inductance of the transformer and the transformer turns-ratio (N_S/N_P) tolerance should be specified as ±1%.

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is delivered entirely to the output. The maximum switching frequency for which the converter remains in DCM (f_{SWDCM}) at all operating conditions can be calculated as:

$$f_{SWDCM} = \frac{\left(D_{VINMIN} \times V_{INMIN}\right)^2 \times \eta}{2 \times V_{OUT} \times (I_{OUT} + I_{COUT\_SS}) \times L_{MAG} \times (1 + TOL)}$$

where,

η = Converter target efficiency assumed to be in the range of 0.8 to 0.9.

$I_{COUT-SS}$ = Output capacitor charging current during soft-start and, is typically 5% to 10% of the I_{OUT}.

When SYNC/DITHER functions are not used, the nominal switching frequency (f_{SWRT}) programmed by R_{RT} should be $\frac{f_{SWDCM}}{1.06}$ or less to ensure DCM operation while delivering full load power.

When an external clock synchronization is used, the f_{SYNC}(max) should be less than f_{SWDCM} to ensure DCM operation. For selecting appropriate f_{SWRT} during SYNC operation, refer to the *External Clock Synchronization and Switching Frequency Dithering (SYNC/DITHER)* section.

When dither function is used, the programmed f_{SWRT} should be $\frac{f_{SWDCM}}{1.06 \times (1 + \%\,DITHER)}$ or less.

Note that the minimum programmable switching frequency is 100kHz (typ).

The above selection of K, L_{MAG}, and f_{SWRT} ensures the DCM operation at the full-load (V_{OUT} x I_{OUT}) of the converter down to minimum operating input voltage. With this L_{MAG}, the converter enters continuous conduction mode (CCM) when delivering an output power greater than the full-load power (V_{OUT} x I_{OUT}). As the load power is further increased, the converter continues to regulate the average output voltage before hitting the primary peak current limit. When the part hits either 16 consecutive peak current limits or one runaway current limit, the MAX17693A/B enter hiccup mode operation.

When the part is operating in CCM, the output regulation degrades marginally due to errors caused by the secondary diode forward drop and transformer secondary DC-resistance drop in the primary-side sensing algorithm.

The primary winding peak current during full-load soft-start ($I_{PEAKDCM-SS}$) can be calculated using this equation:

$$I_{PEAKDCM-SS} = \sqrt{\frac{2 \times V_{OUT} \times (I_{OUT} + I_{COUT-SS})}{0.94 \times f_{SWRT} \times L_{MAG} \times (1 - TOL) \times \eta}}$$

To deliver the required full-load power, the $I_{PEAKDCM-SS}$ should be lower than the minimum value of the peak current limit ($I_{LX-PEAK-MAX}$) set in the part, which is 0.495A.

When delivering full-load power, worst-case steady-state currents in the transformer windings can be calculated using these equations:

The primary winding peak current ($I_{PEAKDCM}$) is given by:

$$I_{PEAKDCM} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{0.94 \times f_{SWRT} \times L_{MAG} \times (1 - TOL) \times \eta}}$$

The primary RMS current (I_{PRIRMS}) is given by:

$$I_{PRIRMS} = I_{PEAKDCM} \times \sqrt{\frac{0.94 \times f_{SWRT} \times I_{PEAKDCM} \times L_{MAG} \times (1 - TOL)}{3 \times V_{INMIN}}}$$

The secondary RMS current (I_{SECRMS}) is given by:

$$I_{SECRMS} = \frac{I_{PEAKDCM}}{K} \times \sqrt{\frac{0.94 \times f_{SWRT} \times K \times I_{PEAKDCM} \times L_{MAG} \times (1 - TOL)}{3 \times (V_{OUT} + V_D)}}$$

The transformer primary saturation current should be greater than or equal to $I_{PEAKDCM-SS}$. This recommendation ensures that the transformer can reliably deliver full-load power across all operating conditions. Although the worst-case peak current limit ($I_{LX-PEAK-MAX}$) of MAX17693A/B is 0.6A, it is not necessary to design the transformer to be compatible with this worst-case peak current-limit specification since the runaway current limit feature of the MAX17693A/B protect the design if the transformer should saturate above $I_{PEAKDCM-SS}$. This allows the transformer size to be optimized to match the required full-load power.

Selecting a Secondary Rectifier

In a flyback converter, since the secondary rectifier is reverse-biased when the integrated nMOSFET is conducting, the voltage stress on the rectifier is the sum of the output voltage and the reflected input voltage. Choose the rectifier with enough margin for reverse blocking voltage as indicated in the below equation.

$$V_{SEC\_RECT} = K_{RSF} \times (K \times V_{INMAX} + V_{OUT})$$

where, K_{RSF} is the safety factor to account for additional voltage stress on the diode due to leakage inductance. It is recommended to choose K_{RSF} in the range of 1.5-2. Select a schottky diode with low forward-voltage drop and low junction capacitance to minimize power loss.

Selection of Temperature Compensation Resistor ($R_{TC/VCM}$)

The output diode forward voltage (V_D) in the V_{OUT} equation has a significant negative temperature coefficient (–1mV/°C to –2mV/°C), which produces approximately 2% to 5% variation on the output voltage across temperatures in low output-voltage applications, such as 3.3V and 5V. To compensate for this variation, a positive temperature coefficient current is internally added to the SET pin by programming the TC/V_{CM} pin with a resistor $R_{TC/VCM}$. Follow the steps below to select the appropriate $R_{TC/VCM}$:

1) From Table 1, select the factor (m_f) for the selected switching frequency (f_{SWRT}).

Table 1. Factor m_f Selection

SWITCHING FREQUENCY (kHz)	m_f
$100 \le f_{SWRT} < 108$	39000
$108 \le f_{SWRT} < 162$	58600

Table 1. Factor m_f Selection (continued)

$162 \le f_{SWRT} < 240$	91100
$240 \le f_{SWRT} \le 350$	136700

2) Calculate the common mode voltage setting (K_{VCM}) with the following equation:

$$K_{VCM} = m_f \times L_{MAG} \times I_{PEAKDCM-SS}$$

3) Calculate the TC/V_{CM} resistor ($R_{TC/VCM}$) based on following equations.

Using the equation given in the *Temperature Compensation and Common-Mode Voltage Setting (TC/V_{CM})* section, and substituting the I_{PTAT} for $K_{VCM} \ge 2.5$:

$$\left[\frac{(V_{OUT}+V_D)}{K} \times \frac{1}{R_{FB}} + 1.2 \times \frac{V_{TC/VCM}}{R_{TC/VCM}}\right] \times R_{SET} = V_{SET}$$

By differentiating the above equation for temperature change:

$$\frac{\frac{\delta V_D}{\delta T}}{K} \times \frac{1}{R_{FB}} = -\frac{\delta V_{TC/VCM}}{\delta T} \times \frac{1.2}{R_{TC/VCM}}$$

By combining above two equations and eliminating R_{FB}:

$$R_{TC/VCM} = 1.2 \times \frac{R_{SET}}{V_{SET}} \times \left(0.55 - \frac{(V_{OUT}+V_D) \times \left(\frac{\delta V_{TC/VCM}}{\delta T}\right)}{\left(\frac{\delta V_D}{\delta T}\right)}\right)$$

For $K_{VCM} < 2.5$:

$$\left[\frac{(V_{OUT}+V_D)}{K} \times \frac{1}{R_{FB}} + 0.15 \times \frac{V_{TC/VCM}}{R_{TC/VCM}}\right] \times R_{SET} = V_{SET}$$

By differentiating the above equation for temperature change:

$$\frac{\frac{\delta V_D}{\delta T}}{K} \times \frac{1}{R_{FB}} = -\frac{\delta V_{TC/VCM}}{\delta T} \times \frac{0.15}{R_{TC/VCM}}$$

By combining above two equations and eliminating R_{FB}:

$$R_{TC/VCM} = 0.15 \times \frac{R_{SET}}{V_{SET}} \times \left(0.55 - \frac{(V_{OUT}+V_D) \times \left(\frac{\delta V_{TC/VCM}}{\delta T}\right)}{\left(\frac{\delta V_D}{\delta T}\right)}\right)$$

where,

$R_{TC/VCM}$ = Temperature compensation resistor in Ω. Resistor values outside of those indicated in Figure 7 are not allowed.

V_D = Forward voltage drop of the secondary rectifier diode in Volts.

$\delta V_D/\delta T$ = Temperature coefficient of the secondary rectifier diode in mV/ºC, which can be obtained from the data sheet of a secondary rectifier diode.

$\delta V_{TC/VCM}/\delta T$ = Internal temperature compensation coefficient (equals +1.85mV/ºC).

For applications that do not require temperature compensation,

For $K_{VCM} \ge 2.5$, leave TC/V_{CM} open.

For K_{VCM} < 2.5, short TC/V_{CM} to GND.

Selection of SET and FB Resistors

The MAX17693A/B use the current in the feedback resistor (R_{FB}) placed between the FB pin and the LX node of the integrated nMOSFET to sense the reflected output voltage during the primary turn-off time. R_{SET} should be set to 10kΩ for a 100µA nominal current in R_{FB}.

When temperature compensation is not needed, the equation for the feedback resistor (R_{FB}) is:

$$R_{FB} = \frac{R_{SET}}{V_{SET}} \times \frac{V_{OUT} + V_D}{K}$$

When temperature compensation is needed, using the equation given in the *Temperature Compensation and Common-Mode Voltage Setting (TC/V_{CM})* section and substituting corresponding I_{PTAT} :

$$R_{FB} = \frac{V_{OUT} + V_D}{K} \times \frac{1}{\left(\frac{V_{SET}}{R_{SET}} - \frac{0.66}{R_{TC/VCM}}\right)} \text{For} K_{VCM} \geq 2.5$$

$$R_{FB} = \frac{V_{OUT} + V_D}{K} \times \frac{1}{\left(\frac{V_{SET}}{R_{SET}} - \frac{0.0825}{R_{TC/VCM}}\right)} \text{For} K_{VCM} < 2.5$$

In practice, the regulated output voltage can differ slightly from the desired output voltage due to secondary leakage-inductance voltage drop and differences in output-diode voltage drop, and can require an R_{FB} adjustment.

Minimum Load Considerations

The MAX17693A/B sample the reflected output voltage information on the primary winding during the time when the integrated nMOSFET is turned-off, and energy stored during the on-time is being delivered to the output. It is therefore mandatory for the MAX17693A/B to switch the integrated nMOSFET to sample the reflected output voltage. Hence, a minimum packet of energy needs to be delivered to the output even during light-load conditions. This minimum deliverable energy creates a minimum load requirement on the output that depends on the minimum primary peak current. For a discontinuous-mode flyback converter, the minimum deliverable load power (P_{OUT_FSWRT}) at f_{SWRT} is given by:

$$P_{OUT\_FSWRT} = \frac{1}{2} \times L_{MAG} \times I^2_{LX-PEAK-MIN} \times f_{SWRT}$$

At lower power levels less than P_{OUT_FSWRT}, the MAX17693A/B modulate the switching frequency between f_{SWRT} / 4 and f_{SWRT} to regulate the output voltage. As the load decreases further, MAX17693A/B completely transition to operation at f_{SWRT} / 4 at a load ($P_{OUT\_FSWRT/4}$) given by:

$$P_{OUT\_FSWRT/4} = \frac{1}{8} \times L_{MAG} \times I^2_{LX-PEAK-MIN} \times f_{SWRT}$$

As the load is decreased further, MAX17693A/B modulate the switching frequency between f_{SWRT} / 4 and f_{SWRT} / 16, until the device completely settles down at f_{SWRT} / 16 at a load ($P_{OUTMIN\_FSWRT/16}$) given by:

$$P_{OUTMIN\_FSWRT/16} = \frac{1}{32} \times L_{MAG} \times I^2_{LX-PEAK-MIN} \times f_{SWRT}$$

At this point, the MAX17693A/B have reached its minimum load condition and cannot regulate the output voltage without this minimum load connected to the output. In the absence of a minimum load, or a load less than the “minimum load,” the output voltage rises to higher values. To protect for this condition, a Zener diode of an appropriate breakdown voltage rating can be installed on the output. Care should be taken to ensure that the Zener breakdown voltage is outside the output voltage envelope in both steady-state and transient conditions. For MAX17693A/B, the guaranteed maximum for $I_{LX-PEAK-MIN}$ is 0.117A.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the converter switching. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equations to limit the ripple voltage amplitude ΔV_{IN} to less than 5% of the input voltage when operating at nominal input voltage,

$$C_{IN} \geq \frac{I_{PEAKDCM} \times D_{VINMIN} \times \left(1 - \frac{D_{VINMIN}}{2}\right)^2}{2 \times 0.94 \times f_{SWRT} \times \Delta V_{IN}}$$

where,

C_{IN} = Derated input capacitance in Farads.

D_{VINMIN} = Maximum duty cycle.

ΔV_{IN} = Target value of input voltage ripple in Volts.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

The MAX17693A implements internal loop compensation for the converter stability. Based on the internal compensation, the minimum output capacitance required for stable converter operation is given by:

$$C_{OUTMIN} = \frac{1.75 \times V_{OUT} \times I_{OUT}}{\sqrt{\eta} \times f_C \times I_{PEAKDCM} \times V_{OUT}^2}$$

where,

η = Target efficiency of the converter.

C_{OUTMIN} = Minimum derated output capacitance in Farads.

f_C = Target closed-loop bandwidth in Hz to be selected as 1/15 of the f_{SWRT} and below 10kHz.

For the target output ripple, the output capacitance required is given by:

$$C_{OUTRIPP} \geq \frac{I_{OUT} \times \left(I_{PEAKDCM} - K \times I_{OUT}\right)^2}{0.94 \times f_{SWRT} \times I_{PEAKDCM}^2 \times V_{OUT\_RIPP}}$$

where,

$C_{OUTRIPP}$ = Derated output capacitance in F.

V_{OUT_RIPP} = Target value of output voltage ripple in V.

The output capacitance ($C_{OUTSTEP}$) for a given load step, required output voltage deviation (ΔV_{OUT}) can be estimated as:

$$C_{OUTSTEP} = \frac{t_{RESPONSE} \times (3 \times I_{OUTFINAL} - I_{OUTINIT} - 2 \times \sqrt{I_{OUTINIT} \times I_{OUTFINAL}})}{4 \times (\Delta V_{OUT})}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SWRT}}\right)$$

where,

$C_{OUTSTEP}$ = Derated output capacitance in F.

$I_{OUTINIT}$ = Load-step start current.

$I_{OUTFINAL}$ = Load-step end current.

$t_{RESPONSE}$ = Response time of the converter.

ΔV_{OUT} = Average output voltage deviation in Volts.

The output capacitance (C_{OUT}) for MAX17693A should be selected to be the larger of C_{OUTMIN}, $C_{OUTRIPP}$, or $C_{OUTSTEP}$. For stability reasons, the maximum allowed output capacitance for the MAX17693A is up to 3 x C_{OUTMIN}. If the required capacitance to meet the specifications exceeds 3 x C_{OUTMIN}, the MAX17693B with external loop compensation should be used. The output capacitance for MAX17693B should be selected to be the larger of $C_{OUTRIPP}$ and $C_{OUTSTEP}$.

Loop Compensation (MAX17693B only)

While the MAX17693A provides ease of design and a low component count, the MAX17693B provides the designer with the flexibility of tailoring the loop compensation according to system needs.

The MAX17693B is compensated using an external frequency compensation network on the COMP pin as shown in Figure 8. The loop compensation values are calculated as follows,

$$R_Z = 8180 \times \left(\frac{f_C}{f_P}\right) \times \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{MAG} \times f_{SWRT}}}$$

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SWRT}}$$

where,

$$f_P = \frac{1}{\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}}$$

where, C_{OUT} is the output capacitance in Farads selected in the *Output Capacitor Selection* section.

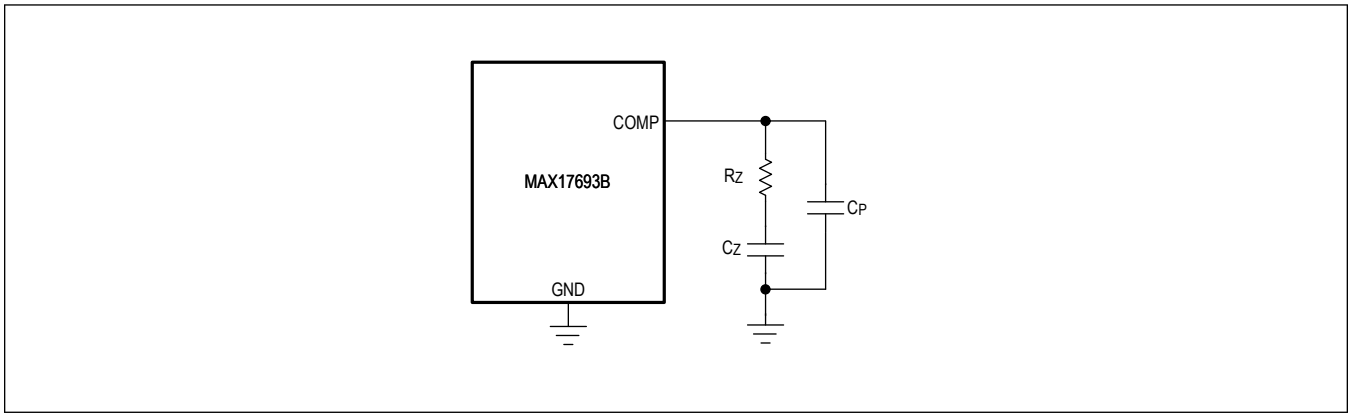


Figure 8. MAX17693B Loop Compensation Arrangement

Voltage Clamp Design

Ideally, the integrated nMOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected output voltage across the primary winding when it turns off. In practice, voltage stress at LX is the sum of the

maximum operating input voltage (V_{INMAX}), the reflected output voltage and the voltage spike due to energy stored in the leakage inductance (V_{LKG}) of the transformer.

$$V_{LX} = V_{INMAX} + \frac{V_{OUT} + V_D}{K} + V_{LKG}$$

An external clamp is used to limit the voltage across the primary winding (reflected output voltage plus leakage inductance voltage spike) such that the LX voltage does not exceed 76V. Therefore, the clamp voltage across the primary winding should be designed for:

$$V_{CLAMP} < 76 - V_{INMAX}$$

When the OVI trip point (V_{OVI}) is selected far away from the V_{INMAX}, V_{INMAX} should be replaced with V_{OVI} in the above equation for limiting LX voltage below 76V.

A simple Zener-diode (ZD) clamp can be used as a voltage-clamp circuit. Figure 9 shows the operating waveform of the ZD clamp. Ideally, the ZD breakdown voltage should be selected to be the same as the V_{CLAMP}. However, in practice, the ZD breakdown voltage should be 5V to 10V below the V_{CLAMP} to accommodate any additional voltage spike due to parasitic inductance in the clamp-circuit path, such that the LX voltage does not exceed 76V. A 0.25W power rating ZD satisfies most applications.

Select a schottky diode with a minimum reverse-voltage rating (V_{DSNUB}) as a clamp diode (D_S):

$$V_{DSNUB} = V_{INMAX}$$

The ZD clamp circuit only limits maximum voltage stress on the integrated nMOSFET. LX node oscillations are still present due to the interaction between leakage inductance (L_{LK}) and the LX node capacitance (C_{PAR}). The MAX17693A/B use the LX node voltage information to sample the output voltage and the earliest sampling instant is 300ns from the rising edge of the LX node. Therefore, it is important to damp the LX node ringing within 300ns.

For designs with ringing on the LX node after 300ns, an additional RC snubber across the transformer primary winding is required. Use the following steps for designing an effective RC snubber:

1) Measure the one-cycle ringing time period (t_1) for the oscillations on the LX node immediately after the clamp period.

$$t_1 = 2\pi\sqrt{L_{LK} \times C_{PAR}}$$

2) Add a test capacitance on the LX node until the time period of this ringing is increased to 1.5 to 2 times of t_1. Start with a 100pF capacitor. With the added capacitance (C_D) measure the new one-cycle ringing time period (t_2),

$$t_2 = 2\pi\sqrt{L_{LK} \times (C_{PAR} + C_D)}$$

3) Use the following formula to calculate the LX node capacitance (C_{PAR}),

$$C_{PAR} = \frac{C_D}{\left(\left(\frac{t_2}{t_1}\right)^2 - 1\right)}$$

4) Use the following formula to calculate the leakage inductance,

$$L_{LK} = \frac{{t_1}^2}{\left(4 \times \pi^2 \times C_{PAR}\right)}$$

5) Now, use the following equations to calculate the RC snubber values,

$$R_C = \sqrt{\frac{L_{LK}}{C_{PAR}}}$$

$$1.5 \times C_{PAR} \le C_C \le 2 \times C_{PAR}$$

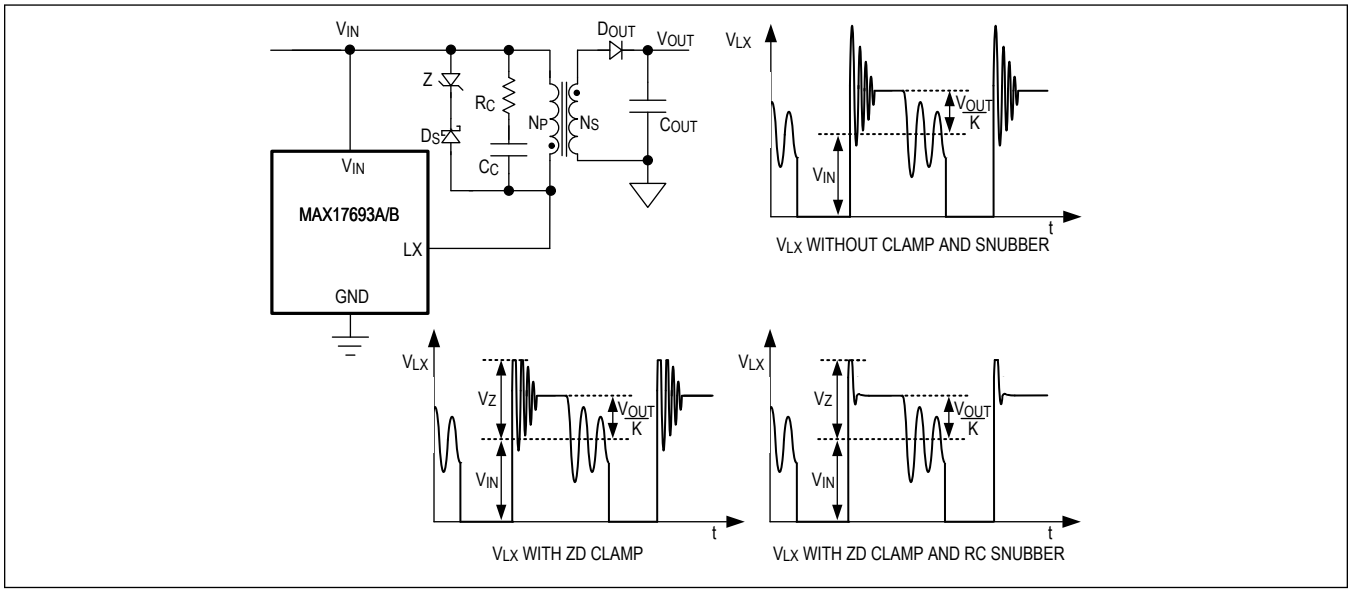


Figure 9. Voltage Clamp Circuit

Thermal Considerations

It should be ensured that the junction temperature of the devices does not exceed +125°C under all operating conditions specified for the power supply.

The total power loss in the MAX17693A/B can be calculated from the following equation:

$$P_{LOSS} = P_Q + P_{COND} + P_{GATE} + P_{SW}$$

where,

P_Q = Converter quiescent power loss.

P_{COND} = Integrated nMOSFET conduction loss.

P_{GATE} = Integrated nMOSFET gate capacitance loss.

P_{SW} = Switching loss in the nMOSFET due to LX node capacitance.

The converter quiescent power loss can be calculated using the following equation:

$$P_Q = V_Q \times I_Q$$

where,

V_Q = Bias voltage when V_{CC} is overdriven, or $V_Q = V_{IN}$, when V_{CC} is not overdriven.

I_Q = V_{IN} supply current at no load as specified in the *Electrical Characteristics* table.

The conduction loss in the integrated nMOSFET can be calculated as:

$$P_{COND} = I^2_{PRIRMS} \times R_{DSON}$$

The gate loss is given by:

$$P_{GATE} = 40 \times V_Q \times f_{SWRT} \times \left[10 \times V_{CC} + V_{INMAX} + \frac{V_{OUT} + V_D}{K}\right] \times 10^{-12}$$

When the integrated nMOSFET is turned-on there exists additional capacitive loss due to the LX node capacitance. The worst-case switching loss (P_{SW}) can be calculated using this equation:

$$P_{SW} = \frac{1}{2} \times C_{PAR} \times \left(V_{INMAX} + \frac{V_{OUT} + V_D}{K}\right)^2 \times f_{SWRT}$$

where, C_{PAR} is the LX node capacitance which is calculated in the *Voltage Clamp Design* section.

For multilayer boards, the junction-ambient thermal resistance (θ_{JA}) for the MAX17693A/B is given by:

$$\theta_{JA} = 41°C/W$$

The junction-temperature rise of the devices can be estimated at any given maximum ambient temperature (T_{AMAX}) from the following equation:

$$T_{JMAX} = T_{AMAX} + (\theta_{JA} \times P_{LOSS})$$

Design Example:

The following industrial specification is used to demonstrate the design calculations for the MAX17693A/B-based flyback converter,

Input voltage range: 18V to 36V

Output voltage: 5V

Load current: 0.25A

1. Selection of Turns-Ratio

Plug-in the V_{INMAX}, V_{OUT} from the above specification and use K_S = 1.2, V_D = 0.4V at the sample instant in the formula below to calculate the minimum require turns-ratio (K_{MIN}):

$$K_{MIN} = \frac{(1 + K_S) * (V_{OUT} + V_D)}{76 - V_{INMAX}} = 0.3$$

For the present application, the K is chosen as 0.45.

Use the following equation to calculate the maximum duty cycle of the converter for the selected turns-ratio:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + K \times V_{INMIN}} = 0.4$$

Since D_{MAX} < 0.65, for the present design, D_{VINMIN} = 0.4.

2. Magnetizing Inductance and Switching Frequency

Use the below formula established earlier in this data sheet to calculate the minimum magnetizing inductance (L_{MAG}):

$$L_{MAG\_TON} = \frac{210 \times 10^{-9}}{0.117} \times V_{INMAX} = 64.6\mu H$$

$$L_{MAG\_TOFF} = 480 \times 10^{-9} \times \frac{V_{OUT} + V_D}{0.07xK} = 82.3\mu H$$

For the present application, the magnetizing inductance (L_{MAG}) is selected as 100µH allowing ±10% tolerance.

The maximum switching frequency (f_{SWDCM}) can be calculated from the following equation with a target efficiency of η = 87%.

$$f_{SWDCM} = \frac{\left(D_{VINMIN} \times V_{INMIN}\right)^2 \times \eta}{2 \times V_{OUT} \times \left(I_{OUT} + I_{COUT-SS}\right) \times L_{MAG} \times (1 + TOL)}$$

$$f_{SWDCM} = \frac{(0.4 \times 18)^2 \times 0.87}{2 \times 5 \times (0.25 + 0.006) \times 100 \times 10^{-6} \times (1 + 0.1)} = 160kHz$$

Hence, the f_{SWRT} is selected to be 150kHz.

The R_{RT} is calculated for the selected f_{SWRT} is:

$$R_{RT} = \frac{10^7}{f_{SWRT}} = 66.6k\Omega$$

A standard resistor of 66.5kΩ is selected for R_{RT}.

The transformer primary peak current value depends on the output power, L_{MAG} and the f_{SWRT}. Use the below formula to calculate the steady-state peak current:

$$I_{PEAKDCM} = \sqrt{\frac{2 \times V_{OUT} \times I_{OUT}}{0.94 \times f_{SWRT} \times L_{MAG} \times (1 - TOL) \times \eta}}$$

$$I_{PEAKDCM} = \sqrt{\frac{2 \times 5 \times 0.25}{0.94 \times 150000 \times 100 \times 10^{-6} \times (1 - 0.1) \times 0.87}} = 0.476A$$

3. Output Capacitor Selection

For a target bandwidth of 10kHz in MAX17693A,

$$C_{OUT} = \frac{1.75 \times V_{OUT} \times I_{OUT}}{\sqrt{\eta} \times f_C \times I_{PEAKDCM} \times V^2_{OUT}}$$

$$C_{OUT} = \frac{1.75 \times 5 \times 0.25}{\sqrt{0.87} \times 10000 \times 0.476 \times 5^2} = 19.7\mu F$$

The output capacitance required for 1% output ripple is,

$$C_{OUT}(Ripple) \geq \frac{I_{OUT} \times (I_{PEAKDCM} - K \times I_{OUT})^2}{0.94 \times f_{SWRT} \times I^2_{PEAKDCM} \times V_{OUT\_RIPP}}$$

$$C_{OUT}(Ripple) \geq \frac{0.25 \times (0.476 - 0.45 \times 0.25)^2}{0.94 \times 150000 \times 0.476^2 \times 50 \times 10^{-3}} = 20.7\mu F$$

Select one 47µF, 10V, 1210 ceramic capacitors (GRM32ER71A476KE15) with an effective derated capacitance of 25µF at 5V.

For MAX17693B, the output capacitor is selected to limit output-voltage deviation within 3% of the rated voltage for a 50% load step. With a target bandwidth of 10kHz,

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SWRT}}\right)$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{10000} + \frac{1}{150000}\right) = 40\mu s$$

$$C_{OUTSTEP} = \frac{t_{RESPONSE} \times (3 \times I_{OUTFINAL} - I_{OUTINIT} - 2 \times \sqrt{I_{OUTINIT} \times I_{OUTFINAL}})}{4 \times (\Delta V_{OUT})}$$

$$C_{OUTSTEP} = \frac{46.1 \times 10^{-6} \times (3 \times 0.25 - 0.125 - 2 \times \sqrt{0.125 \times 0.25})}{4 \times 0.15} = 18\mu F$$

Select one 47µF, 10V, 1210 ceramic capacitors (GRM32ER71A476KE15) with an effective derated capacitance of 25µF at 5V.

Hence, C_{OUT} = 25µF for the MAX17693B design.

4. Soft-Start Time Selection

With 20ms soft-start time, the output capacitor charging current during soft-start is:

$$I_{COUT-SS} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}} = 6.25mA$$

The primary peak current during soft-start is:

$$I_{PEAKDCM-SS} = \sqrt{\frac{2 \times 5 \times (0.25 + 0.006)}{0.94 \times 150000 \times 100 \times 10^{-6} \times 0.9 \times 0.87}} = 0.482A$$

The $I_{PEAKDCM-SS}$ is lower than the minimum value of the peak current limit ($I_{LX-PEAK-MAX}$) set in the part, which is

0.495A.

5. Selection of Secondary Diode

The output diode reverse-voltage rating must be higher than the sum of the output voltage and the reflected input voltage.

$$V_{SEC\_RECT} = 1.5 \times (K \times V_{INMAX} + V_{OUT})$$
$$V_{SEC\_RECT} = 1.5 \times (0.45 \times 36 + 5) = 31.8V$$

The current rating of the secondary diode should be selected so that the power loss in the diode is small and the junction temperature is within limits. For the present design, SBR3U40P1 is selected.

6. $R_{TC/VCM}$ Resistor Selection

By referring to Table 1, use the factor m_f = 58600, and the calculate the common mode voltage setting K_{VCM}:

$$K_{VCM} = m_f \times L_{MAG} \times I_{PEAKDCM-SS}$$
$$K_{VCM} = 58600 \times 100 \times 10^{-6} \times 0.482 = 2.82$$

With $K_{VCM} \geq 2.5$, design $R_{TC/VCM}$ based on following equation for an output diode temperature coefficient of -1.7mV/°C:

$$R_{TC/VCM} = 1.2 \times R_{SET} \times \left(0.55 - \frac{(V_{OUT} + V_D) \times \left(\frac{\delta V_{TC/VCM}}{\delta T}\right)}{\frac{\delta V_D}{\delta T}}\right)$$

$$R_{TC/VCM} = 1.2 \times 10000 \times \left(0.55 + \frac{(5 + 0.4) \times 1.85 \times 10^{-3}}{1.7 \times 10^{-3}}\right) = 77.8k\Omega$$

A standard resistor of 76.8kΩ is selected for $R_{TC/VCM}$.

7. R_{SET} , R_{FB} Resistor Selection

With R_{SET} = 10kΩ, $R_{TC/VCM}$ = 76.8kΩ, $K_{VCM} \geq 2.5$ calculate the R_{FB} as below:

$$R_{FB} = \frac{(V_{OUT} + V_D)}{K} \times \left(\frac{1}{\frac{1}{R_{SET}} - \frac{0.66}{R_{TC/VCM}}}\right)$$

$$R_{FB} = \left(\frac{5 + 0.4}{0.45}\right) \times \left(\frac{1}{\frac{1}{10000} - \frac{0.66}{76800}}\right) = 131k\Omega$$

Based on bench measurement, a standard resistor of 127kΩ is selected for R_{FB}.

8. Input Capacitor Selection

The input capacitor is chosen to have 3% ripple at a nominal 24V input voltage.

$$C_{IN} \geq \frac{I_{PEAKDCM} \times D_{VINMIN} \times \left(1 - \frac{D_{VINMIN}}{2}\right)^2}{1.88 \times f_{SWRT} \times \Delta V_{IN}}$$

$$C_{IN} \geq \frac{0.476 \times 0.4 \times \left(1 - \frac{0.4}{2}\right)^2}{1.88 \times 150000 \times 24 \times 0.03} = 0.58\mu F$$

Select a 4.7µF, 50V, 0805 ceramic capacitor with a derated capacitance of 1.5µF at 24V.

9. Loop Compensation for MAX17693B

The loop compensation values for MAX17693B are calculated as follows

$$R_Z = 8180 \times \left(\frac{f_C}{f_P}\right) \times \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{MAG} \times f_{SWRT}}}$$

$$\text{Loadpole, } f_P = \frac{1}{\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}}$$

$$f_P = \frac{1}{\pi \times \frac{5}{0.25} \times 25 \times 10^{-6}} = 637\text{Hz}$$

$$R_Z = 8180 \times \left(\frac{10000}{637}\right) \times \sqrt{\frac{5 \times 0.25}{2 \times 100 \times 10^{-6} \times 150000}} = 26.2k$$

A standard 24.3kΩ is selected.

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P} = 10.3\text{nF}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SWRT}} = 87\text{pF}$$

The standard 10nF and 100pF are selected.

PCB Layout Guildlines

Careful PCB layout is critical to achieve clean and stable operation. Follow the below guidelines for good PCB layout:

1) Keep the loop area of paths carrying the pulsed currents as small as possible. In flyback design, the high frequency current path from the V_{IN} bypass capacitor through the primary-side winding and the internal nMOSFET switch is a critical loop.

2) A V_{CC} bypass capacitor should be connected right across the V_{CC} and GND pins of the IC.

3) A bypass capacitor should be connected across to the V_{IN} and GND pins, and should be placed close to the IC.

4) The exposed pad of the IC should be directly connected to the GND pin of the IC.

5) When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor.

6) The R_{FB} resistor trace length should be kept as small as possible.

7) To see the actual implementation of above guidelines, refer to the *MAX17693A/B EV kit* layouts, also available at the *MAX17693A/B* product page under the Design Resource tab.

Typical Application Circuits

24V to 5V, 0.25A MAX17693A No-Opto Flyback Application Circuit

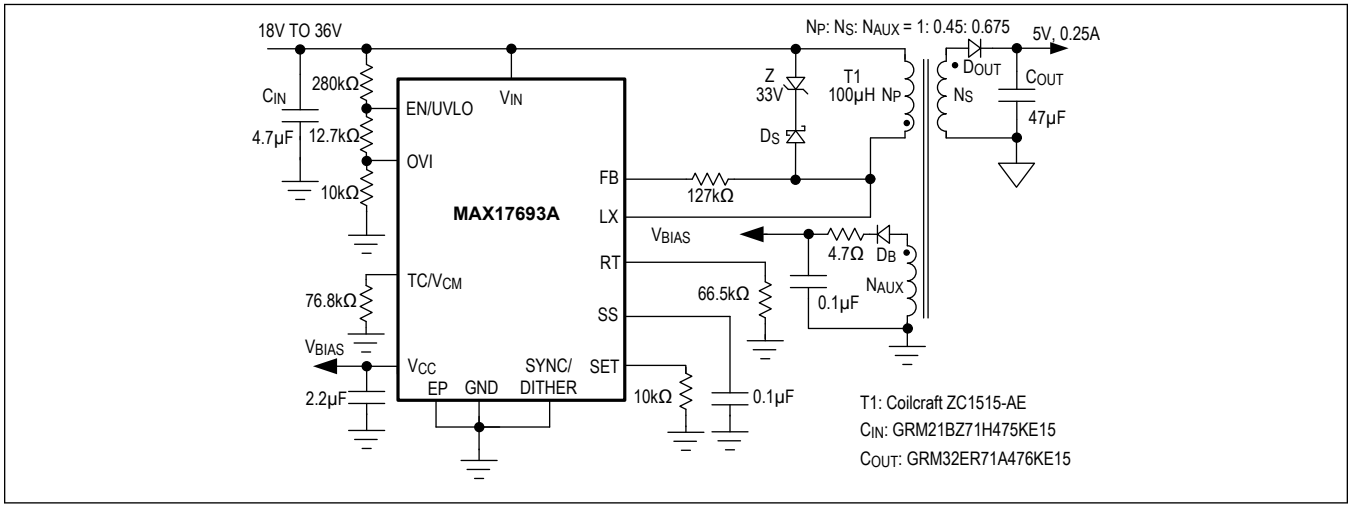


Figure 10. 24V to 5V, 0.25A MAX17693A No-Opto Flyback Application Circuit

24V to 5V, 0.25A MAX17693B No-Opto Flyback Application Circuit

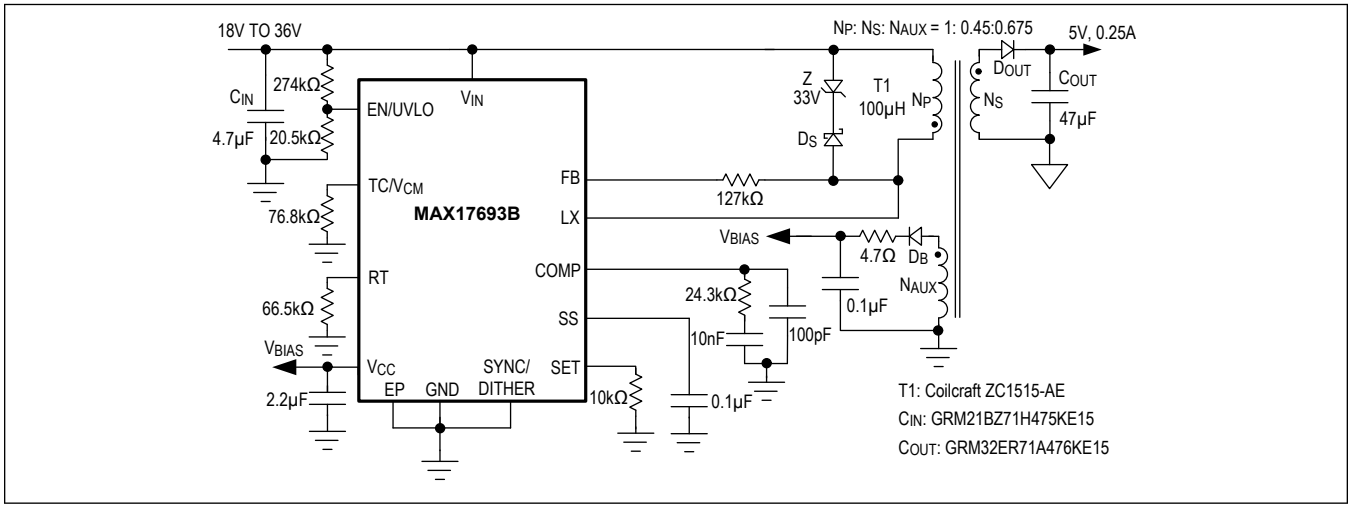


Figure 11. 24V to 5V, 0.25A MAX17693B No-Opto Flyback Application Circuit

Ordering Information

PART NUMBER	TEMP RANGE	PIN PACKAGE
MAX17693AATC+	-40°C to +125°C	12 TDFN
MAX17693AATC+T	-40°C to +125°C	12 TDFN
MAX17693BATC+	-40°C to +125°C	12 TDFN
MAX17693BATC+T	-40°C to +125°C	12 TDFN

+ Denotes lead(Pb)-free/RoHS compliance.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Release for Market Intro	—

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