

MAX17703

4.5V to 60V, Synchronous Step-Down Li-Ion Battery Charger Controller

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17703 is a high-efficiency, high-voltage, synchronous, step-down, Himalaya Li-ion battery-charger controller designed to operate over an input-voltage range of a 4.5V to 60V. The MAX17703 operates over a wide -40°C to $+125^{\circ}\text{C}$ temperature range and offers a complete charging solution for Li-ion batteries with a $\pm 4\%$ accurate constant current. The output voltage is programmable from 1.25V up to $(V_{\text{DCIN}} - 2.1\text{V})$ with $\pm 1\%$ regulation accuracy.

The device uses an external nMOSFET to provide input supply-side short-circuit protection, preventing battery discharge.

The device charges the battery in constant current (CC) and constant voltage (CV) states and terminates in a top-up-charge state after the taper timer is elapsed. The device resumes charging automatically when the battery voltage falls below the recharge voltage threshold. Detection and preconditioning of deeply discharged batteries are enabled by a deep discharge detection comparator.

The MAX17703 is available in a 24-pin 4mm x 4mm TQFN package with an exposed pad.

Applications

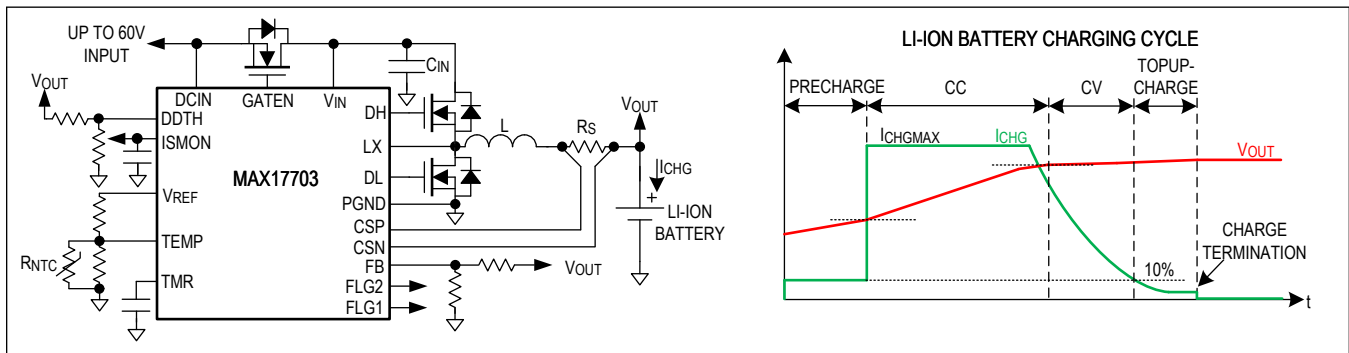
- Industrial Battery Charging and Energy Storage
- Power Tools and Handheld Terminals
- Battery Backup for Lighting, Security Cameras, and Control Panels
- Portable Industrial and Medical Equipment
- Building and Home-Automation Backup Power

Benefits and Features

- Optimized Feature-Set for Li-Ion Batteries Including Li-Polymer, LiFePO₄ and Li-Titanate
 - $\pm 4\%$ Charging Current Regulation Accuracy
 - $\pm 6\%$ Charging Current Monitor Accuracy (ISMON)
 - $\pm 1\%$ Voltage Regulation Accuracy
 - Programmable Constant Current (CC) Mode Charging Current (ILIM)
 - Charge Termination on Full Battery Detection with Taper Current Threshold and Taper Timer
 - Wide 4.5V to 60V Input-Voltage Range
 - Adjustable Output-Voltage Range from 1.25V up to $(V_{\text{DCIN}} - 2.1\text{V})$
 - 125kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization (RT/SYNC)
- Reliable Operation in Adverse Environmental Conditions
 - Input Short-Circuit Protection (GATEN)
 - Safety Timer Feature (TMR)
 - Deeply Discharged Battery Detection and Preconditioning (DDTH)
 - Battery Temperature Sensing and Charge when Within Temperature of Range (TEMP)
 - Cycle-by-Cycle Overcurrent Limit
 - Programmable EN/UVLO Threshold
 - Status Output Monitoring Using Open-Drain Outputs (FLG1 and FLG2)
 - Overtemperature Protection
 - Complies with CISPR 32 (EN55032) Class B Conducted and Radiated Emissions
 - Wide -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature Range/ -40°C to $+150^{\circ}\text{C}$ Junction Temperature Range

Ordering Information appears at end of data sheet.

Simplified Application Circuit



Absolute Maximum Ratings

| | | | |
|--|--|--|---|
| V_{IN} to SGND/EP | -0.3V to +65V | BST to PGND | -0.3V to +70V |
| DCIN to SGND/EP | -0.3V to min(+65V, $V_{IN} + 0.6V$) | DL to PGND | -0.3V to ($V_{CC} + 0.3V$) |
| GATEN to DCIN | -0.3V to +6V | DH to LX | -0.3V to (BST + 0.3V) |
| GATEN to SGND/EP | max(-0.3V, DCIN - 0.3V) to (DCIN + 6V) | EXTVCC to SGND/EP | -0.3V to +26V |
| V_{CC} to SGND/EP | -0.3V to min(+6V, $V_{IN} + 0.3V$) | PGND to SGND/EP | -0.3V to +0.3V |
| CSN, CSP to SGND/EP | -0.3V to ($V_{IN} + 0.6V$) | Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) TQFN (derate 27.85mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$) | 2222mW |
| CSP to CSN | -0.3V to +0.3V | Operating Temperature Range (Note 1) | -40 $^\circ\text{C}$ to +125 $^\circ\text{C}$ |
| V_{REF} , TMR, ILIM to SGND/EP | -0.3V to ($V_{CC} + 0.3V$) | Junction Temperature | +150 $^\circ\text{C}$ |
| COMP, ISMON, RT/SYNC to SGND/EP | -0.3V to ($V_{CC} + 0.3V$) | Storage Temperature Range | -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$ |
| DDTH, FB, TEMP to SGND/EP | -0.3V to +6V | Lead Temperature (soldering, 10s) | +300 $^\circ\text{C}$ |
| FLG1, FLG2, EN/UVLO to SGND/EP | -0.3V to +6V | Soldering Temperature (reflow) | +260 $^\circ\text{C}$ |
| LX to PGND | -0.3V to +65V | | |
| BST to LX | -0.3V to +6V | | |

Note 1: Junction temperature greater than +125 $^\circ\text{C}$ degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN

| | |
|---|------------------------------|
| Package Code | T2444+5C |
| Outline Number | 21-100405 |
| Land Pattern Number | 90-100139 |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction to Ambient (θ_{JA}) | 36 $^\circ\text{C}/\text{W}$ |
| Junction to Case (θ_{JC}) | 3 $^\circ\text{C}/\text{W}$ |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{IN} = V_{DCIN} = 24V$, $C_{VIN} = 4.7\mu\text{F}$, $C_{DCIN} = 100\text{nF}$, $C_{VCC} = 4.7\mu\text{F}$, $C_{VREF} = 100\text{nF}$, $C_{BST} = 470\text{nF}$, (V_{BST} to V_{LX}) = 5V, $V_{EN/UVLO} = V_{LX} = V_{ILIM} = V_{CSN} = V_{CSP} = V_{DDTH} = V_{TMR} = 2.5V$, $V_{TEMP} = V_{FB} = 1.1V$, $V_{EXTVCC} = V_{SGND/EP} = V_{PGND} = 0V$, RT/SYNC = DH = DL = GATEN = COMP = FLG1 = FLG2 = ISMON = Unconnected, $T_A = -40^\circ\text{C}$ to +125 $^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|-----------|--|-----|-----|-----|-------|
| POWER SUPPLY | | | | | | |
| DCIN Voltage Range | | DCIN connected to V_{IN} , External nMOSFET not used | 4.5 | | 60 | V |
| | | External nMOSFET used | 5.5 | | 60 | |
| V_{IN} Voltage Range | | | 4.5 | | 60 | V |
| Input Quiescent Current | I_{QNS} | ($V_{IN} - V_{CSN}$) > 2.1V, $V_{FB} = 1.5V$ | 1.4 | 2.1 | 2.8 | mA |

Electrical Characteristics (continued)

($V_{IN} = V_{DCIN} = 24V$, $C_{VIN} = 4.7\mu F$, $C_{DCIN} = 100nF$, $C_{VCC} = 4.7\mu F$, $C_{VREF} = 100nF$, $C_{BST} = 470nF$, (V_{BST} to V_{LX}) = 5V, $V_{EN/UVLO} = V_{LX} = V_{ILIM} = V_{CSN} = V_{CSP} = V_{DDTH} = V_{TMR} = 2.5V$, $V_{TEMP} = V_{FB} = 1.1V$, $V_{EXTVCC} = V_{SGND/EP} = V_{PGND} = 0V$, $RT/SYNC = DH = DL = GATEN = COMP = FLG1 = FLG2 = ISMON = \text{Unconnected}$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------|--|--------|-------|--------|---------|
| Input Switching Current | I_{QS} | | 1.7 | 2.5 | 3.5 | mA |
| Shutdown Supply Current | I_{IN-SH} | $V_{EN/UVLO} = 0V$ (shutdown mode) | | 7 | 18 | μA |
| ENABLE/UVLO (EN/UVLO) | | | | | | |
| EN/UVLO Rising Threshold | $V_{EN_TH_R}$ | $V_{EN/UVLO}$ rising | 1.22 | 1.25 | 1.27 | V |
| EN/UVLO Falling Threshold | $V_{EN_TH_F}$ | | 1.07 | 1.09 | 1.11 | V |
| EN/UVLO Bias Current | $I_{EN-BIAS}$ | $V_{EN/UVLO} = 0.5V$ | 1.4 | 3.0 | 6.5 | μA |
| EN/UVLO True Shutdown Threshold | V_{ENT} | $V_{EN/UVLO}$ rising | 0.4 | 0.7 | 1.1 | V |
| | | Hysteresis | | 60 | | mV |
| V_{CC} REGULATORS (INT-LDO AND EXT-LDO) | | | | | | |
| V _{CC} Output Voltage | V _{CC} | $6V < V_{IN} < 60V$, $I_{VCC} = 1mA$ (V_{CC} supplied from INT-LDO) | 5.00 | 5.15 | 5.30 | V |
| | | $V_{IN} = 24V$, $I_{VCC} = 0mA$ to 75mA, (V_{CC} supplied from INT-LDO) | 4.95 | 5.10 | 5.25 | |
| | | $6V < V_{EXTVCC} < 24V$, $I_{VCC} = 1mA$ (V_{CC} supplied from EXT-LDO) | 5.00 | 5.15 | 5.30 | |
| | | $V_{EXTVCC} = 12V$, $I_{VCC} = 0mA$ to 75 mA, (V_{CC} supplied from EXT-LDO) | 4.95 | 5.10 | 5.25 | |
| V _{CC} Output-Current Limit | I_{VCC_LIMIT} | $V_{IN} = 8.5V$, $V_{CC} = 4V$ (V_{CC} supplied from INT-LDO) | 80 | 110 | 135 | mA |
| | | $V_{EXTVCC} = 8.5V$, $V_{CC} = 4V$ (V_{CC} supplied from EXT-LDO) | 80 | 110 | 135 | |
| V _{CC} Dropout Voltage | V _{CC-DO} | $V_{IN} = 4.5V$, $I_{VCC} = 75mA$ (V_{CC} supplied from INT-LDO) | | 370 | 750 | mV |
| | | $V_{EXTVCC} = 4.9V$, $I_{VCC} = 75mA$ (V_{CC} supplied from EXT-LDO) | | 185 | 350 | |
| V _{CC} Undervoltage Threshold | V _{CC-UVR} | V _{CC} rising | 4.14 | 4.20 | 4.26 | V |
| | V _{CC-UVF} | V _{CC} falling | 3.74 | 3.80 | 3.86 | |
| EXTVCC Voltage Range | | | 4.8 | | 24 | V |
| EXTVCC Switchover Voltage | | V _{EXTVCC} rising | 4.63 | 4.70 | 4.77 | V |
| | | Hysteresis | | 0.24 | | |
| OSCILLATOR (RT/SYNC) | | | | | | |
| Switching Frequency | f_{SW} | $R_{RT/SYNC} = 350k\Omega$ | 118.75 | 125 | 131.25 | kHz |
| | | $R_{RT/SYNC} = \text{unconnected}$ | 332.5 | 350.0 | 367.5 | |
| | | $R_{RT/SYNC} = 110k\Omega$ | 380 | 400 | 420 | |
| | | $R_{RT/SYNC} = 19k\Omega$ | 2090 | 2200 | 2310 | |

Electrical Characteristics (continued)

($V_{IN} = V_{DCIN} = 24V$, $C_{VIN} = 4.7\mu F$, $C_{DCIN} = 100nF$, $C_{VCC} = 4.7\mu F$, $C_{VREF} = 100nF$, $C_{BST} = 470nF$, (V_{BST} to V_{LX}) = 5V, $V_{EN/UVLO} = V_{LX} = V_{ILIM} = V_{CSN} = V_{CSP} = V_{DDTH} = V_{TMR} = 2.5V$, $V_{TEMP} = V_{FB} = 1.1V$, $V_{EXTVCC} = V_{SGND/EP} = V_{PGND} = 0V$, $RT/SYNC = DH = DL = GATEN = COMP = FLG1 = FLG2 = ISMON = \text{Unconnected}$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|--|----------------|-------|----------------|----------|
| Synchronization Frequency Range | f_{SYNC} | | 0.9 x f_{SW} | | 1.1 x f_{SW} | kHz |
| External Clock Amplitude | | $C_{COUPLING} = 10pF$ | 3 | | | V |
| SYNC High Pulse Width | | | 100 | | | ns |
| SYNC Low Pulse Width | | | 100 | | | ns |
| SYNC Input-Leakage Current | I_{SYNC_LKG} | $V_{RT/SYNC} = 2.5V$, $T_A = +25^\circ C$ | -100 | | +100 | nA |
| GATE DRIVER | | | | | | |
| DH to BST On-Resistance | | Source 100mA | 0.8 | 1.2 | 2.1 | Ω |
| DH to LX On-Resistance | | Sink 100mA | 0.3 | 0.6 | 1.0 | Ω |
| DL to V_{CC} On-Resistance | | Source 100mA | 0.8 | 1.2 | 2.1 | Ω |
| DL to PGND On-Resistance | | Sink 100mA | 0.3 | 0.6 | 1.0 | Ω |
| DH Minimum Controlled On-Time | $t_{MIN_ON_DH}$ | | 60 | 80 | 100 | ns |
| DL Minimum Guaranteed On-Time | $t_{MIN_ON_DL}$ | | 60 | 80 | 100 | ns |
| Dead Time | t_{DT_HL} | DH falling to DL rising, $C_{DH-LX} = 6nF$, $C_{DL-PGND} = 6nF$ | | 30 | | ns |
| | t_{DT_LH} | DL falling to DH rising, $C_{DH-LX} = 6nF$, $C_{DL-PGND} = 6nF$ | | 30 | | |
| DH Transition Time | t_{HR} | DH rising, $C_{DH-LX} = 6nF$ | | 25 | | ns |
| | t_{HF} | DH falling, $C_{DH-LX} = 6nF$ | | 11 | | |
| DL Transition Time | t_{LR} | DL rising, $C_{DL-PGND} = 6nF$ | | 25 | | ns |
| | t_{LF} | DL falling, $C_{DL-PGND} = 6nF$ | | 11 | | |
| REFERENCE VOLTAGE (V_{REF}) | | | | | | |
| V_{REF} Output Voltage | V_{REF} | $I_{VREF} = 0$ to 1mA | 2.465 | 2.500 | 2.535 | V |
| Reference Current Limit | I_{REF_LIM} | $V_{REF} = 2.45V$ | 1.2 | 1.8 | 2.7 | mA |
| CURRENT SENSE (CSP, CSN, ILIM) | | | | | | |
| CSP, CSN Common-Mode Voltage Range | | | 0 | | $(V_{IN} - 2)$ | V |
| CSP-to-CSN Input Operating Voltage | V_{DIFF_CS} | $V_{DIFF_CS} = (V_{CSP} - V_{CSN})$ | -10 | | +100 | mV |
| CSP-to-CSN Regulation Voltage Accuracy | V_{CSREG} | $V_{ILIM} = 1.5V$ | 48 | 50 | 52 | mV |
| | | $V_{ILIM} = 0.9V$ | 28 | 30 | 32 | |
| | | $V_{ILIM} = V_{REF}$ | 48 | 50 | 52 | |

Electrical Characteristics (continued)

($V_{IN} = V_{DCIN} = 24V$, $C_{VIN} = 4.7\mu F$, $C_{DCIN} = 100nF$, $C_{VCC} = 4.7\mu F$, $C_{VREF} = 100nF$, $C_{BST} = 470nF$, (V_{BST} to V_{LX}) = 5V, $V_{EN/UVLO} = V_{LX} = V_{ILIM} = V_{CSN} = V_{CSP} = V_{DDTH} = V_{TMR} = 2.5V$, $V_{TEMP} = V_{FB} = 1.1V$, $V_{EXTVCC} = V_{SGND/EP} = V_{PGND} = 0V$, $RT/SYNC = DH = DL = GATEN = COMP = FLG1 = FLG2 = ISMON = \text{Unconnected}$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|--------------------------|--|-----------------------------------|-------|-------|----------|------|
| CSP Pin Current | | CSP source | | 200 | 1400 | nA | |
| CSN Pin Current | | $V_{EN/UVLO} = 0V$, CSN sink | | 1.3 | 2.3 | μA | |
| | | Charger on, $V_{ILIM} = 0.9V$ to $1.5V$ | $I_{CHG} > I_{TCHG}$, CSN source | 250 | 400 | | 550 |
| | | | $I_{CHG} < I_{TCHG}$, CSN sink | 470 | 700 | | 1000 |
| Current-Loop-Error Amplifier Transconductance | g_{mi} | $(V_{CSP} - V_{CSN}) = V_{CSREG} \pm 25mV$ | 275 | 480 | 685 | μS | |
| ILIM Input Leakage Current | | $V_{ILIM} = 1.5V$, $T_A = 25^\circ C$ | -100 | | 100 | nA | |
| CSN Undervoltage Lockout Threshold | V_{CMUVLO} | $(V_{IN} - V_{CSN})$, rising | 1.97 | 2.04 | 2.10 | V | |
| | | $(V_{IN} - V_{CSN})$, falling | 1.88 | 1.95 | 2.02 | | |
| Overcurrent Threshold | V_{CS_PEAK} | $V_{CS_PEAK} = (V_{CSP} - V_{CSN})$, $V_{ILIM} = 1.5V$ | 70 | 75 | 80 | mV | |
| | | Hysteresis | | 10 | | | |
| Zero-Cross Threshold | V_{ZX} | $(V_{CSP} - V_{CSN})$ falling | | -1.7 | | mV | |
| PWM-Ramp Amplitude | V_{RAMP} | $f_{SW} = 125kHz$ to $2.2MHz$ | 1.37 | 1.44 | 1.51 | V | |
| VOLTAGE REGULATION AMPLIFIER (FB) | | | | | | | |
| FB Reference Voltage | V_{FB_REG} | | 1.237 | 1.250 | 1.263 | V | |
| FB Input-Leakage Current | | $V_{FB} = 1.3V$, $T_A = +25^\circ C$ | -100 | | 100 | nA | |
| Voltage-Loop-Error Amplifier Gain | G_V | | 1.15 | 1.30 | 1.42 | mV/mV | |
| FB to SGND/EP Short Fault Threshold | V_{FBGND} | $V_{FB} < V_{FBGND}$ | 57 | 65 | 73 | mV | |
| INPUT SHORT-CIRCUIT PROTECTION (GATEN) | | | | | | | |
| External nMOSFET Gate Drive Voltage | $(V_{GATEN} - V_{DCIN})$ | | 4.65 | 5 | 5.50 | V | |
| GATEN Drive Current | I_{GATEN} | | 17 | 20 | 23 | μA | |
| GATEN Active Pulldown Resistance | R_{GATEN_A} | $I_{GATEN} = 100mA$ | | 1.1 | 2.1 | Ω | |
| GATEN Passive Pulldown Resistance | R_{GATEN_P} | $V_{EN/UVLO} = 0V$ | | 400 | 800 | Ω | |
| GATEN-DCIN Threshold | V_{GATEN_OK} | | 3.20 | 3.55 | 3.90 | V | |
| GATEN OK Delay | t_{GATEN_OK} | | | 15 | | ms | |
| External nMOSFET Reverse-Blocking Threshold | V_{REV} | $(V_{DCIN} - V_{IN})$ falling | -111 | -93 | -75 | mV | |
| | | Hysteresis | | 20 | | | |

Electrical Characteristics (continued)

($V_{IN} = V_{DCIN} = 24V$, $C_{VIN} = 4.7\mu F$, $C_{DCIN} = 100nF$, $C_{VCC} = 4.7\mu F$, $C_{VREF} = 100nF$, $C_{BST} = 470nF$, (V_{BST} to V_{LX}) = 5V, $V_{EN/UVLO} = V_{LX} = V_{ILIM} = V_{CSN} = V_{CSP} = V_{DDTH} = V_{TMR} = 2.5V$, $V_{TEMP} = V_{FB} = 1.1V$, $V_{EXTVCC} = V_{SGND/EP} = V_{PGND} = 0V$, $RT/SYNC = DH = DL = GATEN = COMP = FLG1 = FLG2 = ISMON = \text{Unconnected}$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|-----------------|---|-------------------|--------------------|-------|--------------------|---------|
| External nMOSFET Reverse-Blocking Response Time | | $C_{GATEN-DCIN} = 10nF$, $V_{DCIN} < (V_{IN} - 93mV)$ to $(V_{GATEN} - V_{DCIN}) < 2V$ | | 100 | 180 | ns | |
| V_{IN} to DCIN Reverse Leakage Current | | $V_{DCIN} = 0V$, $V_{IN} = 60V$ | | $V_{EN/UVLO} = 0V$ | 170 | 260 | μA |
| | | | | | 230 | 350 | |
| CHARGER FUNCTIONS | | | | | | | |
| Constant-Voltage (CV) Mode FB Threshold | V_{FB_CV} | $V_{ILIM} = 1.5V$, V_{FB} rising | 97.15 | 97.50 | 97.85 | % of V_{FB_REG} | |
| | | | Hysteresis | | | | 0.3 |
| FB Recharge-Voltage Threshold | V_{RECHG} | V_{FB} falling | 94.5 | 95 | 95.5 | % of V_{FB_REG} | |
| | | | Hysteresis | | | | 0.56 |
| Deep-Discharge Comparator Threshold (DDTH) | V_{DDREF} | V_{DDTH} rising | 1.245 | 1.260 | 1.275 | V | |
| | | V_{DDTH} falling | 1.235 | 1.250 | 1.265 | | |
| Precharge State CSP-to-CSN Regulation Voltage Accuracy | V_{CSPCHG} | $V_{DDTH} = 1.1V$ | $V_{ILIM} = 1.5V$ | 2.5 | 5 | 7.5 | mV |
| | | | $V_{ILIM} = 0.9V$ | 0.5 | 3 | 5.5 | |
| Taper Current Threshold | I_{TCHG} | Current falling (see Note 3) | 4.8 | 10 | 16.8 | % of I_{CHGMAX} | |
| ISMON Output-Voltage Accuracy | | $(V_{CSP} - V_{CSN}) = 50mV$ $(V_{CSP} - V_{CSN}) = 30mV$ | 1.41 | 1.50 | 1.59 | V | |
| | | | 0.825 | 0.900 | 0.975 | | |
| ISMON Output Resistance | | | | 90 | | k Ω | |
| ISMON Output Bandwidth | | | | 100 | | kHz | |
| CHARGER TIMER (TMR) | | | | | | | |
| Charger Startup Delay | t_{CH_START} | $C_{TMR} = 220nF$ | | 55 | | ms | |
| | | TMR disabled | | 54 | | | |
| TMR-Oscillator Upper Threshold | V_{TMR_H} | | 1.47 | 1.50 | 1.53 | V | |
| TMR-Oscillator Lower Threshold | V_{TMR_L} | | 0.94 | 0.96 | 0.98 | V | |
| TMR Source/Sink Current | I_{TMR} | | 8.9 | 10 | 10.9 | μA | |
| TMR Disable Threshold | V_{TMR_DIS} | $V_{TMR} > V_{TMR_DIS}$ (power-up check only) | 1.9 | 2.0 | 2.1 | V | |
| TMR Short-to-SGND/EP Fault Threshold | V_{TMR_GND} | $V_{TMR} < V_{TMR_GND}$ (power-up check only) | 80 | 100 | 120 | mV | |
| Safety Timer Timeout | t_{FCHG} | | | 1048575 | | TMR CYCLES | |
| Precharge Timer Timeout | t_{PCHG} | | | 131071 | | TMR CYCLES | |

Electrical Characteristics (continued)

($V_{IN} = V_{DCIN} = 24V$, $C_{VIN} = 4.7\mu F$, $C_{DCIN} = 100nF$, $C_{VCC} = 4.7\mu F$, $C_{VREF} = 100nF$, $C_{BST} = 470nF$, (V_{BST} to V_{LX}) = 5V, $V_{EN/UVLO} = V_{LX} = V_{ILIM} = V_{CSN} = V_{CSP} = V_{DDTH} = V_{TMR} = 2.5V$, $V_{TEMP} = V_{FB} = 1.1V$, $V_{EXTVCC} = V_{SGND/EP} = V_{PGND} = 0V$, $RT/SYNC = DH = DL = GATEN = COMP = FLG1 = FLG2 = ISMON = \text{Unconnected}$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------|--|------|--------|------|-------------------|
| Taper-Timer Timeout | t_{TOP} | | | 104857 | | TMR CYCLES |
| BATTERY TEMPERATURE SENSE (TEMP) | | | | | | |
| TEMP Upper Threshold | V_{TEMPU} | Battery temperature falling | 59.4 | 60 | 60.6 | % of V_{REF} |
| | | Hysteresis | | 1 | | |
| TEMP Lower Threshold | V_{TEMPL} | Battery temperature rising | 39.4 | 40 | 40.6 | % of V_{REF} |
| | | Hysteresis | | 1.2 | | |
| CHARGER STATUS OUTPUTS (FLG1, FLG2) | | | | | | |
| FLG1/FLG2 Pulldown Voltage | | $I_{FLG1}, I_{FLG2} = 10mA$ | | | 500 | mV |
| FLG1/FLG2 Leakage Current | | $V_{FLG1}, V_{FLG2} = 5.5V, T_A = +25^\circ C$ | -100 | | +100 | nA |
| IC THERMAL PROTECTION | | | | | | |
| Thermal Shutdown Threshold | | Temperature rising | | 160 | | $^\circ C$ |
| Thermal Shutdown Hysteresis | | | | 10 | | $^\circ C$ |

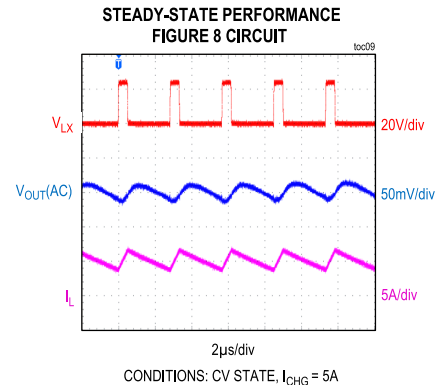
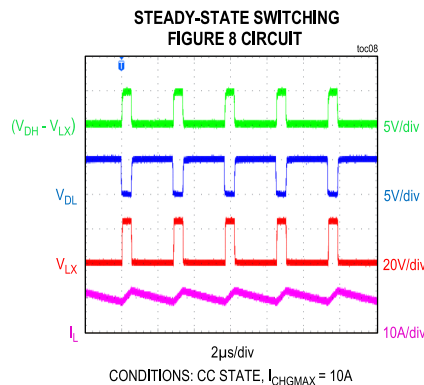
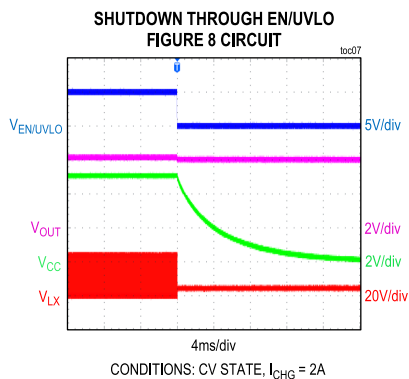
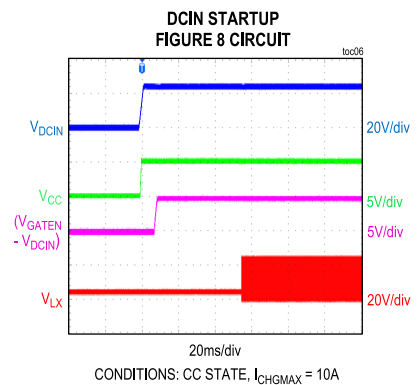
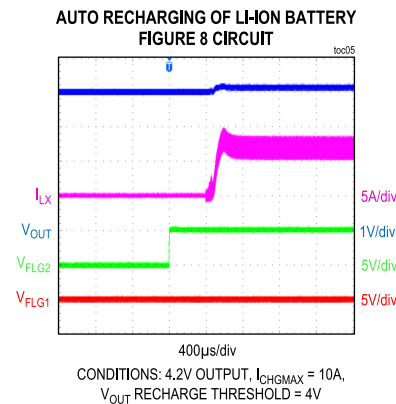
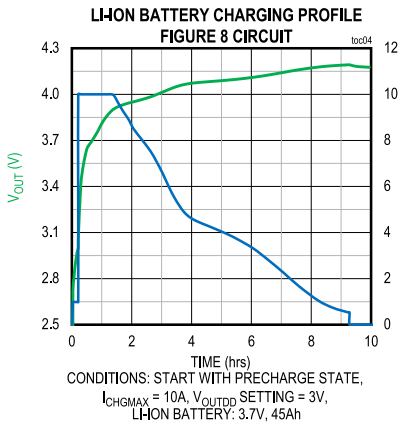
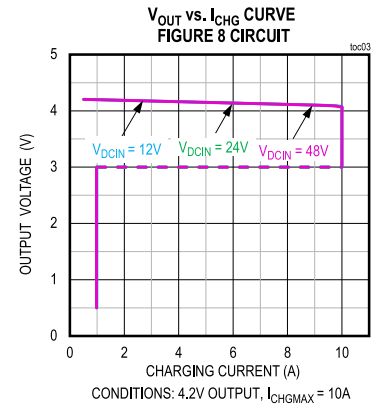
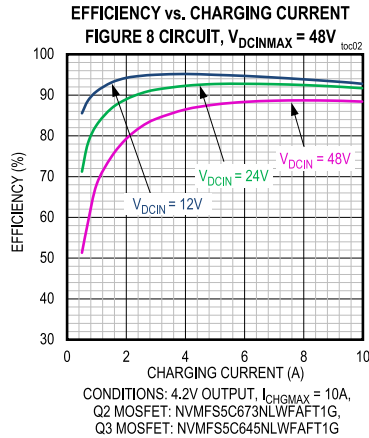
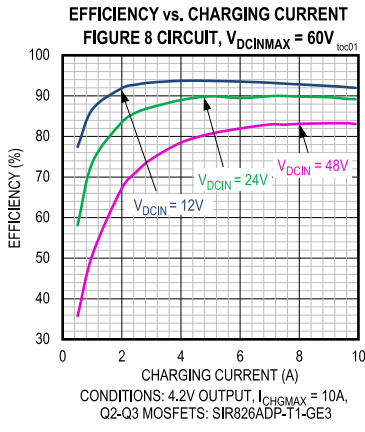
Note 2: Electrical specifications are production tested at $T_A = +25^\circ C$. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 3: CC mode charging current setting is calculated using the following equation

$$I_{CHGMAX} = \frac{V_{CSREG}}{R_S}, \text{ where } R_S \text{ is the current-sense resistor.}$$

Typical Operating Characteristics

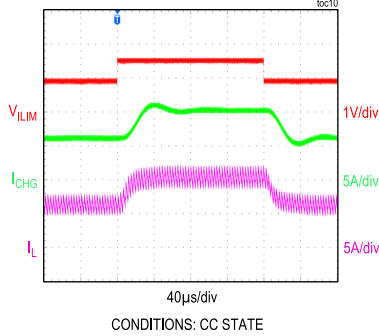
($V_{DCIN} = 24V$, $V_{SGND/EP} = V_{PGND} = 0V$, RT/SYNC = unconnected ($f_{SW} = 350kHz$), $T_A = +25^\circ C$, unless otherwise noted. All voltages are referenced to SGND/EP, unless otherwise noted.)



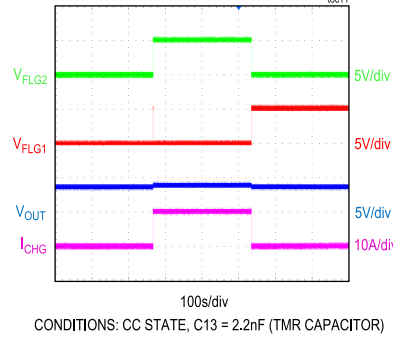
Typical Operating Characteristics (continued)

($V_{DCIN} = 24V$, $V_{SGND/EP} = V_{PGND} = 0V$, RT/SYNC = unconnected ($f_{SW} = 350kHz$), $T_A = +25^\circ C$, unless otherwise noted. All voltages are referenced to SGND/EP, unless otherwise noted.)

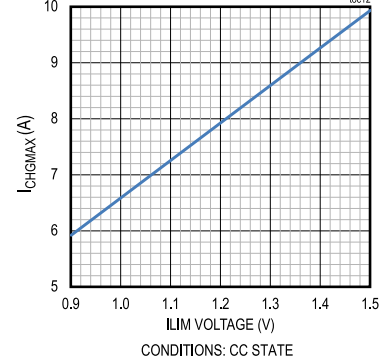
ILIM TRANSIENT PERFORMANCE
 V_{ILIM} IS VARIED BETWEEN 0.9V AND 1.5V
FIGURE 8 CIRCUIT



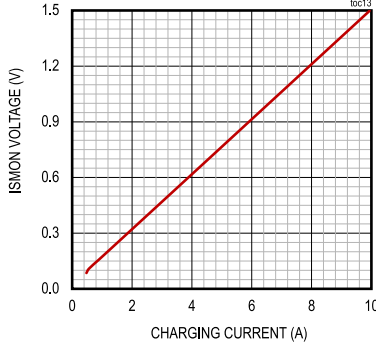
SAFETY TIMER FAULT
FIGURE 8 CIRCUIT



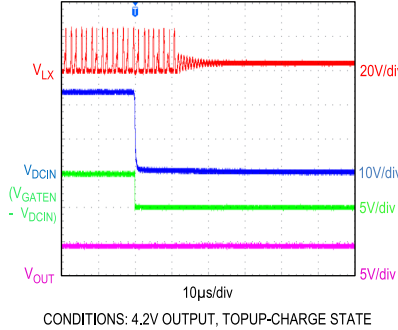
I_{CHGMAX} vs. $ILIM$ VOLTAGE
FIGURE 8 CIRCUIT



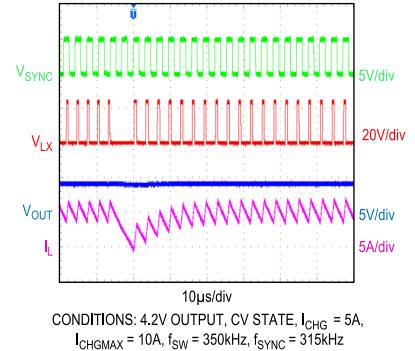
ISMON VOLTAGE vs. CHARGING CURRENT
FIGURE 8 CIRCUIT



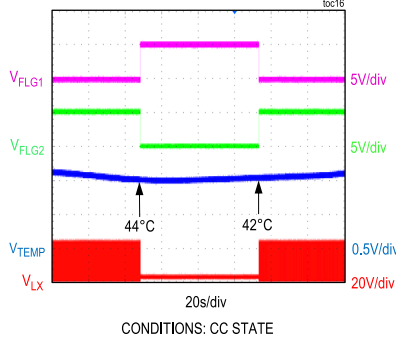
INPUT (DCIN) SHORT PROTECTION
FIGURE 8 CIRCUIT



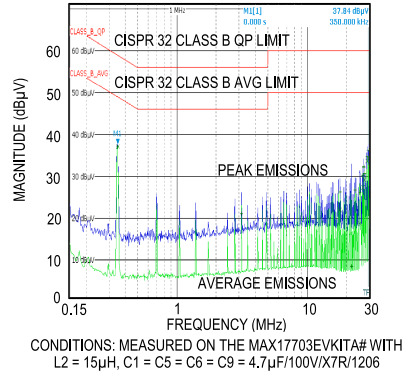
EXTERNAL CLOCK SYNCHRONIZATION
AFTER 112 CYCLES OF f_{SW}
FIGURE 8 CIRCUIT



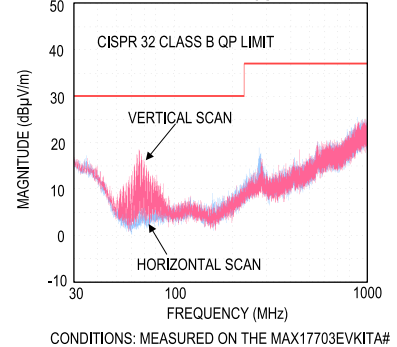
TEMP CHARGING DISABLE AND ENABLE
FIGURE 8 CIRCUIT



4.2V OUTPUT, 10A CHARGING CURRENT
CONDUCTED EMI CURVE

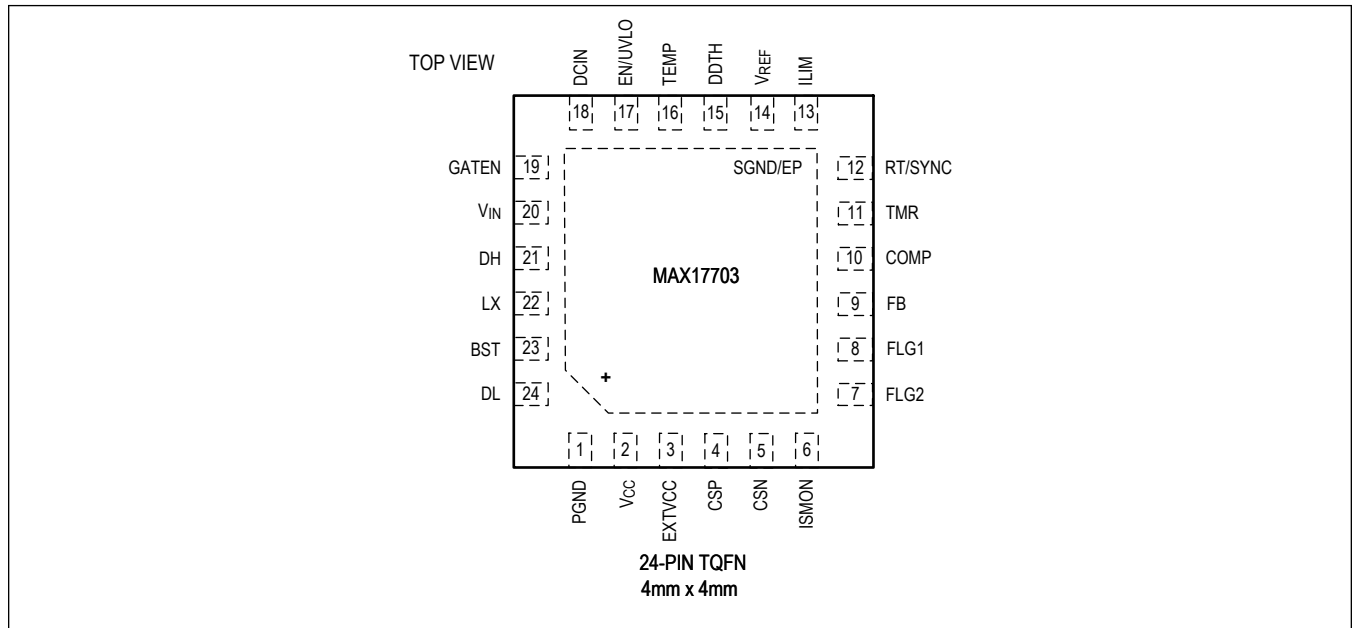


4.2V OUTPUT, 10A CHARGING CURRENT
RADIATED EMI CURVE



Pin Configuration

MAX17703



Pin Description

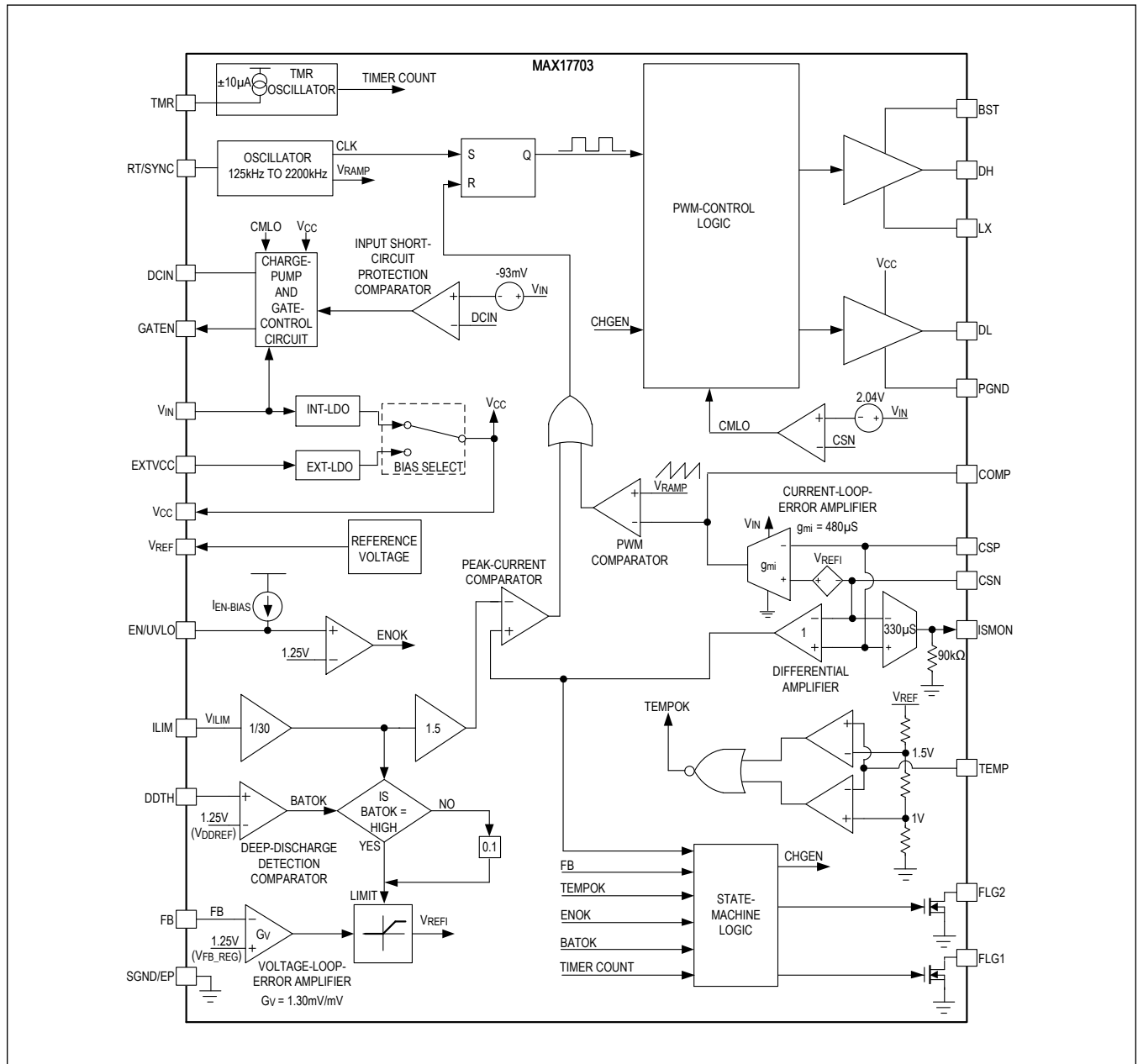
| PIN | NAME | FUNCTION |
|------|------------|---|
| 1 | PGND | Power Ground. Connect to the return terminal of a V_{CC} bypass capacitor placed close to the IC and the source terminal of external low-side nMOSFET. Refer to the MAX17703 evaluation kit data sheet for the PCB layout example. |
| 2 | V_{CC} | Internal LDO Output. Connect a minimum of $4.7\mu\text{F}/0805$, low-ESR ceramic capacitor between V_{CC} and PGND. V_{CC} supports IC internal-control circuitry and gate-drive current for external nMOSFETs. |
| 3 | EXTVCC | External Power-Supply Input for EXT-LDO. To power internal circuitry from an external supply, apply a voltage between 4.8V and 24V to the EXTVCC pin. Connect a minimum of $1\mu\text{F}/0603$, low-ESR ceramic capacitor between EXTVCC and SGND/EP. Leave EXTVCC open when not used. |
| 4 | CSP | Inverting Input of the Current Loop Error Amplifier. The CSP and CSN pins measure the voltage across the current sense resistor R_S (see Figure 5). |
| 5 | CSN | Non-Inverting Input of the Current-Loop-Error Amplifier. Connect CSN to the node connecting the output capacitor and current sense resistor R_S . Use Kelvin connections and route the CSP and CSN traces as a differential pair (see Figure 5). |
| 6 | ISMON | Output of Charging Current Monitor. Bypass ISMON with a 1nF low-ESR ceramic capacitor to SGND/EP. The voltage on this pin is 30 times the voltage drop across the current-sense resistor (R_S). |
| 7, 8 | FLG2, FLG1 | Open Drain Status Output Pins. Connect one 10k Ω pullup resistor each from V_{CC} to FLG1 and FLG2. See the Charger Status Outputs (FLG1, FLG2) section for more details. |
| 9 | FB | Feedback Input. Connect FB to the center node of a resistor-divider from the positive terminal of the battery to SGND/EP to set the output voltage. See the Setting Output Voltage and Voltage Regulation Loop (FB) section for more details. |

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----|-----------|--|
| 10 | COMP | Current Loop Error Amplifier Output. Connect a compensation network at this pin to stabilize the inner current loop. See the Current Regulation Loop Compensation (COMP) section for more details. |
| 11 | TMR | Battery Safety Timer Setting Pin. A capacitor from TMR to SGND/EP sets the charging time in precharge, CC, CV, topup-charge states. Place the timer capacitor close to the TMR pin. Connect TMR to V_{REF} to disable the timer function. See the Charger Timers (TMR) section for more details. |
| 12 | RT/SYNC | Switching Frequency Programming/Synchronization Input. Connect a resistor from RT/SYNC to SGND/EP to set the switching frequency between 125kHz to 2.2MHz. Leave RT/SYNC open for the default 350kHz frequency. See the Setting the Switching Frequency and External Clock Synchronization (RT/SYNC) section for more details. |
| 13 | ILIM | CC Mode Charging Current Programming Input. Connect ILIM to the center node of a resistor divider between V_{REF} and SGND/EP to set the CC mode charging current. Connect to V_{REF} for the default CC mode charging current. See the CC Mode Charging Current Setting (ILIM) section for more details. |
| 14 | V_{REF} | 2.5V Reference Output. Bypass V_{REF} with a 0.1 μ F low-ESR ceramic capacitor to SGND/EP. See the Reference Voltage (V_{REF}) section for more details. |
| 15 | DDTH | Battery Deep-Discharge Detection Input. Connect DDTH to the center node of a resistor divider from the output-voltage node to SGND/EP. If V_{DDTH} falls below V_{DDREF} , the charger enters the precharge state for battery preconditioning. See the Setting the Deep Discharge Voltage Level (DDTH) and Power-Up/Down Sequence and Charger Operation sections for more details. |
| 16 | TEMP | Battery Temperature Input. Connect TEMP to the center node of a resistor divider from V_{REF} to SGND/EP. Connect the battery temperature sensing NTC resistor terminals across the bottom resistor of the divider to program the battery charging temperature window. See the Setting Battery Operating Temperature Range (TEMP) section for more details. |
| 17 | EN/UVLO | Enable/Undervoltage-Lockout Input. Connect to the center node of a resistor divider between DCIN and SGND/EP to set the input voltage at which the device turns on. Connect to SGND/EP to shutdown the device. See the Setting the Input Undervoltage-Lockout Level (EN/UVLO) section for more details. |
| 18 | DCIN | Input-Supply-Voltage Sense Pin. Bypass DCIN with a 0.1 μ F ceramic capacitor to PGND. Refer to the MAX17703 EV kit data sheet for the recommended PCB layout and routing. |
| 19 | GATEN | Gate Drive Output for External nMOSFET. Bypass GATEN with a 2.2nF low-ESR ceramic capacitor to DCIN. GATEN controls the gate of an external nMOSFET connected between DCIN and V_{IN} to prevent battery discharge when DCIN is shorted to PGND. See the Input Short Circuit Protection (GATEN) section for more details. |
| 20 | V_{IN} | MAX17703 IC-Supply Pin. Bypass V_{IN} to PGND with a 0.1 μ F ceramic capacitor. Refer to the MAX17703 EV kit data sheet for the recommended PCB layout and routing. |
| 21 | DH | High-Side nMOSFET Gate Driver Output. Connect to the gate of the high-side nMOSFET. |
| 22 | LX | Switching Node Connection Input. Connect to the switching node of the converter. |
| 23 | BST | Bootstrap Capacitor Connection Input. Connect a capacitor of 0.1 μ F (min) between the BST and LX pins. Connect a Schottky diode from the V_{CC} to the BST pin. See the Bootstrap Capacitor Selection and Bootstrap Diode Selection sections for more details. |
| 24 | DL | Low-Side nMOSFET Gate Driver Output. Connect to the gate of the low-side nMOSFET. |
| — | SGND/EP | Signal Ground, Exposed Pad. Refer to the MAX17703 EV kit data sheet for the recommended method of PCB layout, routing, and thermal vias. |

Functional Diagrams

MAX17703



Detailed Description

The MAX17703 is a 4.5V to 60V wide input, synchronous, step-down Li-ion battery-charger controller designed to operate over a -40°C to +125°C temperature range. It offers a complete battery charge cycle solution for Li-ion batteries including Li-Polymer, LiFePO₄, and Li-Titanate. Charging begins in one of the three states, namely, precharge, constant current (CC), and constant voltage (CV) depending on the battery voltage. The charger enters a topup-charge state when the charging current reduces to the taper-current threshold. Charging is terminated in the topup-charge state, when the taper-timer period elapses. The MAX17703 initiates a recharge cycle when output voltage falls below the recharge threshold voltage. The device provides input short-circuit protection, and prevents battery discharging for input supply-side short-circuit events by means of an external nMOSFET. The MAX17703 offers up to ±4% accurate constant charging current in CC mode and regulates the no-load output voltage with ±1% accuracy. The MAX17703 supports a wide adjustable output-voltage range of 1.25V to (V_{DCIN} - 2.1V).

The MAX17703 features a constant frequency, average current-mode control architecture shown in [Figure 1](#). An internal current loop consists of a transconductance amplifier (g_{mi}) that senses the inductor current flowing through current-sense resistor (R_S) as a voltage drop across the CSP and CSN pins. The current-sense voltage is compared with a current-loop reference voltage (V_{REFI}), which is set by the outer-voltage loop-error amplifier (G_V) and limited by the voltage programmed at the ILIM pin (V_{ILIM}). The voltage at the COMP pin is compared with a 1.44V (typ) ramp using a PWM comparator to set the duty cycle of the converter. The required compensation to stabilize the current loop is applied at the COMP pin using R_Z, C_Z, and C_P. Under steady-state conditions, the inner current loop forces the voltage drop across R_S equal to V_{REFI}.

The output voltage is monitored by the voltage error amplifier G_V with a resistor divider (R_{TOP} and R_{BOT}) connected across the positive and negative battery terminals with the center node connected to the FB pin. The voltage at the FB pin is compared with the FB reference voltage (V_{FB_REG}). The voltage-loop-error amplifier sets the current-loop reference voltage (V_{REFI}). V_{REFI} is limited to $\frac{V_{ILIM}}{30}$ until $V_{FB} \leq \left[V_{FB_REG} - \frac{V_{ILIM}}{30 \times G_V} \right]$. This results in constant current

through R_S. When the output voltage rises such that, $V_{FB} > \left[V_{FB_REG} - \frac{V_{ILIM}}{30 \times G_V} \right]$; V_{REFI}; hence, the charging current (I_{CHG}) proportionately reduces. The charging current for a given output voltage (V_{OUT_SS}) is given by the following equation:

$$I_{CHG} = \left(V_{FB_REG} - V_{OUT_SS} \times \left(\frac{R_{BOT}}{R_{TOP} + R_{BOT}} \right) \right) \times \frac{G_V}{R_S}$$

where,

V_{FB_REG} = FB reference voltage

V_{OUT_SS} = Output voltage

I_{CHG} = Charging current of the charger for a given output voltage

R_{TOP} and R_{BOT} = Output voltage feedback divider resistors

G_V = Voltage loop error amplifier gain (1.30mV/mV)

Deeply discharged batteries can be detected by using the deep-discharge detection comparator with a resistor divider (R_{DDT} and R_{ddb}) connected across the positive and negative battery terminals with the center node connected to the DDTH pin. When V_{DDTH} < 1.25V (V_{DDREF}), the battery is considered to be deeply discharged and the charger enters a precharge state to revive the deeply discharged battery. In precharge state, V_{REFI} is limited to $\frac{V_{ILIM}}{300}$ to limit the charging current to 10% of the CC mode charging current. A safety timer (TMR) sets the maximum allowed charging time in precharge, CC, and CV states to improve system safety.

A NTC sense resistor can be used with MAX17703 to sense battery temperature (TEMP) and charge only within the allowed battery temperature range. The switching frequency of the device can be programmed from 125kHz to

2.2MHz using a resistor at the RT/SYNC pin. RT/SYNC also provides an external clock synchronization feature. Input undervoltage lockout is implemented using the EN/UVLO pin. Two open-drain status outputs (FLG1 and FLG2) indicate the battery charger status. And, the charging current can be monitored using the ISMON pin.

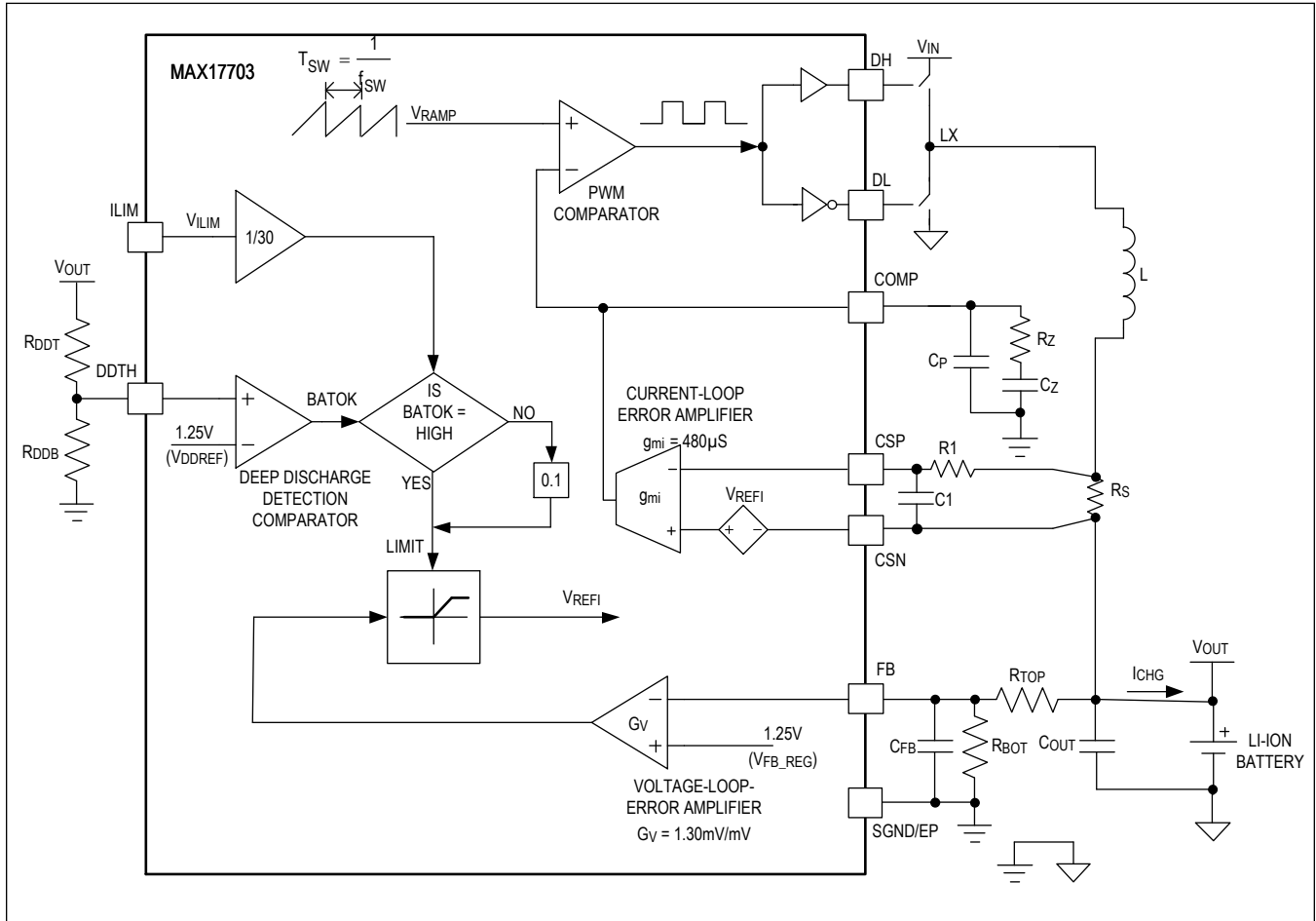


Figure 1. Average Current-Mode Control Loop

Power-Up/Down Sequence and Charger Operation

Figure 2 shows both the MAX17703 power-up/down sequence when the DCIN voltage is applied/removed, and a Li-ion battery charge cycle. Figure 3 shows the Charger-State diagram of the IC. MAX17703 offers precharge, constant-current (CC), constant-voltage (CV), and topup-charge states for charging Li-ion batteries.

When the DCIN voltage reaches a level such that $V_{EN/UVLO}$ is around 0.7V (V_{ENT}), the INT-LDO regulator is enabled and V_{CC} rises. When V_{CC} rises above 4.2V (V_{CC-UVR}) and $V_{EN/UVLO}$ rises above 1.25V ($V_{EN_TH_R}$), the MAX17703 enters a powerup-check state from the charger-off state, initiates EN/UVLO debounce, and checks for hardware faults. If there are no hardware faults detected at power-up (see the [Charger Status Outputs \(FLG1, FLG2\)](#) section), the MAX17703 enables internal blocks during the charger startup delay time (t_{CH_START}).

After the t_{CH_START} delay, the charger enters a full-battery state from the powerup-check state if $V_{FB} > 1.19V$ (V_{RECHG}). The charger initiates LX switching, enters a precharge state from the powerup-check state if $V_{DDTH} < 1.25V$ (V_{DDREF}). The charger enters CC state from the powerup check state if $V_{DDTH} \geq 1.25V$ (V_{DDREF}).

In the precharge state, the charging current reference ($V_{CSPCHG/RS}$) is set to 10% of the CC mode charging current (I_{CHGMAX}) to precondition the battery and revive it from deep discharge. The safety timer counts the charging time in the precharge state and if the output voltage rises above the deep discharge threshold ($V_{DDTH} > 1.26V (V_{DDREF})$) within the precharge-timer timeout (t_{PCHG}), the charger exits the precharge state, resets the safety timer counter, and enters CC state. If the safety timer expires in the precharge state ($t_{TC} > t_{PCHG}$), the charger enters a latched-fault state.

If the timer function is disabled, the charger continues to charge in the precharge state until the output voltage rises above deep discharge rising threshold ($V_{DDTH} > 1.26V (V_{DDREF})$) beyond which the charger enters a CC state.

In the CC state, the safety timer counts the charging time, and the charging current (I_{CHG}) is regulated at the CC mode charging current (I_{CHGMAX}) proportional to V_{ILIM} until the output voltage reaches the CV mode threshold ($V_{FB} > 1.219V (V_{FB_CV})$). When $V_{FB} > 1.219V (V_{FB_CV})$, the charger exits the CC state and enters a CV state without resetting the safety timer counter. If the safety timer expires in the CC state ($t_{TC} > t_{FCHG}$), the charger enters a latched-fault state.

If the timer function is disabled, the charger continues to charge the battery in the CC state until the output voltage reaches the CV mode threshold ($V_{FB} > 1.219V (V_{FB_CV})$) beyond which the charge enters the CV state.

In the CV state, the charging current is a function of the output voltage. The safety timer continues to count charging time in the CV state. If the charging current (I_{CHG}) tapers naturally down to the taper current threshold (I_{TCHG}) within the safety timer timeout ($t_{TC} < t_{FCHG}$), the timer resets, and the charger exits the CV state and enters a topup-charge state. If the safety timer expires in the CV state ($t_{TC} > t_{FCHG}$), the charger enters the latched-fault state.

If the timer function is disabled, the charger continues to charge the battery in CV state until the $I_{CHG} < I_{TCHG}$ is detected. The charger skips the topup-charge state and enters a full-battery state upon detecting $I_{CHG} < I_{TCHG}$ in a CV state.

In the topup-charge state, the charging current is again a function of the output voltage. The safety timer starts counting the charging time in the topup-charge state. The charger exits the topup-charge state and enters a full-battery state when the safety timer in the topup-charge state ($t_{TC} > t_{TOP}$) elapses.

In the full-battery state, the timer stops counting and resets, and the charging is suspended until the $V_{FB} < 1.19V (V_{RECHG})$. When $V_{FB} < 1.19V (V_{RECHG})$, the charger exits the full-battery state, enters CC state, and restarts charging.

In any of the charging states (precharge, CC, CV and topup-charge), if battery operating temperature is detected out of the set range (TEMP Fault condition), the charger enters the respective suspend state (precharge suspend, CC suspend, CV suspend, and topup suspend) and pauses the timer. Upon entering back to an allowed operating temperature range (Exit TEMP Fault condition), the timer resumes, and charging resumes back to the previous state. If the timer function is disabled, the charger enters or exits the charge suspend state based on the battery operating temperature range.

When $V_{EN/UVLO}$ falls below $1.09V (V_{EN_TH_F})$, the MAX17703 initiates a shutdown sequence with a debounce time of 2ms (typ). If the input voltage decreases such that $(V_{IN} - V_{CSN})$ falls below the current-loop-error amplifier undervoltage-lockout falling threshold ($V_{CMUVLO} = 1.95V$), the MAX17703 initiates a shutdown sequence immediately. The converter stops switching, and GATEN is pulled down with $1.1\Omega (R_{GATEN_A})$ to DCIN to turn off the external nMOSFET. The COMP is pulled low after a debounce time of $100\mu s$ (typ).

If $V_{EN/UVLO}$ falls below $0.64V (V_{ENT})$, the MAX17703 initiates a shutdown sequence with a debounce time of $10\mu s$ (typ). During this shutdown sequence, the MAX17703 pulls down the GATEN with $1.1\Omega (R_{GATEN_A})$ to DCIN to turn off the external nMOSFET. See the [Setting the Input Undervoltage-Lockout Level \(EN/UVLO\)](#) section for more details.

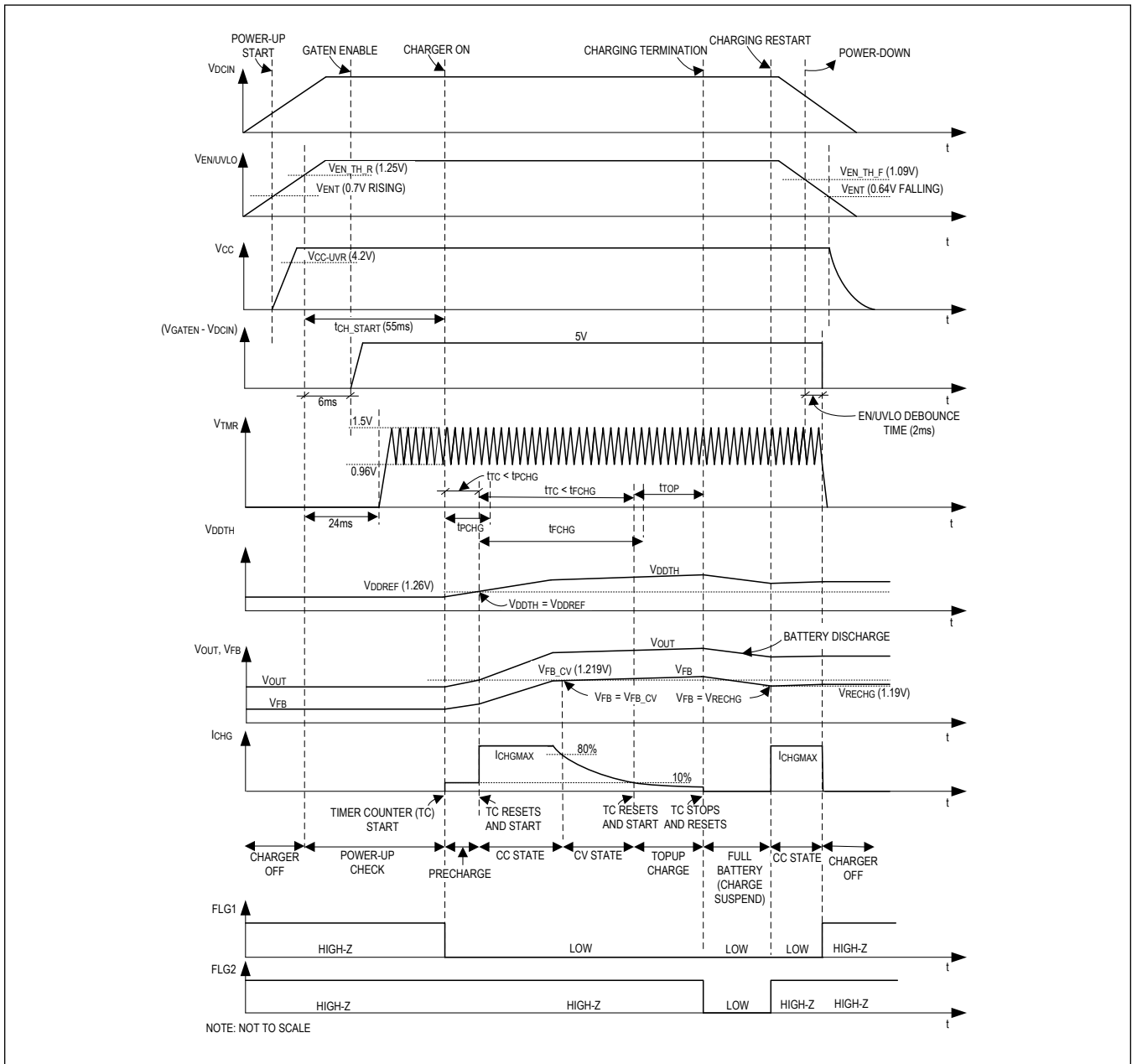


Figure 2. Charger Power-Up/Down Sequence and Li-Ion Battery Charge Cycle

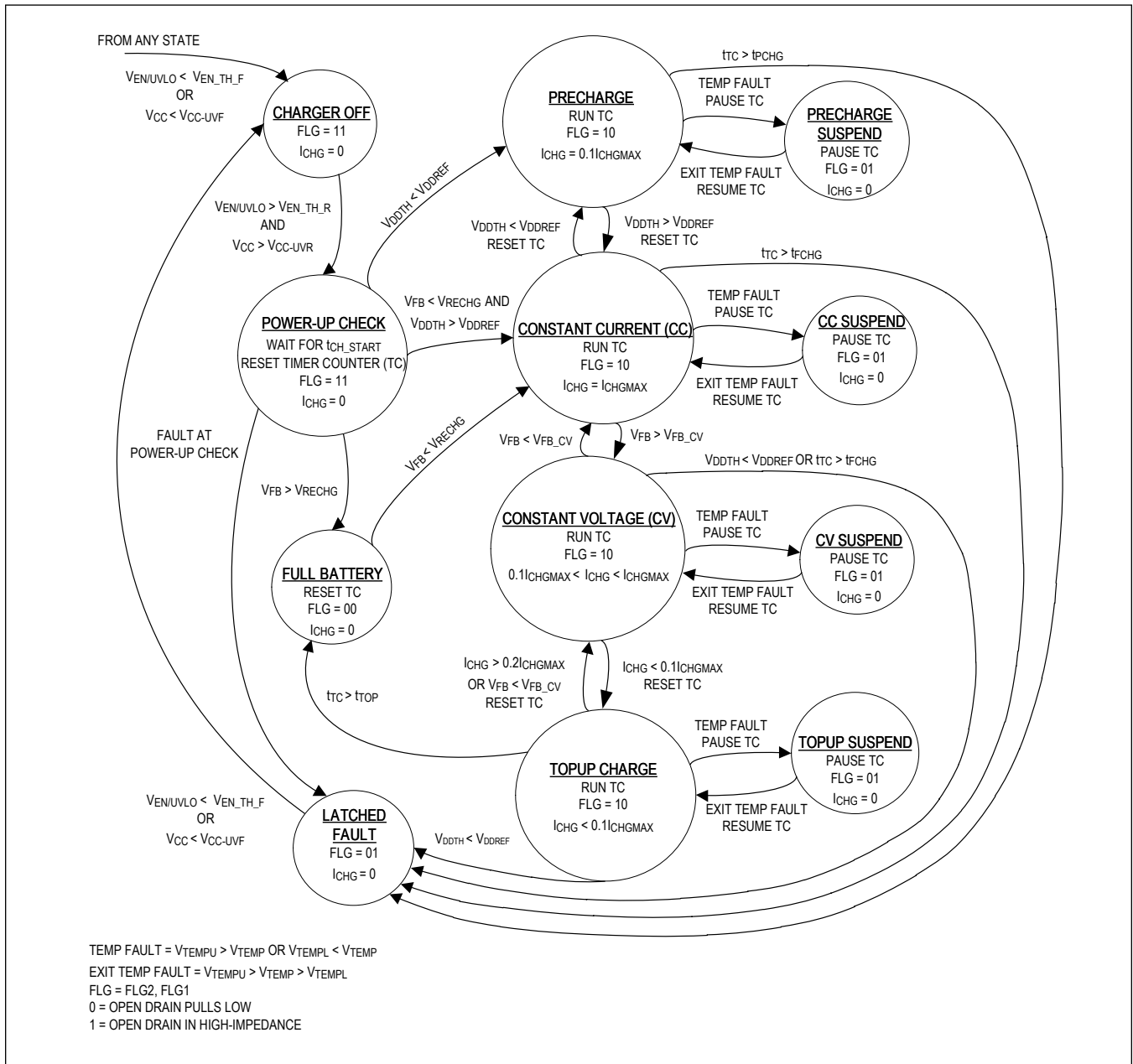


Figure 3. Charger-State Diagram

Input Short-Circuit Protection (GATEN)

The MAX17703 provides a gate drive output (GATEN) that drives a logic-level gate-threshold external nMOSFET, which turns off and prevents battery discharging for input supply short-circuit events. The GATEN is pulled up with 20µA (IGATEN) when VIN is 2.04V (VCMUVLO) above VCSN. If VGATEN does not reach 3.55V (VGATEN_OK) within 15ms (tGATEN_OK), MAX17703 enters a latched-fault state.

Figure 4 depicts the MAX17703 behavior when DCIN is shorted to PGND. When VDCIN is 93mV (VREV) below VIN,

GATEN is pulled down with 1.1Ω (R_{GATEN_A}) and the external nMOSFET is turned off within 100ns (typ). When $V_{EN}/UVLO$ goes below $0.64V$ (V_{ENT}), the MAX17703 shuts down with $10\mu s$ (typ) debounce time. When DCIN-to-PGND short is removed, a power-up sequence is initiated (see the [Power-Up/Down Sequence and Charger Operation](#) section). When the input short-circuit protection is not used, connect a $2.2nF$ capacitor between GATEN and DCIN, and short DCIN to V_{IN} .

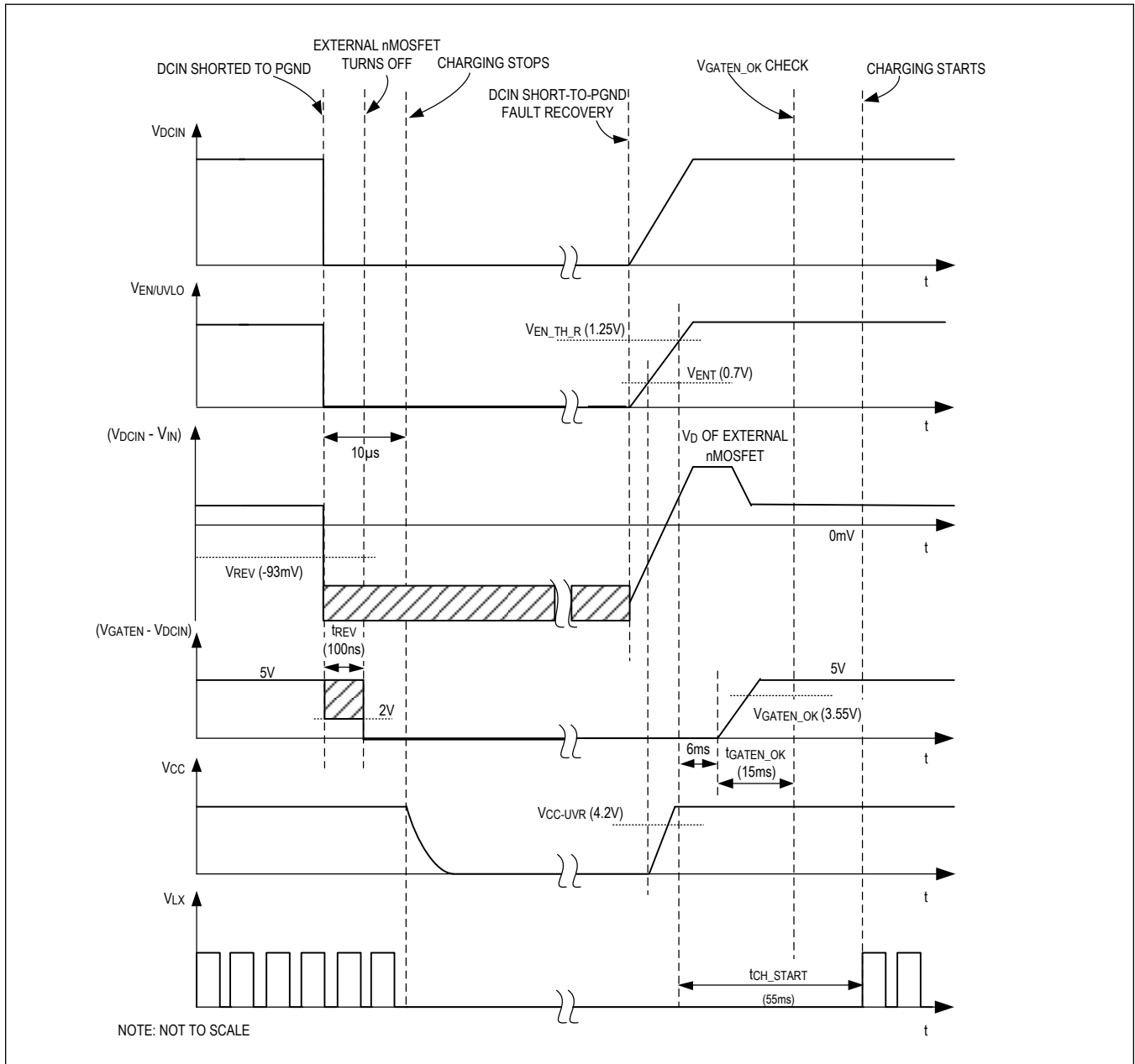


Figure 4. Input Short-Circuit Protection and Recovery Timing Diagram

Charger Timers (TMR)

The MAX17703 offers a programmable timer feature to provide battery charge-cycle control. Connect a capacitor from TMR to SGND/EP to use the timer feature. Connect TMR to V_{REF} to disable the timer feature. The timer counts the charging time in precharge, CC, CV, and topup-charge states.

In the precharge state, if V_{DDTH} does not reach 1.26V (V_{DDREF}) within the precharge timer count (t_{PCHG}), the charger enters a latched-fault state.

In the CC and CV states, if the safety timer count (t_{FCHG}) elapses, the charger enters a latched-fault state.

In the topup-charge state, the charger terminates charging and enters a full-battery state, when the taper-timer count (t_{TOP}) elapses.

[Table 1](#) shows the relative timer counts in different states.

Table 1. Charger Timers

| STATE | TIMER COUNT |
|--------------|--|
| Precharge | t _{PCHG} = t _{FCHG} /8 |
| CC, CV | t _{FCHG} |
| Topup Charge | t _{TOP} = t _{FCHG} /10 |

The MAX17703 supports 2.2nF to 10μF capacitance on the TMR pin, translating to a safety timer timeout period range of 3.6 minutes to 273 hours.

Use the following equation to calculate the C_{TMR} for the required safety timer period in CC and CV states (T_{FCHG}):

$$C_{TMR} \geq 1.15 \times \left(\frac{T_{FCHG}}{2 \times t_{FCHG}} \right) \times \left(\frac{I_{TMR}}{V_{TMR_H} - V_{TMR_L}} \right)$$

where,

T_{FCHG} = Desired safety timer setting in CC and CV states in seconds

C_{TMR} = TMR capacitor in Farad

t_{FCHG} = Number of TMR cycles in CC and CV states (1048575)

V_{TMR_H} = TMR oscillator upper threshold (1.5V)

V_{TMR_L} = TMR oscillator lower threshold (0.96V)

I_{TMR} = TMR pin source/sink current (10μA)

Charger Status Outputs (FLG1, FLG2)

The MAX17703 features two open drain status output pins (FLG1 and FLG2) to indicate the status of the charger. [Table 2](#) shows the status flag summary.

Table 2. Status Output Indications

| CHARGER STATUS FLG (FLG2 and FLG1) | FLG2 | FLG1 | CHARGER STATE |
|------------------------------------|--------------------------------|--------------------------------|--|
| 11 | Open drain in Hi-Impedance (1) | Open drain in Hi-Impedance (1) | Charger Off |
| 10 | Open drain in Hi-Impedance (1) | Open drain pulls low (0) | Charging in progress (precharge, CC, CV, or topup-charge states) |
| 00 | Open drain pulls low (0) | Open drain pulls low (0) | Full-battery state (charging complete) |
| 01 | Open drain pulls low (0) | Open drain in Hi-Impedance (1) | Latched fault or charge suspend due to high- or low-battery-temperature detection* |

*Latched-fault state includes latched hardware faults and faulty battery states. Charge suspended due to high or low battery temperature is not a latched fault. [Table 3](#) provides various fault detection features available and their behaviors in MAX17703.

Table 3. Protection Under System Faults

| FAULT CONDITION | FAULT MONITOR STATE | FAULT BEHAVIOR |
|--|--|--|
| RT/SYNC to SGND/EP short | Power-Up Check | Latched Fault. Need to recycle power to restart the device. |
| GATEN to DCIN short | | |
| TMR unconnected | | |
| TMR to SGND/EP short | | |
| V _{REF} to SGND/EP short | | |
| V _{REF} < 1.95V or V _{REF} > 3.05V | Continuous, During Normal Operation | |
| (V _{GATEN} - V _{DCIN}) < V _{GATEN_OK} | | |
| V _{FB} < 65mV (FB to SGND/EP short or R _{TOP} open fault) | Precharge, CC, and CV States | |
| Faulty battery (timer count in Precharge state t _{TC} > t _{PCHG} , timer count in CC or CV state t _{TC} > t _{FCHG}) | | |
| V _{DDTH} < 1.25V (V _{DDREF}) | CV and Topup-Charge States | |
| High- or low-battery-temperature detection (V _{TEMP} < 1V (V _{TEMPL}) or V _{TEMP} > 1.5V (V _{TEMPU})) | Precharge, CC, CV, Topup-Charge States | Suspend Charge and Pause Timer. Upon entering back to an allowed operating temperature range, the timer resumes, charging resumes back to the previous state |

Linear Regulator (V_{CC} and EXT_{VCC})

The MAX17703 integrates two internal low-dropout (LDO) linear regulators INT-LDO and EXT-LDO that power V_{CC}. V_{CC} powers gate drivers and internal control circuitry. INT-LDO is powered from V_{IN} and turns on when V_{EN/UVLO} > V_{ENT} (0.7V). EXT-LDO is powered from EXT_{VCC}. At any time, only one of these two linear regulators operates, depending on the EXT_{VCC} voltage. If V_{EXTVCC} > 4.7V (typ) then V_{CC} is powered from EXT-LDO. If V_{EXTVCC} < 4.46V(typ), then V_{CC} is powered from INT-LDO. Powering V_{CC} from EXT_{VCC} reduces on-chip power dissipation and increases efficiency at higher input voltages. Connect EXT_{VCC} to V_{OUT} for applications with V_{OUT} ≥ 4.8V. The maximum voltage limit on EXT_{VCC} is 24V. Bypass EXT_{VCC} with a 1μF ceramic capacitor to SGND/EP. Leave EXT_{VCC} open when not used. Bypass V_{CC} to PGND with at least a 4.7μF/0805, low-ESR ceramic capacitor.

Reference Voltage (V_{REF})

The MAX17703 provides a ±1.4% accurate 2.5V reference voltage on the V_{REF} pin. V_{REF} can be used to program V_{ILIM} to set the CC mode charging current (I_{CHGMAX}). V_{REF} can also be used to program TMR and TEMP for disabling the charger timer and setting the battery operating temperature range, respectively. Connect a minimum 0.1μF low-ESR ceramic capacitor between V_{REF} and SGND/EP. See the [CC Mode Charging Current Setting \(ILIM\)](#) and [Setting the Battery Operating Temperature Range \(TEMP\)](#) sections for more details.

Setting the Switching Frequency and External Clock Synchronization (RT/SYNC)

The switching frequency of the device can be programmed from 125kHz to 2.2MHz by using a resistor (R_{RT/SYNC}) connected from the RT/SYNC pin to SGND/EP. R_{RT/SYNC} can be calculated using the following equation:

$$R_{RT/SYNC} = \frac{44830}{f_{SW}} - 1.205$$

Where $R_{RT/SYNC}$ is in $k\Omega$ and f_{SW} is in kHz. Leave the RT/SYNC pin unconnected to operate the device at 350kHz (default) switching frequency.

The MAX17703 can be synchronized to an external clock coupled to the RT/SYNC pin through a 10pF ceramic capacitor. The external clock is detected after checking the rising edge for 112 cycles of the internal clock (set by RT/SYNC). If the external clock frequency is within the allowed SYNC frequency range ($\pm 10\%$ of nominal internal clock frequency), the device stops switching for 2 switching time periods and then restarts with an external clock. When the external clock is removed, the device stops switching for 10 switching time periods and then restarts with the internal clock.

The minimum external-clock pulse width should be greater than 100ns. The off-time duration of the external clock should be at least 100ns.

Peak Current-Limit

The MAX17703 provides a cycle-by-cycle overcurrent protection by limiting the peak current-sense voltage ($V_{CSP} - V_{CSN}$) across the current sense pins. When an overcurrent event ($(V_{CSP} - V_{CSN}) > V_{CS_PEAK}$) is detected, the overcurrent comparator in the MAX17703 terminates the DH pulse and limits the peak current. The overcurrent fault is not latched.

Charging Current Monitoring (ISMON)

The output charge current can be monitored by observing the voltage at the ISMON pin. Connect a 1nF ceramic capacitor on ISMON to filter out the switching frequency component in the ISMON voltage. The charging current is given by the following equation:

$$I_{CHG} = \frac{V_{ISMON}}{30 \times R_S}$$

where,

I_{CHG} = Charging current

V_{ISMON} = Voltage on the ISMON pin

R_S = Current-sense resistance

Thermal-Shutdown Protection

Thermal-shutdown protection limits the junction temperature of the device. When the junction temperature of the device exceeds $+160^\circ\text{C}$, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns on after the junction temperature reduces by 10°C . Carefully evaluate the total power dissipation (see the [Device Power Dissipation](#) section) to avoid unwanted triggering of the thermal shutdown during normal operation.

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), DC resistance (R_{DCR}), and inductor saturation current (I_{SAT}).

The required inductance is calculated based on the inductor current ripple ratio (LIR), i.e., ratio of peak-to-peak ripple current (ΔI_L) to CC mode charging current (I_{CHGMAX}). A good compromise between size and loss is an LIR of 0.3.

The inductance value (L) is given by the higher value of the two calculated inductances:

$$L1 = \frac{V_{OUT} \times (1-D)}{LIR \times I_{CHGMAX} \times f_{SW}}$$

$$L2 = \frac{V_{OUT}}{600000 \times I_{CHGMAX}}$$

where,

V_{OUT} = Desired voltage across the battery

I_{CHGMAX} = CC mode charging current

D = Duty cycle of the converter, V_{OUT}/V_{IN}

V_{IN} = Nominal input voltage

f_{SW} = Switching frequency

Select an inductor that is nearest to the calculated value. The inductor (RMS) current rating should be more than the CC mode charging current. Select a low-loss inductor with acceptable dimensions and the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the overcurrent threshold corresponding to V_{CS_PEAK} .

Output Capacitor Selection

Batteries have significant internal charging resistance and connection resistances (R_{BAT}). The switching ripple component of charger output current flows into R_{BAT} and results in a large output-voltage ripple.

To reduce the voltage ripple across the battery, additional X7R ceramic capacitors and/or low-ESR POSCAP capacitors can be used at the output of the charger. X7R ceramic output capacitors are preferred due to their stability over temperature. For higher values of output capacitance, low-ESR POSCAP capacitors can be used in parallel with ceramic capacitors.

Calculate the required output capacitance (C_{OUT}) based on the following equation:

$$C_{OUT} = \frac{25 \times I_{CHGMAX}}{f_{SW} \times V_{OUT}}$$

where:

I_{CHGMAX} = CC mode charging current setting

f_{SW} = Switching frequency

V_{OUT} = Desired voltage across the battery

Derating of ceramic capacitors with DC-bias voltage must be considered while selecting the capacitors, using the manufacturer data sheet. The selected output capacitor (C_{OUT_SEL}) and its equivalent series resistance (ESR_{COUT}) affect the output voltage ripple (ΔV_{OUT}). Estimate the resultant output-voltage ripple (ΔV_{OUT}) using the following equation:

$$\Delta V_{OUT} \approx \Delta I_L \times \left(ESR_{COUT} + \frac{1}{8 \times f_{SW} \times C_{OUT_SEL}} \right)$$

where ΔI_L is the inductor peak-to-peak ripple current.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the switching converter. Calculate the required input capacitance at V_{IN} (C_{VIN}) using the following

$$\text{equation: } C_{VIN} = \frac{I_{CHGMAX} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

$$D = \frac{V_{OUT}}{V_{IN}} \text{ is the duty ratio of the converter}$$

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input-voltage ripple

η = Efficiency of the converter

I_{CHGMAX} = CC mode charging current

Choose $\Delta V_{IN} \leq 0.5V$ to minimize voltage ripple across the external nMOSFET and to provide robust operation during input short-circuit events.

The input capacitor RMS current (I_{RMS}) is calculated using the following equation:

$$I_{RMS} = I_{CHGMAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Choose low-ESR ceramic input capacitors that exhibit less than a 10°C temperature rise at I_{RMS} for optimal long-term reliability. X7R capacitors are recommended in industrial applications for their temperature stability. Derating of ceramic capacitors with DC-bias voltage must be considered while selecting the capacitors using the manufacturer data sheet.

Choose an electrolytic capacitor at DCIN to prevent the DCIN voltage from being less than -0.3V during input short events. An electrolytic capacitor also provides the damping for potential oscillations caused by inductance of the longer input power path and input ceramic capacitor (C_{VIN}). Additionally, if required, add a Schottky diode at DCIN in parallel with the electrolytic capacitor.

Operating Input-Voltage Range

The following equations are used to calculate the operating input voltage range for a given output voltage and CC mode charging current setting. The minimum operating input voltage on the DCIN pin is given by the higher value from the two calculated voltages:

$$V_{DCIN(MIN1)} = \frac{V_{OUT} + I_{CHGMAX} \times (R_{DS_ON(LS)} + R_{DCR(MAX)})}{1 - (1.05 \times f_{SW} \times (t_{DT_HL} + t_{MIN_ON_DL(MAX)}))} + I_{CHGMAX} \times (R_{DS_ON(HS)} - R_{DS_ON(LS)})$$

$$V_{DCIN(MIN2)} = (V_{OUT} + 2.1V)$$

where:

$V_{DCIN(MIN1)}$, $V_{DCIN(MIN2)}$ = Minimum operating input voltages; the higher of the two values is the minimum operating input voltage, $V_{DCIN(MIN)}$

V_{OUT} = Desired regulation voltage across the battery

I_{CHGMAX} = CC mode charging current setting

f_{SW} = Switching frequency in Hz

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor in Ω

$R_{DS_ON(HS)}$ and $R_{DS_ON(LS)}$ = Worst-case on-state resistances of high-side and low-side internal MOSFETs in Ω ,

respectively

t_{DT_HL} = Dead time (30ns)

$t_{MIN_ON_DL(MAX)}$ = Worst case DL minimum guaranteed on time (100ns)

The maximum operating input voltage on the DCIN pin is calculated as follows:

$$V_{DCIN(MAX)} = \frac{V_{OUT}}{1.05 \times f_{SW} \times t_{MIN_ON_DH(MAX)}}$$

where:

$V_{DCIN(MAX)}$ = Maximum operating input voltage

$t_{MIN_ON_DH(MAX)}$ = Worst case DH minimum guaranteed on time (100ns)

CC Mode Charging Current Setting (ILIM)

The CC mode charge current setting involves setting up a voltage on the ILIM pin (V_{ILIM}) and choice of current sense resistor R_S . Selection of R_S involves a trade-off between power loss and charging current accuracy. The best MAX17703 charging current accuracy is obtained with a voltage drop ($V_{CSP} - V_{CSN}$) of 50mV across R_S . ($V_{CSP} - V_{CSN}$) can be reduced at the expense of charging current accuracy to reduce power loss. The recommended range for voltage across R_S is 30mV ($\pm 6.7\%$ charging current accuracy) to 50mV ($\pm 4\%$ charging current accuracy). R_S can be calculated using the following equation:

$$R_S \leq \frac{(V_{CSP} - V_{CSN})}{I_{CHGMAX}}$$

Once R_S is selected, V_{ILIM} can be calculated using the following equation:

$$V_{ILIM} = 30 \times R_S \times I_{CHGMAX}$$

A resistor divider from V_{REF} to SGND/EP can be used to program V_{ILIM} as shown in [Figure 5](#). The resistor divider values are calculated as follows:

$$R_{LIM1} = 20 \times (V_{REF} - V_{ILIM})k\Omega$$

$$R_{LIM2} = 20 \times V_{ILIM}k\Omega$$

The permitted voltage range for the V_{ILIM} setting is 0.9V to 1.5V. The MAX17703 can be set to the default I_{CHGMAX} setting corresponding to ($V_{CSP} - V_{CSN}$) = 50mV across R_S by connecting ILIM to V_{REF} .

Connect an R-C filter in the current-sense signal path as shown in [Figure 5](#) to attenuate switching noise while preserving accuracy and bandwidth. Select an R-C filter corner frequency at 5 times the switching frequency. The recommended filter resistance ($R1$) is 40 Ω for minimal impact on the current-sense accuracy. Place the filter close to the CSP and CSN pins of the device. Calculate the value of filter capacitor C1 using the following equation:

$$C1 = \frac{1}{2\pi \times R1 \times 5 \times f_{SW}}$$

where f_{SW} = Switching frequency

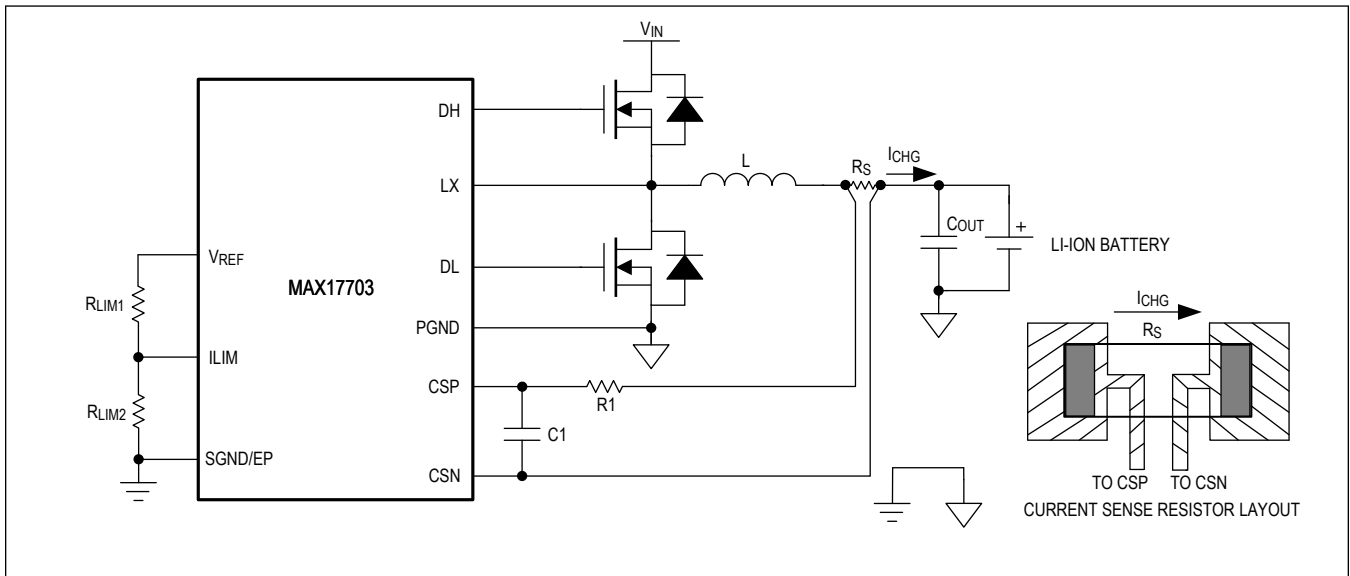


Figure 5. Current-Sense Circuit

Setting the Input Undervoltage-Lockout Level (EN/UVLO)

The MAX17703 offers an adjustable input undervoltage-lockout level using the EN/UVLO pin. Pulling the EN/UVLO pin below 1.09V (typ) stops charger operation. Pulling EN/UVLO below 0.64V (typ) causes the MAX17703 to shut down. In this state, the device draws I_{IN_SH} (7µA) quiescent current. [Figure 6](#) shows the recommended EN/UVLO configuration based on the required input-voltage range. Connect EN/UVLO to the center node of a resistor divider from the DCIN to SGND/EP to set the input voltage at which the device turns on. Choose R1 as follows:

$$R1 \leq (10000 \times V_{DCIN(MIN)})$$

where $V_{DCIN(MIN)}$ is the voltage at which the device is required to turn on.

Calculate the value of R2 using the following equation:

$$R2 = \frac{V_{EN_TH_R} \times R1}{(V_{DCIN(MIN)} - V_{EN_TH_R} + (I_{EN_BIAS} \times R1))}$$

where:

I_{EN_BIAS} = Internal bias pullup current on the EN/ULVO pin

$V_{EN_TH_R}$ = EN/UVLO rising threshold voltage (1.25V)

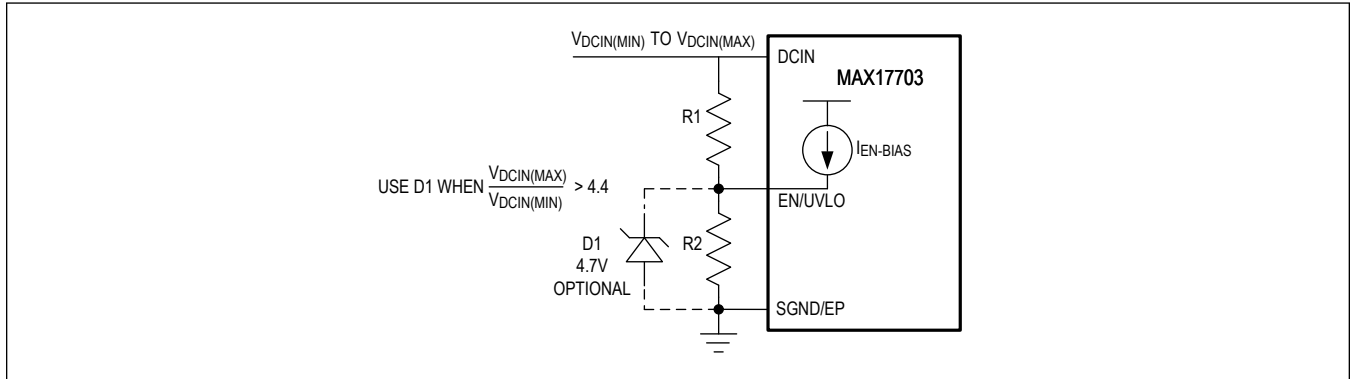


Figure 6. Setting the Input Undervoltage-Lockout

Current-Regulation Loop Compensation (COMP)

The MAX17703 features a COMP pin to tune the current loop to control performance of the average current-mode controller. Refer to [Figure 1](#) for a depiction of the compensation network on the COMP pin using R_Z , C_Z , and C_P . The choice of the compensation component values depends on the chosen inductor (L) and its DC resistance (R_{DCR}), switching frequency (f_{SW}), current sense resistor (R_S), maximum operating input voltage ($V_{DCIN(MAX)}$), the desired regulation voltage across the battery (V_{OUT}), battery charging resistance (R_{BAT}), and the on-resistances of the step-down converter nMOSFETs ($R_{DS_ON(HS)}$ and $R_{DS_ON(LS)}$).

Calculate the compensation resistor R_Z using the following equation:

$$R_Z = \frac{3000 \times L \times f_{SW}}{V_{DCIN(MAX)} \times R_S}$$

Calculate the compensation capacitor C_Z using the following equation:

$$C_Z = \frac{0.8 \times L}{R_Z \times R_E}$$

where,

$$R_E = [R_{DCR} + R_S + R_{DS_ON(HS)} \times D_{MIN} + R_{DS_ON(LS)} \times (1 - D_{MIN}) + R_{BAT}]$$

$$D_{MIN} = \frac{V_{OUT}}{V_{DCIN(MAX)}}$$

Calculate the high-frequency pole capacitor (C_P) using the following equation:

$$C_P = \frac{0.35}{R_Z \times f_{SW}}$$

Setting Output Voltage and Voltage Regulation Loop (FB)

The MAX17703 features a FB pin to regulate the voltage across the battery to a desired level. Connect a feedback resistor divider (R_{TOP} and R_{BOT}) with a compensating capacitor (C_{FB}) as depicted in [Figure 1](#). The choice of feedback components depends on the desired regulation voltage across the battery (V_{OUT}), the chosen switching frequency (f_{SW}), and the operating input-voltage range ($V_{DCIN(MAX)}$ and $V_{DCIN(MIN)}$).

Calculate R_{TOP} and R_{BOT} using the following equations:

$$R_{TOP} = 10 \times V_{OUT} \text{ k}\Omega$$

$$R_{\text{BOT}} = \frac{R_{\text{TOP}}}{\left(\frac{V_{\text{OUT}}}{V_{\text{FB_REG}}} - 1\right)} \text{ k}\Omega$$

where $V_{\text{FB_REG}}$ is the FB reference voltage.

Calculate C_{FB} using the following equation:

$$C_{\text{FB}} = \frac{5}{R_{\text{PAR}} \times f_{\text{SW}}} \times \frac{V_{\text{DCIN(MAX)}}}{V_{\text{DCIN(MIN)}}$$

where,

$$R_{\text{par}} = \frac{R_{\text{TOP}} \times R_{\text{BOT}}}{R_{\text{TOP}} + R_{\text{BOT}}} \text{ in } \Omega.$$

Setting Battery Deep-Discharge Voltage Level (DDTH)

The MAX17703 offers a battery deep-discharge state detection mechanism through the DDTH pin. During power-up the device enters a precharge state when the voltage at the DDTH pin (V_{DDTH}) is less than 1.25V (V_{DDREF}). The device transitions into a CC state when V_{DDTH} exceeds V_{DDREF} . The deep-discharge voltage sense level of a battery can be set by connecting DDTH to the center node of a resistor-divider from output to SGND/EP as shown in [Figure 1](#). Connect DDTH to V_{REF} when not used.

Select R_{DDT} in the range of 50k Ω to 100k Ω .

Calculate resistor R_{DDB} from the following equation:

$$R_{\text{DDB}} = \frac{R_{\text{DDT}}}{\left(\frac{V_{\text{OUTDD}}}{V_{\text{DDREF}}} - 1\right)}$$

where,

V_{OUTDD} = Deep-discharge level of the battery

V_{DDREF} = Deep-discharge detection comparator threshold (1.25V)

Setting the Battery Operating Temperature Range (TEMP)

The MAX17703 features a TEMP pin for battery temperature sensing and suspends charging when the temperature is out of the programmed operating temperature range using a negative temperature coefficient (NTC) resistor. Connect an NTC resistor to the TEMP pin along with a resistor divider from V_{REF} to SGND/EP as shown in [Figure 7](#). A 47k Ω NTC resistor with B-constant (25°C - 85°C) = 4108 is recommended. Calculate R_{TEMP1} and R_{TEMP2} using the following equations:

$$R_{\text{TEMP1}} = \frac{1.25 \times R_{\text{NTCCOLD}} \times R_{\text{NTCHOT}}}{(R_{\text{NTCCOLD}} - 2.25 \times R_{\text{NTCHOT}})}$$

$$R_{\text{TEMP2}} = \frac{0.67 \times R_{\text{NTCCOLD}} \times R_{\text{TEMP1}}}{(R_{\text{NTCCOLD}} + R_{\text{TEMP1}})}$$

Where R_{NTCCOLD} is the resistance value of the selected NTC resistor at a low battery-operating temperature limit and R_{NTCHOT} is the resistance value of the selected NTC resistor at a high battery-operating temperature limit.

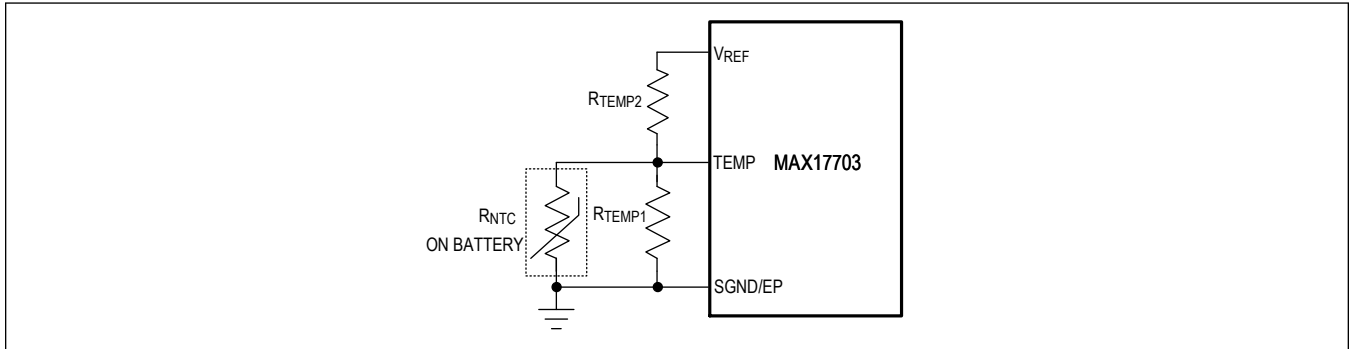


Figure 7. Setting the Battery Operating Temperature Range

Bootstrap Capacitor Selection

The bootstrap capacitance (C_{BST}) value is determined by the selection of the high-side nMOSFET(s). Choose C_{BST} using the following equation:

$$C_{BST} \geq \frac{\Delta Q_G}{\Delta V_{BST}}$$

where:

ΔQ_G = Total gate charge of the high-side nMOSFET(s)

ΔV_{BST} = Voltage variation allowed on the high-side nMOSFET(s) driver after turn-on

Choose $\Delta V_{BST} \leq 100\text{mV}$ to select C_{BST} . The bootstrap capacitor should be a low-ESR ceramic capacitor. A minimum value of $0.1\mu\text{F}$ is recommended.

Bootstrap Diode Selection

Select a Schottky diode with the following ratings:

- Reverse voltage rating \geq (Maximum input operating voltage + 10V)
- Average forward current rating $\geq 1\text{A}$

Choose a diode with low forward voltage drop and low reverse leakage current across the operating temperature range.

Input Short-Circuit Protection External nMOSFET Selection

The MAX17703 is designed to control an external logic-level nMOSFET that turns off in less than 100ns and isolates the V_{IN} node from input short-circuit events. This feature prevents discharge of the battery into the input during input short-circuit events. The external nMOSFET used for this feature only turns on once during power-up and turns off during shutdown and, therefore, does not need to be optimized for switching performance. Select an external nMOSFET with low R_{DS-ON} for low forward path conduction losses. The MAX17703 supports external nMOSFETs with gate charge up to 250nC at $V_{GS} = 3.9\text{V}$. Using larger gate charge values results in a gate charging time larger than t_{GATEN_OK} (15ms typ) and causes the MAX17703 to enter a latched-fault condition.

Step-Down Converter nMOSFET Selection

The MAX17703 drives two external logic-level nMOSFETs to implement the step-down converter high-side and low-side switches. These nMOSFETs must be logic-level compatible with guaranteed on-resistance specifications provided at $V_{GS} = 4.5\text{V}$. The key selection parameters to choose these MOSFETs include:

- On-resistance (R_{DS-ON})
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Miller Plateau voltage on the nMOSFET Gate (V_{MIL})

- Total gate charge (Q_G)
- Output capacitance (C_{OSS})
- Power-dissipation rating and package thermal resistance
- Maximum operating junction temperature

For the step-down converter, nMOSFETs should be chosen in such a way that the switching losses and conduction losses are balanced and optimized. The duty cycles for the high-side and low-side external nMOSFETs can be calculated as follows:

$$D = \frac{V_{OUT}}{V_{IN}}$$

High-side nMOSFET duty cycle: D

Low-side nMOSFET duty cycle: $1 - D$

High-side nMOSFET losses can be estimated using the following formula:

$$P_{HS-MOSFET} = P_{HS-MOSFET_CONDUCTION} + P_{HS-MOSFET_SWITCHING}$$

$$P_{HS-MOSFET_CONDUCTION} = I_{CHG}^2 \times R_{DS-ON(HS)} \times D$$

$$P_{HS-MOSFET_SWITCHING} = f_{SW} \times \left(\left[\frac{V_{IN} \times I_{CHG}}{2} \times \frac{Q_{SW} \times R_{DR}}{V_{CC} - V_{MIL}} \right] + [V_{IN} \times Q_{rr}] + \left[\frac{1}{2} \times C_{OSSHS} \times V_{IN}^2 \right] + \left[\frac{1}{2} \times C_{OSSLS} \times V_{IN}^2 \right] \right)$$

where,

f_{SW} = Switching frequency

I_{CHG} = Charging current

Q_{SW} = Switching charge of the high-side nMOSFET from the nMOSFET data sheet,

R_{DR} = Sum of the DH pin driver pullup resistance and the high-side nMOSFET internal gate resistance,

V_{MIL} = V_{GS} of the high-side nMOSFET that corresponds to $I_D = I_{CHGMAX}$ on the V_{GS} vs. I_D curve in the nMOSFET data sheet

Q_{rr} = Reverse-recovery charge of low-side nMOSFET(s) body diode

C_{OSSHS} = Effective output capacitance of the high-side nMOSFET(s)

C_{OSSLS} = Effective output capacitance of the low-side nMOSFET(s)

Low-side nMOSFET losses can be estimated using the following formula:

$$P_{LS-MOSFET} = I_{CHG}^2 \times R_{DS-ON(LS)} \times (1 - D) + V_D \times I_{CHG} \times t_{DT} \times f_{SW} \times 2$$

where,

V_D = Forward-drop of the low-side nMOSFET(s) body diode

t_{DT} = Dead time (30ns)

Take R_{DS-ON} variation with respect to temperature into account while calculating the power losses and ensure that the losses of each nMOSFET do not exceed their power rating and operate within a safe junction temperature rating. When parallel nMOSFETs are used, it is recommended to use appropriate independent series gate resistors for each nMOSFET to account for gate charge variation from one nMOSFET to another.

System Considerations

The MAX17703 is designed to charge Li-ion batteries. When load current is drawn during the battery charging process, the charging current available for battery charging reduces. This influences the overall charging time period in CC and CV states. The safety timer period (T_{FCHG}) must be adjusted accordingly. Disable the timer function to charge the Li-ion batteries with parallel system load current equal to or greater than taper current threshold (I_{TCHG}), to avoid undesired latched-fault in CC or CV states.

For safe operation, follow the procedure below while making connections:

1. Connect the battery terminals to the output of the charger circuit. Note that the output capacitors of the charger can

draw current from the battery during a hot plug-in/connection process.

2. Connect the input power source to the battery charger circuit only after securely connecting the battery at the output.
3. Do not operate the charger without battery.

Device Power Dissipation

The MAX17703 must dissipate losses due to quiescent-current consumption and the internal gate driver.

If V_{CC} is powered from V_{IN} , use the following equation to calculate the approximate IC losses:

$$P_{MAX17703} = V_{IN} \times [(Q_G \times f_{SW}) + I_{QNS}]$$

When V_{OUT} is used to power V_{CC} by connecting the EXT V_{CC} pin to an output voltage greater than 4.8V, use the following equation to calculate the approximate IC losses:

$$P_{MAX17703} = V_{EXTVCC} \times [(Q_G \times f_{SW}) + I_{QNS}]$$

where,

Q_G = Total gate charge of high-side and low-side nMOSFETs,

I_{QNS} = Input Quiescent current (2.1mA)

Calculate the junction temperature using the following equation and ensure that it does not exceed +125°C.

$$T_J = T_{A(MAX)} + (\theta_{JA} \times P_{MAX17703})$$

where,

T_J = Junction temperature

$P_{MAX17703}$ = Power loss in the device

θ_{JA} = Junction-to-ambient thermal resistance

$T_{A(MAX)}$ = Maximum ambient temperature

PCB Layout Guidelines

Careful PCB layout is critical to achieve low losses, and low EMI emissions. Use the following guidelines for PCB layout:

- Place ceramic input filter capacitors as close as possible across the drain of the high-side nMOSFET and source of the low-side nMOSFET.
- Route the V_{IN} and DCIN traces from input short-circuit protection nMOSFET source and drain terminals as a differential pair and connect to V_{IN} and DCIN pins of the device. Place V_{IN} and DCIN bypass capacitors close to V_{IN} and DCIN pins respectively.
- Place V_{CC} and EXT V_{CC} bypass capacitors and the BST capacitor near the respective pins.
- Place GATEN-to-DCIN bypass capacitor close to the GATEN, DCIN pins of the device.
- Place bootstrap capacitor close to BST, LX pins of the device.
- Route the bootstrap diode connections from V_{CC} capacitor and to bootstrap capacitor as short as possible to minimize the loop inductance.
- Route switching traces (BST, LX, DH, and DL) away from sensitive signal traces (RT/SYNC, COMP, CSP, CSN, and FB).
- The gate current traces must be short in length. Use multiple vias to route these signals if routed from one layer of the PCB to another layer.
- Route current-sense traces as a differential pair to minimize the loop inductance and avoid differential noise.
- Place the current-sense filter resistor and capacitor near both the CSP and CSN pins.
- Place feedback and compensation components close to the device and connect to the SGND/EP copper area.
- Place all power components on the top side of the board and run the power-stage currents using traces or copper fills on the top side only, without adding vias, wherever possible.
- Keep the power traces and load connections short. Use multilayer, thick copper PCBs (2oz or higher) to enhance efficiency and minimize trace inductance and resistance.

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4.5V to 60V, Synchronous Step-Down Li-Ion Battery Charger Controller

- Allocate a large PGND copper area for the output node, and connect the return terminals of the input filter capacitors, output capacitors, and the source terminals of the low-side nMOSFET(s) to that area.
- Refer to the MAX17703 EV kit data sheet for recommended PCB layout and routing.

Typical Application Circuit

10A Li-Ion Battery Charger

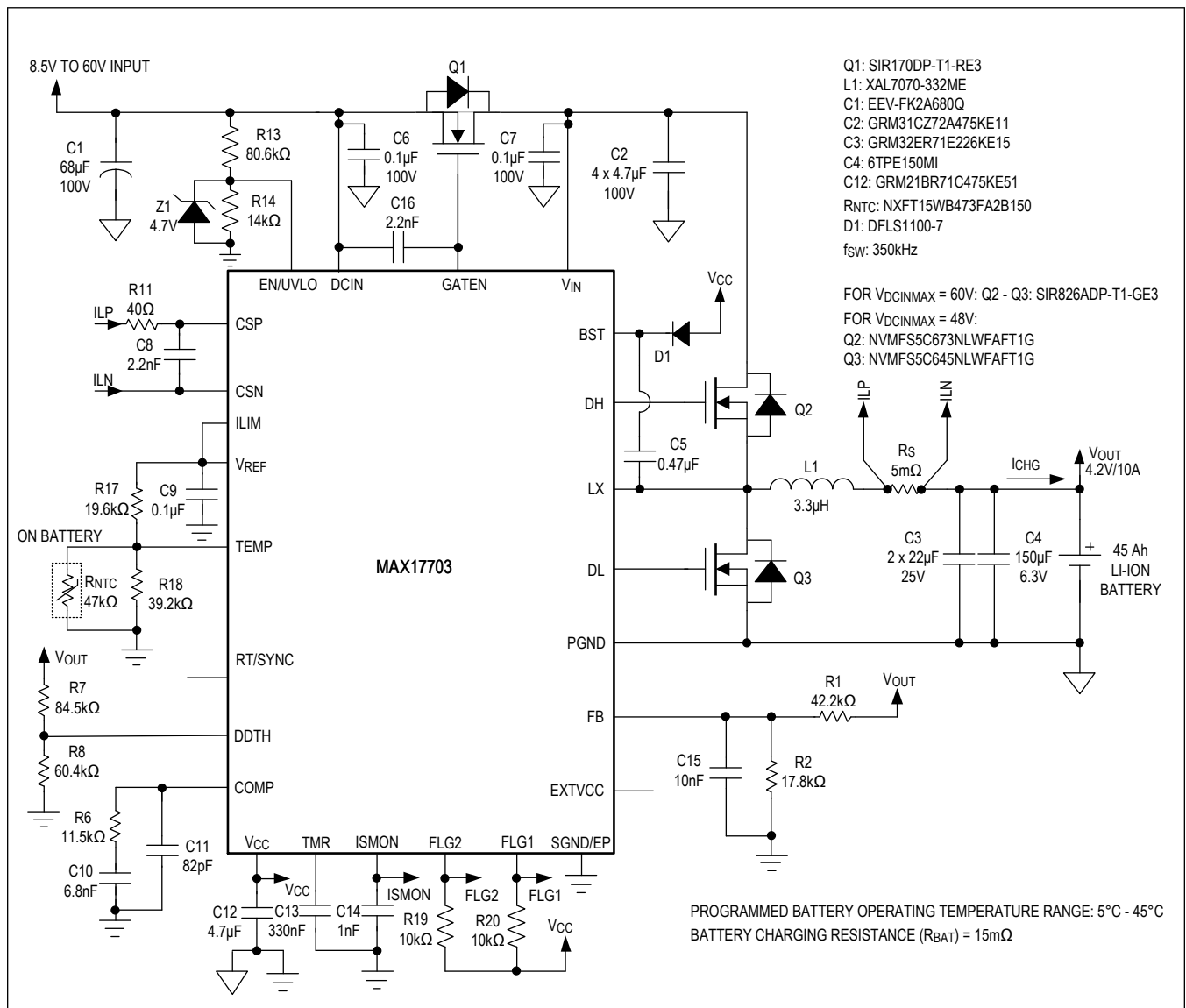


Figure 8. 4.2V/10A Li-Ion Battery Charger

MAX17703

4.5V to 60V, Synchronous Step-Down
Li-Ion Battery Charger Controller

Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PIN-PACKAGE |
|---------------|-------------------|-------------|
| MAX17703ATG+ | -40°C to +125°C | 24 TQFN-EP |
| MAX17703ATG+T | -40°C to +125°C | 24 TQFN-EP |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

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4.5V to 60V, Synchronous Step-Down
Li-Ion Battery Charger Controller

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--------------------------|---------------|
| 0 | 4/21 | Release for Market Intro | — |

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