

## General Description

The MAX17761, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 76V input. The converter can deliver up to 1A current. Output voltage is programmable from 0.8V up to 90% of  $V_{IN}$ . The feedback voltage regulation accuracy over  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  is  $\pm 1.5\%$ .

The device features a peak-current-mode control architecture and can be operated in either the pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes.

The MAX17761 is available in a 12-pin (3mm x 3mm) TDFN package. Simulation models are available.

## Applications

- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Basestation Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems

[Ordering Information](#) appears at end of data sheet.

## Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky—Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 76V Input
  - Output Adjustable from 0.8V up to 90% of  $V_{IN}$
  - Delivers up to 1A Over Temperature
  - 200kHz to 600kHz Adjustable Frequency with External Clock Synchronization
  - Programmable Current Limit
- Reduces Power Dissipation
  - Peak Efficiency > 90%
  - PFM Mode Enables Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - 5 $\mu\text{A}$  Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Adjustable Soft-Start and Prebiased Power-Up
  - Built-in Output-Voltage Monitoring with RESET
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - High Industrial  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range/ $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  Junction Temperature Range

### Absolute Maximum Ratings

$V_{IN}$ to SGND .....	-0.3V to +80V	Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )
EN/UVLO to SGND .....	-0.3V to +26V	(derate 24.4mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$ )
EXTVCC to SGND .....	-0.3V to +26V	(Multilayer board).....
LX to PGND.....	-0.3V to ( $V_{IN} + 0.3\text{V}$ )	1951.2mW
FB, RESET, SS, MODE/ILIM, $V_{CC}$ , RT/SYNC to SGND .....	-0.3V to +6V	Output Short-Circuit Duration .....
PGND to SGND.....	-0.3V to +0.3V	Continuous
LX Total RMS Current .....	$\pm 1.6\text{A}$	Operating Temperature Range (Note 1).....
		-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
		Junction Temperature.....
		+150 $^\circ\text{C}$
		Storage Temperature Range.....
		-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
		Lead Temperature (soldering, 10s) .....
		+300 $^\circ\text{C}$
		Soldering Temperature (reflow).....
		+260 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Junction temperature greater than +125 $^\circ\text{C}$  degrades operating lifetimes.

### Package Information

<b>PACKAGE TYPE: 12 TDFN</b>	
Package Code	TD1233+1C
Outline Number	<a href="#">21-0664</a>
Land Pattern Number	<a href="#">90-0397</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction to Ambient ( $\theta_{JA}$ )	41 $^\circ\text{C}/\text{W}$
Junction to Case ( $\theta_{JC}$ )	8.5 $^\circ\text{C}/\text{W}$

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### Electrical Characteristics

( $V_{IN} = 24\text{V}$ ,  $V_{EN}/UVLO = \text{unconnected}$ ,  $R_{RT} = 105\text{k}\Omega$  ( $f_{SW} = 400\text{kHz}$ ), LX = unconnected,  $T_A = -40^\circ\text{C}$  to +125 $^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ . All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT SUPPLY (<math>V_{IN}</math>)</b>						
Input Voltage Range	$V_{IN}$		4.5		76	V
Input Shutdown Current	$I_{IN-SH}$	$V_{EN} = 0\text{V}$ , shutdown mode	2.5	5	10	$\mu\text{A}$
Input Quiescent Current	$I_{Q\_PFM}$	$R_{ILIM} = \text{open or } 422\text{k}\Omega$		195		$\mu\text{A}$
	$I_{Q\_PWM}$	$R_{ILIM} = 243\text{k}\Omega \text{ or } 121\text{k}\Omega$	3	4	5	mA
<b>ENABLE/UVLO (EN)</b>						
EN Threshold	$V_{ENR}$	$V_{EN}/UVLO$ rising	1.19	1.215	1.24	V
	$V_{ENF}$	$V_{EN}/UVLO$ falling	1.09	1.115	1.14	
	$V_{EN-TRUESD}$	$V_{EN}/UVLO$ falling, true shutdown		0.7		
EN Pullup Current	$I_{EN}$	$V_{EN}/UVLO = 1.215\text{V}$	2.2	2.5	2.8	$\mu\text{A}$

**Electrical Characteristics (continued)**

( $V_{IN} = 24V$ ,  $V_{EN/UVLO} = \text{unconnected}$ ,  $R_{RT} = 105k\Omega$  ( $f_{SW} = 400kHz$ ),  $LX = \text{unconnected}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LDO (V<sub>CC</sub>)</b>						
V <sub>CC</sub> Output Voltage Range	V <sub>CC</sub>	6V < V <sub>IN</sub> < 76V, 0mA < I <sub>VCC</sub> < 5mA	4.75	5	5.25	V
V <sub>CC</sub> Current Limit	I <sub>VCC-MAX</sub>	V <sub>CC</sub> = 4.3V, V <sub>IN</sub> = 12V	13	26	52	mA
V <sub>CC</sub> Dropout	V <sub>CC-DO</sub>	V <sub>IN</sub> = 4.5V, I <sub>VCC</sub> = 5mA			0.25	V
V <sub>CC</sub> UVLO	V <sub>CC-UVR</sub>	V <sub>CC</sub> rising	4.05	4.2	4.35	V
	V <sub>CC-UVF</sub>	V <sub>CC</sub> falling	3.65	3.8	3.95	V
<b>EXT LDO</b>						
EXTVCC Switchover Threshold		EXTVCC rising	4.65	4.744	4.85	V
EXTVCC Switchover Threshold Hysteresis				0.3		V
EXTVCC Dropout	EXTVCC-DO	EXTVCC = 4.75V, I <sub>VCC</sub> = 5mA			0.1	V
EXTVCC Current Limit	I <sub>VCC-MAX</sub>	V <sub>CC</sub> = 4.3V, EXTVCC = 5V	15	21	34	mA
<b>POWER MOSFETs</b>						
High-Side pMOS On-Resistance	R <sub>DS-ONH</sub>	I <sub>LX</sub> = 0.3A, sourcing		0.9	1.8	Ω
Low-Side nMOS On-Resistance	R <sub>DS-ONL</sub>	I <sub>LX</sub> = 0.3A, sinking		0.275	0.55	Ω
LX Leakage Current	I <sub>LX-LKG</sub>	V <sub>IN</sub> = 76V, T <sub>A</sub> = +25°C, V <sub>LX</sub> = (V <sub>PGND</sub> + 1V) to (V <sub>IN</sub> - 1V)	-1		+1	μA
<b>SOFT-START</b>						
Charging Current	I <sub>SS</sub>		4.7	5	5.3	μA
<b>FEEDBACK (FB)</b>						
FB Regulation Voltage	V <sub>FB-REG</sub>	R <sub>ILIM</sub> = 243kΩ or 121kΩ	0.788	0.8	0.812	V
FB Regulation Voltage	V <sub>FB-REG</sub>	R <sub>ILIM</sub> = open or 422kΩ	0.788	0.812	0.824	V
FB Input Leakage Current	I <sub>FB</sub>	V <sub>FB</sub> = 1V, T <sub>A</sub> = +25°C	-100		+100	nA
<b>CURRENT LIMIT</b>						
Peak Current-Limit Threshold	I <sub>SOURCE-LIMIT</sub>	R <sub>ILIM</sub> = open or R <sub>ILIM</sub> = 243KΩ	1.41	1.6	1.83	A
		R <sub>ILIM</sub> = 121kΩ or R <sub>ILIM</sub> = 422kΩ	0.94	1.14	1.3	A
Negative Current-Limit Threshold	I <sub>SINK-LIMIT</sub>	R <sub>ILIM</sub> = open or R <sub>ILIM</sub> = 422kΩ		2.5		mA
		R <sub>ILIM</sub> = 243kΩ	0.57	0.65	0.725	A
		R <sub>ILIM</sub> = 121kΩ	0.35	0.455	0.56	A
PFM Current Level	IPFM	R <sub>ILIM</sub> = open	0.235	0.33	0.44	A
		R <sub>ILIM</sub> = 422kΩ	0.125	0.23	0.32	A

**Electrical Characteristics (continued)**

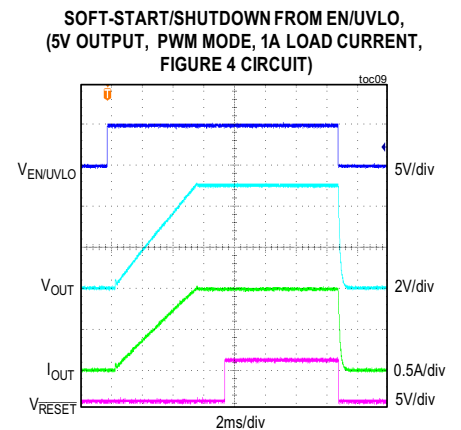
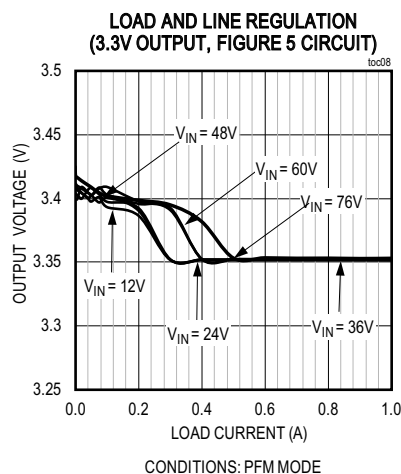
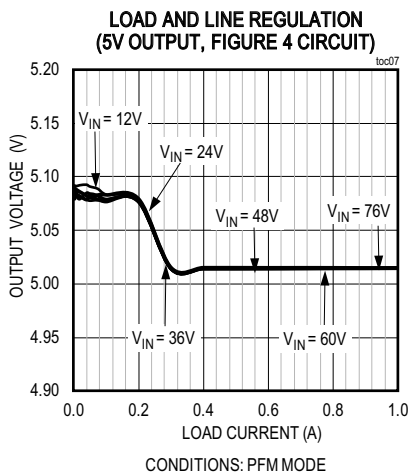
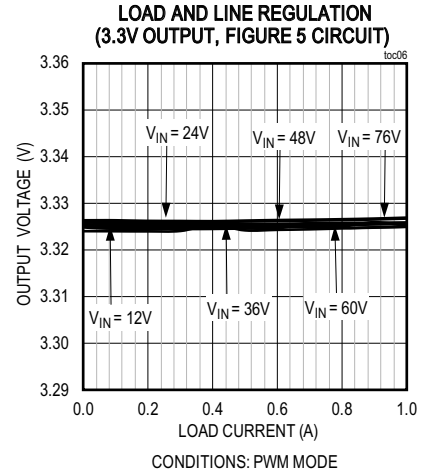
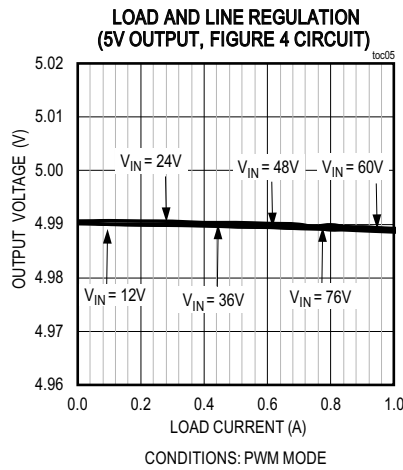
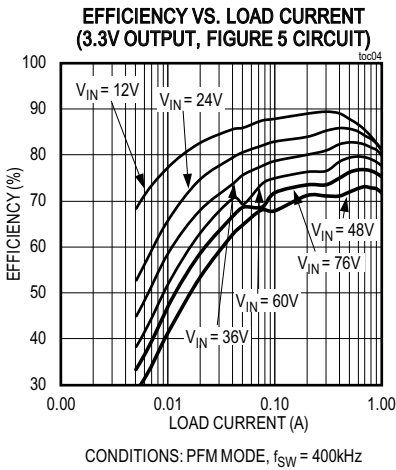
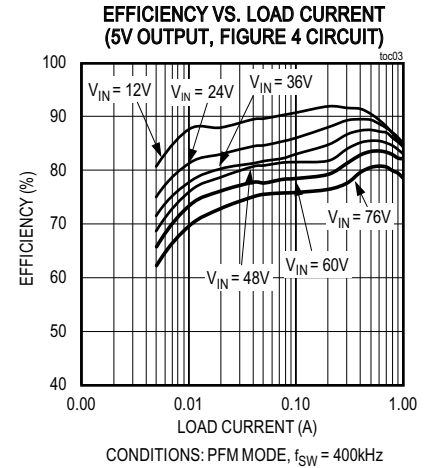
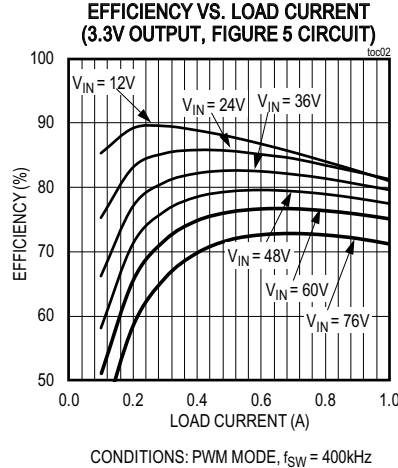
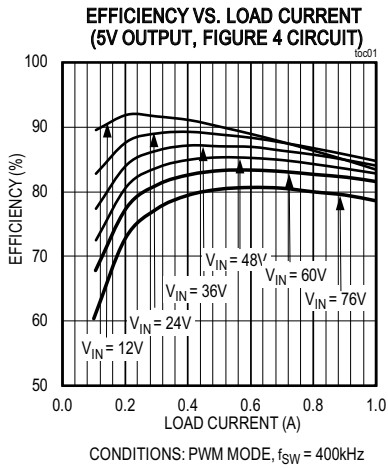
( $V_{IN} = 24V$ ,  $V_{EN/UVLO} = \text{unconnected}$ ,  $R_{RT} = 105k\Omega$  ( $f_{SW} = 400kHz$ ),  $LX = \text{unconnected}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>MODE</b>						
MODE PFM Threshold		Rising	1	1.22	1.44	V
Hysteresis				0.19		V
<b>TIMINGS</b>						
Minimum On-Time	$t_{ON-MIN}$		45	70	110	ns
Maximum Duty Cycle	$D_{MAX}$		90	93	97	%
<b>OSCILLATOR</b>						
Switching Frequency	$f_{SW}$	$R_{RT} = 210k\Omega$	180	200	220	kHz
		$R_{RT} = 140k\Omega$	270	300	330	kHz
		$R_{RT} = 105k\Omega$	360	400	440	kHz
		$R_{RT} = 69.8k\Omega$	540	600	660	kHz
Switching Frequency Adjustable Range			200		600	kHz
SYNC Input Frequency			$1.15 \times f_{SW}$		$1.4 \times f_{SW}$	kHz
SYNC Pulse Minimum Off time			40			ns
SYNC High Threshold	$V_{SYNC-H}$		1	1.22	1.44	V
Hysteresis	$V_{SYNC-HYS}$			0.18		V
Number of SYNC Pulses to Enable Synchronization				1		Cycles
<b>RESET</b>						
FB Threshold for $\overline{RESET}$ Rising	$V_{FB-OKR}$	$V_{FB}$ rising		95		%
FB Threshold for $\overline{RESET}$ Falling	$V_{FB-OKF}$	$V_{FB}$ falling		92		%
$\overline{RESET}$ Delay After FB Reaches 95% Regulation				2.1		ms
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}} = 1mA$			0.07	V
$\overline{RESET}$ Output Leakage Current		$V_{FB} = 1.063 \times V_{FB-REG}$ , $T_A = +25^\circ C$			1	$\mu A$
<b>THERMAL SHUTDOWN</b>						
Thermal-Shutdown Threshold		Temperature rising		160		$^\circ C$
Thermal-Shutdown Hysteresis				20		$^\circ C$

**Note 2:** Electrical specifications are production tested at  $T_A = +25^\circ C$ . Specifications over the entire operating temperature range are guaranteed by design and characterization.

Typical Operating Characteristics

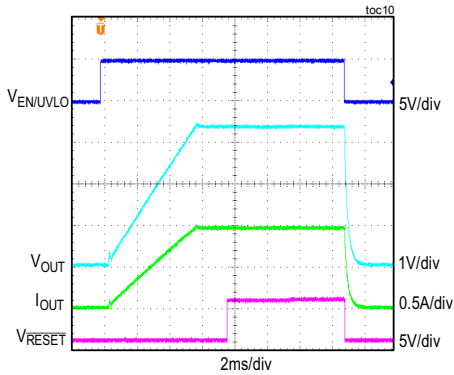
( $V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{VIN} = 2.2\mu F$ ,  $C_{VCC} = 1\mu F$ ,  $V_{EN/UVLO} = \text{Open}$ ,  $C_{SS} = 33nF$ ,  $\text{MODE/ILIM} = \text{unconnected}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted.)



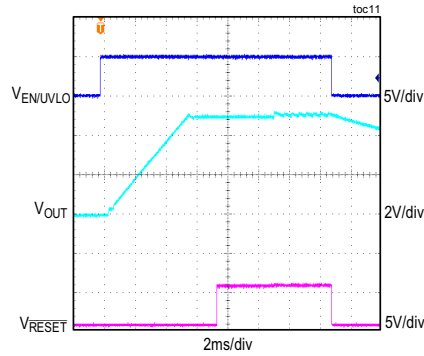
**Typical Operating Characteristics (continued)**

( $V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{VIN} = 2.2\mu F$ ,  $C_{VCC} = 1\mu F$ ,  $V_{EN/UVLO} = \text{Open}$ ,  $C_{SS} = 33nF$ ,  $\text{MODE/ILIM} = \text{unconnected}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted.)

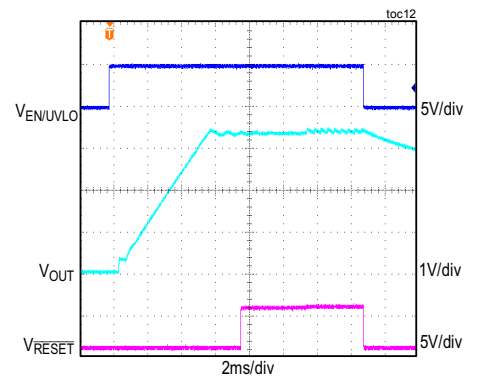
**SOFT-START/SHUTDOWN FROM EN/UVLO,  
(3.3V OUTPUT, PWM MODE, 1A LOAD CURRENT,  
FIGURE 5 CIRCUIT)**



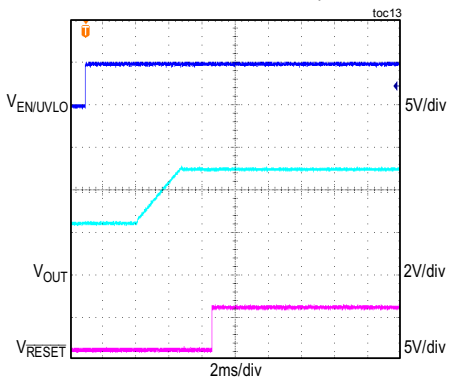
**SOFT-START/SHUTDOWN FROM EN/UVLO,  
(5V OUTPUT, PFM MODE, 5mA LOAD CURRENT,  
FIGURE 4 CIRCUIT)**



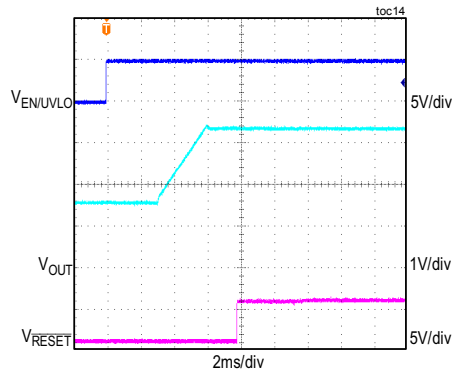
**SOFT-START/SHUTDOWN FROM EN/UVLO,  
(3.3V OUTPUT, PFM MODE, 5mA LOAD CURRENT,  
FIGURE 5 CIRCUIT)**



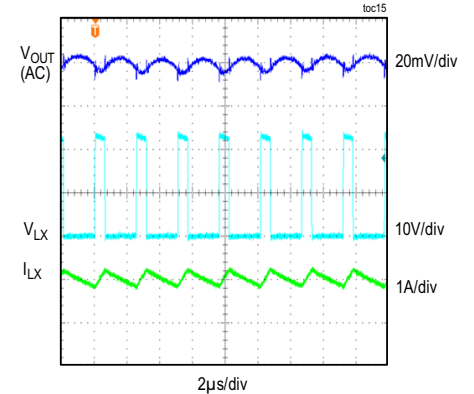
**SOFT-START WITH 2.5V PRE-BIAS,  
(5V OUTPUT, PWM MODE, 5mA LOAD CURRENT,  
FIGURE 4 CIRCUIT)**



**SOFT-START WITH 1.65V PRE-BIAS,  
(3.3V OUTPUT, PWM MODE, 5mA LOAD CURRENT,  
FIGURE 5 CIRCUIT)**

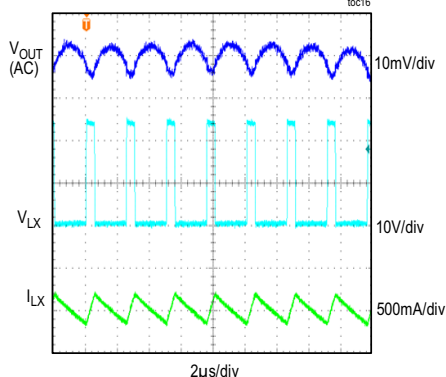


**STEADY-STATE SWITCHING WAVEFORMS  
(5V OUTPUT, FIGURE 4 CIRCUIT)**



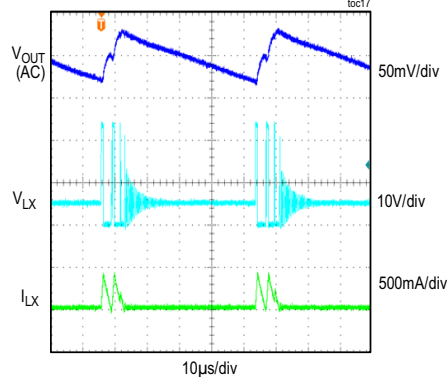
CONDITIONS: 1A LOAD CURRENT

**STEADY-STATE SWITCHING WAVEFORMS  
(5V OUTPUT, FIGURE 4 CIRCUIT)**



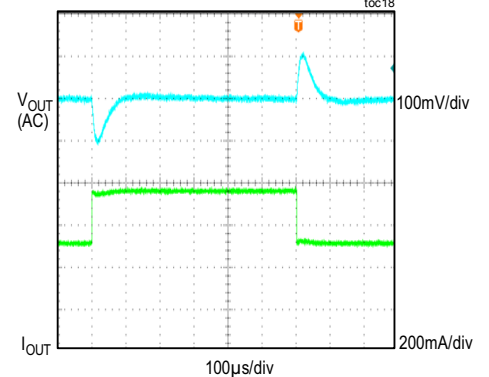
CONDITIONS: NO LOAD CURRENT

**STEADY-STATE SWITCHING WAVEFORMS  
(5V OUTPUT, FIGURE 4 CIRCUIT)**



CONDITIONS: PFM MODE, 25mA LOAD CURRENT

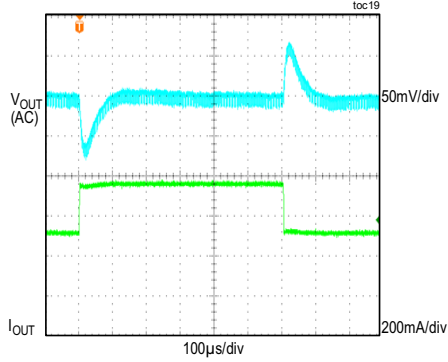
**LOAD CURRENT STEPPED FROM 0.5A TO 0.75A  
(5V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT)**



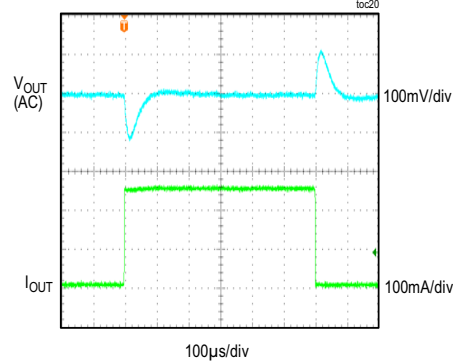
Typical Operating Characteristics (continued)

( $V_{IN} = 24V$ ,  $V_{SGND} = V_{PGND} = 0V$ ,  $C_{VIN} = 2.2\mu F$ ,  $C_{VCC} = 1\mu F$ ,  $V_{EN/UVLO} = \text{Open}$ ,  $C_{SS} = 33nF$ ,  $\text{MODE/ILIM} = \text{unconnected}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to SGND, unless otherwise noted.)

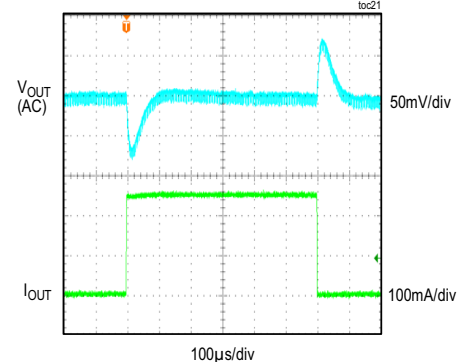
LOAD CURRENT STEPPED FROM 0.5A TO 0.75A (3.3V OUTPUT, PWM MODE, FIGURE 5 CIRCUIT)



LOAD CURRENT STEPPED FROM 0A TO 0.25A (5V OUTPUT, FIGURE 4 CIRCUIT)



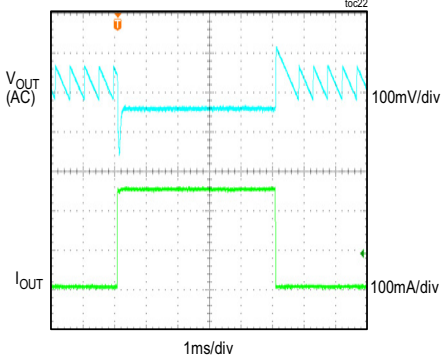
LOAD CURRENT STEPPED FROM 0A TO 0.25A (3.3V OUTPUT, FIGURE 5 CIRCUIT)



CONDITIONS: PWM MODE

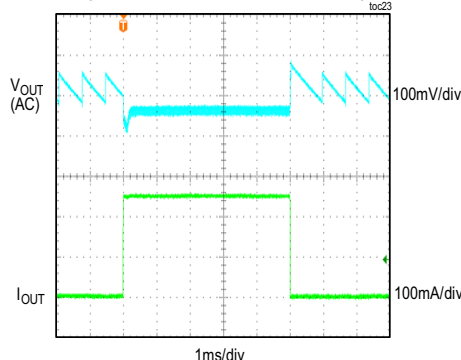
CONDITIONS: PWM MODE

LOAD CURRENT STEPPED FROM 0A TO 0.25A (5V OUTPUT, FIGURE 4 CIRCUIT)



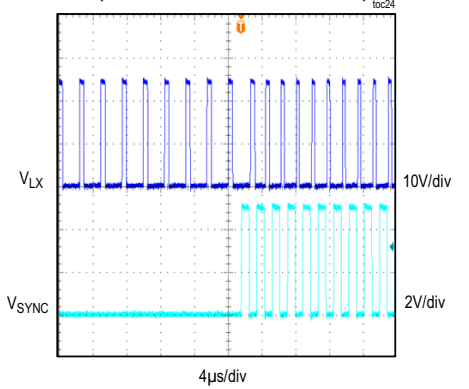
CONDITIONS: PFM MODE

LOAD CURRENT STEPPED FROM 0A TO 0.25A (3.3V OUTPUT, FIGURE 5 CIRCUIT)

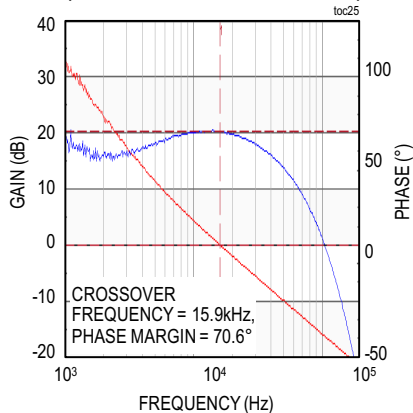


CONDITIONS: PFM MODE

APPLICATION OF EXTERNAL CLOCK AT 600kHz (5V OUTPUT, FIGURE 4 CIRCUIT)

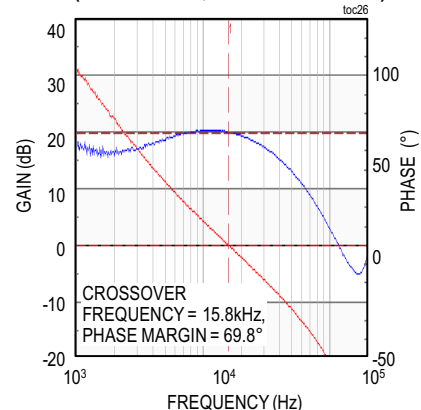


BODE PLOT (5V OUTPUT, FIGURE 4 CIRCUIT)



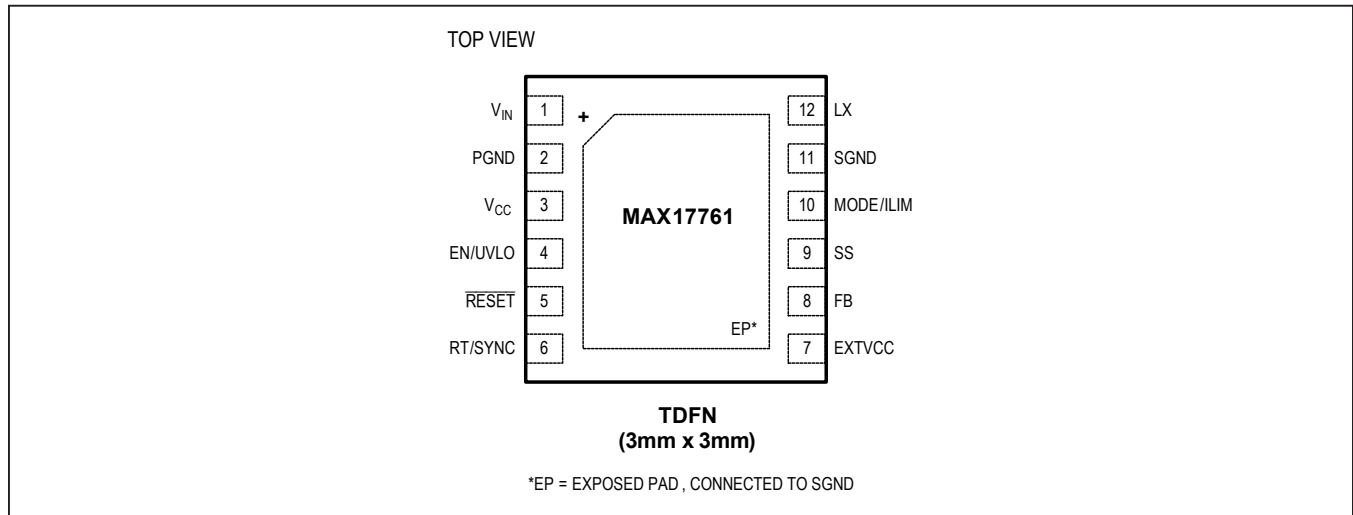
CONDITIONS: 1A LOAD CURRENT

BODE PLOT (3.3V OUTPUT, FIGURE 5 CIRCUIT)



CONDITIONS: 1A LOAD CURRENT

## Pin Configuration

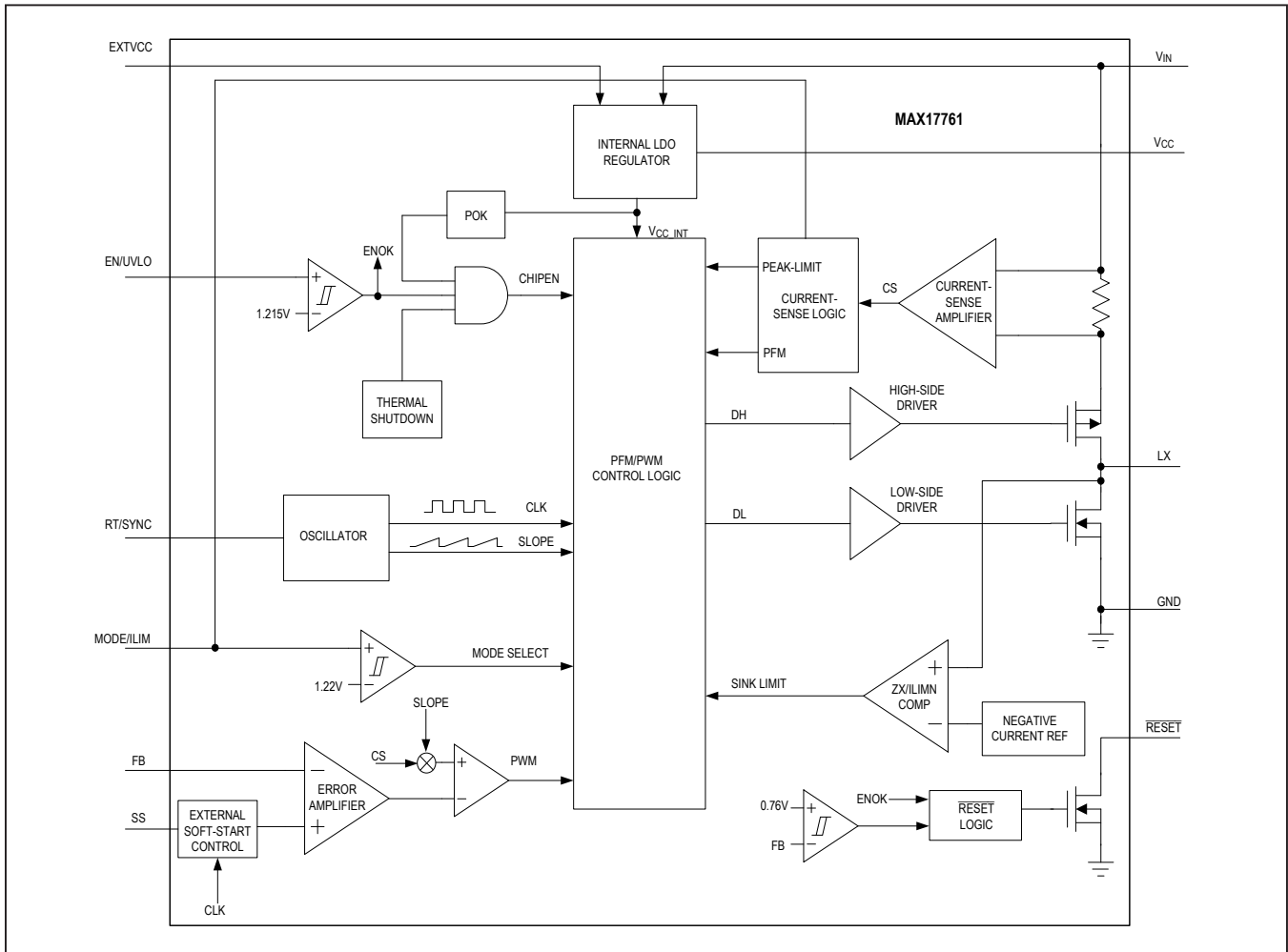


## Pin Description

PIN	NAME	FUNCTION
V <sub>IN</sub>	1	Power-Supply Input. 4.5V to 76V input supply range. Decouple to PGND with a 2.2μF capacitor; place the capacitor close to the V <sub>IN</sub> and PGND pins.
PGND	2	Power Ground Pin of the Converter. Connect externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V <sub>CC</sub> bypass capacitor.
V <sub>CC</sub>	3	5V LDO Output. Bypass V <sub>CC</sub> with a 1μF ceramic capacitance to SGND.
EN/UVLO	4	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between V <sub>IN</sub> and SGND to set the input voltage at which the part turns on. Leave the pin floating for always on operation.
RESET	5	Open-Drain RESET Output. The RESET output is driven low if FB drops below 92% of its set value. RESET goes high 2.1ms after FB rises above 95% of its set value.
RT/SYNC	6	Programmable Switching Frequency Input. Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part between 200kHz and 600kHz. An external clock can be connected to the RT/SYNC pin to synchronize the part with an external frequency.
EXTVCC	7	External Power Supply Input for the Internal LDO.
FB	8	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage.
SS	9	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
MODE/ILIM	10	Connect a resistor from MODE/ILIM to SGND to program the peak current limit and mode of operation of the part. See the <i>Current Limit and Mode of Operation Selection</i> section for more details.
SGND	11	Analog Ground.
LX	12	Switching Node. Connect LX pin to the switching-side of the inductor.
EP	—	Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17761 EV kit data sheet for an example of the correct method for EP connection and thermal vias.



Functional (or Block) Diagram



Detailed Description

The MAX17761 step-down regulator operates from 4.5V to 76V and delivers up to 1A load current on output. Feedback voltage regulation accuracy meets  $\pm 1.5\%$  over load, line, and temperature.

The device uses a peak-current-mode control scheme. An internal transconductance error amplifier generates an integrated error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator.

At each rising-edge of the clock, the high-side pMOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected.

During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side nMOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current limit is detected. The inductor releases the stored energy as its current ramps down, and provides current to the output. The internal low  $R_{DS(on)}$  pMOS/nMOS switches ensure high efficiency at full load.

This device also integrates switching frequency selector pin, current limit and mode of operation selector pin, enable/undervoltage lockout (EN/UVLO) pin, programmable soft-start pin and open-drain  $\overline{RESET}$  signal.

### Current Limit and Mode of Operation Selection

The following table lists the value of the resistors to program PWM or PFM modes of operation and 1.6A or 1.14A peak current limits.

The mode of operation cannot be changed on-the-fly after power-up.

**Table 1. R<sub>ILIM</sub> Resistor vs. Modes of Operation and Peak Current Limit**

R <sub>ILIM</sub> (kΩ)	MODE OF OPERATION	PEAK CURRENT LIMIT (A)
OPEN	PFM	1.6
422	PFM	1.14
243	PWM	1.6
121	PWM	1.14

### PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to the PFM mode of operation.

### PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak every clock cycle until the output rises to 102% of the nominal voltage. Once the output reaches 102% of the nominal voltage, both the high side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks and again commences the process of delivering pulses of energy to the output until it reaches 102% of the nominal output voltage.

The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. However, the output-voltage ripple is higher compared to PWM mode of operation and switching frequency is not constant at light loads.

### Linear Regulator (V<sub>CC</sub>)

The MAX17761 has two internal low dropout regulators (LDO), which power V<sub>CC</sub>. One LDO is powered from input voltage and the other LDO is powered from the EXTVCC pin. Only one of the two LDOs is in operation at a time, depending on the voltage levels present at the EXTVCC pin.

If EXTVCC is greater than 4.74V (typ), V<sub>CC</sub> is powered from the EXTVCC pin. If EXTVCC is lower than 4.44V (typ), V<sub>CC</sub> is powered from input voltage. Powering V<sub>CC</sub> from EXTVCC increases efficiency particularly at higher input voltages. Typical V<sub>CC</sub> output voltage is 5V. Bypass V<sub>CC</sub> to SGND with a 1μF cap. Both the LDOs can source up to 13mA.

When V<sub>CC</sub> falls below its undervoltage lockout (3.8V(typ)), the internal step-down controller is turned off, and LX switching is disabled. The LX switching is enabled again when the V<sub>CC</sub> voltage exceeds 4.2V (typ). The 400mV (typ) hysteresis prevents chattering on power-up/power-down.

When the EXTVCC is connected to the output and the output is shorted such that inductive ringings cause the output voltage to become temporarily negative, a R-C network should be connected between the output and the EXTVCC pin. A 4.7Ω between the output and the pin and a 0.1μF from the pin to ground is recommended.

### Switching Frequency Selection and External Frequency Synchronization

The RT/SYNC pin programs the switching frequency of the converter. Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part at any one of four discrete frequencies—200kHz, 300kHz, 400kHz, and 600kHz. Table 2 provides resistor values.

The internal oscillator of the device can be synchronized to an external clock signal on the RT/SYNC pin. The external synchronization clock frequency must be between 1.15 x f<sub>SW</sub> and 1.4 x f<sub>SW</sub>, where f<sub>SW</sub> is the frequency programmed by the resistor connected from the RT/SYNC pin.

**Table 2. Switching Frequency vs. RT Resistor**

SWITCHING FREQUENCY (kHz)	RT/SYNC RESISTOR VALUE (kΩ)
200	210
300	140
400	105
600	69.8

### Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR(MAX)} + R_{DS-ONL(MAX)}))}{D_{MAX}} + (I_{OUT(MAX)} \times (R_{DS-ONH(MAX)} - R_{DS-ONL(MAX)}))$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON-MIN(MAX)}}$$

where:

$V_{OUT}$  = Steady-state output voltage

$I_{OUT(MAX)}$  = Maximum load current

$R_{DCR(MAX)}$  = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$  = Maximum switching frequency

$D_{MAX(MIN)}$  = Minimum value of the maximum allowable duty ratio (0.9)

$t_{ON-MIN(MAX)}$  = Worst-case minimum switch on-time (110ns)

$R_{DS-ONL(MAX)}$  and  $R_{DS-ONH(MAX)}$  = Worst-case on-time resistances of low-side and high-side internal MOSFETs, respectively.

### Overcurrent Protection

The device is provided with a robust overcurrent-protection scheme that protects the device under overload and output short-circuits conditions. The positive current limit is triggered when the peak value of the inductor current hits a fixed threshold ( $ILIM\_P$ , 1.6A/1.14A, depending on the value of the resistor connected to the MODE/ILIM pin). At this point, the high-side switch is turned off and the low-side switch is turned on. The low-side switch is kept on until the inductor current discharges below  $0.7 \times ILIM\_P$ .

While in PWM mode of operation, the negative current limit is triggered when the valley value of the inductor current hits a fixed threshold ( $ILIM\_N$ , -0.65A/-0.455A, depending on the value of the resistor connected to the MODE/ILIM pin). At this point, the low-side switch is turned off and the high-side switch is turned on.

### RESET Output

The device includes  $\overline{RESET}$  pin to monitor the output voltage. The open-drain  $\overline{RESET}$  output requires an external pullup resistor.  $\overline{RESET}$  goes high (high impedance) in 2.1ms after the output voltage increases above 95% of the nominal voltage.  $\overline{RESET}$  goes low when the output voltage drops to below 92% of the nominal voltage.  $\overline{RESET}$  also goes low during thermal shutdown.

### Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences first with the high-side switch. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

### Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +160°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the [Power Dissipation](#) section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

### Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement ( $I_{RMS}$ ) for a single output is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where,  $I_{OUT(MAX)}$  = The maximum load current,  $I_{RMS}$  has a maximum value when the input voltage equals twice the output voltage ( $V_{IN} = 2 \times V_{OUT}$ ), so  $I_{RMS(MAX)} = I_{OUT(MAX)}/2$ .

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where,

$D = V_{OUT}/V_{IN}$  is the duty ratio of the controller,

$f_{SW}$  = The switching frequency,

$\Delta V_{IN}$  = The allowable input voltage ripple,

$\eta$  = The efficiency.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

### Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current ( $I_{SAT}$ ) and DC resistance ( $R_{DCR}$ ). The switching frequency and output voltage determine the inductor value as follows:

For  $R_{ILIM} = OPEN$  or  $R_{ILIM} = 243k\Omega$ ,

$$L = \frac{2.6 \times V_{OUT}}{f_{SW}}$$

For  $R_{ILIM} = 121k\Omega$  or  $R_{ILIM} = 422k\Omega$ ,

$$L = \frac{3.7 \times V_{OUT}}{f_{SW}}$$

where,  $V_{OUT}$  and  $f_{SW}$  are nominal values. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating ( $I_{SAT}$ ) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

### Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in Industrial applications. The output capacitor is sized to support a step load of 25% of the maximum output current in the application, such that the output voltage deviation is contained to 3% of the output voltage change. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.33}{f_C}$$

where,

$I_{STEP}$  = The load-current step,

$t_{RESPONSE}$  = The response time of the controller,

$\Delta V_{OUT}$  = The allowable output-voltage deviation,

$f_C$  = The target closed-loop crossover frequency ( $f_C$  is chosen to be 15kHz or 1/20<sup>th</sup> of  $f_{SW}$ , whichever is lower),

$f_{SW}$  = The switching frequency.

Derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

### Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time for the corresponding output voltage. The selected output capacitance ( $C_{SEL}$ ) and the output voltage ( $V_{OUT}$ ) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 30 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time ( $t_{SS}$ ) is related to the capacitor connected at SS ( $C_{SS}$ ) by the following equation:

$$t_{SS} = \frac{C_{SS}}{6.25 \times 10^{-6}}$$

For example, to program a 5.3ms soft-start time, a 33nF capacitor should be connected from the SS pin to SGND. The minimum possible soft-start time is 5ms.

### Adjusting Output Voltage

Set the output voltage with resistive voltage-dividers connected from the positive terminal of the output capacitor ( $V_{OUT}$ ) to SGND (Figure 1). Connect the centre node of the divider to the FB pin. To optimize efficiency and output accuracy, use the following calculations to choose the resistive divider values:

$$R4 = \frac{15 \times V_{OUT}}{0.8}$$

$$R5 = \frac{R4 \times 0.8}{(V_{OUT} - 0.8)}$$

where R4 and R5 are in k $\Omega$ .

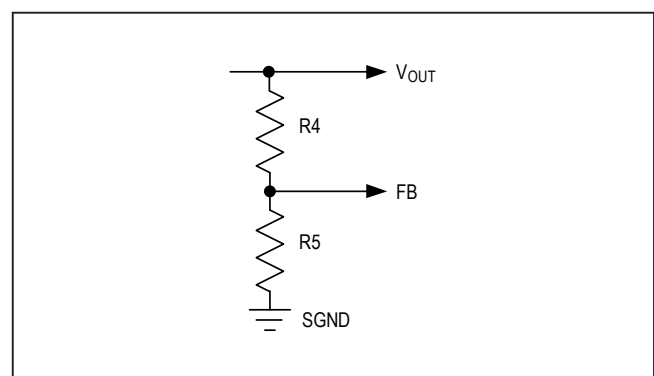


Figure 1. Adjusting Output Voltage

**Setting the Undervoltage Lockout Level**

Drive EN/UVLO high to enable the output. Leave the pin floating for always on operation. Set the voltage at which each converter turns on with a resistive voltage-divider connected from V<sub>IN</sub> to SGND (see Figure 2). Connect the center node of the divider to EN/UVLO pin.

Choose R1 as follows:

$$R1 \leq (110000 \times V_{INU})$$

where V<sub>INU</sub> is the input voltage at which the MAX17761 is required to turn on and R1 is in Ω. Calculate the value of R2 as follows:

$$R2 = \frac{1.215 \times R1}{(V_{INU} - 1.215 + (2.5\mu A \times R1))}$$

**Series R-C Selection Across Bottom Feedback Resistor**

In order to achieve the targeted bandwidth, R-C series circuit is connected across bottom feedback resistor (Figure 3). Selection procedure for series R-C (R6 and C6) values are as follows:

$$R6 = \frac{R4 \times R5}{R4 + R5} \times \frac{k}{1 - 0.99k}$$

$$C6 = \frac{1.125 \times 10^6}{f_C \times \sqrt{\frac{k}{1 - K^2}}} \times R6$$

where,

$$k = \frac{f_C \times C_{OUT} \times \left(1 + \frac{R4}{R5}\right)}{3.6274 \times 10^6}$$

C<sub>OUT</sub> = The actual derated capacitance value for a given bias voltage of selected output capacitor in μF,

f<sub>C</sub> = The targeted crossover frequency in Hz,

R4 and R5 = The feedback network values in kΩ,

R6 and C6 are in kΩ and nF respectively.

**Power Dissipation**

The exposed pad of the IC should be properly soldered to the PCB to ensure good thermal contact.

At a particular operating condition, the power losses that lead to temperature rise of the device are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - (I_{OUT}^2 \times R_{DCR})$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where,

P<sub>OUT</sub> = The output power,

η = The efficiency of the device

R<sub>DCR</sub> = The DC resistance of the output inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a multilayer board, the thermal performance metrics for the 12-pin TDFN package are given as:

$$\theta_{JA} = 41^\circ C/W$$

$$\theta_{JC} = 8.5^\circ C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T<sub>A\_MAX</sub>) from the following equation:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T<sub>EP\_MAX</sub>) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrade operating lifetimes.

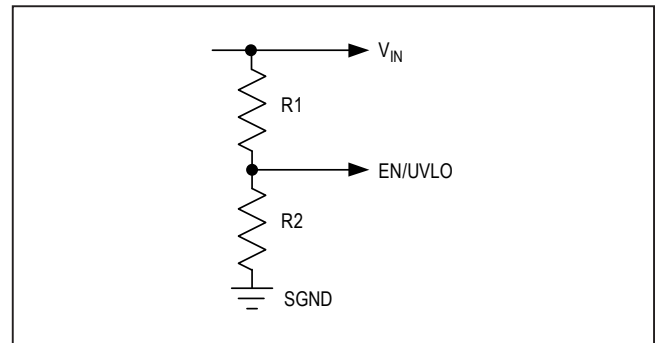


Figure 2. Setting the Undervoltage Lockout Level

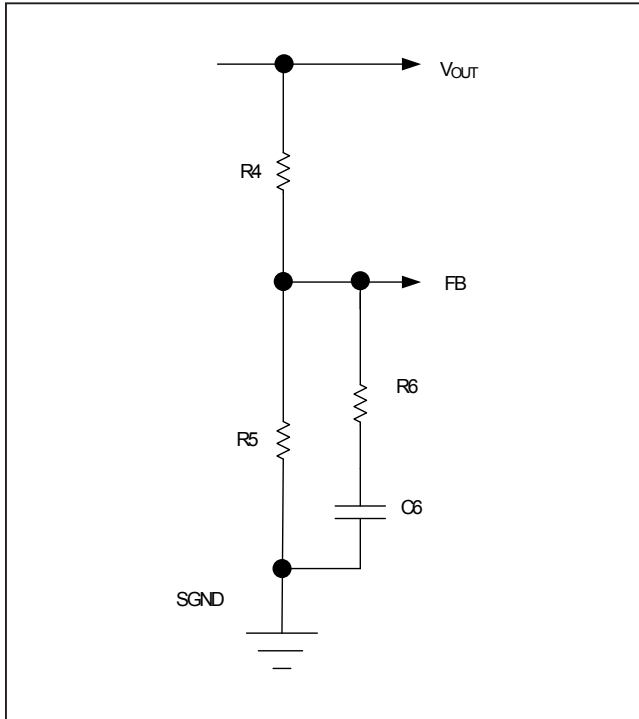


Figure 3. Setting R-C Series Network

### PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17761 evaluation kit layouts available at [www.maximintegrated.com](http://www.maximintegrated.com). Follow these guidelines for good PCB layout:

All connections carrying pulsed currents must be very short and as wide as possible. The loop area of these connections must be made very small to reduce stray inductance and radiated EMI.

A ceramic input filter capacitor should be placed close to the  $V_{IN}$  pin of the device. The bypass capacitor for the  $V_{CC}$  pin should also be placed close to the  $V_{CC}$  pin. The feedback trace should be routed as far as possible from the inductor.

The analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at minimum, typically the return terminal of the  $V_{CC}$  bypass capacitor. The ground plane should be kept continuous as much as possible.

A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the device for efficient heat dissipation.

Typical Application Circuits

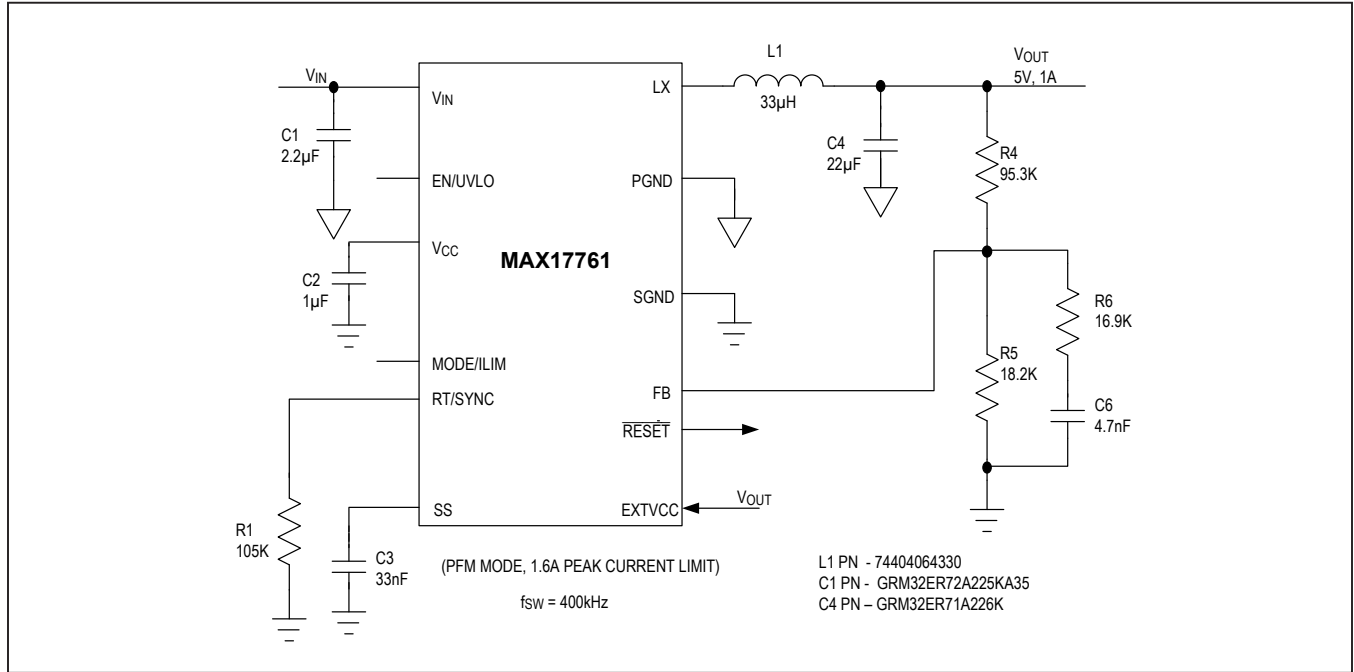


Figure 4. 5V Output Typical Application Circuit (Part is Always On when the EN/UVLO Pin is Unconnected)

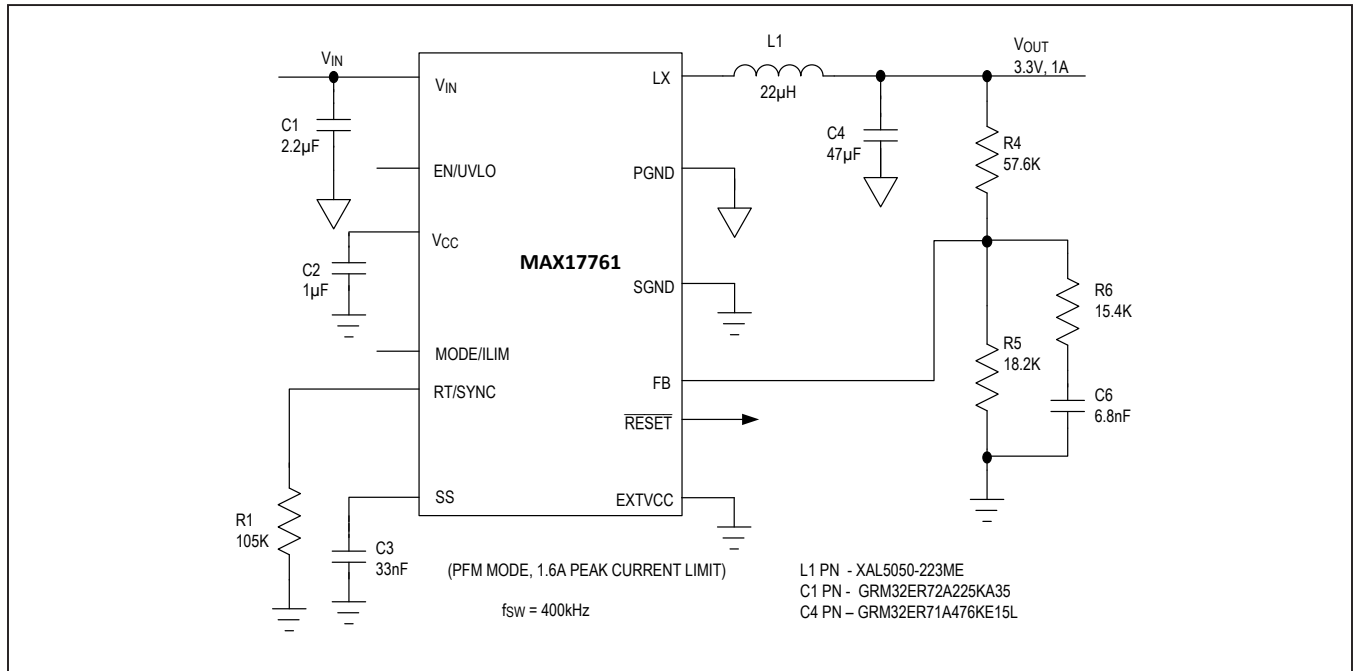


Figure 5. 3.3V Output Typical Application Circuit (Part is Always On when the EN/UVLO Pin is Unconnected)

MAX17761

4.5V to 76V, 1A, High-Efficiency,  
Synchronous Step-Down DC-DC Converter

### Ordering Information

PART	PIN-PACKAGE	PIN-PACKAGE
MAX17761ATC+	12 TDFN-EP*	3mm x 3mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

### Chip Information

PROCESS: BiCMOS



## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	2/18	Updated the <i>General Description, Benefits and Features, Absolute Maximum Ratings, Typical Operating Characteristics, Operating Input Voltage Range, and Soft-Start Capacitor Selection</i> sections. Updated the <i>Electrical Characteristics</i> and <i>Pin Description</i> tables. Replaced the <i>Functional Diagram</i> and <i>Typical Application Circuits</i> .	1–2, 4–12, 15

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