*Click **here** to ask about the production status of specific part numbers.*

MAX77960B/MAX77961B

25V$_{IN}$, 3A$_{OUT}$ to 6A$_{OUT}$, USB-C Buck-Boost Charger with Integrated FETs for 2S/3S Li-Ion Batteries

General Description

The MAX77960B/MAX77961B are high-performance wide-input 3A (MAX77960B)/6A (MAX77961B) buck-boost chargers with Smart Power Selector™ and operate as a reverse buck converter without an additional inductor, allowing the ICs to power USB on-the-go (OTG) accessories. The devices integrate low-loss power switches and provide high efficiency, low heat, and fast battery charging in a small solution size. The reverse buck has true load disconnect and is protected by an adjustable output current limit. The devices are highly flexible and programmable through I^{2}C configuration or autonomously through resistor configuration.

The battery charger includes the Smart Power Selector to accommodate a wide range of battery sizes and system loads. The Smart Power Selector allows the system to start up smoothly when an input source is available even when the battery is deeply discharged (dead battery) or missing. For battery safety/authentication reasons, the ICs can be configured to keep charging disabled, and allow the DC-DC to switch and regulate the SYS voltage. The system processor can later enable charging using I^{2}C commands as appropriate. Alternatively, the ICs can be configured to automatically start charging.

Applications

- USB Type-C Powered Wide-Input Charging Applications
- 2- and 3-Cell Battery-Powered Devices
- Smartphones, Tablets, and 2-in-1 Laptops
- Medical Devices, Health and Fitness Monitors
- Digital Still, Video, and Action Cameras
- Handheld Computers and Terminals
- Handheld Radios
- Power Tools
- Drones
- Battery Backup
- Wireless Speakers

Benefits and Features

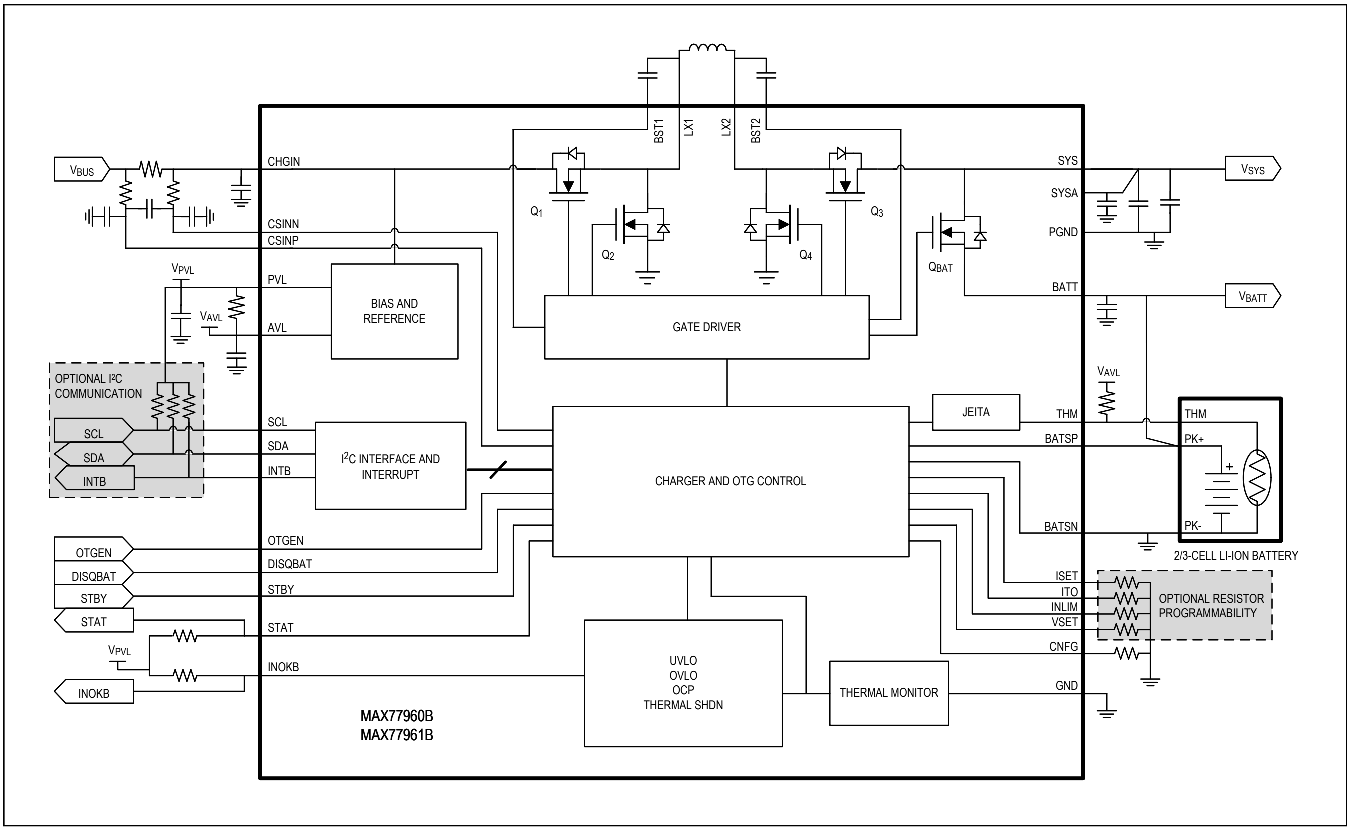
- 3.5V to 25.4V Input Operating Range, 30V$_{DC}$ Withstand
- 97% Peak Efficiency for 2S Battery at 9V$_{IN}$/7.4V$_{OUT}$/1.5A$_{OUT}$
- 97% Peak Efficiency for 3S Battery at 15V$_{IN}$/12.6V$_{OUT}$/2A$_{OUT}$
- MAX77960B
  - 100mA to 3.15A Programmable Input Current Limit
  - 100mA to 3A Programmable Constant Current Charge
- MAX77961B
  - 100mA to 6.3A Programmable Input Current Limit
  - 100mA to 6A Programmable Constant Current Charge
- Remote Differential Voltage Sensing
- 600kHz or 1.2MHz Switching Frequency Options
- System Instant On with Smart Power Selector Power Path
- Charge Safety Timer
- Die Temperature Regulation with Thermal Foldback Loop
- Input Power Management with Adaptive Input Current Limit (AICL) and Input Voltage Regulation
- 10mΩ BATT to SYS Switch, Up to 10A Overcurrent Threshold
- Reverse Buck Mode 5.1V/3A to Support USB OTG
- JEITA Compliant with NTC Thermistor Monitor
- I^{2}C or Resistor Programmable
- 4mm x 4mm, 30-Lead FC2QFN

***Ordering Information* appears at end of data sheet.**

19-101123; Rev 0; 6/21

maxim integrated™

Simplified Block Diagram



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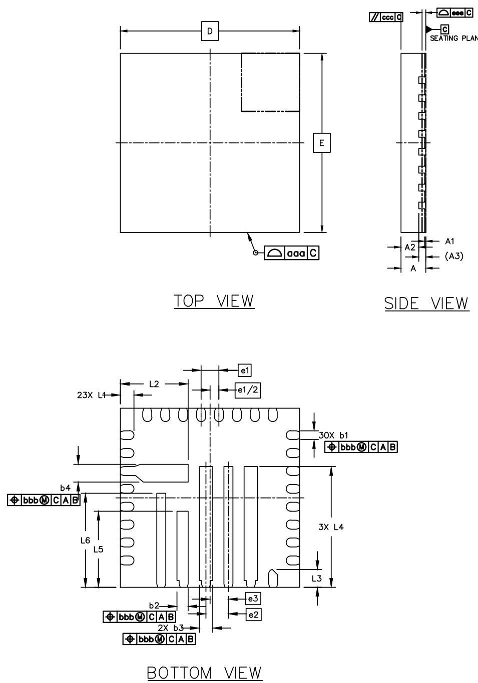
DISQBAT, OTGEN, STBY, STAT, INOKB, INTB, SDA, SCL to GND .... -0.3V to +6.0V
CHGIN Continuous Current .... $6.5A_{RMS}$
LX_, PGND Continuous Current .... $6.5A_{RMS}$
SYS, BATT Continuous Current .... $10.0A_{RMS}$
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 40.37mW/°C above +70°C.) 3229.71mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

30-Lead FC2QFN

Package Code	F304A4F+1
Outline Number	21-100278
Land Pattern Number	90-100100
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	24.77°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.67°C/W



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b1	0.15	0.2	0.25
		b2	0.2	0.25	0.3
		b3	0.25	0.3	0.35
		b4	0.35	0.4	0.45
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e1		0.4 BSC	
		e2		0.5 BSC	
		e3		0.41 BSC	
LEAD LENGTH		L1	0.2	0.3	0.4
		L2	1.41	1.51	1.61
		L3	0.3	0.4	0.5
		L4	2.6	2.7	2.8
		L5	1.6	1.7	1.8
		L6	2	2.1	2.2
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	

NOTES

1. REFER TO JEDEC MO-220
2. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD
3. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET SPECIFICATIONS
4. FINISH: Cu/EP • Sn8~20s
5. MAXIM PKG CODE : F304A4F-1
6. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.

-DRAWING NOT TO SCALE-

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TITLE: PACKAGE OUTLINE, 30L FC2QFN 4x4x0.55mm

APPROVAL | DOCUMENT CONTROL NO. 21-100278 | REV. B | 1/1

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS						
CHGIN Voltage Range	V_{CHGIN}	Operating voltage	3.5		25.4	V
CHGIN Overvoltage Threshold	V_{CHGIN_OVLO}	V_{CHGIN} rising, 365mV hysteresis	25.4	26.05	26.7	V
CHGIN Overvoltage Delay	$t_{D\_CHGIN\_OVLO}$	V_{CHGIN} rising, 100mV overdrive		10		μs
		V_{CHGIN} falling, 100mV overdrive		7		ms
CHGIN Undervoltage Threshold	V_{CHGIN_UVLO}	V_{CHGIN} rising, 20% hysteresis	3.43	3.5	3.57	V
CHGIN Quiescent Current (I_{SYS} = 0A)	I_{CHGIN}	V_{CHGIN} = 2.4V, the input is undervoltage and R_{INSD} is the only loading		0.075		mA
		V_{CHGIN} = 9.0V, charger disabled		0.17	0.5	
		V_{CHGIN} = 9.0V, charger enabled, V_{SYS} = V_{BATT} = 8.7V (2S configuration), no switching		2.7	4	
	I_{CHGIN_STBY}	MODE[3:0] = 0x0 (DC-DC off), STBY = H or STBY_EN = 1, V_{CHGIN} = 5V			1	
BATT Quiescent Current (I_{SYS} = 0A)	I_{SHDN}	FSHIP_MODE = 1 or DISQBAT = high, V_{CHGIN} = 0V, I_{SYS} = 0A, V_{BATT} = 13.5V		2.3	5.0	μA
	I_{BATT}	DISQBAT = low, I^2C enabled, V_{CHGIN} = 0V, I_{SYS} = 0A, V_{BATT} = 13.5V		100	200	
		V_{SYS} = 7.6V, V_{BATT} = 0V, charger disabled, T_A = +25°C		0.01	10	
		V_{SYS} = 7.6V, V_{BATT} = 0V, charger disabled, T_A = +85°C		10		
	I_{BATTDN}	V_{CHGIN} = 9V, V_{BATT} = 8.4V, Q_{BAT} is off, battery overcurrent protection disabled, charger is enabled but in its done mode, T_A = +25°C		57	65	
		V_{CHGIN} = 9V, V_{BATT} = 8.4V, Q_{BAT} is off, battery overcurrent protection disabled, charger is enabled but in its done mode, T_A = +85°C		57		
SYS Operating Voltage	V_{SYS}	Guaranteed by $V_{SYSUVLO}$ and $V_{SYSOVLO}$	SYSUVLO rising		SYSOVLO rising	V
SYS Undervoltage Lockout Threshold	$V_{SYSUVLO}$	V_{SYS} falling, 530mV hysteresis	3.95	4.1	4.25	V
SYS Overvoltage Lockout Threshold	$V_{SYSOVLO}$	V_{SYS} rising, 430mV hysteresis, 2S battery	10.65	10.9	11.15	V
		V_{SYS} rising, 267mV hysteresis, 3S battery	13.75	14.1	14.45	
PVL Output Voltage	V_{PVL}		1.7	1.8	1.9	V
Thermal Shutdown Threshold	T_{SHDN}	T_J rising		165		°C
Thermal Shutdown Hysteresis				15		°C

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Self-Discharge Resistance	R_{INSD}	V_{CHGIN} = 3V		44		kΩ
BATT Self-Discharge Resistance	R_{BATSD}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 5V		600		Ω
SYS Self-Discharge Resistance	R_{SYSSD}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 5V		600		Ω
Self-Discharge Latch Time				300		ms
SWITCH MODE CHARGER / CHARGER						
BATT Regulation Voltage Range	$V_{BATTREG}$	Programmable from 8.0V to 9.26V (2S battery) and 12.0V to 13.05V (3S battery), production tested at 8V, 8.38V, 8.8V and 9.26V only (2S battery) and 12V, 12.57V, 13.2V, and 13.89V only (3S battery)	8.00		13.05	V
BATT Regulation Voltage Accuracy		8.8V or 13.2V settings, T_A = +25°C	-0.9	-0.3	+0.3	%
		8.8V or 13.2V settings, T_A = 0°C to +85°C (Note 1)	-1	-0.3	+0.5	
BATT Overvoltage Lockout Threshold	$V_{BATTOVLO}$	V_{BATT} rising above $V_{BATTREG}$, 2% hysteresis	75	240	375	mV/cell
BATT Undervoltage Lockout Threshold	$V_{BATTUVLO}$	V_{BATT} rising, 100mV hysteresis	2.0	2.5	3.0	V
Fast-Charge Current Program Range	I_{FC}	MAX77960B; 100mA to 3A; production tested at 100mA, 200mA, 500mA, 1000mA, 1500mA, 2000mA, and 3000mA settings	0.10		3	A
		MAX77961B; 100mA to 6A; production tested at 100mA, 200mA, 500mA, 1000mA, 1500mA, 2000mA, 3000mA, 3500mA, and 3800mA settings	0.10		6	
Fast-Charge Current Accuracy		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 100mA	80	100	120	mA
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 200mA	180	200	220	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 500mA	481	500	519	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 1000mA	962	1000	1038	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 2000mA	1925	2000	2075	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3000mA	2887	3000	3113	
		MAX77961B. T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3500mA	3369	3500	3631	
		MAX77961B. T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3800mA	3657	3800	3943	

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast-Charge Current Accuracy (Over Temperature)		-40°C < T_A < +85°C, V_{BATT} > V_{SYSMIN}, programmed for 200mA or less (Note 1)	-20		+20	mA
		-40°C < T_A < +85°C, V_{BATT} > V_{SYSMIN}, programmed for greater than 200mA (Note 1)	-5		+5	%
CHGIN Adaptive Voltage Regulation Range	V_{CHGIN_REG}	I^2C programmable	4.025		19.05	V
CHGIN Adaptive Voltage Regulation Accuracy		4.55V setting	4.42	4.55	4.68	V
CHGIN Current Limit Range	CHGIN_ILIM	MAX77960B; programmable; production tested at 100mA, 150mA, 200mA, 500mA, 1000mA, 1500mA, and 3000mA settings only	0.1		3.15	A
		MAX77961B; programmable; production tested at 100mA, 150mA, 200mA, 500mA, 1000mA, 1500mA, 3000mA, 4000mA, and 6300mA settings only	0.1		6.3	
CHGIN Current Limit Accuracy		Charger enabled, 100mA input current setting, T_A = +25°C	88	98	108	mA
		Charger enabled, 200mA input current setting, T_A = +25°C	175	195	215	
		Charger enabled, 500mA input current setting, T_A = +25°C	475	488	500	
		Charger enabled, 1000mA input current setting, T_A = +25°C	950	975	1000	
		Charger enabled, 3000mA input current setting, T_A = +25°C	2850	2925	3000	
		MAX77961B; charger enabled, 4000mA input current setting, T_A = +25°C	3800	3900	4000	
		MAX77961B; charger enabled, 6300mA input current setting, T_A = +25°C	5985	6143	6300	
CHGIN Current Limit Accuracy (Over Temperature)		Charger enabled, 200mA or less input current setting, -40°C < T_A < +85°C (Note 1)	-22.5		+17.5	%
		Charger enabled, greater than 200mA input current setting, -40°C < T_A < +85°C (Note 1)	-7.5		+2.5	
Precharge Voltage Threshold	V_{PRECHG}	V_{BATT} rising, voltage threshold per cell	2.4	2.5	2.6	V/Cell
Precharge Current	I_{PRECHG}		35	50	65	mA
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to V_{PRECHG}		150		mV/Cell

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum SYS Voltage Accuracy	V_{SYSMIN}	Programmable from 5.535V to 6.970V (2S battery) and 8.303V to 10.455V (3S battery), V_{BATT} = 5.6V (2S battery) or 8.4V (3S battery), tested at 3V/cell setting	-3		+3	%
Trickle Charge Current	$I_{TRICKLE}$	Default setting = enabled; ITRICKLE[1:0] = 00	75	100	125	mA
		Default setting = enabled; ITRICKLE[1:0] = 01 (Note 1)	150	200	250	
		Default setting = enabled; ITRICKLE[1:0] = 10 (Note 1)	225	300	375	
		Default setting = enabled; ITRICKLE[1:0] = 11	300	400	500	
Top-Off Current Program Range	I_{TO}	Programmable from 100mA to 600mA	100		600	mA
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time		160		ms
Charger Restart Threshold Range	V_{RSTRT}	Program options for disabled, 100mV/cell, 150mV/cell, and 200mV/cell with CHG_RSTRT[1:0]	100		200	mV/cell
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time		130		ms
Charger State Change Interrupt Deglitch Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state		30		ms
SWITCH MODE CHARGER / CHARGE TIMER						
Prequalification Time	t_{PQ}	Applies to both low-battery prequalification and dead-battery prequalification modes		30		min
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}	Adjustable from 3hrs, 4hrs, 5hrs, 6hrs, 7hrs, 8hrs, 10hrs including a disable setting; 3hrs default		3		hrs
Top-Off Time	t_{TO}	Adjustable from 30s to 70min in 10min steps		30		min
SWITCH MODE CHARGER / WATCHDOG TIMER						
Watchdog Timer Period	t_{WD}	(Note 2)	80			s
SWITCH MODE CHARGER / BUCK-BOOST						
CHGIN OK to Start Switching Delay	t_{START}	Delay from INOKB H → L to LX_ start switching		150		ms
Buck-Boost Current Limit	HSILIM	MAX77960B, V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V	4.3	5	5.7	A
		MAX77961B, V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V	8.6	10	11.4	
SWITCH MODE CHARGER / BUCK-BOOST / SWITCH IMPEDANCE AND LEAKAGE CURRENT						
LX1 High-Side Resistance	R_{LX1_HS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		16.5	26	mΩ

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX1 Low-Side Resistance	R_{LX1_LS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		17	30	mΩ
LX2 High-Side Resistance	R_{LX2_HS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		9	18	mΩ
LX2 Low-Side Resistance	R_{LX2_LS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		21	33	mΩ
LX_ Leakage Current		LX1 = PGND or CHGIN, LX2 = PGND or SYS, T_A = +25°C		0.01	10	µA
		LX1 = PGND or CHGIN, LX2 = PGND or SYS, T_A = +85°C		1		
BST_ Leakage Current		BST_ = 1.8V, T_A = +25°C		0.01	10	µA
		BST_ = 1.8V, T_A = +85°C		1		
SYS, SYSA Leakage Current		V_{SYS} = V_{SYSA} = 8.4V, V_{BATT} = 0V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{SYS} = V_{SYSA} = 8.4V, V_{BATT} = 0V, charger disabled, T_A = +85°C		1		
CSINP, CSINN Leakage Current	I_{CSINP}, I_{CSINN}	V_{CHGIN} = 26.05V, V_{CSINP} = V_{CSINN} = 26.05V, T_A = +25°C	-1		+1	µA
SWITCH MODE CHARGER / SMART POWER SELECTOR						
BAT to SYS Dropout Resistance	$R_{BAT2SYS}$			10	17	mΩ
BATT to SYS Reverse Regulation Voltage	V_{BSREG}			90		mV
SWITCH MODE CHARGER / BATT TO SYS OVERCURRENT ALERT						
Battery Overcurrent Threshold Range	I_{BOVCR}	Programmable from 3A to 10A. Option to disable.	3		10	A
Battery Overcurrent Debounce Time	t_{BOVRC}	Response time for generating the overcurrent interrupt (Note 2)			3.3	ms
SWITCH MODE CHARGER / THERMAL FOLDBACK						
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{REG}	Junction temperature when charge current is reduced; programmable from 85°C to 130°C in 5°C steps; default value is 115°C	85		130	°C

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 5% of the fast-charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3A (MAX77960B)/6A (MAX77961B) is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 480mA, this slope is valid for charge current reductions down to 80mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is 20°C above the programmed loop set point.		-5		%/°C
SWITCH MODE CHARGER / THERMISTOR MONITOR						
THM Threshold, COLD	THM_COLD	V_{THM}/V_{AVL} rising, 1% hysteresis (thermistor temperature falling)	73.36	74.56	75.76	%
THM Threshold, COOL	THM_COOL	V_{THM}/V_{AVL} rising, 1% hysteresis (thermistor temperature falling)	58.8	60	61.2	%
THM Threshold, WARM	THM_WARM	V_{THM}/V_{AVL} falling, 1% hysteresis (thermistor temperature rising)	33.68	34.68	35.68	%
THM Threshold, HOT	THM_HOT	V_{THM}/V_{AVL} falling, 1% hysteresis (thermistor temperature rising)	21.59	22.5	23.41	%
THM Threshold, Disabled		VTHM/AVL falling, 1% hysteresis, THM function is disabled below this voltage	4.9	5.9	6.9	%
THM Threshold, Battery Removal Detection		V_{THM}/V_{AVL} rising, 1% hysteresis, battery removal	85.6	87	88.4	%
THM Input Leakage Current		V_{THM} = GND or V_{AVL}; T_A = +25°C		0.1	1	µA
		V_{THM} = GND or V_{AVL}; T_A = +85°C		0.1		
REVERSE BUCK						
Buck Current Limit	HSILIM_REV	f_{SW} = 600kHz	4.3	5	5.7	A
Reverse Buck Quiescent Current		Not switching: output forced 200mV above its target regulation voltage		1150		µA
Minimum BATT Voltage in OTG Mode	$V_{BATT.MIN.OTG}$	V_{BATT} = V_{SYS}, SYS UVLO falling threshold in OTG mode	5.96	6.14	6.32	V
CHGIN Voltage in OTG Mode	$V_{CHGIN.OTG}$	V_{BATT} = $V_{BATT.MIN.OTG}$, OTGEN = high	4.94	5.1	5.26	V
CHGIN Undervoltage Threshold in OTG Mode	$V_{CHGIN.OTG.UV}$	V_{CHGIN} falling, OTGEN = high		85		%
CHGIN Overvoltage Threshold in OTG Mode	$V_{CHGIN.OTG.OV}$	V_{CHGIN} rising, OTGEN = high		110		%

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Output Current Limit in OTG Mode	$I_{CHGIN.OTG.LIM}$	V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b000, OTGEN = high		500	550	mA
		V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b001, OTGEN = high		900	990	
		V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b011, OTGEN = high		1500	1650	
		V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b111, OTGEN = high		3000	3300	
CHGIN Output Voltage Ripple in OTG Mode		Discontinuous inductor current (i.e., skip mode), OTGEN = high		±150		mV
		Continuous inductor current, OTGEN = high		±150		
IO CHARACTERISTICS						
R_{INLIM}, R_{ISET}, R_{VSET}, R_{TO}, R_{CNFG} Resistor Range	$R_{PROG\_}$		5.49		226	kΩ
Output Low Voltage INOKB, STAT		I_{SINK} = 1mA, T_A = +25°C			0.4	V
Output High Leakage INOKB, STAT		5.5V, T_A = +25°C	-1	0	+1	µA
		5.5V, T_A = +85°C		0.1		
DISQBAT, OTGEN, STBY Logic Input Low Threshold	V_{IL}				0.4	V
DISQBAT, OTGEN, STBY Logic Input High Threshold	V_{IH}		1.4			V
DISQBAT, OTGEN, STBY Logic Input Leakage Current		5.5V (including current through pulldown resistor)		5.5	10	µA
DISQBAT, OTGEN, STBY Pulldown Resistor	$R_{DISQBAT}$			1000	1200	kΩ
INTERFACE / I2C INTERFACE AND INTERRUPT						
SCL, SDA Input Low Level					0.3 x V_{AVL}	V
SCL, SDA Input High Level			0.7 x V_{AVL}			V
SCL, SDA Input Hysteresis				0.05 x V_{AVL}		V
SCL, SDA Logic Input Current		SDA = SCL = 5.5V	-10		+10	µA
SCL, SDA Input Capacitance				10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
Output High Leakage INTB		V_{INTB} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{INTB} = 5.5V, T_A = +85°C		0.1		
INTERFACE / I²C COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Set-Up Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Set-Up time	$t_{SU;DAT}$		50			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns
INTERFACE / I²C COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Set-Up Time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
INTERFACE / I²C COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. T_A = +25°C (typ). Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

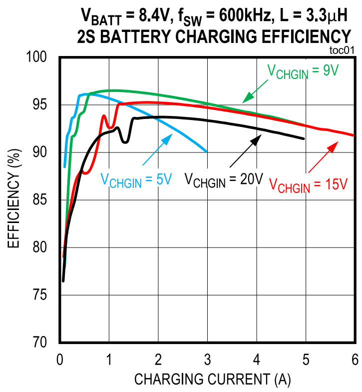
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Set-Up time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns

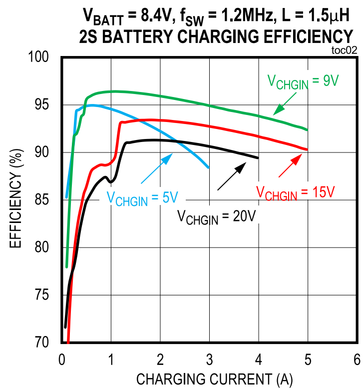
Note 1: Guaranteed by design. Not production tested.

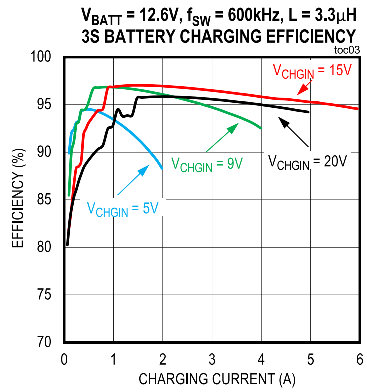
Note 2: Guaranteed by design. Production tested through scan.

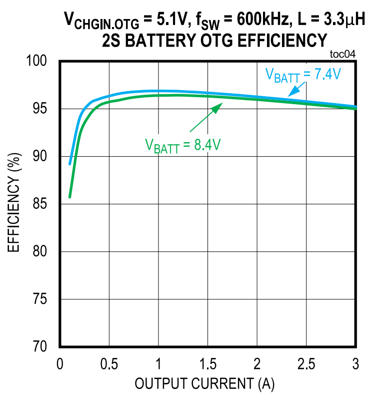
Typical Operating Characteristics

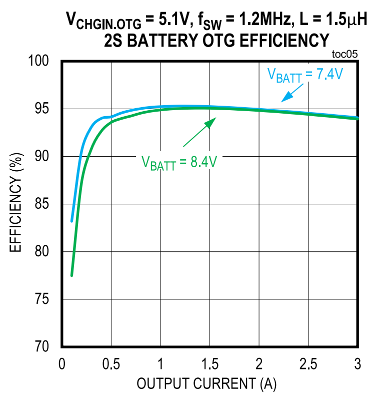
(C_{CHGIN} = 10µF, C_{SYS} = 2 x 47µF, L = 3.3µH (PA5007.332NLT) or 1.5µH (PA5003.152NLT), T_A = +25°C unless otherwise noted.)

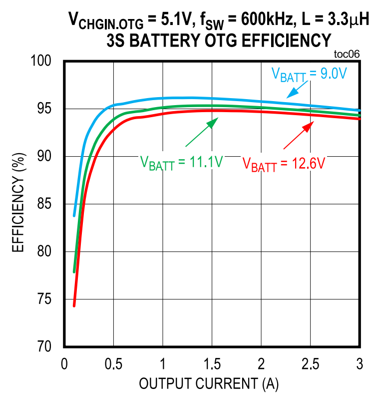






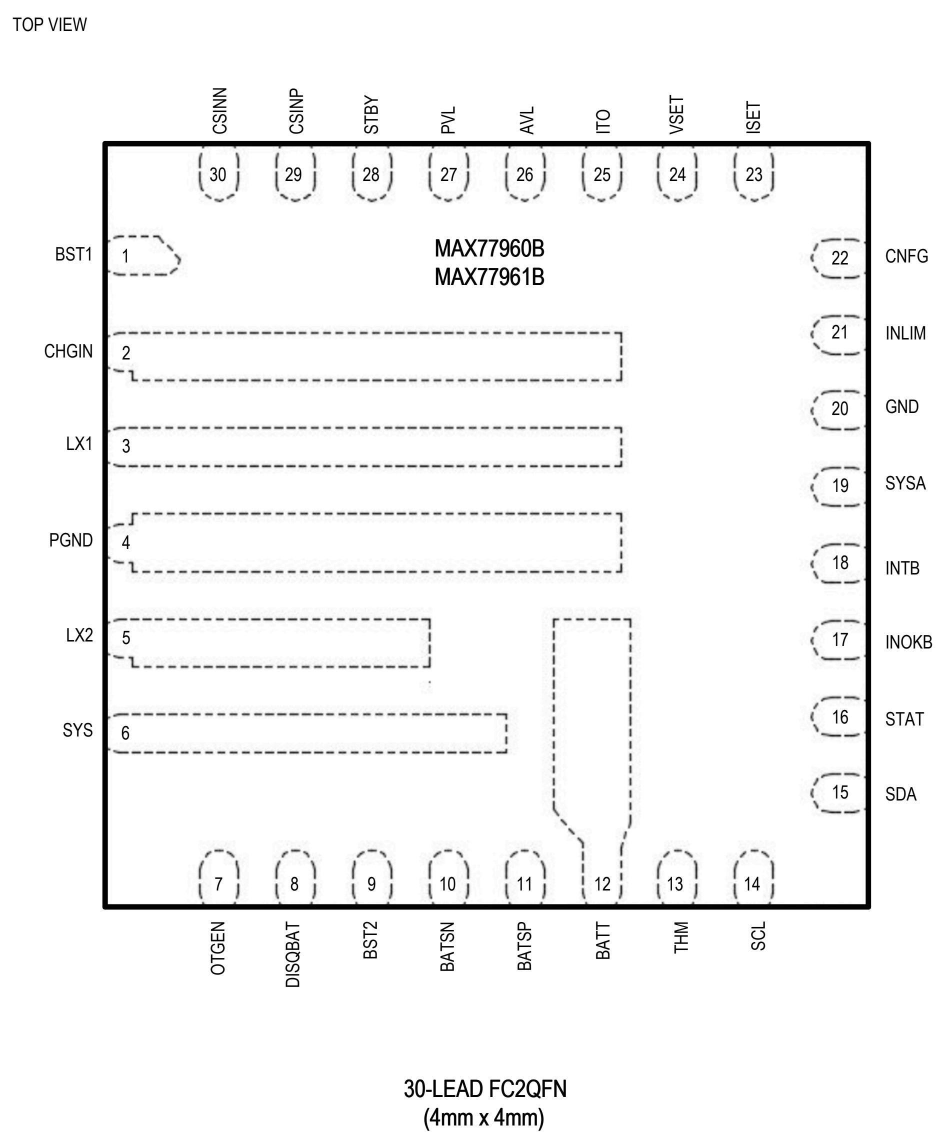






Pin Configuration

MAX77960B/MAX77961B



Pin Description

PIN	NAME	FUNCTION
1	BST1	High-Side Input MOSFET Driver Supply. Bypass BST1 to LX1 with a 0.22µF/6.3V capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
2	CHGIN	Buck-Boost Charger Input. CHGIN is also the buck output when the charger is operating in the reverse mode. Bypass with two 10µF/35V ceramic capacitors from CHGIN to PGND.
3	LX1	Inductor Connection One. Connect an inductor between LX1 and LX2.
4	PGND	Power Ground for Buck-Boost Low-Side MOSFETs
5	LX2	Inductor Connection Two. Connect an inductor between LX1 and LX2.
6	SYS	System Supply Output. Bypass SYS to PGND with a minimum of two 47µF/25V ceramic capacitors.
7	OTGEN	Active-High Input. Connect the OTGEN pin to high enables the OTG function. When OTGEN pin is pulled low, the OTG enable function is controlled by I^2C. To pull the OTGEN pin low with a pulldown resistor, the resistance must be lower than 44kΩ.
8	DISQBAT	Active-High Input. Connect high to disable the integrated Q_{BAT} FET between SYS and BATT. Charging is disabled when DISQBAT connects to high. When DISQBAT is pulled low, Q_{BAT} FET control is defined in the *Q_{BAT} and DC-DC Control—Configuration Table*. To pull the DISQBAT pin low with a pulldown resistor, the resistance must be lower than 44kΩ.
9	BST2	High-Side Output MOSFET Driver Supply. Bypass BST2 to LX2 with a 0.22µF/6.3V capacitor.
10	BATSN	Battery Voltage Differential Sense Negative Input. Connect to the negative terminal of the battery pack.
11	BATSP	Battery Voltage Differential Sense Positive Input. Connect to the positive terminal of the battery pack.
12	BATT	Battery Power Connection. Connect to the positive terminal of the battery pack. Bypass BATT to PGND with a 10µF/25V capacitor. All BATT pins must be connected together externally.
13	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor from THM to GND. Connect a resistor equal to the thermistor +25°C resistance from THM to AVL. JEITA-controlled charging available with JEITA_EN = 1. Charging is suspended when the thermistor voltage is outside of the hot and cold limits. Connect THM to GND to disable the thermistor temperature sensor. Connect THM to AVL to emulate battery removal and prevent charging.
14	SCL	Serial Interface I^2C Clock Input
15	SDA	Serial Interface I^2C Data. Open-drain output.
16	STAT	Charger Status Output. Active-low, open-drain output, connect to the pullup through a 10kΩ resistor. Pulls low when the charging is in progress. Otherwise, STAT is high impedance. STAT toggles between low and high (when connected to a pullup rail) during charge. STAT becomes low when top-off threshold is detected and charger enters the done state. STAT becomes high (when connected to a pullup rail) when charge faults are detected.
17	INOKB	Input Power-OK/OTG Power-OK Output. Active-low, open-drain output pulls low when the CHGIN voltage is valid.
18	INTB	Active-Low Open-Drain Interrupt Output. Connect a pullup resistor to the pullup power source.
19	SYSA	SYS Voltage Sensing Input for SYS UVLO and OVLO Detection
20	GND	Analog Ground
21	INLIM	Charger Input Current Limit Setting Input. Connect a resistor (R_{INLIM}) from INLIM to GND programs the charger input current limit. Refer to Table 5.
22	CNFG	Device Configuration Input. Connect a resistor (R_{CNFG}) from CNFG to GND to program the following parameter, see Table 1. ● Switching frequency (600kHz or 1.2MHz) ● Number of battery cells in series connection (2S or 3S)
23	ISET	Fast-Charge Current Setting Input. Connect a resistor (R_{ISET}) from ISET to GND programs the fast charge current. See Table 6.

Pin Description (continued)

PIN	NAME	FUNCTION
24	VSET	Charge Termination Voltage Setting Input. Connect a resistor (R_{VSET}) from VSET to GND programs the charge termination voltage. See Table 8.
25	ITO	Top-Off Current Setting Input. Connect a resistor (R_{ITO}) from ITO to GND programs the top-off current. See Table 7.
26	AVL	Analog Voltage Supply for On-Chip, Low-Noise Circuits. Bypass with a 4.7μF/6.3V ceramic capacitor to GND and connect AVL to PVL with a 4.7Ω resistor.
27	PVL	Internal Bias Regulator High Current Output Bypass. Supports internal noisy and high current gate drive loads. Bypass to GND with a minimum 4.7μF/6.3V ceramic capacitor, and connect AVL to PVL with a 4.7Ω resistor. Powering external loads from PVL is not recommended, other than pullup resistors.
28	STBY	Active-High Input. Connect high to disable the DC-DC between CHGIN input and SYS output. Battery supplies the system power if the Q_{BAT} is on. See Table 2. Connect low to control the DC-DC with the power-path state machine. To pull the STBY pin low with a pulldown resistor, the resistance must be lower than 44kΩ.
29	CSINP	Input Current-Sense Positive Input
30	CSINN	Input Current-Sense Negative Input

Detailed Description

Charger Configuration

The MAX77960B/MAX77961B are highly flexible, highly integrated switch mode charger. Autonomous charging inputs configure the charger without host I^2C interface, see the *Autonomous Charging* section for more details. The MAX77960B/MAX77961B have an I^2C interface that allows the host controller to program and monitor the charger. Charger configuration registers, interrupt, interrupt mask, and status registers are described in the *Register Map*.

Device Configuration Input (CNFG)

CNFG is the MAX77960B/MAX77961B's configuration input for the following parameters:

- Switching frequency (600kHz or 1.2MHz)
- Number of battery cells in series connection (2S or 3S)

Connect a resistor (R_{CNFG}) from CNFG to GND to program. See Table 1. Note that for 1.2MHz switching frequency, only 2S battery is supported.

Table 1. CNFG Program Options Lookup Table

PART NUMBER	SWITCHING FREQUENCY (MHz)	NUMBER OF SERIES BATTERY CELLS	R_{CNFG} (Ω)
MAX77960BEFV06+ MAX77961BEFV06+	0.6	2	Tied to PVL or 86600
		3	8660
MAX77960BEFV12+ MAX77961BEFV12+	1.2	2	Tied to PVL or 69800

CHGIN Standby Input (STBY)

The host can reduce the MAX77960B/MAX77961B's CHGIN supply current by driving STBY pin to high or setting STBY_EN bit to 1. When STBY is pulled high or STBY_EN bit is set to 1, the DC-DC turns off. When STBY is pulled low and STBY_EN bit is set to 0, the DC-DC is controlled by the power-path state machine. To pull the STBY pin low with a pulldown resistor, the resistance must be lower than 44kΩ.

Battery to SYS Q_{BAT} Disable Input (DISQBAT)

The host can disable the Q_{BAT} switch by setting DISIBS bit to 1 or driving DISQBAT pin to high. Charging stops when Q_{BAT} switch is disabled.

When DISQBAT is pulled low and DISIBS bit is set to 0, Q_{BAT} FET control is defined in Table 2. To pull the DISQBAT pin low with a pulldown resistor, the resistance must be lower than 44kΩ.

Q_{BAT} and DC-DC Control—Configuration Table

The Q_{BAT} control and the DC-DC control depend on both hardware pins (OTGEN, DISQBAT, and STBY) and their associated I^2C registers.

Table 2. Q_{BAT} and DC-DC Control Configuration Table

OTGEN (PIN) OR MODE [3:0] = 0xA (I^2C)	DISQBAT (PIN) OR DISIBS (I^2C)	STBY (PIN) OR STBY_EN (I^2C)	Q_{BAT}	DC-DC
0	0	0	Power-path state machine/internal logic control	Power-path state machine/internal logic control

Table 2. Q_{BAT} and DC-DC Control Configuration Table (continued)

OTGEN (PIN) OR MODE [3:0] = 0xA (I^2C)	DISQBAT (PIN) OR DISIBS (I^2C)	STBY (PIN) OR STBY_EN (I^2C)	Q_{BAT}	DC-DC
0	0	1	Enable (SYS is powered from battery through Q_{BAT} switch while DC-DC is disabled)	Disable
0	1	0	Disable	Power-path state machine/internal logic control
0	1	1	Disable (SYS is powered from battery through Q_{BAT} body diode while DC-DC is disabled)	Disable
1	x	x	Enable	Power-path state machine/internal logic control

Thermistor Input (THM)

The thermistor input can be utilized to achieve functions that include charge suspension, JEITA-compliant charging, and battery removal detection. Thermistor monitoring feature can be disabled by connecting the THM pin to ground.

Charge Suspension

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature. Charging stops when the thermistor temperature is out of range ($T < T_{COLD}$ or $T > T_{HOT}$). The charge timers are reset and the CHG_DTLS[3:0], CHG_OK register bits report the charging suspension status and CHG_I interrupt bit is set. When the thermistor comes back into range ($T_{COLD} < T < T_{HOT}$), charging resumes and the charge timer restarts.

JEITA-Compliant Charging

JEITA-compliant charging is available with JEITA_EN = 1. See the *JEITA Compliance* section for more details.

Battery Removal Detection

Connecting THM to AVL emulates battery removal and prevents charging.

Disable Thermistor Monitoring

Connecting THM to GND disables the thermistor monitoring function, and JEITA-controlled charging is unavailable in this configuration. The MAX77960B/MAX77961B detect an always-connected battery when THM is grounded, and charging starts automatically when a valid adapter is plugged in. In applications with removable batteries, do not connect THM to GND because the MAX77960B/MAX77961B cannot detect battery removal when THM is grounded. Instead, connecting THM to the thermistor pin in the battery pack is recommended.

Since the thermistor monitoring circuit employs an external bias resistor from THM to AVL, the thermistor is not limited only to 10kΩ (at +25ºC). Any resistance thermistor can be used as long as the value is equivalent to the thermistors +25ºC resistance. For example, with a 10kΩ at R_{TB} resistor, the charger enters a temperature suspend state when the thermistor resistance falls below 3.97kΩ (too hot) or rises above 28.7kΩ (too cold). This corresponds to 0ºC to +50ºC range when using a 10kΩ NTC thermistor with a beta of 3500. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} x e^{\{\beta x (\frac{1}{T + 273^\circ C} - \frac{1}{298^\circ C})\}}$$

where:

R_T = The resistance in Ω of the thermistor at temperature T in Celsius

R_{25} = The resistance in Ω of the thermistor at +25ºC

β = The material constant of the thermistor, which typically ranges from 3000k to 5000k

T = The temperature of the thermistor in °C

Some designs might prefer other thermistor temperature limits. Threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with different β. For example, a +45ºC hot threshold and 0°C cold threshold can be realized by using a thermistor with a β to 4250 and connecting 120kΩ in parallel. Since the thermistor resistance near 0ºC is much higher than it is near +50ºC, a large parallel resistance lowers the cold threshold, while only slightly lowering the hot threshold. Conversely, a small series resistance raises the cold threshold, while only slightly raising the hot threshold. Raising R_{TB} raises both the hot and cold threshold, while lowering R_{TB} lowers both thresholds.

Since AVL is active whenever a valid power is provided at CHGIN or BATT, thermistor bias current flows at all times, even when charging is disabled. When using a 10kΩ thermistor and a 10kΩ pullup to AVL, this results in an additional 90µA load. This load can be reduced to 9µA by instead using a 100kΩ thermistor and 100kΩ pullup resistor.

Table 3. Trip Temperatures for Different Thermistors

THERMISTOR					TRIP TEMPERATURES			
R_{25} (Ω)	β	R_{TB} (Ω)	R_{15} (Ω)	R_{45} (Ω)	T_{COLD} (˚C)	T_{COOL} (˚C)	T_{WARM} (˚C)	T_{HOT} (˚C)
10000	3380	10000	14826	4900	-0.8	+14.7	+42.6	+61.4
10000	3940	10000	15826	4354	+2.6	+16.1	+40.0	+55.7
47000	4050	47000	75342	19993	+3.2	+16.4	+39.6	+54.8
100000	4250	100000	164083	40781	+4.1	+16.8	+38.8	+53.2

Autonomous Charging

The MAX77960B/MAX77961B support autonomous charging without I^2C. In applications without I^2C serial communication, use the following pins to configure the MAX77960B/MAX77961B charger:

CNFG, INLIM, ITO, ISET, VSET, OTGEN, DISQBAT, STBY.

The INLIM, ITO, ISET, and VSET pins are used to program the charger's input current limit, top-off current, constant charging current, and termination voltage.

Connect a valid resistor from each of these pins to ground to program the charger. See the *Pin Description* for details.

Connect all four pins (INLIM, ITO, ISET, VSET) to PVL to use the default values for the associated charger registers.

For autonomous charging, it is considered an abnormal condition if some of these pins (INLIM, ITO, ISET, VSET) connect to a valid resistor, but others do not (for example open or connects to PVL or connects to a resistor that is out of range). When this happens, the MAX77960B/MAX77961B allow the DC-DC to switch and regulate the SYS voltage, but disable charging for safety reasons. The STAT pin reports no charge.

Table 4. INLIM, ITO, ISET, and VSET Pin Connections for Autonomous Charging

INLIM PIN	ITO PIN	ISET PIN	VSET PIN	AUTONOMOUS CHARGING
Valid resistor	Valid resistor	Valid resistor	Valid resistor	Normal, charger configuration is programmed by resistors
Tied to PVL	Tied to PVL	Tied to PVL	Tied to PVL	Normal, charger configuration uses default values
All other connections				Abnormal, no charging

Charger Input Current Limit Setting Input (INLIM)

When a valid charge source is applied to CHGIN, the MAX77960B/MAX77961B limit the current drawn from the charge source to the value programmed with INLIM pin.

The default charger input current limit is programmed with the resistance from INLIM to GND. See Table 5.

If I^2C is used in the application, the CHGIN input current limit can also be reprogrammed with CHGIN_ILIM[6:0] register bits after the devices power up. Connect INLIM pin to PVL to use I^2C default settings.

Table 5. INLIM Program Options Lookup Table

R_{INLIM} (Ω)	MAX77960B CHGIN INPUT CURRENT LIMIT (mA) DEFAULT VALUE OF CHGIN_ILIM[6:0]	MAX77961B CHGIN INPUT CURRENT LIMIT (mA) DEFAULT VALUE OF CHGIN_ILIM[6:0]
Tied to PVL	500	500
226000	100	100
178000	200	200
140000	300	300
110000	400	400
86600	500	500
69800	1000	1000
54900	1500	1500
39200	2000	2000
22600	2500	2500
17800	3000	3000
14000	N/A	3500
11000	N/A	4000
8660	N/A	4500
6980	N/A	5000
5490	N/A	6000

Fast-Charge Current Setting Input (ISET)

When a valid input source is present, the battery charger attempts to charge the battery with a fast-charge current programmed with ISET pin.

The default fast-charge current is programmed with the resistance from ISET to GND. See Table 6.

If I^2C is used in the application, the fast-charge current can also be reprogrammed with CHGCC[5:0] register bits after the devices power up. Connect ISET pin to PVL to use I^2C default settings.

Table 6. ISET Program Options Lookup Table

R_{ISET} (Ω)	MAX77960B FAST-CHARGE CURRENT SELECTION (mA) DEFAULT VALUE OF CHGCC[5:0]	MAX77961B FAST-CHARGE CURRENT SELECTION (mA) DEFAULT VALUE OF CHGCC[5:0]
Tied to PVL	450	450
226000	100	100

Table 6. ISET Program Options Lookup Table (continued)

R_{ISET} (Ω)	MAX77960B FAST-CHARGE CURRENT SELECTION (mA) DEFAULT VALUE OF CHGCC[5:0]	MAX77961B FAST-CHARGE CURRENT SELECTION (mA) DEFAULT VALUE OF CHGCC[5:0]
178000	200	200
140000	300	300
110000	400	400
86600	500	500
69800	1000	1000
54900	1500	1500
39200	2000	2000
22600	2500	2500
17800	3000	3000
14000	N/A	3500
11000	N/A	4000
8660	N/A	4500
6980	N/A	5000
5490	N/A	6000

Top-Off Current Setting Input (ITO)

When the battery charger is in the top-off state, the top-off charge current is programmed by ITO pin.

The default top-off charge current is programmed with the resistance from ITO to GND. See Table 7.

If I^2C is used in the application, the top-off current can also be reprogrammed with TO_ITH[2:0] register bits after the device powers up. Connect ITO pin to PVL to use I^2C default settings.

Table 7. ITO Program Options Lookup Table

R_{ITO} (Ω)	TOP-OFF CURRENT THRESHOLD (mA) DEFAULT VALUE OF TO_ITH[2:0]
Tied to PVL	100
226000	100
178000	200
140000	300
110000	400
86600	500
69800	600

Charge Termination Voltage Setting Input (VSET)

The default charge termination voltage is programmed with the resistance from VSET to GND. See Table 8.

If I^2C is used in the application, the charge termination voltage can also be reprogrammed with CHG_CV_PRM[5:0] register bits after the device powers up. Connect the VSET pin to PVL to use I^2C default settings.

Table 8. VSET Program Options Lookup Table

R_{VSET} (Ω)	CHARGE TERMINATION VOLTAGE SETTING - 2S (V) DEFAULT VALUE OF CHG_CV_PRM[5:0]	CHARGE TERMINATION VOLTAGE SETTING - 3S (V) DEFAULT VALUE OF CHG_CV_PRM[5:0]
Tied to PVL	8.0	12.0
226000	8.0	12.0
178000	8.1	12.15
140000	8.2	12.3
110000	8.3	12.45
86600	8.4	12.6
69800	8.5	12.75
54900	8.6	12.9
39200	8.7	13.05
22600	8.8	N/A
17800	8.9	N/A
14000	9.0	N/A
11000	9.1	N/A
8660	9.2	N/A
6980	9.26	N/A
5490	9.26	N/A

Switch Mode Charger

The MAX77960B/MAX77961B feature a switch mode buck-boost charger for a two-cell or three-cell lithium ion (Li+) or lithium polymer (Li-polymer) battery. The charger operates from a wide input range from 3.5V to 25.4V, ideal for USB-C charging applications. The charger input current limit is programmable from 100mA to 3.15A (MAX77960B)/100mA to 6.3A (MAX77961B), which is flexible to operate from either an AC-to-DC wall charger or a USB-C adapter.

The MAX77960B/MAX77961B offer a high level of integration and do not require any external MOSFETs to operate, which significantly reduces the solution size. They operate with a programmable switching frequency of 600kHz or 1.2MHz, which is ideal for portable devices that benefit from small solution size and high efficiency. The battery charging current is programmable from 100mA to 3A (MAX77960B)/100mA to 6A (MAX77961B) to accommodate small or large capacity batteries.

When the input source is not available, the MAX77960B/MAX77961B can be enabled in a reverse buck mode, delivering energy from the battery to the input, CHGIN, commonly known as USB on-the-go (OTG). In OTG mode, the regulated CHGIN voltage is 5.1V with programmable current limit up to 3A.

Maxim's Smart Power Selector architecture makes the best use of the limited adapter power and the battery power to power the system. Adapter power that is not used for the system charges the battery. When system load exceeds the input limit, battery provides additional current to the system up to the BATT to SYS overcurrent threshold, programmable with B2SOVRC[3:0] I^2C register bits. All power switches for charging and switching the system load between battery and adapter power are integrated on chip—no external MOSFETs required.

Maxim's proprietary process technology allows for low-R_{DSON} devices in a small solution size. The resistance between BATT and SYS is 10mΩ (typ), allowing low power dissipation and long battery life.

A multitude of safety features ensure reliable charging. Features include charge timers, watchdog, junction thermal regulation, and over-/undervoltage protection.

Smart Power Selector (SPS)

The smart power selector (SPS) architecture includes a network of internal switches and control loops that efficiently distributes energy between an external power source (CHGIN), the battery (BAT) and the system (SYS). This architecture allows power path operation with system instant on with a dead battery.

The *Simplified Block Diagram* shows the smart power selector switches and gives them the following names: Q_1, Q_2, Q_3, Q_4 and Q_{BAT}.

Power Switches and Current Sense Resistor Descriptions

- CHGIN Current-Sense Resistor: As shown in the *Simplified Block Diagram*, the CHGIN current is monitored with the input current sensing resistor, R_{S1}, connected between CSINP and CSINN pins.
- DC-DC Switches: Q_1, Q_2, Q_3, and Q_4 are the DC-DC switches that can operate as a buck (step down) or a boost (step up), depending on the external power source and battery voltage conditions.
- Battery-to-System Switch: Q_{BAT} is used to control battery charging and discharging operations.

I²C Configuration Register Bits

- MODE[3:0] configures the Smart Power Selector mode to be Charging, OTG or DC-DC mode respectively. See MODE[3:0] register bits in the *Register Map* for details.
- VCHGIN_REG[4:0] sets the CHGIN regulation voltage, when the MAX77960B/MAX77961B operate in forward mode (CHGIN has a valid power source). See the *CHGIN Regulation Voltage* section for details.
- MINVSYS[2:0] sets the minimum system regulation voltage. See the *SYS Regulation Voltage* section for details.
- B2SOVRC[3:0] sets the battery to system discharge overcurrent protection threshold.

Energy Distribution Priority

- With a valid external power source at CHGIN:
  - The external power source is the primary source of energy.
  - The battery is the secondary source of energy.
  - Energy delivery to SYS has the highest priority.
  - Any remaining energy from the power source that is not required by the system is available to the battery charger.
- With no valid external power source at CHGIN:
  - The battery is the primary source of energy.
  - When OTG mode is enabled, energy delivery to SYS has the highest priority.
  - Any remaining energy from the battery that is not required by the system is available to power the CHGIN.

CHGIN Regulation Voltage

- In forward mode (when CHGIN is powered from a valid external source), CHGIN voltage is regulated to VCHGIN_REG[4:0] when a high impedance or current limited source is applied. VCHGIN might experience significant voltage droop from the high-impedance source when the MAX77960B/MAX77961B extract high power from the source. Regulating VCHGIN allows the MAX77960B/MAX77961B to extract the most power from the power source. See the *Adaptive Input Current Limit (AICL) and Input Voltage Regulation* section for more detail.
- In reverse mode (OTG), CHGIN voltage is regulated to 5.1V with programmable current limit up to 3A (OTG_ILIM[2:0]).

SYS Regulation Voltage

With a valid external power source at CHGIN:

- When the DC-DC is disabled (MODE[3:0] = 0x00 or STBY_EN = 0b1 or STBY pin = high), the Q_{BAT} switch is fully on and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$.
- When the DC-DC is enabled and the charger is disabled (MODE[3:0] = 0x04), V_{SYS} is regulated to $V_{BATTREG}$ (CHG_CV_PRM) and Q_{BAT} is off.
- When the DC-DC is enabled and the charger is enabled (MODE[3:0] = 0x05), but in a noncharging state such as Done, Thermistor Suspend, Watchdog Suspend, or Timer Fault, V_{SYS} is regulated to $V_{BATTREG}$ (CHG_CV_PRM) and Q_{BAT} is off.
- When the DC-DC is enabled and the charger is enabled (MODE[3:0] = 0x05) and in a valid charging state such as

Precharge or Trickle Charge ($V_{BATT} < V_{SYSMIN}$ - 500mV), V_{SYS} is regulated to $V_{BATTREG}$ (CHG_CV_PRM). The charger operates as a linear regulator, and the power dissipation can be calculated with P = ($V_{BATTREG}$ - V_{BATT}) x I_{BATT}.

- When the DC-DC is enabled and the charger is enabled (MODE[3:0] = 0x05) and in a valid charging state such as Fast Charge (CC or CV) or Top-Off ($V_{BATT} > V_{SYSMIN}$ - 500mV), the Q_{BAT} switch is fully on, and $V_{SYS} = V_{BATT} + I_{BATT} \times R_{BAT2SYS}$.
- In all the modes described above when the power demand on SYS exceeds the input source power limit, the battery automatically provides supplemental power to the system. If the Q_{BAT} switch is initially off when V_{SYS} drops to $V_{BATT} - V_{BSREG}$, the Q_{BAT} switch turns on, and V_{SYS} is regulated to $V_{BATT} - V_{BSREG}$.

Without a valid external power source at CHGIN, including with OTG mode (MODE[3:0] = 0x0A):

- The Q_{BAT} switch is fully on, and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$.

Power States

The MAX77960B/MAX77961B transition between power states as input/battery and load conditions dictate.

The MAX77960B/MAX77961B provide four (4) power states and one (1) no power state. Under power limited conditions, the power path feature maintains SYS and USB-OTG loads at the expense of battery charge current. In addition, the battery supplements the input power when needed. See the *Smart Power Selector (SPS)* section for more details. As shown, transitions between power states are initiated by detection/removal of valid power sources, OTG events, and undervoltage conditions.

1. NO INPUT POWER, *MODE[3:0] = undefined*: No input adapter or battery is detected. The charger and system are off. Battery is disconnected.

2. BATTERY-ONLY, *MODE[3:0] = any mode*: CHGIN is invalid or outside the input voltage operating range. Battery is connected to power the SYS load (Q_{BAT} = on).

3. NO CHARGE - DC-DC in FORWARD mode, *MODE[3:0] = 0x04*: CHGIN input is valid, DC-DC supplies power to SYS. DC-DC operates from a valid input. Battery is disconnected (Q_{BAT} = off) when SYS load is less than the power that DC-DC can supply.

4. CHARGE - DC-DC in FORWARD mode, *MODE[3:0] = 0x05*: CHGIN input is valid, DC-DC supplies power to SYS and charges the battery with IBATT. DC-DC operates from a valid input.

5. OTG - DC-DC in REVERSE mode (OTG), *MODE[3:0] = 0x0A*: OTG is active. Battery is connected to support SYS and OTG loads (Q_{BAT} = on), and charger operates in REVERSE buck mode.

Powering Up with the Charger Disabled by Default

The MAX77960B/MAX77961B's default power state is CHARGE - DC-DC in FORWARD mode, MODE[3:0] = 0x05. For battery authentication/safety purposes, the MAX77960B/MAX77961B can be configured to keep charging disabled while allowing the DC-DC to switch and regulate the SYS voltage when power is applied to CHGIN. To implement this and enable the charger when appropriate:

- Connect at least one of the INLIM, ITO, ISET or VSET pins to a valid resistor while tying the others (at least one) to PVL. CHG_DTLS = 0x05 and CHG_OK = 0.
- The system processor can configure the charger through the I^2C interface.
- The system processor enables charging by setting COMM_MODE to 1 (default is 0).

See *Wide-Input I^2C Programmable Charger with Charger Disabled* for a pin connection example. Pin INLIM is connected to a valid resistor while ITO, ISET and VSET tie to PVL. The default input current limit is programmed by R_{INLIM}, while default top-off current, constant charging current, and termination voltage use their default value. The system processor can re-program all four settings through the I^2C interface if needed.

Input Validation

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following characteristics to be valid:

- CHGIN must be above V_{CHGIN_UVLO} to be valid. Once CHGIN is above UVLO threshold, the information is latched and can only be reset when charger is in adaptive input current loop (AICL) and input current is lower than IULO threshold of 30mA.
- CHGIN must be below its overvoltage lockout threshold (V_{CHGIN_OVLO}).

The devices generate a CHGIN_I interrupt (maskable with CHGIN_M bit) when the CHGIN status changes. Read the CHGIN input status with CHGIN_OK and CHGIN_DTLS[1:0] register bits.

Adaptive Input Current Limit (AICL) and Input Voltage Regulation

The MAX77960B/MAX77961B feature input power management to extract maximum input power while avoiding input source overload. The adaptive input current limit (AICL) and the input voltage regulation (CHGIN_REG) features allow the charger to extract more energy from relatively high resistance charge sources with long cables, noncompliant USB hubs or current limited adapters. In addition, the input power management allows the MAX77960B/MAX77961B to perform well with adapters that have poor transient load responses.

With a high-resistance source, the charger input voltage drops substantially when it draws large current from the source. The charger's input voltage regulation loop automatically reduces the current drawn from the input to regulate the input voltage at V_{CHGIN_REG}. If the input current is reduced to $I_{CHGIN\_REG\_OFF}$ (50mA typ) and the input voltage is still below V_{CHGIN_REG}, the charger input turns off. V_{CHGIN_REG} is programmable with VCHGIN_REG[4:0] register bits.

With a current limited source, if the MAX77960B/MAX77961B's input current limit is programmed above the current limit of the adapter, the charger input voltage starts to drop when the input current drawn exceeds the source current limit. The charger's input voltage regulation loop allows the MAX77960B/MAX77961B to reduce its input current and operate at the current limit of the adapter.

When operating with the input voltage regulation loop active, an AICL_I interrupt is generated, AICL_OK sets to 0. The device prioritize system energy delivery over battery charging. See the *Smart Power Selector (SPS)* section for more details.

To extract most input power from a current limited charge source, monitor the AICL_OK status while decreasing the CHGIN_ILIM[6:0] register setting. Setting the CHGIN_ILIM[6:0] to a reduced to a value below the current limit of the adapter causes the input voltage to rise. Although the CHGIN_ILIM[6:0] is lowered, more power can be extracted from the adapter when the input voltage rises.

Input Self-Discharge

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed, the input voltage decays below the UVLO threshold in a reasonable time (t_{INSD}). The input self-discharge is implemented by with a 44kΩ resistor (R_{INSD}) from CHGIN input to ground.

System Self-Discharge with No Power

To ensure a timely, complete, repeatable, and reliable reset behavior when the system has no power, the MAX77960B/MAX77961B actively discharge the BATT and SYS nodes when the adapter is missing, the battery is removed and V_{SYS} is less than $V_{SYSUVLO}$. The BATT and SYS discharge resistors are both 600Ω.

Charger States

The MAX77960B/MAX77961B utilize several charging states to safely and quickly charge batteries as shown in Figure 1 and Figure 2. Figure 1 shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery are close to room temperature: Prequalification → Fast-charge → Top-off → Done.

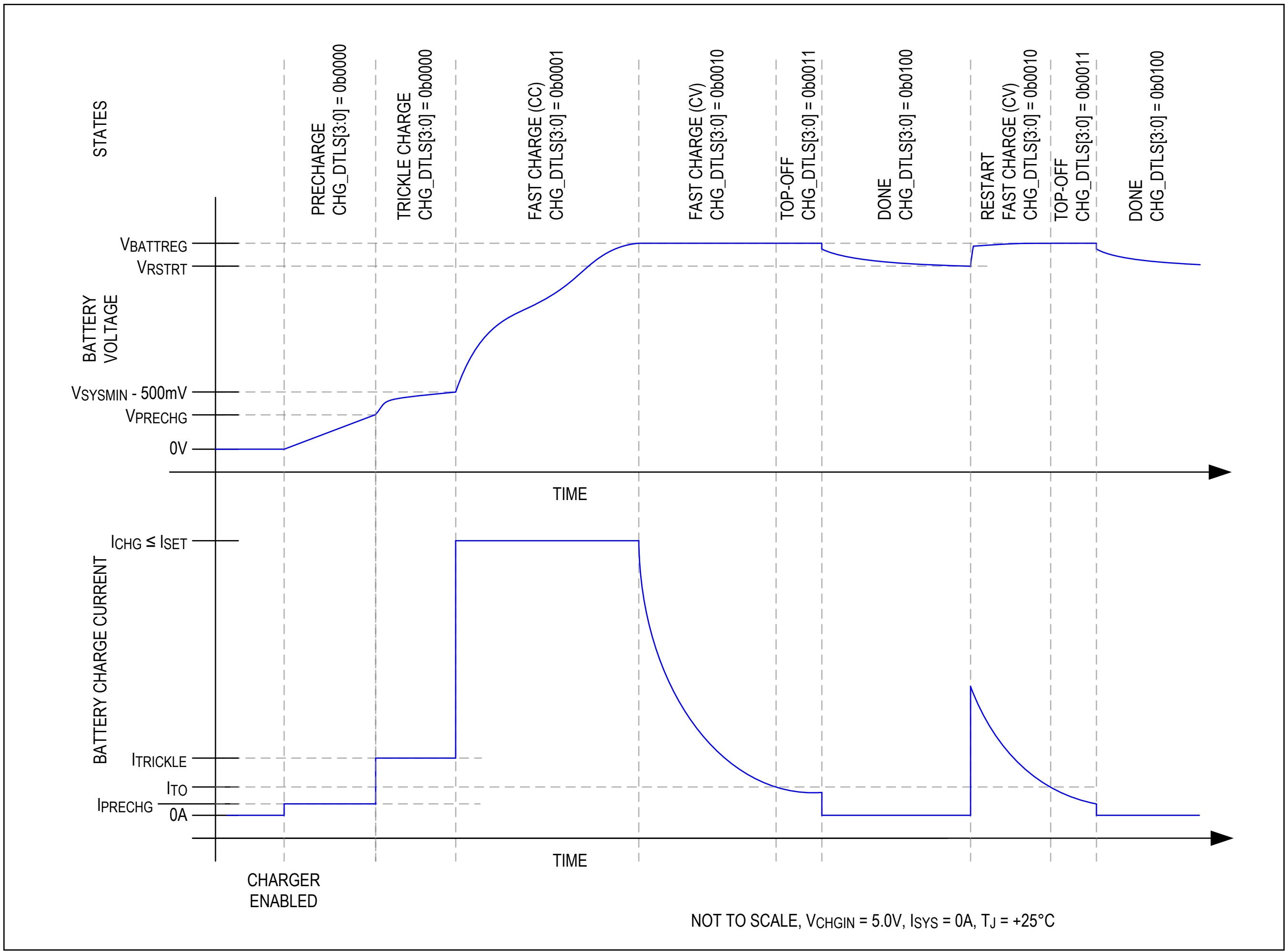


Figure 1. Li Battery Charge Profile

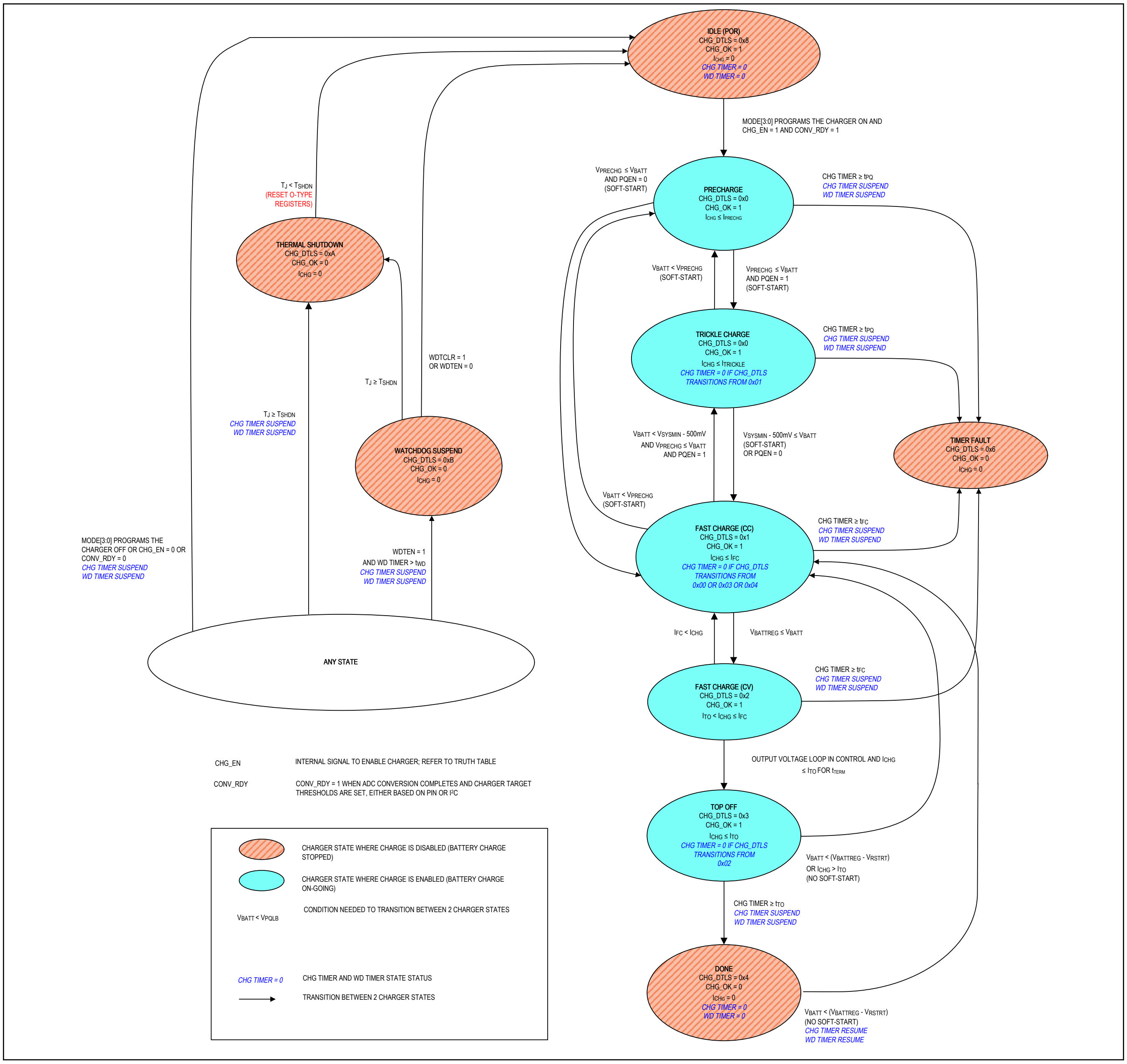


Figure 2. Charger State Diagram

No Input Power or Charger Disabled Idle State

From any state shown in Figure 2 except thermal shutdown, the no input power or charger disabled state is entered whenever the charger is programmed to be off or the charger input CHGIN is invalid. After being in this state for t_{SCIDG}, CHG_DTLS is set to 0x08 and CHG_OK is set to 1. A CHG_I interrupt is generated if CHG_OK was 0 previously.

While in the no input power or charger disabled state, the charger current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power are available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary.

To exit the no input power or charger disabled state, the charger input must be valid and the charger must be enabled.

Precharge State

As shown in Figure 2, the charger enters the precharge state when the battery voltage is less than V_{PRECHG}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1 and CHG_DTLS is set to 0x00. In the precharge state, charge current into the battery is I_{PRECHG}.

The following events cause the state machine to exit this state:

- Battery voltage rises above V_{PRECHG} and the charger enters the next state in the charging cycle: Trickle Charge.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the Timer Fault state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note that the precharge state works with battery voltages down to 0V. The 0V operation typically allows this battery charger to recover batteries that have an open internal pack protector. Typically, a battery pack's internal protection circuit opens if the battery has seen an overcurrent, undervoltage, or overvoltage. When a battery with an open internal pack protector is used with this charger, the precharge mode current flows into the 0V battery; this current raises the pack’s terminal voltage to the level where the internal pack protection switch closes.

Note that a normal battery typically stays in the precharge state for several minutes or less. Therefore a battery that stays in the precharge for longer than t_{PQ} might be experiencing a problem.

Trickle Charge State

As shown in Figure 2, the charger state machine is in trickle charge state when $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$ - 500mV. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1 and CHG_DTLS = 0x00.

With PQEN = 1 (default) and the MAX77960B/MAX77961B are in the trickle charge state, the current in the battery is less than or equal to ITRICKLE. When PQEN = 0, the charger skips trickle charge state and transitions directly to fast charge state and the battery charging current is less than or equal to I_{FC}.

Charge current may be less than $I_{TRICKLE}/I_{FC}$ for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Typical systems operate with PQEN = 1. When operating with PQEN = 0, the system’s software usually sets I_{FC} to a low value such as 200mA and then monitors the battery voltage. When the battery exceeds a relatively low voltage such as 6V, then the system’s software usually increases I_{FC}.

The following events cause the state machine to exit this state:

- When the battery voltage rises above V_{SYSMIN} - 500mV or the PQEN bit is cleared, the charger enters the next state in the charging cycle: Fast Charge (CC).
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the Timer Fault state.
- If the watchdog timer is not serviced, the charger state machine transitions to the Watchdog Suspend state.

Note that a normal battery typically stays in the trickle charge state for several minutes or less. Therefore, a battery that stays in trickle charge for longer than t_{PQ} might be experiencing a problem.

Fast-Charge Constant Current State

As shown in Figure 2, the charger enters the fast-charge constant current (CC) state when V_{SYSMIN} - 500mV (typ) < $V_{BATT} < V_{BATTREG}$. After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1 and CHG_DTLS = 0x01.

In the fast-charge CC state, the battery charging current is less than or equal to I_{FC}. Charge current can be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charging current.

The following events cause the state machine to exit this state:

- When the battery voltage rises above $V_{BATTREG}$, the charger enters the next state in the charging cycle: Fast Charge (CV).
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the Timer Fault state.
- If the watchdog timer is not serviced, the charger state machine transitions to the Watchdog Suspend state.

The battery charger dissipates the most power in the fast-charge constant current state, which causes the die temperature to rise. If the die temperature exceeds T_{REG}, the thermal foldback loop is engaged and I_{FC} is reduced. See the *Thermal Foldback* section for more information.

Fast-Charge Constant Voltage State

As shown in Figure 2, the charger enters the fast-charge constant voltage (CV) state when the battery voltage rises to $V_{BATTREG}$ from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1 and CHG_DTLS = 0x02.

In the fast-charge CV state, the battery charger maintains $V_{BATTREG}$ across the battery and the charge current is less than or equal to I_{FC}. As shown in Figure 1, charger current decreases exponentially in this state as the battery becomes fully charged.

The smart power selector control circuitry can reduce the charge current for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the charger current is below I_{TO} for t_{TERM}, the charger enters the *Top-Off State.*
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the *Timer Fault State*.
- If the watchdog timer is not serviced, the charger state machine transitions to the *Watchdog Timer Suspend State*.

Top-Off State

As shown in Figure 2, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x03. In the top-off state the battery charger maintains $V_{BATTREG}$ across the battery and typically the charge current is less than or equal to I_{TO}.

The smart power selector control circuitry can reduce the charge current for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the top-off time (t_{TO}), the charger enters the *Done State*.
- If V_{BATT} < $V_{BATTREG}$ - V_{RSTRT}, the charger goes back to the *Fast-Charge Constant Current State*.
- If the watchdog timer is not serviced, the charger state machine transitions to the *Watchdog Timer Suspend State.*

Done State

As shown in Figure 2, the battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 0 and CHG_DTLS = 0x04.

The following events cause the state machine to exit this state:

- If V_{BATT} < $V_{BATTREG}$ - V_{RSTRT}, the charger goes back to the *Fast-Charge Constant Current State*.
- If the watchdog timer is not serviced, the charger state machine transitions to the *Watchdog Timer Suspend State*.

In the done state, the battery charging current (I_{CHG}) is 0A and the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low (<< 100μA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the charging restart threshold (V_{RSTRT}) and the charger state machine transitions back into the fast-charge CC state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 2, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC}, which is programmable with FCHGTIME. Finally the time that the charger is in the top-off state is t_{TO} which is programmable with TO_TIME. Upon entering the timer fault state a CHG_I interrupt is generated without a delay, CHG_OK is cleared and CHG_DTLS = 0x06.

The charger is off in the timer fault state. The charger can exit the timer fault state when the charger is programmed to be off then on again through the MODE bits or when DISQBAT pin is toggled from L-H-L. Alternatively, the charger input can be removed and reinserted to exit the timer fault state (see the ANY STATE bubble in Figure 2).

Watchdog Timer Suspend State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 2, the watchdog timer protects the battery from charging indefinitely in the event that the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. Enable the feature by setting WDTEN = 1. With watchdog timer enabled, the host controller must reset the watchdog timer within the timer period (t_{WD}) in order for the charger to operate properly. Reset the watchdog timer by programming WDTCLR = 0x01.

If the watchdog timer expires, charging stops, a CHG_I interrupt is generated if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS indicates that the charger is off because the watchdog timer expired. Once the watchdog timer expires, the charger can be restarted by programming WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer is expired.

Thermal Shutdown State

As shown in Figure 2, the state machine enters the thermal shutdown state when the junction temperature (T_J) exceeds the device's thermal shutdown threshold (T_{SHDN}). When T_J is close to T_{SHDN}, the charger would have already folded back the input current to 0A, (see the *Thermal Foldback* section for more details), so the charger and the DC-DC are effectively off. Upon entering this state, CHG_I interrupt is generated if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS = 0x0A.

In the thermal shutdown state, the charger is off. MODE register (CHG_CNFG_00[3:0]) is reset to its default value as well as all O type registers.

Thermal Management

The MAX77960B/MAX77961B charger use several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the MAX77960B/MAX77961B junction temperature. As shown in Figure 3, when the die temperature exceeds the value programmed by REGTEMP (T_{REG}), a thermal limiting circuit reduces the battery charger's target current by 5%/°C (A_{TJREG}) with an analog control loop. When the charger transitions in and out of the thermal foldback loop, a CHG_I interrupt is generated and the host microprocessor can read the status of the thermal regulation loop with the TREG status bit. Note that an active thermal foldback loop is not an abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

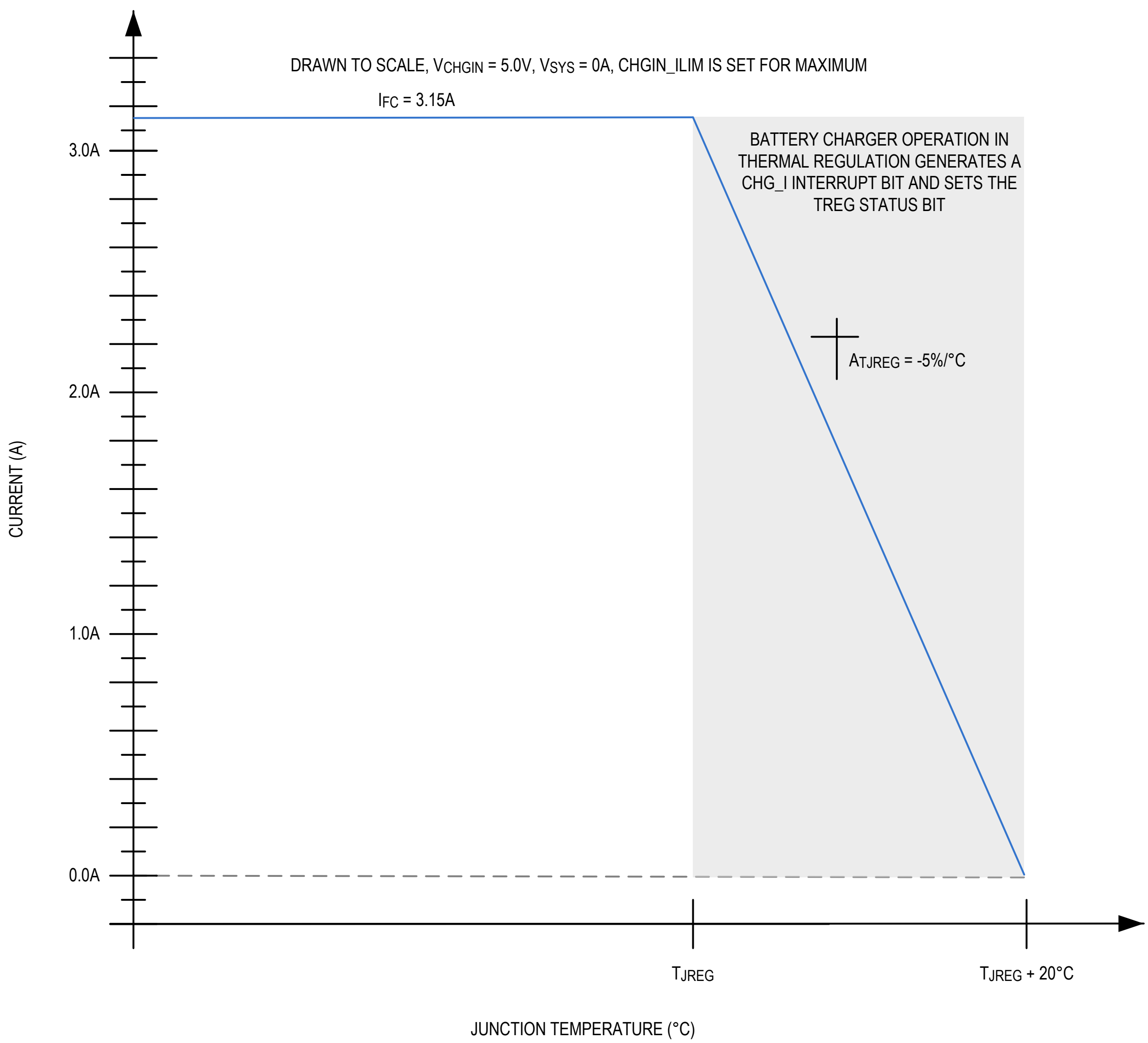


Figure 3. Charge Currents vs. Junction Temperature

JEITA Compliance

The MAX77960B/MAX77961B safely charge Li+ batteries in accordance with JEITA specifications. The MAX77960B/MAX77961B monitor the battery temperature with a NTC thermistor connected at THM pin and automatically adjust the fast-charge current and/or charge termination voltage as the battery temperature varies. JEITA-controlled charging can be disabled by setting JEITA_EN to 0. CHG_DTLS and THM_DTLS registers report JEITA-controlled charging status.

The JEITA controlled fast-charging current (I_{CHGCC_JEITA}) and charge termination voltage (V_{CHGCV_JEITA}) for $T_{COLD} < T < T_{COOL}$ are programmable with I^2C bits I_{CHGCC_COOL} and V_{CHGCV_COOL}.

The charge termination voltage for $T_{WARM} < T < T_{HOT}$ is reduced to (CHG_CV_PRM - 180mV/cell), as shown in Figure 4.

Charging is suspended when the battery temperature is too cold or too hot ($T < T_{COLD}$ or $T_{HOT} < T$).

Temperature thresholds (T_{COLD}, T_{COOL}, T_{WARM}, and T_{HOT}) depend on the thermistor selection. See the *Thermistor Input (THM)* section for more details.

When battery charge current is reduced by 50%, the charger timer is doubled.

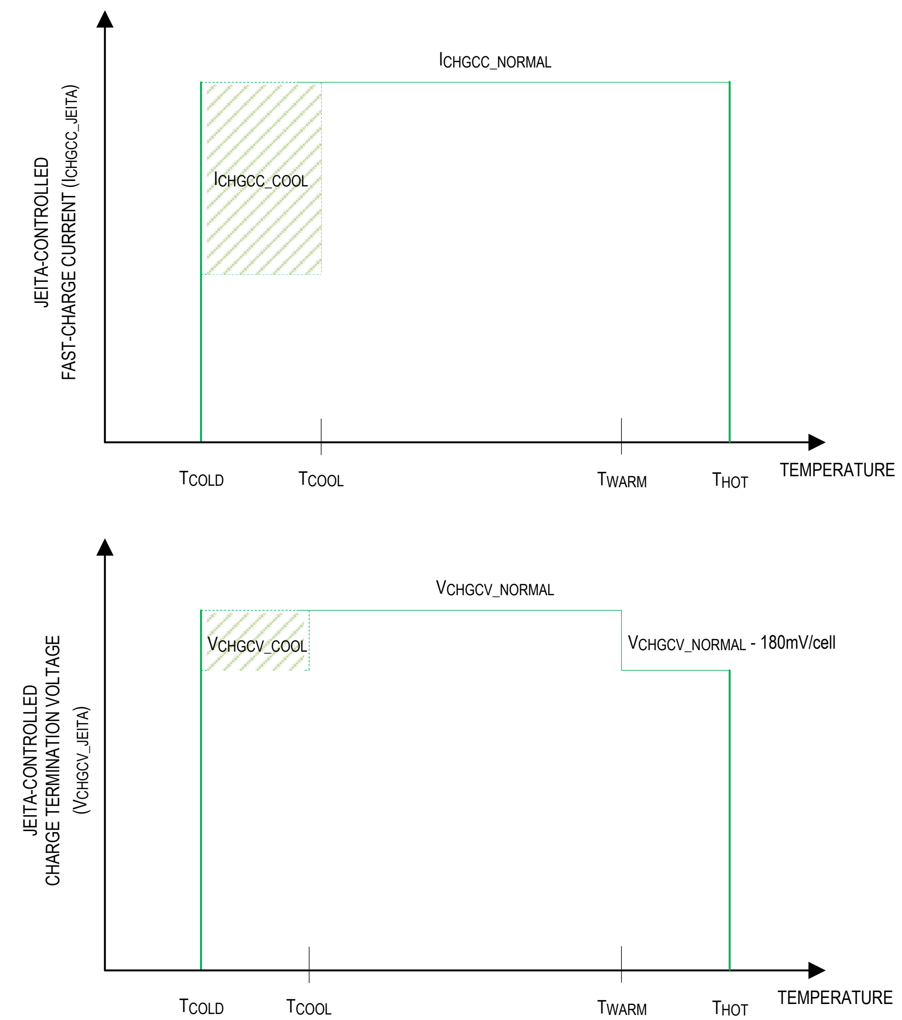


Figure 4. JEITA Compliance

Thermal Shutdown

The MAX77960B/MAX77961B have a die temperature sensing circuit. When the die temperature exceeds the thermal shutdown threshold, T_{SHDN}, the MAX77960B/MAX77961B shut down and reset O type I^2C registers. There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown bus deasserts and the devices reenable. The battery charger has an independent thermal regulation loop. See the *Thermal Shutdown State* section for more details.

Factory Ship Mode

The MAX77960B/MAX77961B support factory ship mode with low battery quiescent current, I_{SHDN}.

When the input source is not valid, and the device is powered by battery, the devices enter factory ship mode if DISQBAT is pulled high or FSHIP_MODE bit is set to 1. I^2C communication is unavailable in factory ship mode. When a valid input source is applied to the device's CHGIN pin, the devices exit factory ship mode. I^2C communication is enabled, charging is enabled if all conditions to charge are met (e.g., DISQBAT pin is pulled low and MODE[3:0] = 0x05).

Minimum System Voltage

The system voltage is regulated to the minimum SYS voltage (V_{SYSMIN}) when the battery is low ($V_{BATT} < V_{SYSMIN}$ - 500mV).

- The charging current is I_{PRECHG} when $V_{BATT} < V_{PRECHG}$.
- The charging current is $I_{TRICKLE}$ when $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$ - 500mV.
- The charging current is I_{FC} when V_{SYSMIN} - 500mV < V_{BATT}.

Battery Differential Voltage Sense (BATSP, BATSN)

BATSP and BATSN are differential remote voltage sense lines for the battery. The MAX77960B/MAX77961B's remote sensing feature improves accuracy and decreases charging time. The thermistor voltage is interpreted with respect to BATSN. For best results, connect BATSP and BATSN as close as possible to the battery connector.

Battery Overcurrent Alert

Excessive battery discharge current can occur for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The battery overcurrent alert feature is enabled with B2SOVRC[3:0]; disabling this feature reduces the battery current consumption by I_{BOVRC}.

When the battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold for at least t_{BOVRC}, the Q_{BAT} switch closes to reduce the power loss in the MAX77960B/MAX77961B. A B2SOVRC_I and a BAT_I interrupt are generated, BAT_OK is cleared, and BAT_DTLS reports an overcurrent condition. Typically, when the host processor detects this overcurrent interrupt, it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent within t_{OCP}, then the MAX77960B/MAX77961B turn off the DC-DC.

t_{OCP} time duration can be set through the B2SOVRC_DTC register bit (Battery to SYS Overcurrent Debounce Time Control): 0x0 (dflt): t_{OCP} = 6ms, 0x1: t_{OCP} = 100ms.

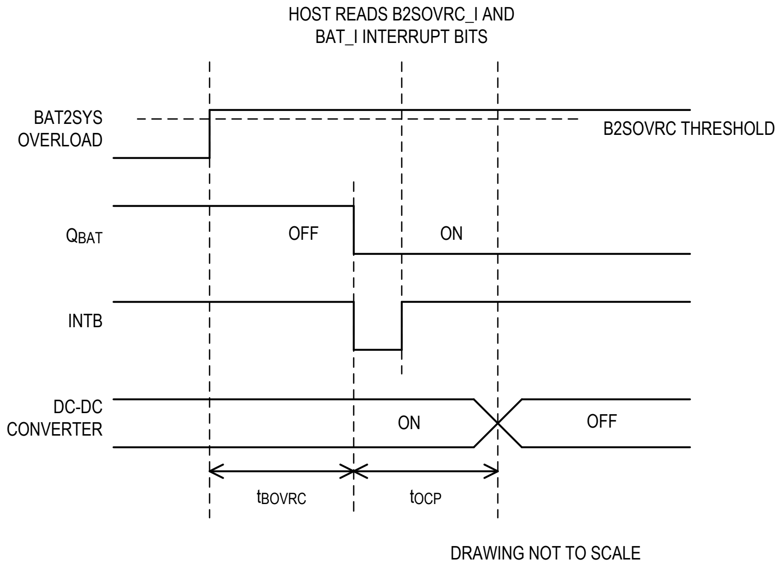


Figure 5. B2SOVRC

Charger Interrupt Debounce Time

Table 9. List of Charger Interrupt Debounce Time

INTERRUPT	DEBOUNCE TIME			
	RISING		FALLING	
	MIN	MAX	MIN	MAX
AICL_I	30ms	—	30ms	—
CHGIN _I	7ms	—	None	—
B2SOVRC_I	—	3.3ms	None	—
BAT_I (OV)	30ms	—	None	—
OTG_PLIM_I (OTG Fault)	37.5ms	—	None	—
OTG_PLIM_I (Buck-Boost Positive Current Limit)	450µs	—	None	—

Input Power-OK/OTG Power-OK Output (INOKB)

INOKB is an open-drain and active-low output that indicates CHGIN power-OK status.

When OTG mode is disabled, (OTGEN = low and MODE[3:0] ≠ 0x0A), INOKB pulls low when a valid input source is inserted at CHGIN, $V_{CHGIN\_UVLO} < V_{CHGIN} < V_{CHGIN\_OVLO}$.

When OTG mode is enabled, (OTGEN = high or MODE[3:0] = 0x0A), INOKB pulls low to indicate the OTG output power OK when $V_{CHGIN.OTG.UV} < V_{CHGIN} < V_{CHGIN.OTG.OV}$.

INOKB can be used as a logic output by adding a 200kΩ pullup resistor to a system IO voltage.

INOKB can be also used as a LED indicator driver by adding a current limiting resistor and a LED to a pullup voltage source.

Charge Status Output (STAT)

STAT is an open-drain and active-low output that indicates charge status. STAT can be used as a logic input to the host processor by adding a 200kΩ pullup resistor to a system IO rail and a rectifier (a diode and a capacitor).

Table 10. Charge Status Indicator by STAT

CHARGE STATUS	STAT	LOGIC STATE
No input	High impedance	High
No DC-DC/no charge: valid adapter with STBY_EN = 1 or MODE = 0x0/1/2/3/4	High impedance	High
Trickle, precharge, fast charge	Repeat low and high impedance with 1Hz, 50% duty cycle	High, rectified with an external diode and a capacitor
Top-off and done	Low	Low
Faults	High impedance	High

Reverse Buck Mode (OTG)

The DC-DC converter topology of the MAX77960B/MAX77961B allows it to operate as a forward buck-boost converter or as a reverse buck converter. The modes of the DC-DC converter are controlled with MODE[3:0] register bits. When MODE[3:0] = 0x0A or OTGEN = high, the DC-DC converter operates in reverse buck mode, allowing it to source current to CHGIN, commonly referred to as USB OTG mode.

In OTG mode, the DC-DC converter operates in reverse buck mode and regulates V_{CHGIN} to $V_{CHGIN.OTG}$ (5.1V typ). The current through the CHGIN current-sensing resistor (CSINN, CSINP) is limited to the value programmed by OTG_ILIM[2:0]. There are eight OTG_ILIM options to program CHGIN current limit from 500mA to 3A. When the OTG mode is enabled, the unipolar CHGIN transfer function measures current going out of CHGIN. When OTG mode is disabled, the unipolar CHGIN transfer function measures current going into CHGIN.

OTG_I, OTG_M, OTG_OK are the interrupt bit, interrupt mask bit and interrupt status bit associated with OTG function. OTG_DTLS[1:0] reports the status of the OTG operation. OTG_DTLS[1:0] is latched until the host reads the register.

If the external OTG load at CHGIN exceeds $I_{CHGIN.OTG.ILIM}$ current limit for a minimum of 37.5ms, an OTG_I interrupt is generated, OTG_OK = 0 and OTG_DTLS[1:0] = 01. The reverse buck operates as a current limited voltage source when overloaded. The DC-DC converter stops switching when the OTG_ILIM condition lasts for 60ms and automatically resumes switching after 300ms off time. If the OTG_ILIM fault condition at CHGIN persists, the DC-DC toggles on and off with ~60ms on and ~300ms off.

VBUS is normally an external-facing pin in the application, and it might have a risk of being shorted to GND. In this case, the MAX77960B/MAX77961B can experience a short-circuit condition at its output. If such risk is real, it is recommended to add a current-limited load switch at VBUS for overcurrent protection. The load switch guarantees the OTG output current does not exceed its current limit under any circumstances. The current limit should be set no lower than $I_{CHGIN.OTG.ILIM}$ of the MAX77960B/MAX77961B.

When CHGIN voltage drops below $V_{CHGIN.OTG.UVLO}$, the DC-DC stops switching and an OTG_I interrupt is generated. OTG_OK = 0 and OTG_DTLS[1:0] = 00.

When CHGIN voltage exceeds $V_{CHGIN.OTG.OV}$, the DC-DC stops switching and an OTG_I interrupt is generated. OTG_OK = 0 and OTG_DTLS[1:0] = 10.

If the DC-DC stops switching due to a OTG_UV or OTG_OV fault condition, it automatically retries after 300ms off time.

INOKB is the hardware indication of the OTG power good. See the *Input Power-OK/OTG Power-OK Output (INOKB)* section for details.

OTG Enable (OTGEN)

The OTGEN is an active high input. When OTGEN pin is pulled high, the OTG function is enabled. When the OTGEN pin is pulled low, the OTG function can be enabled through I^2C by setting MODE[3:0] = 0x0A. To pull the OTGEN pin low with a pulldown resistor, the resistance must be lower than 44kΩ.

The devices enable reverse buck operation only when the voltage on the CHGIN bypass cap, V_{CHGIN}, falls below V_{CHGIN_UVLO}.

In case V_{CHGIN} is above V_{CHGIN_UVLO} threshold at the OTG enable, the devices ensure V_{CHGIN} node discharge through a 8kΩ pulldown resistor before enabling the OTG function and reverse buck switching.

Pulldown is released once V_{CHGIN_UVLO} is reached.

Analog Low-Noise Power Input (AVL)

AVL is the power input for the MAX77960B/MAX77961B's analog circuitry. Do not power external devices from this pin. Bypass with a 4.7Ω resistor between AVL and PVL and a 4.7μF capacitor from AVL to GND.

Low-Side Gate Driver Power Supply (PVL)

PVL is an internal 1.8V LDO output that powers the MAX77960B/MAX77961B's low-side gate driver circuitry. Do not power external devices other than pullup resistors from this pin. Bypass with a 4.7μF capacitor to GND.

System Faults

V_{SYS} Fault

The MAX77960B/MAX77961B monitor the V_{SYS} node for undervoltage and overvoltage events. The following sections describe the devices' behavior if any of these events is to occur.

V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)

When the voltage from SYS to GND (V_{SYS}) is less than the undervoltage lockout threshold ($V_{SYSUVLO}$), the MAX77960B/MAX77961B generate a SYSUVLO_I interrupt immediately. If V_{SYS} is undervoltage for greater than 8ms, the device shuts down and resets O Type I^2C registers.

V_{SYS} Overvoltage Lockout ($V_{SYSOVLO}$)

When the V_{SYS} exceeds $V_{SYSOVLO}$, the MAX77960B/MAX77961B generate a SYSOVLO_I interrupt immediately and the device shuts down and resets O Type I^2C registers.

Thermal Fault

The MAX77960B/MAX77961B have a die temperature sensing circuit. When the die temperature exceeds the thermal shutdown threshold, 165°C (T_{SHDN}), the MAX77960B/MAX77961B shut down and reset O Type I^2C registers. There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown bus deasserts and IC reenables. The battery charger has an independent thermal regulation loop. See the *Thermal Foldback* section for more details.

Interrupt Output (INTB)

The INTB is an active-low, open-drain output. Connect a pullup resistor to the pullup power source.

The MAX77960B/MAX77961B's INTB can be connected to the host's interrupt input and signals to the host when unmasked interrupt events occur within the MAX77960B/MAX77961B.

I^2C Serial Interface

The I^2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I^2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I^2C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 6 shows an example of a typical I^2C system. A device on I^2C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX77960B/MAX77961B I^2C-compatible interface is operating, it is a slave on I^2C bus and it can be both a transmitter and a receiver.

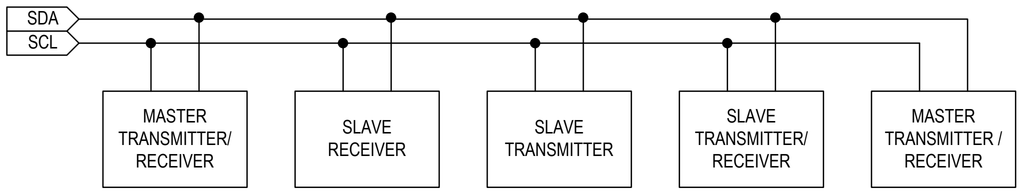


Figure 6. Functional Logic Diagram for Communications Controller

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

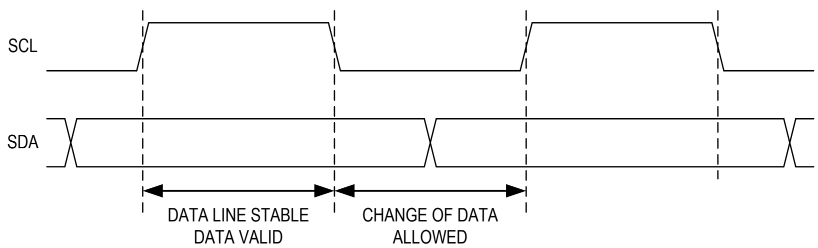


Figure 7. I^2C Bit Transfer

START and STOP Conditions

When I^2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the ICs internally disconnect SCL from the I^2C serial interface until the next START condition, minimizing digital noise and feed-through.

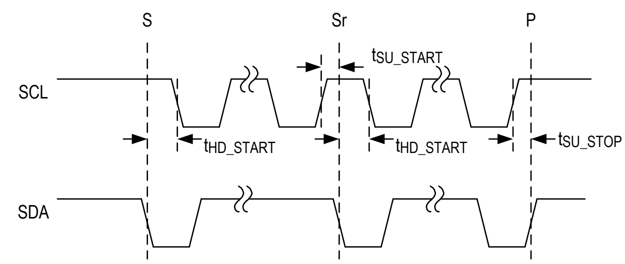


Figure 8. I²C Start Stop

Acknowledge

Both the I²C bus master and the IC (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The devices act as a slave transmitter/receiver. The slave address of the IC is 0xD2h/0xD3h. The least significant bit is the read/$\overline{\text{write}}$ indicator (1 for read, 0 for write).

Clock Stretching

In general, the clock signal generation for I²C bus is the responsibility of the master device. I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

General Call Address

The devices do not implement an I²C specification general call address. If the devices see a general call address (00000000b), they do not issue an ACKNOWLEDGE (A).

Communication Speed

The devices provide I²C 3.0-compatible (1MHz) serial interface.

- I²C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (standard mode)
  - 0Hz to 400kHz (fast mode)
  - 0Hz to 1MHz (fast-mode plus)
- Does not utilize I²C clock stretching

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I^2C 3.0 specification. The major considerations with respect to the IC are:

- I^2C bus master uses current source pullups to shorten the signal rise times.
- I^2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the IC input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Communication Protocols* section.

Communication Protocols

The devices support both writing and reading from their registers.

Writing to a Single Register

Figure 9 shows the protocol for the I^2C master device to write one byte of data to the ICs. This protocol is the same as SMBus specification's Write Byte protocol.

The Write Byte protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

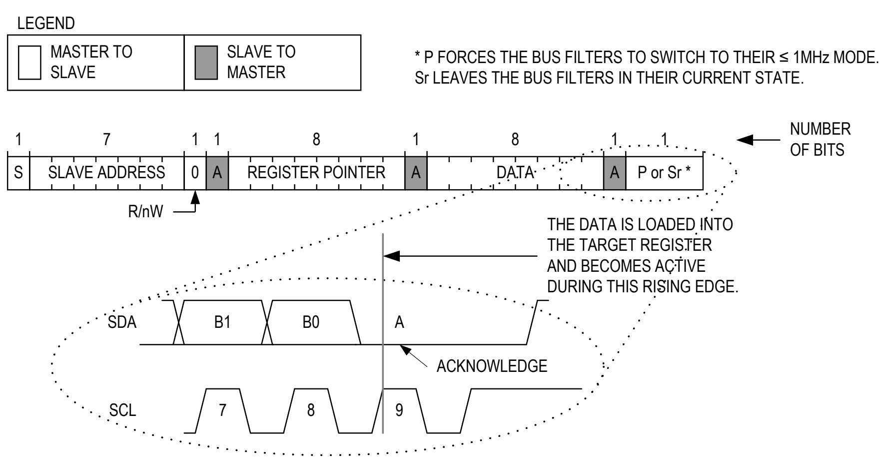


Figure 9. Writing to a Single Register

Writing to Sequential Registers

Figure 10 shows the protocol for writing to sequential registers. This protocol is similar to the Write Byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The Writing to Sequential Registers protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

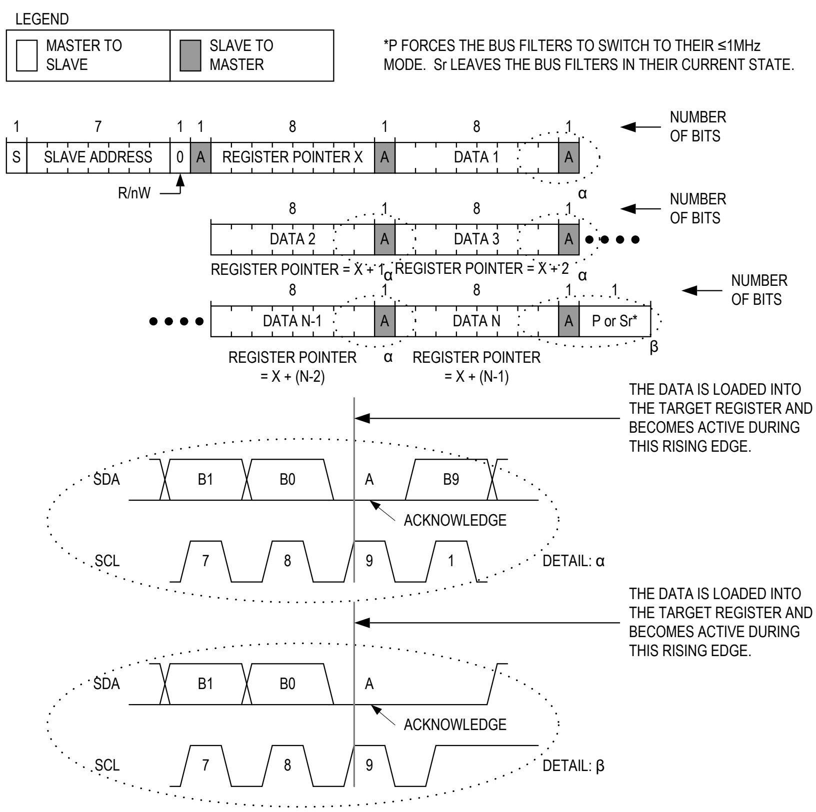


Figure 10. Writing to Sequential Registers

Writing Multiple Bytes using Register-Data Pairs

Figure 11 shows the protocol for the I²C master device to write multiple bytes to the devices using register data pairs. This protocol allows the I²C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a STOP condition.

The Multiple Byte Register Data Pair protocol is as follows:

1. The master sends a START command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 4 to 7 are repeated as many times as the master requires.
9. The master sends a STOP condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

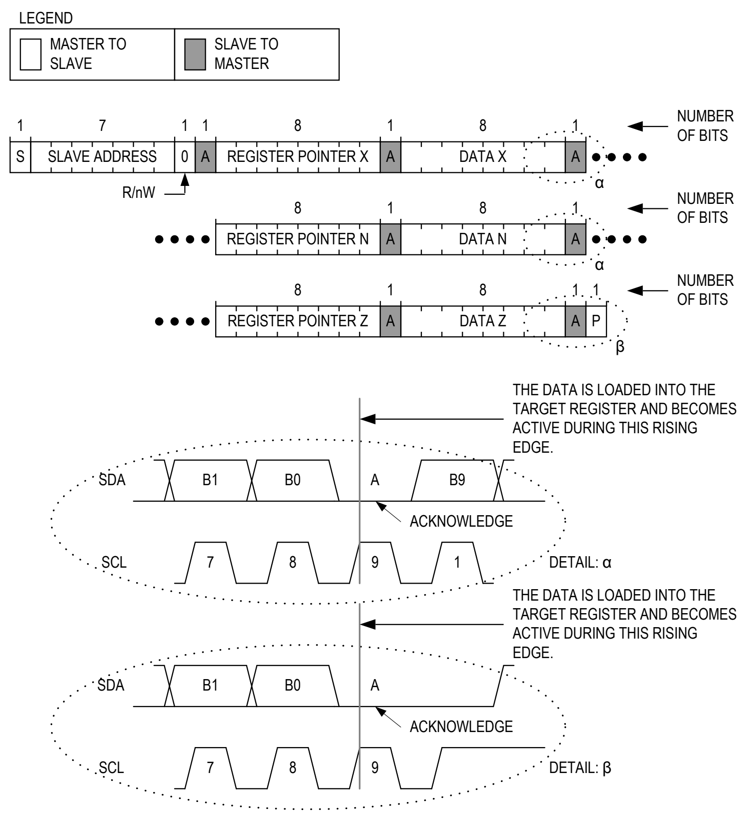


Figure 11. Writing to Multiple Registers with "Multiple Byte Register-Data Pairs" Protocol

Reading from a Single Register

The I^2C master device reads one byte of data to the devices. This protocol is the same as SMBus specification's Read Byte protocol.

The Read Byte protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit ($R/\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

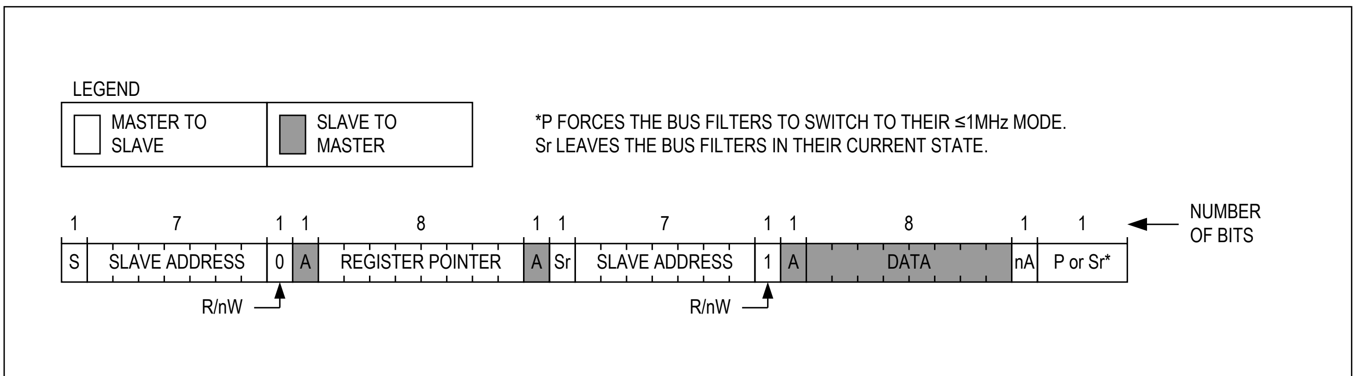


Figure 12. Reading from a Single Register

Reading from Sequential Registers

Figure 13 shows the protocol for reading from sequential registers. This protocol is similar to the Read Byte protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data—when the master has all the data it requires, it issues a not-acknowledge (nA) and a STOP (P) to end the transmission.

The Continuous Read from Sequential Registers protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit ($R/\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

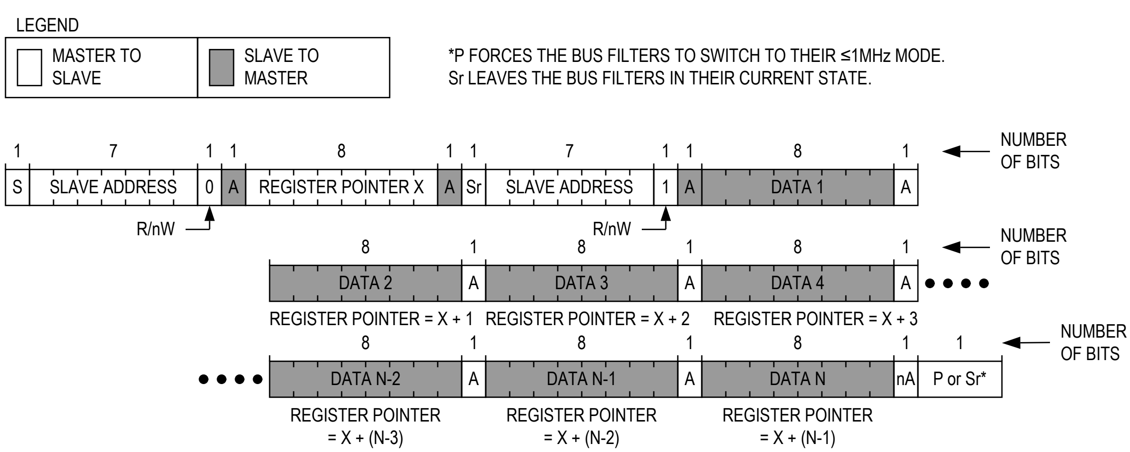


Figure 13. Reading from Sequential Registers

Register Map

FUNC

<table>
<tr><th>ADDRESS</th><th>NAME</th><th>MSB</th><th></th><th></th><th></th><th></th><th></th><th></th><th>LSB</th></tr>
<tr><td colspan="10">TOP</td></tr>
<tr><td>0x00</td><td>CID[7:0]</td><td colspan="3">REVISION[2:0]</td><td colspan="5">VERSION[4:0]</td></tr>
<tr><td>0x01</td><td>SWRST[7:0]</td><td colspan="8">SW_RST[7:0]</td></tr>
<tr><td>0x02</td><td>TOP_INT[7:0]</td><td colspan="5">SPR[4:0]</td><td>TSHDN_I</td><td>SYSOVLO_I</td><td>SYSUVLO_I</td></tr>
<tr><td>0x03</td><td>TOP_INT_MASK[7:0]</td><td colspan="5">SPR[4:0]</td><td>TSHDN_M</td><td>SYSOVLO_M</td><td>SYSUVLO_M</td></tr>
<tr><td>0x04</td><td>TOP_INT_OK[7:0]</td><td colspan="5">SPR[4:0]</td><td>TSHDN_OK</td><td>SYSOVLO_OK</td><td>SYSUVLO_OK</td></tr>
<tr><td colspan="10">CHARGER_FUNC</td></tr>
<tr><td>0x10</td><td>CHG_INT[7:0]</td><td>AICL_I</td><td>CHGIN_I</td><td>B2SOVRC_I</td><td>CHG_I</td><td>BAT_I</td><td>CHGINILIM_I</td><td>DISQBAT_I</td><td>OTG_PLIM_I</td></tr>
<tr><td>0x11</td><td>CHG_INT_MASK[7:0]</td><td>AICL_M</td><td>CHGIN_M</td><td>B2SOVRC_M</td><td>CHG_M</td><td>BAT_M</td><td>CHGINILIM_M</td><td>DISQBAT_M</td><td>OTG_PLIM_M</td></tr>
<tr><td>0x12</td><td>CHG_INT_OK[7:0]</td><td>AICL_OK</td><td>CHGIN_OK</td><td>B2SOVRC_OK</td><td>CHG_OK</td><td>BAT_OK</td><td>CHGINILIM_OK</td><td>DISQBAT_OK</td><td>OTG_PLIM_OK</td></tr>
<tr><td>0x13</td><td>CHG_DETAILS_00[7:0]</td><td>SPR7</td><td colspan="2">CHGIN_DTLS[1:0]</td><td colspan="2">OTG_DTLS[1:0]</td><td colspan="2">SPR2_1[1:0]</td><td>QB_DTLS</td></tr>
<tr><td>0x14</td><td>CHG_DETAILS_01[7:0]</td><td>TREG</td><td colspan="3">BAT_DTLS[2:0]</td><td colspan="4">CHG_DTLS[3:0]</td></tr>
<tr><td>0x15</td><td>CHG_DETAILS_02[7:0]</td><td>SPR</td><td colspan="3">THM_DTLS[2:0]</td><td>APP_MODE_DTLS</td><td colspan="2">FSW_DTLS[1:0]</td><td>NUM_CELL_DTLS</td></tr>
<tr><td>0x16</td><td>CHG_CNFG_00[7:0]</td><td>COMM_MODE</td><td>DISIBS</td><td>STBY_EN</td><td>WDTEN</td><td colspan="4">MODE[3:0]</td></tr>
<tr><td>0x17</td><td>CHG_CNFG_01[7:0]</td><td>PQEN</td><td>LPM</td><td colspan="2">CHG_RSTRT[1:0]</td><td>STAT_EN</td><td colspan="3">FCHGTIME[2:0]</td></tr>
<tr><td>0x18</td><td>CHG_CNFG_02[7:0]</td><td colspan="2">SPR[1:0]</td><td colspan="6">CHGCC[5:0]</td></tr>
<tr><td>0x19</td><td>CHG_CNFG_03[7:0]</td><td>SYS_TRACK_DIS</td><td>B2SOVRC_DTC</td><td colspan="3">TO_TIME[2:0]</td><td colspan="3">TO_ITH[2:0]</td></tr>
<tr><td>0x1A</td><td>CHG_CNFG_04[7:0]</td><td colspan="2">SPR[1:0]</td><td colspan="6">CHG_CV_PRM[5:0]</td></tr>
<tr><td>0x1B</td><td>CHG_CNFG_05[7:0]</td><td colspan="2">RESERVED[1:0]</td><td colspan="2">ITRICKLE[1:0]</td><td colspan="4">B2SOVRC[3:0]</td></tr>
<tr><td>0x1C</td><td>CHG_CNFG_06[7:0]</td><td>SPR7</td><td colspan="2">RESERVED[1:0]</td><td>SPR4</td><td colspan="2">CHGPROT[1:0]</td><td colspan="2">WDTCLR[1:0]</td></tr>
<tr><td>0x1D</td><td>CHG_CNFG_07[7:0]</td><td>JEITA_EN</td><td colspan="4">REGTEMP[3:0]</td><td>VCHGCV_COOL</td><td>ICHGCC_COOL</td><td>FSHIP_MODE</td></tr>
<tr><td>0x1E</td><td>CHG_CNFG_08[7:0]</td><td>RESERVED</td><td colspan="7">CHGIN_ILIM[6:0]</td></tr>
<tr><td>0x1F</td><td>CHG_CNFG_09[7:0]</td><td colspan="2">INLIM_CLK[1:0]</td><td colspan="3">OTG_ILIM[2:0]</td><td colspan="3">MINVSYS[2:0]</td></tr>
<tr><td>0x20</td><td>CHG_CNFG_10[7:0]</td><td colspan="2">SPR[1:0]</td><td colspan="5">VCHGIN_REG[4:0]</td><td>DISKIP</td></tr>
</table>

Register Details

CID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	REVISION[2:0]			VERSION[4:0]				
Reset	0x6			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
REVISION	7:5	Silicon Revision	
VERSION	4:0	OTP Recipe Version	

SWRST (0x1)

BIT	7	6	5	4	3	2	1	0
Field	SW_RST[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SW_RST	7:0	Software Reset	0xA5: Type O registers are reset. SW_RST register is autoclear as under O-type reset control All others: No reset

TOP_INT (0x2)

BIT	7	6	5	4	3	2	1	0
Field	SPR[4:0]					TSHDN_I	SYSOVLO_I	SYSUVLO_I
Reset	0x0					0x0	0x0	0x0
Access Type	Read Clears All					Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:3	Spare Bit	
TSHDN_I	2	Thermal Shutdown Interrupt	0b0: No interrupt detected 0b1: Interrupt detected
SYSOVLO_I	1	SYSOVLO Interrupt	0b0: No interrupt detected 0b1: Interrupt detected
SYSUVLO_I	0	SYSUVLO Interrupt	0b0: No interrupt detected 0b1: Interrupt detected

TOP_INT_MASK (0x3)

BIT	7	6	5	4	3	2	1	0
Field	SPR[4:0]					TSHDN_M	SYSOVLO_M	SYSUVLO_M
Reset	0x1F					0x1	0x1	0x1
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:3	Spare Bit	
TSHDN_M	2	Thermal Shutdown Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSOVLO_M	1	SYSOVLO Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSUVLO_M	0	SYSUVLO Interrupt Mask	0b0: Unmasked 0b1: Masked

TOP_INT_OK (0x4)

BIT	7	6	5	4	3	2	1	0
Field	SPR[4:0]					TSHDN_OK	SYSOVLO_OK	SYSUVLO_OK
Reset	0x0					0x1	0x1	0x1
Access Type	Read Only					Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:3	Spare Bit	
TSHDN_OK	2	Thermal shutdown Status Indicator	0b0: Device is in thermal shutdown 0b1: Device is not in thermal shutdown
SYSOVLO_OK	1	SYSOVLO Status Indicator	0b0: SYS voltage is above SYSOVLO threhold 0b1: SYS voltage is below SYSOVLO threhold
SYSUVLO_OK	0	SYSUVLO Status Indicator	0b0: SYS voltage is below SYSUVLO threhold 0b1: SYS voltage is above SYSUVLO threhold

CHG_INT (0x10)

Interrupt status register for the charger block.

BIT	7	6	5	4	3	2	1	0
Field	AICL_I	CHGIN_I	B2SOVRC_I	CHG_I	BAT_I	CHGINILIM_I	DISQBAT_I	OTG_PLIM_I
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_I	7	AICL Interrupt	0b0: The AICL_OK bit has not changed since the last time this bit was read. 0b1: The AICL_OK bit has changed since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_I	6	CHGIN Interrupt	0b0: The CHGIN_OK bit has not changed since the last time this bit was read. 0b1: The CHGIN_OK bit has changed since the last time this bit was read.
B2SOVRC_I	5	B2SOVRC Interrupt	0b0: The B2SOVRC_OK bit has not changed since the last time this bit was read. 0b1: The B2SOVRC_OK bit has changed since the last time this bit was read.
CHG_I	4	Charger Interrupt	0b0: The CHG_OK bit has not changed since the last time this bit was read. 0b1: The CHG_OK bit has changed since the last time this bit was read.
BAT_I	3	Battery Interrupt	0b0: The BAT_OK bit has not changed since the last time this bit was read. 0b1: The BAT_OK bit has changed since the last time this bit was read.
CHGINILIM_I	2	CHGINILIM Interrupt	0b0: The CHGINILIM_OK bit has not changed since the last time this bit was read. 0b1: The CHGINILIM_OK bit has changed since the last time this bit was read.
DISQBAT_I	1	DISQBAT Interrupt	0b0: The DISQBAT_OK bit has not changed since the last time this bit was read. 0b1: The DISQBAT_OK bit has changed since the last time this bit was read.
OTG_PLIM_I	0	OTG Interrupt/PLIM Interrupt	0b0: Mode = 0xA: The OTG_OK bit has not changed since the last time this bit was read. Mode ≠ 0xA: PLIM_OK bit has not changed since the last time this bit was read. 0b1: Mode = 0xA: The OTG_OK bit has changed since the last time this bit was read. Mode ≠ 0xA: The PLIM_OK bit has changed since the last time this bit was read.

CHG_INT_MASK (0x11)

Mask register to mask the corresponding charger interrupts.

BIT	7	6	5	4	3	2	1	0
Field	AICL_M	CHGIN_M	B2SOVRC_M	CHG_M	BAT_M	CHGINILIM_M	DISQBAT_M	OTG_PLIM_M
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_M	7	AICL Interrupt Mask	0b0: Unmasked 0b1: Masked
CHGIN_M	6	CHGIN Interrupt Mask	0b0: Unmasked 0b1: Masked
B2SOVRC_M	5	B2SOVRC Interrupt Mask	0b0: Unmasked 0b1: Masked
CHG_M	4	Charger Interrupt Mask	0b0: Unmasked 0b1: Masked

BITFIELD	BITS	DESCRIPTION	DECODE
BAT_M	3	Battery Interrupt Mask	0b0: Unmasked 0b1: Masked
CHGINILIM_M	2	CHGINILIM Interrupt Mask	0b0: Unmasked 0b1: Masked
DISQBAT_M	1	DISQBAT Interrupt Mask	0b0: Unmasked 0b1: Masked
OTG_PLIM_M	0	OTG/PLIM Interrupt Mask	0b0: Unmasked 0b1: Masked

CHG_INT_OK (0x12)

BIT	7	6	5	4	3	2	1	0
Field	AICL_OK	CHGIN_OK	B2SOVRC_OK	CHG_OK	BAT_OK	CHGINILIM_OK	DISQBAT_OK	OTG_PLIM_OK
Reset	0x1	0x0	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_OK	7	AICL_OK Status	0b0: AICL mode 0b1: Not in AICL mode
CHGIN_OK	6	CHGIN Input Status Indicator. See CHGIN_DTLS for more information.	0b0: The CHGIN input is invalid. CHGIN_DTLS ≠ 0x03. 0b1: The CHGIN input is valid. CHGIN_DTLS = 0x03.
B2SOVRC_OK	5	B2SOVRC Status	0b0: BATT to SYS exceeds current limit. 0b1: BATT to SYS does not exceed current limit.
CHG_OK	4	Charger Status Indicator. See CHG_DTLS for more information.	0b0: The charger has reduced charge current or charge termination voltage based on JEITA control, suspended charging, or TREG = 1. 0b1: The charger is OK or the charger is off.
BAT_OK	3	Battery Status Indicator. See BAT_DTLS for more information.	0b0: The battery has an issue or the charger has been suspended. BAT_DTLS ≠ 0x03 and ≠ 0x07. 0b1: The battery is OK. BAT_DTLS = 0x03 or BAT_DTLS = 0x07.
CHGINILIM_OK	2	CHGINILIM Status	0b0: The CHGIN input has reached the current limit. 0b1: The CHGIN input has not reached the current limit.
DISQBAT_OK	1	DISQBAT Status	0b0: DISQBAT pin is high or DISIBS bit is set to 1 and Q_{BAT} disabled. 0b1: DISQBAT is low and DISIBS bit is 0 and Q_{BAT} not disabled.
OTG_PLIM_OK	0	Mode = 0xA: OTG Status Indicator. See OTG_DTLS for more information. Mode ≠ 0xA: PLIM status indicator (buck-boost limit reached).	0b0: Mode = 0xA: There is a fault in OTG mode. OTG_DTLS ≠ 0x11. Mode ≠ 0xA: Buck-boost reaches positive current limit. 0b1: Mode = 0xA: The OTG operation is OK. OTG_DTLS = 0x11. Mode ≠ 0xA: Buck-boost does not reach positive current limit.

CHG_DETAILS_00 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	SPR7	CHGIN_DTLS[1:0]		OTG_DTLS[1:0]		SPR2_1[1:0]		QB_DTLS
Reset	0x0	0x0		0x0		0x0		0x0
Access Type	Read Only	Read Only		Read Only		Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPR7	7	Spare Bit	
CHGIN_DTLS	6:5	CHGIN Details	0b00: V_{BUS} is invalid. $V_{CHGIN} < V_{CHGIN\_UVLO}$ 0b01: RSVD 0b10: V_{BUS} is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0b11: V_{BUS} is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$ and $V_{CHGIN} < V_{CHGIN\_OVLO}$
OTG_DTLS	4:3	OTG Details	0b00: OTG output (V_{CHGIN}) is in undervoltage condition. $V_{CHGIN} < V_{OTG\_UVLO}$ 0b01: OTG output (V_{CHGIN}) is in current limit (OTG_ILIM) within the last 37.5ms. 0b10: OTG output (V_{CHGIN}) is in overvoltage condition. $V_{CHGIN} > V_{OTG\_OVLO}$ 0b11: OTG is disabled ($\overline{\text{OTGEN}}$ = low and MODE ≠ 0xA) or OTG output (V_{CHGIN}) is valid. $V_{CHGIN} > V_{OTG\_UVLO}$ and $V_{CHGIN} < V_{OTG\_OVLO}$ and it's not in current limit.
SPR2_1	2:1	Spare Bit	
QB_DTLS	0	Q_{BAT} status Read back value of QB_DTLS reflects the actual Q_{BAT} state.	0b0: Q_{BAT} is off. 0b1: Q_{BAT} is on.

CHG_DETAILS_01 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
Reset	0x0	0x7			0x8			
Access Type	Read Only	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
TREG	7	Temperature Regulation Status	0b0: The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 0b1: The junction temperature is greater than the threshold set by REGTEMP and the charge current limit can be folding back to reduce power dissipation.

BITFIELD	BITS	DESCRIPTION	DECODE
BAT_DTLS	6:4	Battery Details Note: Only B2SOVRC is reported in Battery Only mode. As a consequence, BAT_OK = 1 is also reported in BAT_DTLS = 0x07. In the event that multiple faults occur within the battery details category, overcurrent has priority followed by no battery, then overvoltage, then timer fault, then below prequal.	0b000: Battery removal is detected on THM pin. 0b001: V_{BATT} < V_{PRECHG}. This condition is also reported in the CHG_DTLS as 0x00. 0b010: The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has suspended and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS as 0x06. 0b011: The battery is OK and its voltage is greater than the minimum system voltage (V_{SYSMIN} - 500mV < V_{BATT}), Q_{BAT} is on and V_{SYS} is approximately equal to V_{BATT}. 0b100: The battery is okay but its voltage is low: V_{PRECHG} < V_{BATT} < V_{SYSMIN} - 500mV. This condition is also reported in the CHG_DTLS as 0x00. 0b101: The battery voltage has been greater than the battery overvoltage threshold (CHG_CV_PRM + 240mV/cell) for the last 30ms. This flag is only generated when there is a valid input. 0b110: The battery has been overcurrent for at least 3ms since the last time this register has been read. 0b111: Battery level not available. In battery only mode, all battery comparators are off except for B2SOVRC.

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_DTLS	3:0	Charger Details	0x00: Charger is in precharge or trickle charge mode CHG_OK = 1 and $V_{BATT} < V_{SYSMIN}$ - 500mV and $T_J < T_{SHDN}$ 0x01: Charger is in fast-charge constant current mode CHG_OK = 1 and $V_{BATT} < V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x02: Charger is in fast-charge constant voltage mode CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x03: Charger is in top-off mode CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x04: Charger is in done mode CHG_OK = 0 and $V_{BATT} > V_{BATTREG} - V_{RSTRT}$ and $T_J < T_{SHDN}$ 0x05: Charger is off because at least one pin of INLIM, ITO, ISET, or VSET has valid resistance while others don't (invalid resistance, open or tied to PVL). Configure charger with I^2C, then set COMM_MODE to 1 enables charging. CHG_OK = 0 0x06: Charger is in timer fault mode CHG_OK = 0 and if BAT_DTLS = 0b001 then $V_{BATT} < V_{SYSMIN}$ - 500mV or $V_{BATT} < V_{PRECHG}$ and $T_J < T_{SHDN}$ 0x07: Charger is suspended because Q_{BAT} is disabled (DISQBAT = high or DISIBS = 1) CHG_OK = 0 0x08: Charger is off, charger input invalid and/or charger is disabled CHG_OK = 1 0x09: Reserved 0x0A: Charger is off and the junction temperature is > T_{SHDN} CHG_OK = 0 0x0B: Charger is off because the watchdog timer expired CHG_OK = 0 0x0C: Charger is suspended or charge current or voltage is reduced based on JEITA control. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0D: Charger is suspended because battery removal is detected on THM pin. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0E: Reserved 0x0F: Reserved

CHG_DETAILS_02 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	SPR	THM_DTLS[2:0]			APP_MODE_DTLS	FSW_DTLS[1:0]		NUM_CELL_DTLS
Reset	0x0	0x2			0x0	0x0		0x0
Access Type	Read Only	Read Only			Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7	Spare bit	
THM_DTLS	6:4	Thermistor Status. This is also reported in the CHG_DTLS as 0x0C.	0b000: Low temperature and charging suspended (COLD) 0b001: Low temperature charging (cool) 0b010: Normal temperature charging (normal) 0b011: High temperature charging (warm) 0b100: High temperature and charging suspended (hot) 0b101: Battery removal detected on THM pin 0b110: Thermistor monitoring is disabled 0b111: Reserved
APP_MODE_DTLS	3	Application Mode Status	0b0: Device is configured to operate as a standalone DC-DC converter. 0b1: Device is configured to operate as a charger.
FSW_DTLS	2:1	Programmed Switching Frequency Details	0x0: 600kHz 0x1: 1.2MHz 0x2: Reserved 0x3: Reserved
NUM_CELL_DTLS	0	Number of Serially Connected Battery Cells Details	0b0: Device is configured to support a 2-cell battery. 0b1: Device is configured to support a 3-cell battery.

CHG_CNFG_00 (0x16)

Charger configuration 0

BIT	7	6	5	4	3	2	1	0
Field	COMM_MODE	DISIBS	STBY_EN	WDTEN	MODE[3:0]			
Reset	0x0	0x0	0x0	0x0	0x5			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
COMM_MODE	7	I²C Mode Enable	0b0: Autonomous Mode CHGIN_ILIM, CHGCC, CHG_CV_PRM, and TO_ITH registers are programmed by external resistors on INLIM, ISET, VSET and ITO pins. Writing 0 to COMM_MODE is ignored. 0b1: I²C Mode Enabled CHGIN_ILIM, CHGCC, CHG_CV_PRM and TO_ITH registers are programmed by I²C. Writing 1 to COMM_MODE is allowed. Writting COMM_MODE=1 clears any charger suspension due to invalid resistance detected on INLIM, ISET, VSET, and ITO pins. Charger starts with I²C programmed settings in CHGIN_ILIM, CHGCC, CHG_CV_PRM, and TO_ITH registers.
DISIBS	6	BATT to SYS FET Disable Control Read back value of DISIBS register bit reflects the actual DISIBS command or DISQBAT PIN state.	0b0: BATT to SYS FET is controlled by the power path state machine. 0b1: BATT to SYS FET is forced off.
STBY_EN	5	CHGIN Standby Enable Read back value of the STBY_EN register bit reflects the actual CHGIN standby setting.	0b0: DC-DC is controlled by the power path state machine. 0b1: Force DC-DC off. Device goes to CHGIN low quiescent current standby.
WDTEN	4	Watchdog Timer Enable. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.	0b0: Watchdog timer disabled 0b1: Watchdog timer enabled

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	3:0	Smart Power Selector Configuration. Read back value of the MODE register reflects the actual smart power selector configuration.	0x0: Charger = off, OTG = off, DC-DC = off. When the Q_{BAT} switch is on (DISQBAT = low and DISIBS = 0), the battery powers the system. 0x1: Same as 0b0000 0x2: Same as 0b0000 0x3: Same as 0b0000 0x4: Charger = off, OTG = off, DC-DC = on. When there is a valid input, the DC-DC converter regulates the system voltage to be the maximum of (V_{SYSMIN} and V_{BATT} + 4%). 0x5: Charger = on,OTG = off, DC-DC = on. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + I_{BATT} x $R_{BAT2SYS}$. 0x6: Same as 0b0101 0x7: Same as 0b0101 0x8: RSVD 0x9: RSVD 0xA: Charger = off, OTG = on, DC-DC = off. The Q_{BAT} switch is on to allow the battery to support the system, the charger's DC-DC operates in reverse mode as a buck converter. The OTG output, CHGIN, can source current up to $I_{CHGIN.OTG.LIM}$. The CHGIN target voltage is $V_{CHGIN.OTG}$. 0xB: RSVD 0xC: RSVD 0xD: RSVD 0xE: RSVD 0xF: RSVD

CHG_CNFG_01 (0x17)

Charger configuration 1

BIT	7	6	5	4	3	2	1	0
Field	PQEN	LPM	CHG_RSTRT[1:0]		STAT_EN	FCHGTIME[2:0]		
Reset	0x1	0x0	0x1		0x1	0x1		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PQEN	7	Low-Battery Prequalification Mode Enable	0b0: Low-Battery Prequalification mode is disabled. 0b1: Low-Battery Prequalification mode is enabled.
LPM	6	Low Power Mode control	0b0: Q_{BAT} charge pump runs in Normal mode. 0b1: Q_{BAT} charge pump is in Low Power Mode.
CHG_RSTRT	5:4	Charger Restart Threshold	0b00: 100mV/cell below the value programmed by CHG_CV_PRM 0b01: 150mV/cell below the value programmed by CHG_CV_PRM 10: 200mV/cell below the value programmed by CHG_CV_PRM 11: Disabled
STAT_EN	3	Charge Indicator Output Enable	0b0: Disable STAT output 0b1: Enable STAT output

BITFIELD	BITS	DESCRIPTION	DECODE
FCHGTIME	2:0	Fast-Charge Timer setting (t_{FC}, hrs)	0b000: Disable 0b001: 3 0b010: 4 0b011: 5 0b100: 6 0b101: 7 0b110: 8 0b111: 10

CHG_CNFG_02 (0x18)

Charger configuration 2

BIT	7	6	5	4	3	2	1	0
Field	SPR[1:0]		CHGCC[5:0]					
Reset	0x0		0x7					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:6	Spare Bit	

BITFIELD	BITS	DESCRIPTION	DECODE
CHGCC	5:0	Fast-Charge Current Selection (mA). When the charger is enabled, the charge current limit is set by these bits. Read back value of the CHGCC register reflects the actual fast charge current programmed in the charger. The thermal foldback loop can reduce the battery charger's target current by A_{TJREG}.	0x00: 100 0x01: 150 0x02: 200 0x03: 250 0x04: 300 0x05: 350 0x06: 400 0x07: 450 0x08: 500 0x09: 600 0x0A: 700 0x0B: 800 0x0C: 900 0x0D: 1000 0x0E: 1100 0x0F: 1200 0x10: 1300 0x11: 1400 0x12: 1500 0x13: 1600 0x14: 1700 0x15: 1800 0x16: 1900 0x17: 2000 0x18: 2100 0x19: 2200 0x1A: 2300 0x1B: 2400 0x1C: 2500 0x1D: 2600 0x1E: 2700 0x1F: 2800 0x20: 2900 0x21: 3000 0x22: 3100 0x23: 3200 0x24: 3300 0x25: 3400 0x26: 3500 0x27: 3600 0x28: 3700 0x29: 3800 0x2A: 3900 0x2B: 4000 0x2C: 4100 0x2D: 4200 0x2E: 4300 0x2F: 4400 0x30: 4500 0x31: 4600 0x32: 4700 0x33: 4800 0x34: 4900 0x35: 5000 0x36: 5100 0x37: 5200 0x38: 5300 0x39: 5400 0x3A: 5500

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: 5600 0x3C: 5700 0x3D: 5800 0x3E: 5900 0x3F: 6000

CHG_CNFG_03 (0x19)

Charger configuration 3

BIT	7	6	5	4	3	2	1	0
Field	SYS_TRACK_DIS	B2SOVRC_DTC	TO_TIME[2:0]			TO_ITH[2:0]		
Reset	0x1	0x0	0x3			0x0		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SYS_TRACK_DIS	7	SYS Tracking Disable Control	0x0: SYS tracking is enabled. SYS is regulated to MAX of (V_{BATT} + 4%, V_{SYSMIN}). This is also valid in Charge Done state. 0x1: SYS tracking is disabled. SYS is regulated to $V_{CHG\_CV\_PRM}$.
B2SOVRC_DTC	6	Battery to SYS Overcurrent Debounce Time Control. While under OVRC condition, after t_{OCP} switcher (and therfore charge) is disabled.	0x0: t_{OCP} = 6ms 0x1: t_{OCP} = 100ms
TO_TIME	5:3	Top-Off Timer Setting (min)	0b000: 30s 0b001: 10 0b010: 20 0b011: 30 0b100: 40 0b101: 50 0b110: 60 0b111: 70
TO_ITH	2:0	Top-Off Current Threshold (mA). The charger transitions from its fast-charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME. Read back value of the TO_ITH register reflects the actual top-off current programmed in the charger.	0b000: 100 0b001: 200 0b010: 300 0b011: 400 0b100: 500 0b101: 600 0b110: 600 0b111: 600

CHG_CNFG_04 (0x1A)

Charger configuration 4

BIT	7	6	5	4	3	2	1	0
Field	SPR[1:0]		CHG_CV_PRM[5:0]					
Reset	0x0		0x00					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:6	Spare Bit	

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CV_PRM	5:0	Charge Termination Voltage Setting (V). Read back value of the CHG_CV_PRM register reflects the actual charge termination voltage programmed in the charger when JEITA_EN = 0. When JEITA_EN = 1, charge termination voltage is controlled by V_{CHGCV_COOL} and V_{CHGCV_WARM} register settings.	2 Cell Battery 0x00: 8.000 0x01: 8.020 0x02: 8.040 0x03: 8.060 0x04: 8.080 0x05: 8.100 0x06: 8.120 0x07: 8.140 0x08: 8.160 0x09: 8.180 0x0A: 8.200 0x0B: 8.220 0x0C: 8.240 0x0D: 8.260 0x0E: 8.280 0x0F: 8.300 0x10: 8.320 0x11: 8.340 0x12: 8.360 0x13: 8.380 0x14: 8.400 0x15: 8.420 0x16: 8.440 0x17: 8.460 0x18: 8.480 0x19: 8.500 0x1A: 8.520 0x1B: 8.540 0x1C: 8.560 0x1D: 8.580 0x1E: 8.600 0x1F: 8.620 0x20: 8.640 0x21: 8.660 0x22: 8.680 0x23: 8.700 0x24: 8.720 0x25: 8.740 0x26: 8.760 0x27: 8.780 0x28: 8.800 0x29: 8.820 0x2A: 8.840 0x2B: 8.860 0x2C: 8.880 0x2D: 8.900 0x2E: 8.920 0x2F: 8.940 0x30: 8.960 0x31: 8.980 0x32: 9.000 0x33: 9.020 0x34: 9.040 0x35: 9.060 0x36: 9.080 0x37: 9.100 0x38: 9.120 0x39: 9.140

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3A: 9.160 0x3B: 9.180 0x3C: 9.200 0x3D: 9.220 0x3E: 9.240 0x3F: 9.260 3 Cell Battery 0x00: 12.000 0x01: 12.030 0x02: 12.060 0x03: 12.090 0x04: 12.120 0x05: 12.150 0x06: 12.180 0x07: 12.210 0x08: 12.240 0x09: 12.270 0x0A: 12.300 0x0B: 12.330 0x0C: 12.360 0x0D: 12.390 0x0E: 12.420 0x0F: 12.450 0x10: 12.480 0x11: 12.510 0x12: 12.540 0x13: 12.570 0x14: 12.600 0x15: 12.630 0x16: 12.660 0x17: 12.690 0x18: 12.720 0x19: 12.750 0x1A: 12.780 0x1B: 12.810 0x1C: 12.840 0x1D: 12.870 0x1E: 12.900 0x1F: 12.930 0x20: 12.960 0x21: 12.990 0x22: 13.020 0x23: 13.050

CHG_CNFG_05 (0x1B)

Charger configuration 5

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		ITRICKLE[1:0]		B2SOVRC[3:0]			
Reset	0x1		0x0		0x4			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
ITRICKLE	5:4	Trickle Charge Current Selection (mA)	0b00: 100 0b01: 200 0b10: 300 0b11: 400
B2SOVRC	3:0	BATT to SYS Overcurrent Threshold (A)	0x00: Disable 0x01: 3.000 0x02: 3.500 0x03: 4.000 0x04: 4.500 0x05: 5.000 0x06: 5.500 0x07: 6.000 0x08: 6.500 0x09: 7.000 0x0A: 7.500 0x0B: 8.000 0x0C: 8.500 0x0D: 9.000 0x0E: 9.500 0x0F: 10.000

CHG_CNFG_06 (0x1C)

Charger configuration 6

BIT	7	6	5	4	3	2	1	0
Field	SPR7	RESERVED[1:0]		SPR4	CHGPROT[1:0]		WDTCLR[1:0]	
Reset	0x0	0x0		0x0	0x0		0x0	
Access Type	Write, Read	Write, Read		Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPR7	7	Spare bit	
RESERVED	6:5	Reserved	
SPR4	4	Spare bit	
CHGPROT	3:2	Charger Settings Protection Bit. Writing 11 to these bits unlocks the write capability for the registers that are Protected with CHGPROT. Writing any value besides 11 locks the protected registers.	0b00: Write capability locked 0b01: Write capability locked 0b10: Write capability locked 0b11: Write capability unlocked
WDTCLR	1:0	Watchdog Timer Clear Bit. Writing 01 to these bits clears the watchdog timer when the watchdog timer is enabled.	0b00: the watchdog timer is not cleared 0b01: the watchdog timer is cleared 0b10: the watchdog timer is not cleared 0b11: the watchdog timer is not cleared

CHG_CNFG_07 (0x1D)

Charger configuration 7

BIT	7	6	5	4	3	2	1	0
Field	JEITA_EN	REGTEMP[3:0]				VCHGCV_COOL	ICHGCC_COOL	FSHIP_MODE
Reset	0x0	0x6				0x0	0x1	0x0
Access Type	Write, Read	Write, Read				Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
JEITA_EN	7	JEITA Enable	0b0: JEITA disabled. Fast-charge current and charge termination voltage do not change based on thermistor temperature. 0b1: JEITA enabled. Fast-charge current and charge termination voltage change based on thermistor temperature.
REGTEMP	6:3	Junction Temperature Thermal Regulation (ºC). The charger's target current limit starts to foldback and the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint.	0x0: 85 0x1: 90 0x2: 95 0x3: 100 0x4: 105 0x5: 110 0x6: 115 0x7: 120 0x8: 125 0x9: 130
VCHGCV_COOL	2	JEITA-Controlled Battery Termination Voltage When Thermistor Temperature is Between T_{COLD} and T_{COOL}	0b0: Battery termination voltage is set by CHG_CV_PRM. 0b1: Battery termination voltage is set by (CHG_CV_PRM - 180mV/cell).
ICHGCC_COOL	1	JEITA-Controlled Battery Fast-Charge Current When Thermistor Temperature is Between T_{COLD} and T_{COOL}	0b0: Battery fast-charge current is set by CHGCC 0b1: Battery fast-charge current is reduced to 50% of CHGCC
FSHIP_MODE	0	Factory Ship Mode Enable	0b0: Disable factory ship mode 0b1: Enable factory ship mode

CHG_CNFG_08 (0x1E)

Charger configuration 8

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	CHGIN_ILIM[6:0]						
Reset	0x1	0x0B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_ILIM	6:0	CHGIN Input Current Limit (mA). Read back value of the CHGIN_ILIM register reflect the actual input current limit programmed in the charger.	0x00: 100 0x01: 100 0x02: 100 0x03: 100 0x04: 150 0x05: 200 0x06: 250 0x07: 300 0x08: 350 0x09: 400 0x0A: 450 0x0B: 500 0x0C: 550 0x0D: 600 0x0E: 650 0x0F: 700 0x10: 750 0x11: 800 0x12: 850 0x13: 900 0x14: 950 0x15: 1000 0x16: 1050 0x17: 1100 0x18: 1150 0x19: 1200 0x1A: 1250 0x1B: 1300 0x1C: 1350 0x1D: 1400 0x1E: 1450 0x1F: 1500 0x20: 1550 0x21: 1600 0x22: 1650 0x23: 1700 0x24: 1750 0x25: 1800 0x26: 1850 0x27: 1900 0x28: 1950 0x29: 2000 0x2A: 2050 0x2B: 2100 0x2C: 2150 0x2D: 2200 0x2E: 2250 0x2F: 2300 0x30: 2350 0x31: 2400 0x32: 2450 0x33: 2500 0x34: 2550 0x35: 2600 0x36: 2650 0x37: 2700 0x38: 2750 0x39: 2800 0x3A: 2850

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: 2900 0x3C: 2950 0x3D: 3000 0x3E: 3050 0x3F: 3100 0x40: 3150 0x41: 3200 0x42: 3250 0x43: 3300 0x44: 3350 0x45: 3400 0x46: 3450 0x47: 3500 0x48: 3550 0x49: 3600 0x4A: 3650 0x4B: 3700 0x4C: 3750 0x4D: 3800 0x4E: 3850 0x4F: 3900 0x50: 3950 0x51: 4000 0x52: 4050 0x53: 4100 0x54: 4150 0x55: 4200 0x56: 4250 0x57: 4300 0x58: 4350 0x59: 4400 0x5A: 4450 0x5B: 4500 0x5C: 4550 0x5D: 4600 0x5E: 4650 0x5F: 4700 0x60: 4750 0x61: 4800 0x62: 4850 0x63: 4900 0x64: 4950 0x65: 5000 0x66: 5050 0x67: 5100 0x68: 5150 0x69: 5200 0x6A: 5250 0x6B: 5300 0x6C: 5350 0x6D: 5400 0x6E: 5450 0x6F: 5500 0x70: 5550 0x71: 5600 0x72: 5650 0x73: 5700 0x74: 5750 0x75: 5800

BITFIELD	BITS	DESCRIPTION	DECODE
			0x76: 5850 0x77: 5900 0x78: 5950 0x79: 6000 0x7A: 6050 0x7B: 6100 0x7C: 6150 0x7D: 6200 0x7E: 6250 0x7F: 6300

CHG_CNFG_09 (0x1F)

Charger configuration 9

BIT	7	6	5	4	3	2	1	0
Field	INLIM_CLK[1:0]		OTG_ILIM[2:0]			MINVSYS[2:0]		
Reset	0x2		0x3			0x3		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
INLIM_CLK	7:6	Input Current Limit Soft-Start Period (µs) Between Consecutive Increments of 25mA	0b00: 8 0b01: 256 0b10: 1024 0b11: 4096
OTG_ILIM	5:3	OTG Mode Current Limit Setting (mA)	0b000: 500 0b001: 900 0b010: 1200 0b011: 1500 0b100: 2000 0b101: 2250 0b110: 2500 0b111: 3000
MINVSYS	2:0	Minimum System Regulation Voltage (V)	2 Cell Battery 0b000: 5.535 0b001: 5.740 0b010: 5.945 0b011: 6.150 0b100: 6.355 0b101: 6.560 0b110: 6.765 0b111: 6.970 3 Cell Battery 0b000: 8.303 0b001: 8.610 0b010: 8.918 0b011: 9.225 0b100: 9.533 0b101: 9.840 0b110: 10.148 0b111: 10.455

CHG_CNFG_10 (0x20)

Charger configuration 10

BIT	7	6	5	4	3	2	1	0
Field	SPR[1:0]		VCHGIN_REG[4:0]					DISKIP
Reset	0x0		0x04					0x0
Access Type	Write, Read		Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:6	Spare Bit	
VCHGIN_REG	5:1	CHGIN Voltage Regulation Threshold (V)	0x00: 4.025 0x01: 4.200 0x02: 4.375 0x03: 4.550 0x04: 4.725 0x05: 4.900 0x06: 5.425 0x07: 5.950 0x08: 6.475 0x09: 7.000 0x0A: 7.525 0x0B: 8.050 0x0C: 8.575 0x0D: 9.100 0x0E: 9.625 0x0F: 10.150 0x10: 10.675 0x11: 10.950 0x12: 11.550 0x13: 12.150 0x14: 12.750 0x15: 13.350 0x16: 13.950 0x17: 14.550 0x18: 15.150 0x19: 15.750 0x1A: 16.350 0x1B: 16.950 0x1C: 17.550 0x1D: 18.150 0x1E: 18.750 0x1F: 19.050
DISKIP	0	Charger Skip Mode Disable	0b0: Autoskip mode 0b1: Disable skip mode

Applications Information

Inductor Selection

Buck-boost allows a range of inductance for different combinations of switching frequency and maximum nominal CHGIN voltage. See Table 11 for recommendations. The lower the inductor DCR is, the higher the buck-boost efficiency is. The user needs to weigh the trade-offs between inductor size and DCR value and choose a suitable inductor for the buck-boost. See Table 12 for inductor recommendations.

Table 11. Recommended Inductance for Combinations of Switching Frequency and Maximum Nominal CHGIN Voltage

SWITCHING FREQUENCY (kHz)	MAXIMUM NOMINAL CHGIN VOLTAGE (V)	RECOMMENDED NOMINAL INDUCTANCE (µH)
600	15 or lower	2.2, 3.3
	Higher than 15	3.3
1200	15 or lower	1.0, 1.5, 2.2, 3.3
	Higher than 15	1.5, 2.2, 3.3

Table 12. Suggested Inductors

ROOT PART NUMBER	MFGR.	SERIES	NOMINAL INDUCTANCE (µH)	TYPICAL DC RESISTANCE (mΩ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT = +40°C RISE	DIMENSIONS L x W x H (mm)
MAX77960B	TDK	VLS3012HBX-1R0M	1.0	39.0	6.11	5.13	3.0 x 3.0 x 1.2
	Coilcraft	XAL4020-152ME	1.5	21.5	7.1	7.5	4.0 x 4.0 x 2.1
	Coilcraft	XAL4020-222ME	2.2	35.2	5.6	5.5	4.0 x 4.0 x 2.1
	Coilcraft	XAL4030-332ME	3.3	26.0	5.5	6.6	4.0 x 4.0 x 3.1
MAX77961B	Pulse	PA5002.102NLT	1.0	12.0	12.8	10.5	5.5 x 5.3 x 1.8
	Pulse	PA5003.152NLT	1.5	10.1	12.5	10.5	5.5 x 5.3 x 2.9
	Cyntec	CMLE063T-2R2MS	2.2	11.0	14.0	10.0	6.95 x 6.6 x 2.8
	Pulse	PA5007.332NLT	3.3	16.3	15.0	10.0	7.8 x 7.6 x 2.9

CHGIN Capacitor Selection

The CHGIN capacitor, C_{CHGIN}, reduces the current peaks drawn from the input power source and reduces switching noise in the device. In OTG mode, it also reduces the output voltage ripple and ensures regulation loop stability. The impedance of C_{CHGIN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. See Table 13 for CHGIN capacitor recommendations.

Table 13. Suggested CHGIN Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Murata	GRM32ER7YA106KA12	10	35	X7R	1210	3.2 x 2.5 x 2.5
Murata	GRT31CR6YA106KE01	10	35	X5R	1206	3.2 x 1.6 x 1.6
Murata	GRM21BR6YA106ME43	10	35	X5R	0805	2.0 x 1.25 x 1.25

SYS Capacitor Selection

The SYS capacitor, C_{SYS}, is required to keep the output voltage ripple small and to ensure regulation loop stability. The C_{SYS} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, buck-boost requires 40μF of minimum effective output capacitance. Considering the DC bias characteristic of ceramic capacitors, 2 x 47μF (1210) or 3 x 47μF (1206) or 7 x 22μF (0805) capacitors are recommended for 2-cell applications, and 3 x 47μF (1210) or 4 x 47μF (1206) capacitors are recommended for 3-cell applications. See Table 14 for SYS capacitor recommendations.

Table 14. Suggested SYS Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (μF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Taiyo Yuden	EMK325ABJ476MM8P	47	16	X5R	1210	3.2 x 2.5 x 2.5
Murata	GRM31CR61C476ME44	47	16	X5R	1206	3.2 x 1.6 x 1.6
Murata	GRM21BR61C226ME44	22	16	X5R	0805	2.0 x 1.25 x 1.25

Battery Insertion Protection

When the battery hot inserts into the MAX77960B/MAX77961B, it creates high inrush current flowing through the body diode of Q_{BAT} FET. The inrush current peaks at tens of amperes and lasts for less than a few hundreds of microseconds. Such current can possibly damage the Q_{BAT} FET. For IC protection, the following battery insertion protection is required on the board:

- For system designs with a 2S battery, include an external 3A Schottky diode from BATT to SYS. The Schottky diode has low forward voltage drop when conducting high current in the forward direction. It diverts the inrush current from BATT to SYS at battery insertion. The inrush current flowing through the Q_{BAT} FET is greatly reduced and therefore the IC is protected. See Figure 14.
- For system designs with a 3S battery, the inrush current is higher than a 2S battery due to higher battery voltage. In addition to the 3A Schottky diode from BATT to SYS, it is required to include an inrush protection circuit. The inrush protection circuit consists of an FET and RC network. See Figure 15 for a complete solution. At battery hot insertion, V_{GS} of the FET is slowly charged by the RC network. The FET gradually turns on and limits the inrush current. For FET selection, check the current and voltage rating of the FET to guarantee that it satisfies the system specification.

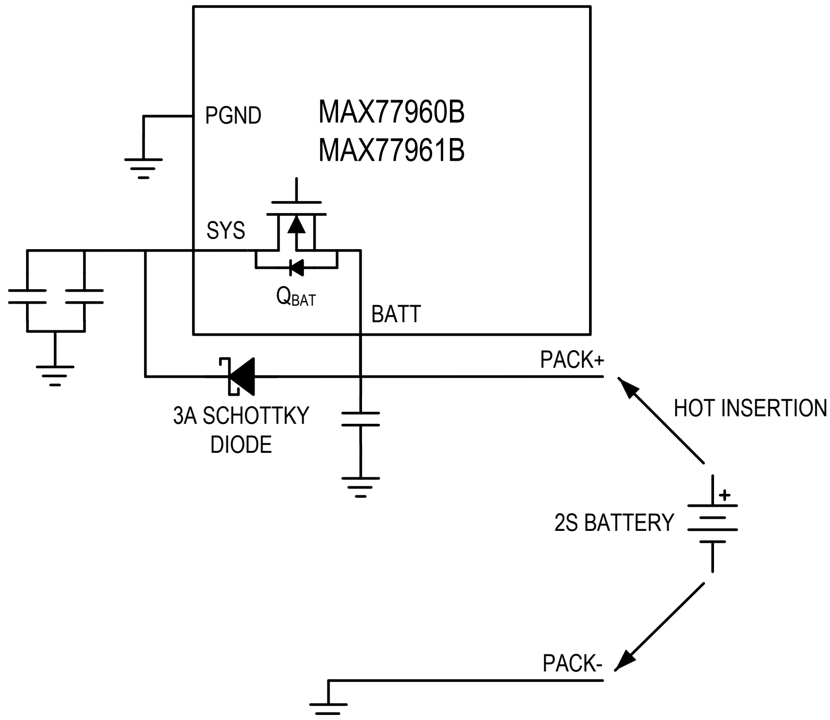


Figure 14. Battery Insertion Protection with 2S Battery

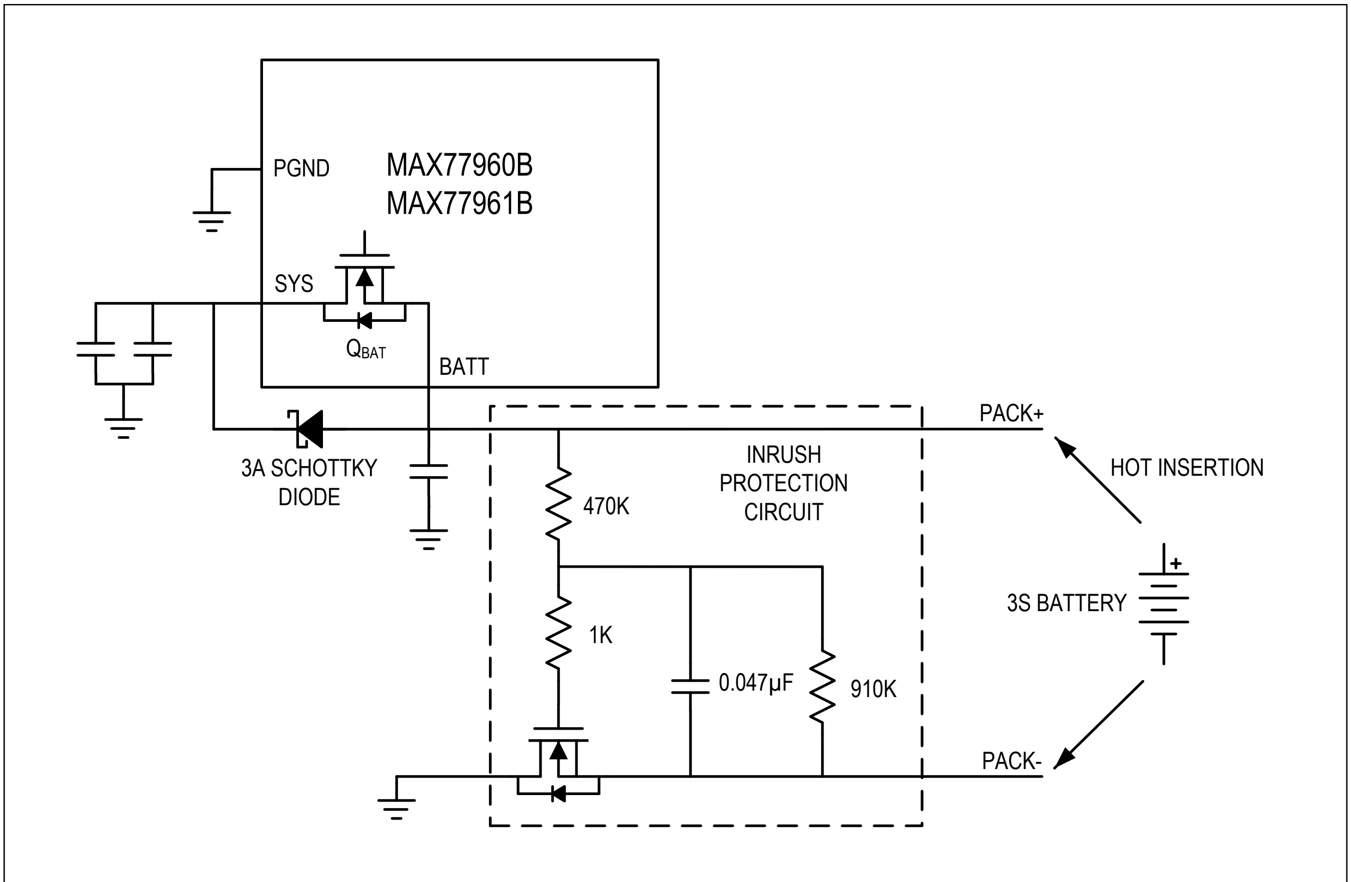


Figure 15. Battery Insertion Protection with 3S Battery

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 16 shows a PCB layout example.

When designing the PCB, follow these guidelines:

1. Place the CHGIN capacitor (C_{CHGIN}) and SYS capacitors (C_{SYS}) immediately next to the CHGIN pin and SYS pin of the IC, respectively. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops which can cause high voltage spikes and can damage the internal switching MOSFETs.
2. Place the inductor next to the LX pins and make the traces between the LX pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer, make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3. Route LX nodes to their corresponding bootstrap capacitors (C_{BST}) as short as possible. Prioritize C_{BST} placement to reduce trace length to the IC.
4. Route CSINP and CSINN traces as symmetrical as possible. Having the same trace parasitics improves accuracy of the differential CHGIN current sensing.
5. Place the PVL capacitor (C_{PVL}) immediately next to the PVL pin. Proximity to the IC provides a stable supply for the internal circuitry.
6. Place the BATT capacitor (C_{BATT}) and SYSA capacitor (C_{SYSA}) immediately next to the BATT pin and SYSA pin of the IC, respectively.

7. Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
8. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *SYS Capacitor Selection* section and refer to *Tutorial 5527* for more information.

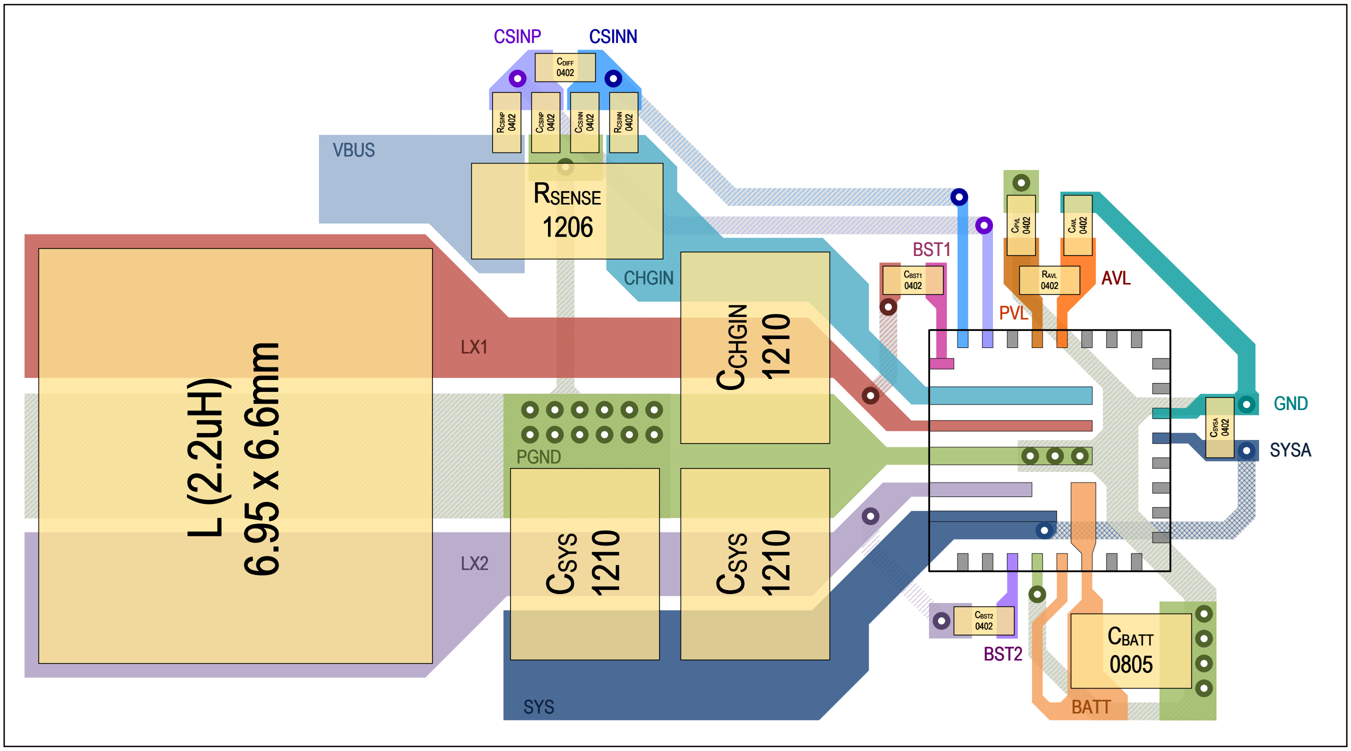
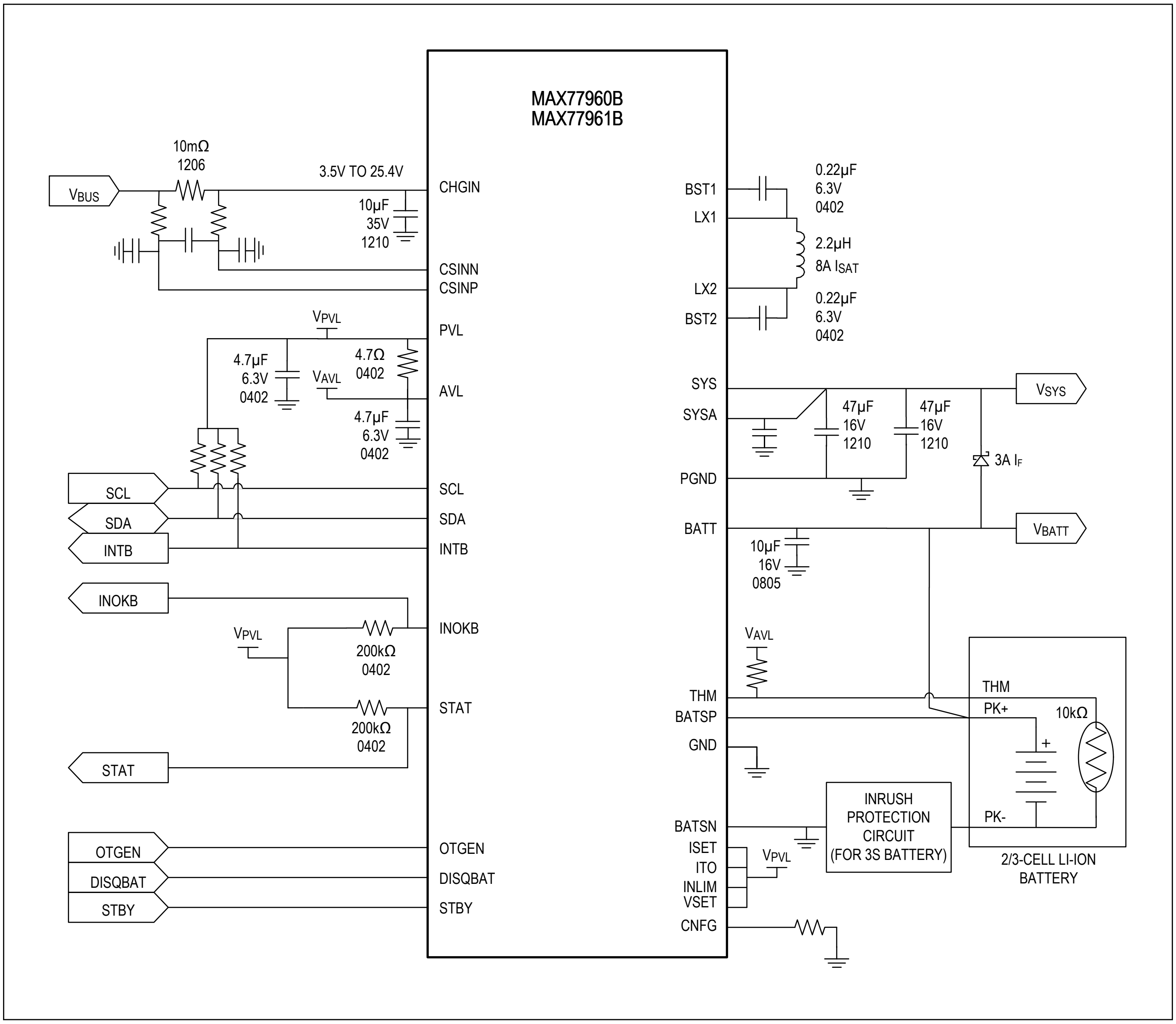


Figure 16. PCB Layout Example

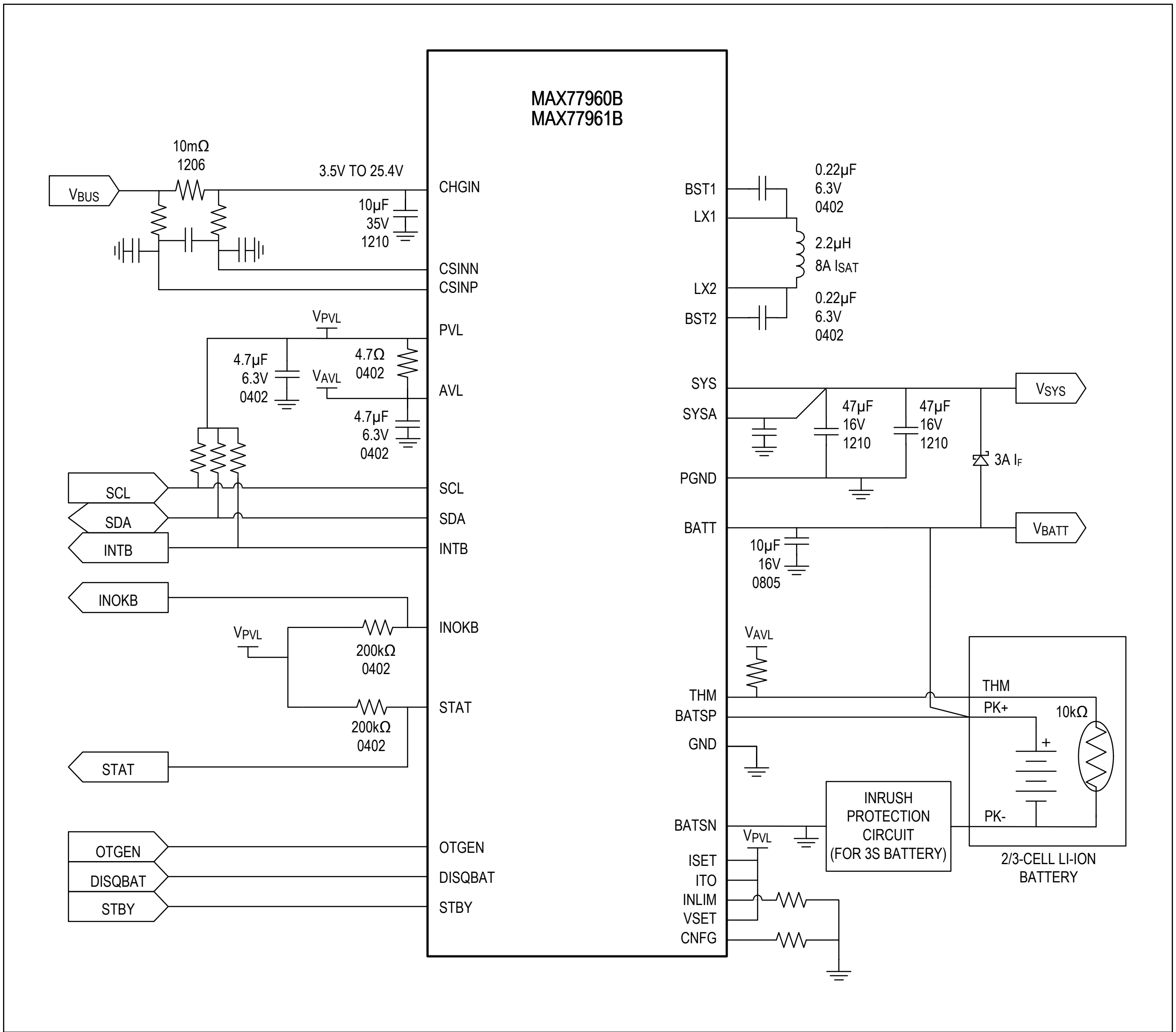
Typical Application Circuits

Wide-Input I²C Programmable Charger



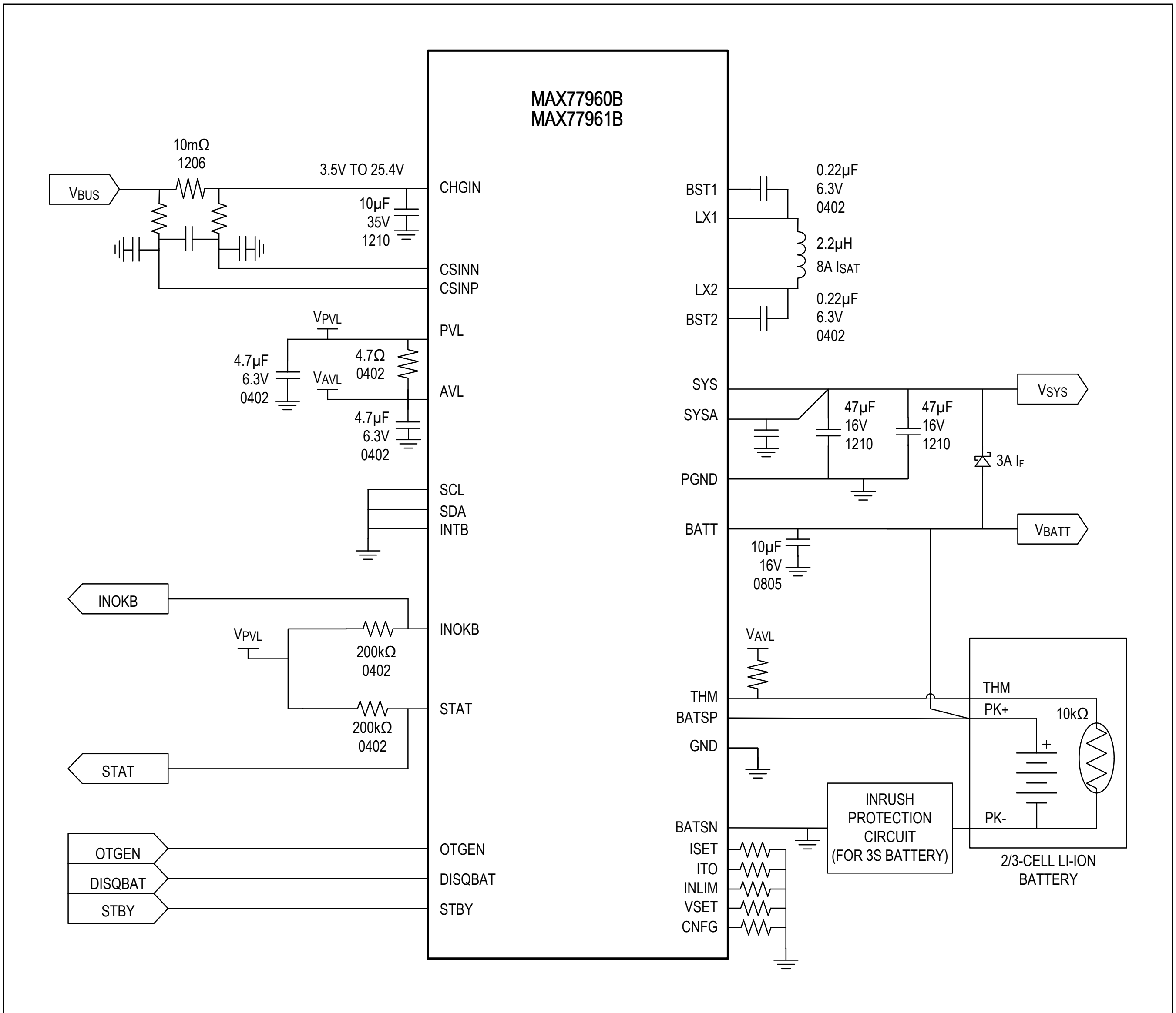
Typical Application Circuits (continued)

Wide-Input I²C Programmable Charger with Charger Disabled



Typical Application Circuits (continued)

Wide-Input Autonomous Charger



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	SWITCHING FREQUENCY	NUMBER OF SERIES BATTERY CELLS	MAXIMUM CHARGING CURRENT
MAX77960BEFV06+	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	600kHz	2, 3	3A
MAX77960BEFV06+T	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	600kHz	2, 3	3A
MAX77960BEFV12+	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	1.2MHz	2	3A
MAX77960BEFV12+T	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	1.2MHz	2	3A
MAX77961BEFV06+	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	600kHz	2, 3	6A
MAX77961BEFV06+T	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	600kHz	2, 3	6A
MAX77961BEFV12+	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	1.2MHz	2	5A
MAX77961BEFV12+T	-40°C to +85°C	4mm x 4mm, 30-Lead FC2QFN	1.2MHz	2	5A

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—