MAX8698C PMIC Datasheet

for

Samsung Application Processor – S5PC100

Rev 08

Revision History

Rev	Date	Changes	Author
0	11/13/2008	Preliminary- Initial Release	John (Bang Sup) Lee
2	2/5/2009	Power up sequence is revised. In order to control Buck1 and Buck2 by PWREN hardware pin, the I2C control registers of Buck1 and Buck2 must be set to 0 after power up. LDO6 default voltage is changed to 2.6V. LDO5 default voltage is changed to 2.8V. No Load Supply Current 2 is revised	John (Bang Sup) Lee
3	2/18/2009	Load Regulation for LDO4/LDO9 changed to 25mV from 40mV	John (Bang Sup) Lee
4	3/10/2009	Part number is changed to MAX8698CEWO+T	John (Bang Sup) Lee
5	5/7/2009	No load supply current 2 has been updated.	John (Bang Sup) Lee
6	5/18/2009	Revised Figure 6	John (Bang Sup) Lee
7	10/13/2009	Revised Turn-off technical description in Page 28. In the description, removed ELDO9 from the turn-off sources.	John (Bang Sup) Lee
8	12/08/2009	Corrected typos in LDO1 description	John (Bang Sup) Lee

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High Efficiency, Low I_Q, PMIC with Dynamic Voltage Management for Samsung Application Processor S5PC100

General Description

The MAX8698C power management ICs are optimized for devices using Samsung S5PC100® processors, including smart cellular phones, PDAs, internet appliances, and other portable devices requiring substantial computing and multimedia capability and low power consumption.

The MAX8698C integrates 12 high-performance low-operating-current power supplies along with management functions. Regulator outputs include three step-down DC-DC outputs, 8 linear regulators, an always-on RTCLDO and a backup charger. Step-down DC-DC converter outputs include a 1.8V for memory and two serial-programmed and GPIO controlled outputs to separately power both the processor core and processor internal memory. The processor core and internal memory outputs feature dynamic voltage management and default to 1.2V for processor core and 1.2V for internal memory(Default are off during power up). Additional functions include on/off control for outputs, low-battery detection, a 60ms reset output, and a two-wire I^2C^{TM} serial interface.

All Step-down DC-to-DC outputs are able of running at a switching frequency of up to 4MHz, minimizing the size of the external components. They utilize a proprietary hysteretic PWM control scheme that switches with nearly fixed frequency. Input voltage range is from 2.7V to 5.5V allowing a 1-cell Li-Ion, 3-cell NiMH, or a 5V input. The MAX8698C are available in 42-pin 3.53mm x 3.15mm x 0.64mm WLP package.

Applications

PDA, Palmtop, and Wireless Handhelds
Smart Cell phones
Portable GPS Navigation
Personal Media Players
Digital Cameras

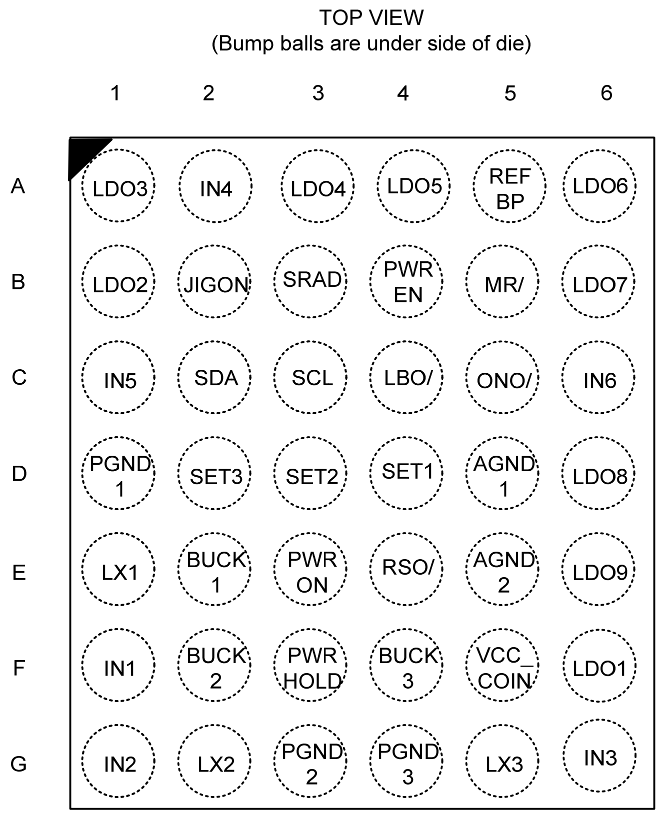
Features

- Optimized for Samsung S5PC100®Processors
- 3 Synchronous Step-Down Converters
    - Buck1 Serial Programmed for Core/ maximum 1.2V/1A
    - Buck2 Serial Programmed for Internal Memory / maximum 1.2V/1A
    - Buck3 for Memory/ maximum 1.8V/800mA
- 9 LDO Regulators
    - LDO1 3.0V Always-On Supply @ 10mA for RTC
    - LDO2 1.2V @ 10mA for VCC_ALIVE
    - LDO3 1.2V @ 50mA
    - LDO4 1.8V @ 450mA
    - LDO5 2.8V @ 300mA
    - LDO6 2.6V @ 150mA
    - LDO7 3.0V @ 150mA
    - LDO8 3.3V @ 150mA
    - LDO9 3.0V @ 450mA
- 1 Back up Battery charger
- 4MHz PWM Switching Allows Small External Components
- Low-Battery Monitor and Reset Output
- 42-pin 3.53mm x 3.15mm WLP Package
- I2C Interface for Programming

Ordering Information

PART	PACKAGE CODE	TEMP RANGE	PIN-PACKAGE
MAX8698CEWO+T	W423A3-1	-40°C to +85°C	42 pins, WLP (0.5 pitch), 3.53mm x 3.15mm

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

IN1, IN2, IN3, IN4, IN5, IN6, SCL, SDA to AGND .... -0.3V to +6.0V
BUCK1 to PGND1 .... -0.3V to (V_{IN1}+0.3V)
BUCK2 to PGND2 .... -0.3V to (V_{IN2}+0.3V)
BUCK3 to PGND3 .... -0.3V to (V_{IN3}+0.3V)
LDO2, LDO3, LDO4, LDO5, to AGND .... -0.3V to (V_{IN4}+0.3V)
REFBP, LDO1, VCC_COIN, PWREN, /LBO\, /RSO\, /MR\, SET1, SET2, SET3, JIGON, PWRON, ONO\,
PWRHOLD, SRAD, JIGON to AGND .... -0.3V to (V_{IN5}+0.3V)
LDO6,LDO7, LDO8, LDO9, to AGND .... -0.3V to (V_{IN6}+0.3V)
IN1, IN2, IN3, IN4, IN5 to IN6 .... -0.3V to +0.3V
LX1 Continuous RMS Current (Note1) 1A
LX2 Continuous RMS Current (Note1) 1A
LX3 Continuous RMS Current (Note1) 0.8A
PGND_ to AGND .... -0.3V to +0.3 V
BUCK1, BUCK2, BUCK3, LDO3 to LDO9, and Backup Charger Output Short-Circuit Duration .Continuous
Continuous Power Dissipation (T_A=+70°C) (Derate 29mW/°C above 70°C) 2.3W
Operating Temperature Range .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

Note 1: LX_ has internal clamp diodes to PG_ and PV_. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C, where V_{IN1} to V_{IN6}=main battery voltage.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
	No Load Supply Current 1	Backup Charger, LDO1 and Battery Monitor on, other circuits off. V_{IN1} to V_{IN6}=4.2V		17	30	µA
	No Load Supply Current 2	Buck3, LDO1, LDO2, LDO3, LDO5, LDO6, LDO8 LDO9, Battery Monitor, and Backup charger on, other circuits off. V_{IN1} to V_{IN6}=4.2V		220	<340>	µA
	No Load Supply Current 3	BUCK1 to Buck3, LDO1 to LDO9, Backup charger and Battery Monitor on, V_{IN1} to V_{IN6}=4.2V		260		µA
	Light Load Supply Current (Note1)	BUCK1 to Buck3 with 500uA load & LDO1, LDO2, LDO5, LDO6~LDO9, and Backup charger on, other circuits off. V_{IN1} to V_{IN6}=4.2V		830		µA
	Undervoltage Lockout (UVLO)					
	Undervoltage Lockout Threshold Undervoltage Lockout Threshold	V_{IN5} rising V_{IN5} falling	2.7	2.85 2.35	3.05	V
	Programmable Low Battery Detect					

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	Programmable Low Battery Detect Hysteresis	See the register " LBHYST in LBCNFG"			100 200(Default) 300 400		mV
	Programmable Low Battery Detect Threshold	V_{IN5} falling (See the register " LBTH in LBCNFG"			2.8 2.9 3.0 3.1(Default) 3.2 3.3 3.4 3.5		V
	THERMAL SHUTDOWN						
	Threshold				160		°C
	Hysteresis				15		°C
	REFERENCE						
	Reference Bypass Output Voltage			-1.5%	1.25	+1.5%	V
	REF Supply Rejection	2.5V≤IN1≤5.5V, Test purposes only			0.2	5	mV
	LOGIC AND CONTROL INPUTS						
	Input Low Level	PWRHOLD, SCL, SDA, MR\, PWRON, JIGON, SET1, SET2, SET3, PWREN, $2.5V \leq V_{IN1\sim6} \leq 5.5V$, Ta=25°C				0.4	V
	Input High Level	PWRHOLD, SCL, SDA, MR\, PWRON, JIGON, SET1,SET2, SET3, PWREN, $2.5V \leq V_{IN1\sim6} \leq 5.5V$, Ta=25°C		1.4			V
	SCL, SDA Input Hysteresis				0.1		V
	SRAD Low Level	Three state input				0.5	V
	SRAD High Level	Three state input		V_{IN5} - 0.5			V
	Logic Input Current PWRHOLD, SCL, SDA, MR\, SRAD, SET1, SET2, SET3, PWREN,	0V<Vin<5.5V	T_A = 25°C	-1		1	µA
			T_A = 85°C		0.1		uA
	SCL, SDA Input capacitance					10	pF
	SDA Output Low Voltage	2.6V<= Vin <= 5.5V, Sinking 3mA				0.2	V
	ONO\, RSO\, LBO\ Output Low Voltage	Isink = 1mA				0.4	V

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	ONO\, RSO\, LBO\ Output High Leakage	V_{IN5} = 5.5V	T_A = 25°C	-1	0	1	uA
			T_A = 85°C		0.1		
	MR\ Pull-up resistor to V_{IN5}			400	800	1600	kΩ
	PWRON Pull-down resistor to GND			400	800	1600	kΩ
	JIGON Pull-down resistor to GND			400	800	1600	kΩ
	RSO\ De-assert Delay				60		msec

Note1. Design guidance only, not tested during final test.

Buck Converter 1 & 2 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20μF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	Ground Current	I_{LOAD} =0, no switching (Note1)			26		μA
	Input Voltage Range			2.7		5.5	V
	Default output Voltage	I_{Load}=100mA	BUCK1	-3%	1.2	+3%	V
			BUCK2	-3%	1.2	+3%	
	Programmable Output Voltage	I_{Load}=100mA, Programmable Output Voltage Steps (BUCK1 and BUCK2) =50mV		-3%	0.75 0.80 0.85 0.90 0.95 1.00 1.05 1.10 1.15 1.20 1.25 1.30 1.35 1.40 1.45 1.50	+3%	V
	Output Voltage Line regulation	V_{IN1} to V_{IN6}= +2.7V to 5.5V			0.3		%/V
	Current Limit	PFET Switch		1200	1600	2000	mA
		NFET Rectifier		800	1200	1600	mA
	On-Resistance	PFET Switch, I_{LX} = -150mA			0.2		Ω
		NFET Rectifier, I_{LX} = 150mA			0.11		Ω
	Rectifier Off Current Threshold				40		mA
	Minimum On- and Off-Times	Ton			70		nsec

		Toff		70		nsec
	Shutdown Output Resistance	I2C programmable. See the Register Buck1_ADISCHG= “1” Buck2_ADISCHG= “1”		1000		Ω
	Output Load Regulation	Equal to inductor DC resistance divided by 4		$R_L/4$		V/A
	Lx Leakage Current	Lx=PGND or IN, Ta=25℃		0.1	1	uA

Note1. Design guidance only, not tested during final test.

Buck Converter 3 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20μF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
	Ground Current	I_{LOAD} =0, no switching (Note1)		26		μA
	Input Voltage Range		2.7		5.5	V
	Default output Voltage	I_{Load}=100mA	-3%	1.8	+3%	V
	Programmable Output Voltage	I_{Load}=100mA, Programmable Step = 100mV	-3%	1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
	Output Voltage Line regulation	V_{IN1} to V_{IN6}= +2.7V to 5.5V		0.3		%/V
	Current Limit	PFET Switch	900	1350	1800	mA
		NFET Rectifier	700	1050	1400	mA
	On-Resistance	PFET Switch, I_{LX} = -150mA		0.45		Ohms
		NFET Rectifier, I_{LX} = 150mA		0.25		Ohms
	Rectifier Off Current Threshold			40		mA
	Minimum On- and Off-Times	Ton		70		nsec
		Toff		70		nsec

	Shutdown Output Resistance	I2C programmable. See the Register Buck3_ADISCHG= "1"		1000		Ω
	Output Load Regulation	Equal to inductor DC resistance divided by 4		$R_L/4$		V/A
	Lx Leakage Current	Lx=PGND or IN, Ta=25°C		0.1	1	uA

Note1. Design guidance only, not tested during final test.

LDO1 (Always On LDO) Electrical Characteristics –VCC_RTC

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range (Note1)	Input Supply = VCC_COIN	2.7		5.5	V
Ground Current (Note1)	I_{LDO1}=500µA		5		µA
Output voltage LDO1	10uA@ VCC_COIN = 5.5V 1mA@ VCC_COIN = 3.1V	2.90	3.0	3.10	V
Output current				10	mA
Minimum Operating output Voltage	10uA@VCC_COIN=1.7V, V_{IN1} to V_{IN6}= 0V	1.5	1.65		V
Softstart Ramp Rate(Note1)		0.002		3	V/us

Note1. Design guidance only, not tested during final test.

LDO2 Electrical Characteristics – VCC_ALIVE

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO2	1mA@ V_{IN4} = +5.5V 10mA@ V_{IN4} =IN4=3.4V	-3%	1.2	+3%	V
Programmable Output Voltage	I_{LDO2}=5mA	-3%	0.80 0.85 0.90 0.95 1.00 1.05 1.10 1.15 1.20 1.25 1.30	+3%	V
Output current				10	mA
Current limit	LDO2 short to GND	65			mA
Line regulation	$3.4V \le V_{IN4} \le 5.5V$, I_{LDO2}=5mA		0.5		mV

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Load regulation	50μA < I_{LDO2} < 10mA		0.5		mV
Ground current (Note1)	I_{LDO2}=500μA		6		μA
Output Noise Voltage (RMS)	100Hz-100kHz, CLDO2=1uF, I_{LDO1}=10mA		80		uV_{RMS}
Output capacitor for stable operation (Note1)	0μA < I_{LDO2} < 30mA MAX ESR = 100mΩ	0.7	1.0		μF
Start up time from shutdown(Note1)	C_{LDO2} = 1μF, I_{LDO2} = 30mA		40	100	μs
Shutdown Output Resistance	I2C programmable. See the Register LDO2_ADISCHG= "1"		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO3 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20μF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO3	1mA@ V_{IN4}= +5.5V 30mA@ V_{IN4}=3.4V	-3%	1.2	+3%	V
Programmable Output Voltage	I_{LDO3}= 15mA	-3%	0.80 0.85 0.90 0.95 1.00 1.05 1.10 1.15 1.20 1.25 1.30	+3%	V
Output current				50	mA
Current limit	LDO3 short to GND	65			mA
Line regulation	3.4V≤V_{IN4}≤5.5V, I_{LDO3}=15mA		0.5		mV
Load regulation	50μA < I_{LDO3} < 50mA		1		mV
Ground current (Note1)	I_{LDO3}=500μA		6		μA
Output capacitor for stable operation (Note1)	0μA < I_{LDO3} < 50mA MAX ESR = 100mΩ	0.7	1.0		μF
Start up time from shutdown(Note1)	C_{LDO3} = 1μF, I_{LDO3} = 30mA		40	100	μs
Shutdown Output Resistance	I2C programmable. See the Register LDO3_ADISCHG= "1"		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO4 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO4	1mA@ V_{IN4}= +5.5V 300mA@ V_{IN4}=3.4V	-3%	1.8	+3%	V
Programmable Output Voltage	V_{IN1} to V_{IN6}= +4.2V I_{LDO4}=150mA	-3%	1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
Output current				450	mA
Current limit	LDO4 short to GND	460	820	1400	mA
Drop-out voltage	I_{LDO4}=200mA , T_A =25°C		120	400	mV
Line regulation	3.4V≤V_{IN4}≤5.5V, I_{LDO4}=150mA, V_{LDO4}= 3.0V		2.4		mV
Load regulation	50µA < I_{LDO4} < 450mA		25		mV
Ground current (Note1)	I_{LDO4}=500µA		21		µA
Output capacitor for stable operation (Note1)	0µA < I_{LDO4} < 450mA MAX ESR = 100mΩ	1.4	2.2		µF
Start up time from shutdown (Note1)	C_{LDO4} = 2.2µF, I_{LDO4} = 300mA		40	100	µs
Start-up transient overshoot (Note1)	C_{LDO4} = 2.2µF, I_{LDO4} = 300mA		3	50	mV
Power Supply Reject ΔLDO4/ΔV_{IN4}	f=10Hz-10kHz, C_{LDO4} = 2.2µF,I_{LDO4}=30mA		60		dB
Output Noise Volt. (RMS)	100Hz-100kHz, C_{LDO4}= 2.2µF, I_{LDO4}=30mA		80		μV_{RMS}

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Output Resistance	I2C programmable. See the Register LDO4_ADISCHG= “1”		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO5 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO5	1mA@ V_{IN4}= +5.5V 300mA@ V_{IN4}=3.4V	2.716	2.800	2.884	V
Programmable Output Voltage	V_{IN1} to V_{IN6}= +4.2V I_{LDO5}= 150mA	-3%	1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
Output current				300	mA
Current limit	LDO5 short to GND	310	550	940	mA
Drop-out voltage	I_{LDO5}=200mA , T_A =25°C		120	400	mV
Line regulation	3.4V≤V_{IN4}≤5.5V, I_{LDO5}=150mA		2.4		mV
Load regulation	50µA < I_{LDO5} < 300mA		25		mV
Ground current (Note1)	I_{LDO5}=500µA		21		µA
Output capacitor for stable operation (Note1)	0µA < I_{LDO5} < 300mA MAX ESR = 100mΩ	1.4	2.2		µF
Start up time from shutdown(Note1)	C_{LDO5} = 2.2µF, I_{LDO5} = 300mA		40	100	µs
Start-up transient overshoot (Note1)	C_{LDO5} = 2.2µF, I_{LDO5} = 300mA		3	50	mV
Power Supply Reject $\Delta LDO5/\Delta V_{IN4}$	f=10Hz-10kHz, C_{LDO5} = 2.2µF,I_{LDO5}=30mA		60		dB

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise Volt. (RMS)	100Hz-100kHz, C_{LDO5}= 2.2µF, I_{LDO5}=30mA		80		$µV_{RMS}$
Shutdown Output Resistance	I2C programmable. See the Register LDO5_ADISCHG= "1"		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO6 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Output voltage LDO6	1mA@ V_{IN6}= +5.5V 150mA@ V_{IN6}=3.4V	-3%	2.6	+3%	V
Programmable Output Voltage	V_{IN1} to V_{IN6}= +4.2V I_{LDO6}= 75mA	-3%	1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
Output current				150	mA
Current limit	LDO6 short to GND	165	360	650	mA
Drop-out voltage	I_{LDO6}=100mA , T_A =25°C		60		mV
Line regulation	3.4V≤V_{IN6}≤5.5V, I_{LDO6}=100mA		2.4		mV
Load regulation	50µA < I_{LDO6} < 150mA		25		mV
Ground current (Note1)	I_{LDO6}=500µA		21		µA
Output capacitor for stable operation (Note1)	0µA < I_{LDO6} < 150mA MAX ESR = 100mΩ	0.7	1.0		µF
Start up time from shutdown(Note1)	C_{LDO6} = 1µF, I_{LDO6} = 150mA		40	100	µs
Start-up transient overshoot (Note1)	C_{LDO6} = 1µF, I_{LDO6} = 150mA		3	50	mV

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Reject $\Delta LDO6/\Delta V_{IN6}$	f=10Hz-10kHz, C_{LDO6} = 1µF,I_{LDO6}=30mA		60		dB
Output Noise Volt. (RMS)	100Hz-100kHz, C_{LDO6}= 1µF, I_{LDO6}=30mA		80		μV_{RMS}
Shutdown Output Resistance	I2C programmable. See the Register LDO6_ADISCHG= “1”		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO7 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO7	1mA@ V_{IN6}= +5.5V 150mA@ V_{IN6}=3.4V	-3%	3.0	+3%	V
Programmable Output Voltage	V_{IN1} to V_{IN6}= +4.2V I_{LDO7}= 75mA	-3%	1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
Output current				150	mA
Current limit	LDO7 short to GND	165	360	650	mA
Drop-out voltage	I_{LDO7}=100mA , T_A =25°C		60		mV
Line regulation	3.4V≤V_{IN6}≤5.5V, I_{LDO6}=100mA		2.4		mV
Load regulation	50µA < I_{LDO7} < 150mA		25		mV
Ground current (Note1)	I_{LDO7}=500µA		21		µA
Output capacitor for stable operation (Note1)	0µA < I_{LDO7} < 150mA MAX ESR = 100mΩ	0.7	1.0		µF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Start up time from shutdown(Note1)	C_{LDO7} = 1µF, I_{LDO7} = 150mA		40	100	µs
Start-up transient overshoot (Note1)	C_{LDO7} = 1µF, I_{LDO7} = 150mA		3	50	mV
Power Supply Reject ∆LDO7/∆V_{IN6}	f=10Hz-10kHz, C_{LDO7} = 1µF,I_{LDO7}=30mA		60		dB
Output Noise Volt. (RMS)	100Hz-100kHz, C_{LDO7}= 1µF, I_{LDO7}=30mA		80		µV_{RMS}
Shutdown Output Resistance	I2C programmable. See the Register LDO7_ADISCHG= "1"		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO8 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO8	1mA@ V_{IN6}= +5.5V 150mA@ V_{IN6}=3.7V	-3%	3.3	+3%	V
Programmable Output Voltage	V_{IN1} to V_{IN6}= +4.2V I_{LDO8}=75mA	-3%	3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
Output current				150	mA
Current limit	LDO8 short to GND	165	360	650	mA
Drop-out voltage	I_{LDO8}=100mA , T_A =25°C		60		mV
Line regulation	3.4V≤V_{IN6}≤5.5V, I_{LDO8}=100mA, VLDO8=3.0V		2.4		mV
Load regulation	50µA < I_{LDO8} < 150mA		25		mV
Ground current (Note1)	I_{LDO8}=500µA		21		µA
Output capacitor for stable operation (Note1)	0µA < I_{LDO8} < 150mA MAX ESR = 100mΩ	0.7	1.0		µF
Start up time from shutdown(Note1)	C_{LDO8} = 1µF, I_{LDO8} = 150mA		40	100	µs
Start-up transient overshoot (Note1)	C_{LDO8} = 1µF, I_{LDO8} = 150mA		3	50	mV
Power Supply Reject ∆LDO8/∆V_{IN6}	f=10Hz-10kHz, C_{LDO8} = 1µF,I_{LDO8}=30mA		60		dB
Output Noise Volt. (RMS)	100Hz-100kHz, C_{LDO8}= 1µF, I_{LDO8}=30mA		80		µV_{RMS}

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Output Resistance	I2C programmable. See the Register LDO7_ADISCHG= “1”		1000		Ω

Note1. Design guidance only, not tested during final test.

LDO9 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range[1]		2.7		5.5	V
Default output voltage LDO9	1mA@ V_{IN6}= +5.5V 300mA@ V_{IN6}=3.4V	-3%	3.0	+3%	V
Programmable Output Voltage	V_{IN1} to V_{IN6}= +4.2V I_{LDO9}=150mA	-3%	1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4 3.5 3.6	+3%	V
Output current				450	mA
Current limit	LDO9 short to GND	460	820	1400	mA
Drop-out voltage	I_{LDO9}=200mA , T_A =25°C		120	400	mV
Line regulation	3.4V≤V_{IN6}≤5.5V, I_{LDO9}=150mA		2.4		mV
Load regulation	50µA < I_{LDO9} < 450mA		25		mV
Ground current (Note1)	I_{LDO9}=500µA		21		µA
Output capacitor for stable operation (Note1)	0µA < I_{LDO9} < 450mA MAX ESR = 100mΩ	1.4	2.2		µF
Start up time from shutdown(Note1)	C_{LDO9} = 2.2µF, I_{LDO9} = 300mA		40	100	µs
Start-up transient overshoot (Note1)	C_{LDO9} = 2.2µF, I_{LDO9} = 300mA		3	50	mV

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Reject $\Delta LDO9/\Delta V_{IN6}$	f=10Hz-10kHz, C_{LDO9} = 2.2µF, I_{LDO9}=30mA		60		dB
Output Noise Volt. (RMS)	100Hz-100kHz, C_{LDO9}= 2.2µF, I_{LDO9}=30mA		80		μV_{RMS}
Shutdown Output Resistance	I2C programmable. See the Register LDO9_ADISCHG= "1"		1000		Ω

Note1. Design guidance only, not tested during final test.

Backup Battery Charger Electrical Characteristics – VCC_COIN

Operating conditions (unless otherwise specified) V_{IN1} to V_{IN6}= +3.7V, $C_{BATT+\Sigma IN\_}$=20µF, C_{REFBP} = 100nF, T_A =-40°C to +85°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Default output voltage VCC_COIN	Iload=1µA	-3%	3.2	+3%	V
Programmable output voltage range	Iload=1µA	-3%	2.9 3.0 3.1 3.2 3.3	+3%	
Constant Current Limit	V_{COIN} short to GND		200		uA
Internal Series Resistor			1		kΩ
Reverse Leakage current from Output	V_{IN5}=0V,V_{COIN}=3.2V			10	µA
Regulator ground current	Iload=1µA (note1)		5		µA

Note 1: Design guidance only, not tested during final test.

Pin Description

PIN	NAME	FUNCTION
A1	LDO3	LDO3 output. 1kΩ in off condition when ADISCHG_bit is 1.
A2	IN4	Connect to Battery positive terminal. Input for LDO2/3/4/5.
A3	LDO4	LDO4 output. 1kΩ in off condition when ADISCHG_bit is 1.
A4	LDO5	LDO5 output. 1kΩ in off condition when ADISCHG_bit is 1.
A5	REFBP	The output of internal reference voltage. A ceramic capacitor is connected to this. Do not load. Hi-Z in off condition.
A6	LDO6	LDO6 output. 1kΩ in off condition when ADISCHG_bit is 1.
B1	LDO2	LDO2 output. 1kΩ in off condition when ADISCHG_bit is 1 .
B2	JIGON	Input signal from JIG switch. This pin has an internal 800kΩ pull-down resistor to GND.
B3	SRAD	Three state input to determine MAX8698C's I2C address. High-Z in off condition.
B4	PWREN	Input signal from SS AP. Power enable signal. Buck1 and Buck2 are enabled/disabled by this pin. High-Z in off condition
B5	MR\	Manual reset input for hardware reset. This pin has an internal 800kΩ pull-up resistor to IN5.
B6	LDO7	LDO7 output. 1kΩ in off condition when ADISCHG_bit is 1.
C1	IN5	Connect to Battery positive terminal. Input for LDO1, backup charger and logic supply.
C2	SDA	Data high-Z input for I^2C serial interface.
C3	SCL	Clock high-Z input for I2C serial interface.
C4	LBO\	Battery Monitor output, Open drain output. When Battery Monitor is disabled (ELBCNFG=0), LBO\= High.
C5	ONO\	PWRON signal indicator. Active low. Open drain output. High-Z in off condition.
C6	IN6	Connect to Battery positive terminal. Input for LDO6/7/8/9
D1	PGND1	Power ground for buck1 converter. AGND and PGND are externally connected at a single point.
D2	SET3	Input signal from SS AP. It selects the Buck2 output voltage. High-Z in off condition.
D3	SET2	Input signal from SS AP. Two bits of Set1 and Set2 select the output voltage of Buck1. High-Z in off condition.
D4	SET1	Input signal from SS AP. Two bits of Set1 and Set2 select the output voltage of Buck1. High-Z in off condition.
D5	AGND1	Analog Ground,
D6	LDO8	LDO8 output. 1kΩ in off condition when ADISCHG_bit is 1.
E1	LX1	Buck1 switching node. It connects to an external inductor. 1kΩ in off condition when ADISCHG_bit is 0.
E2	BUCK1	Buck1 output feedback voltage.
E3	PWRON	Input signal from an external Power on switch. It connects a manual power on switch. Active high. This pin has an internal 800kΩ pull-down resistor to GND.
E4	RSO\	Reset output signal for SS AP. Active low. Typical 60ms.Open drain output. Lower than 0.4V at 1mA sink currents in off condition.
E5	AGND2	Analog Ground, AGND2 is assigned for sensing terminal.
E6	LDO9	LDO9 output. 1kΩ in off condition when ADISCHG_bit is 1.
F1	IN1	Connect to Battery positive terminal. Input for Buck1
F2	BUCK2	Buck2 output feedback voltage.
F3	PWRHOLD	Power hold input signal. It comes from SS AP. High-Z in off condition.
F4	BUCK3	Buck3 output feedback voltage.
F5	VCC_COIN	Backup Battery charger output. Coin battery connects to this. Always on. It is the input of LDO1.
F6	LDO1	LDO1 output. High-Z in off condition.

PIN	NAME	FUNCTION
G1	IN2	Connect to Battery positive terminal. Input for Buck2.
G2	LX2	Buck2 switching node. It connects to an external inductor. 1kΩ in off condition when ADISCHG_bit is 0.
G3	PGND2	Power ground for buck2 converter. AGND and PGND are externally connected at a single point.
G4	PGND3	Power ground for buck3 converter. AGND and PGND are externally connected at a single point.
G5	LX3	Buck3 switching node. It connects to an external inductor. 1kΩ in off condition when ADISCHG_bit is 0.
G6	IN3	Connect to Battery positive terminal. Input for Buck3.

Functional Block Diagram

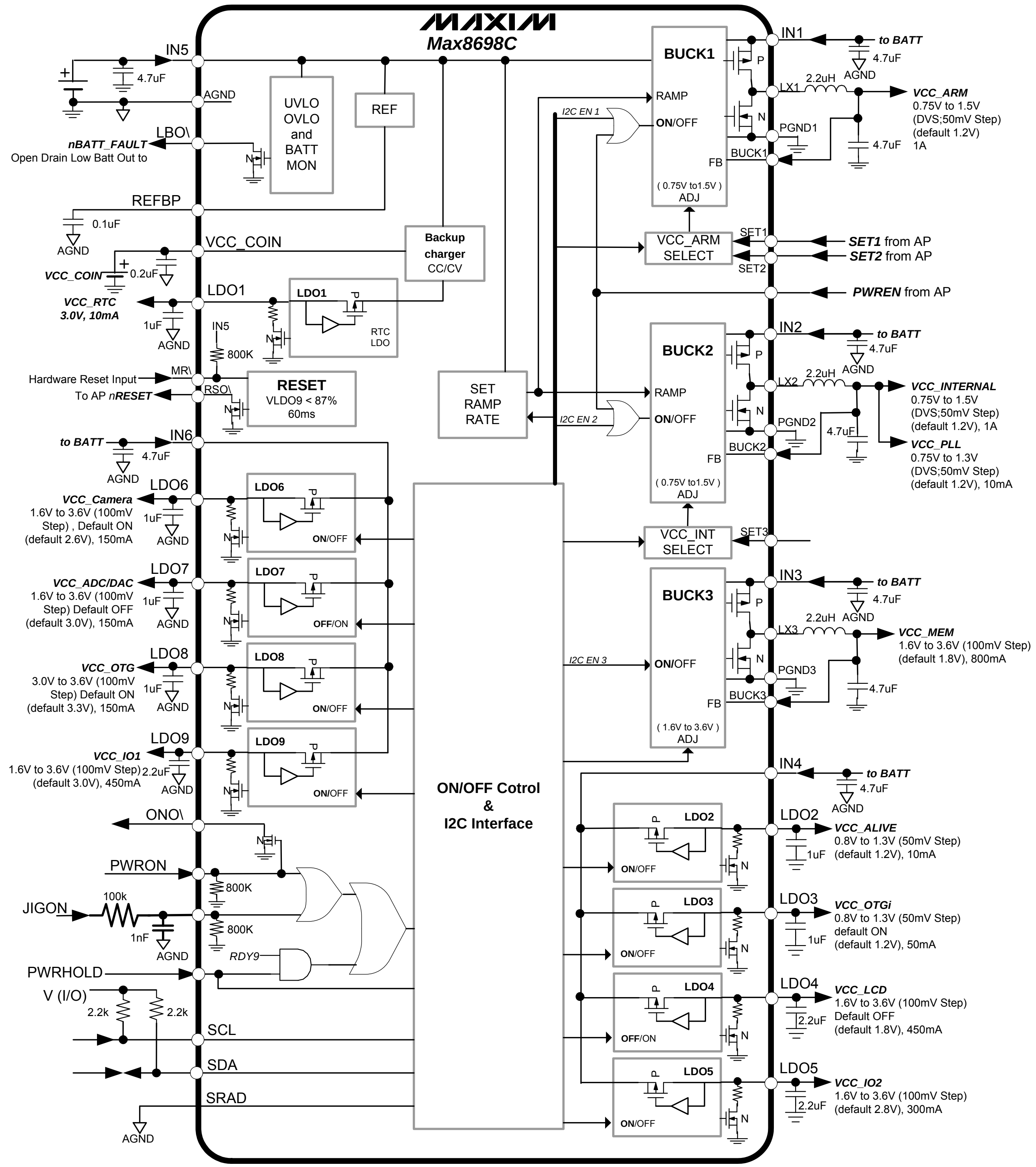


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Figure 1. Functional Block Diagram

Technical Description

Step-Down DC-DC Converters (BUCK1, BUCK2, and BUCK3)

BUCK1 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I^2C adjustable output voltage from 0.75V to 1.50V in 50mV increments with Dynamic Voltage Scaling. BUCK1 has an I^2C enable bit and a shared hardware enable pin (PWREN). See the *Buck1 and Buck2 Enable* section for more information. BUCK1 enable is logically ORed by PWREN and I2C. Drive PWREN high to enable BUCK1/BUCK2 or drive PWREN low to disable BUCK1/BUCK2. The output voltage selection is made by 2 bits of GPIO (SET1 and SET2). See the Dynamic Voltage Scaling (DVS) session. In systems based on Samsung S5PC100 processors, PWREN and SET1 and SET2 are typically connected to S5PC100 GPIO pins.

BUCK2 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I^2C adjustable output voltage from 0.75V to 1.50V in 50mV increments with Dynamic Voltage Scaling. BUCK2 has an I^2C enable bit and a shared hardware enable pin (PWREN). See the *Buck1 and Buck2 Enable* section for more information. BUCK2 enable is ORed by PWREN and I2C. Drive PWREN high to enable BUCK1/BUCK2 or drive PWREN low to disable BUCK1/BUCK2. The output voltage selection is made by 1 bit of GPIO (SET3). See the Dynamic Voltage Scaling (DVS) session. In systems based on Samsung S5PC100 processors, PWREN and SET3 are typically connected to S5PC100 GPIO pins.

BUCK3 is a high efficiency 4MHz hysteretic PWM DC-DC converter that has an I^2C adjustable output voltage from 1.6V to 3.6V in 100mV increments . The default output voltage is 1.8V. See the I2C in *MAX8698C Address* section for details on how to adjust the output voltage.

Linear Regulators (LDO1 – LDO9);

LDO1 Always-On Regulator
The output of LDO1 is always active when the input voltage (V_{IN}) is above the under-voltage lockout threshold. The linear regulator is supplied from VCC_COIN or backup battery charger and its output regulates to 3.0V and supplies up to10mA.

LDO2 is a linear regulator with an I^2 adjustable output voltage from 0.8V to 1.3V in 50mV increments. The default LDO2 voltage is 1.2V. The power up default is ON. LDO2 delivers up to 10mA. See register section for details on how to adjust the output voltage. The power input for the LDO2 linear regulator is IN4.

LDO3 is a linear regulator with an I^2 adjustable output voltage from 0.8V to 1.3V in 50mV increments. The default LDO3 voltage is 1.2V. The power up default is ON. LDO3 delivers up to 50mA. See the register section for details on how to adjust the output voltage. The power input for the LDO3 linear regulator is IN4.

LDO4 is a linear regulator with an I^2 adjustable output voltage from 1.6V to 3.6V in 100mV increments. The default LDO4 voltage is 1.8V. The power up default is OFF. LDO4 delivers up to 450mA. See the register section for details on how to adjust the output voltage. The power input for the LDO4 linear regulator is IN4.

LDO5 is a linear regulator with an I^2 adjustable output voltage from 1.6V to 3.6V in 100mV increments. The default LDO3 voltage is 2.8V. The power up default is ON. LDO5 delivers up to 300mA. See the register section for details on how to adjust the output voltage. The power input for the LDO5 linear regulator is IN4.

LDO6 is a linear regulator with an I^2 adjustable output voltage from 1.6V to 3.6V in 100mV increments. The default LDO6 voltage is 2.6V. The power up default is ON. LDO6 delivers up to 150mA. See the register section for details on how to adjust the output voltage. The power input for the LDO6 linear regulator is IN6.

LDO7 is a linear regulator with an I^2 adjustable output voltage from 1.6V to 3.6V in 100mV increments. The default LDO7 voltage is 3.0V. The power up default is OFF. LDO7 delivers up to 150mA. See the register section for details on how to adjust the output voltage. The power input for the LDO7 linear regulator is IN6.

LDO8 is a linear regulator with an I^2 adjustable output voltage from 3.0V to 3.6V in 100mV increments. The default LDO8 voltage is 3.3V. The power up default is ON. LDO8 delivers up to 150mA. See the register section for details on how to adjust the output voltage. The power input for the LDO8 linear regulator is IN6.

LDO9 is a linear regulator with an IC^2 adjustable output voltage from 1.6V to 3.6V in 100mV increments. The default LDO9 voltage is 3.0V. The power up default is ON. LDO9 delivers up to 450mA. See the register section for details on how to adjust the output voltage. The power input for the LDO9 linear regulator is IN6.

Backup Battery Charger ;Always On

The output of the Backup Charger is always active when the input voltage (V_{IN}) is above the undervoltage lockout threshold of 2.55V (max). The charger is supplied from IN5 . Backup Charger has an I^2C adjustable output voltage from 2.9V to 3.3V in 100mV increments. The default output voltage is 3.2V. The power up default is ON. See the register section for details on how to adjust the output voltage.

Dynamic Voltage Scaling (DVS) Modes

BUCK1 DVS Modes

In normal operation, Buck1 output voltage is dynamically changed by setting SET1 and SET2. As shown in the Figure below, I2C writes output voltages in the 4 registers. Each register can be any output voltage ranging from 0.75V to 1.5V. The Buck1 output voltage is selected by 2 bits of SET1 and SET2. See the Table 1.

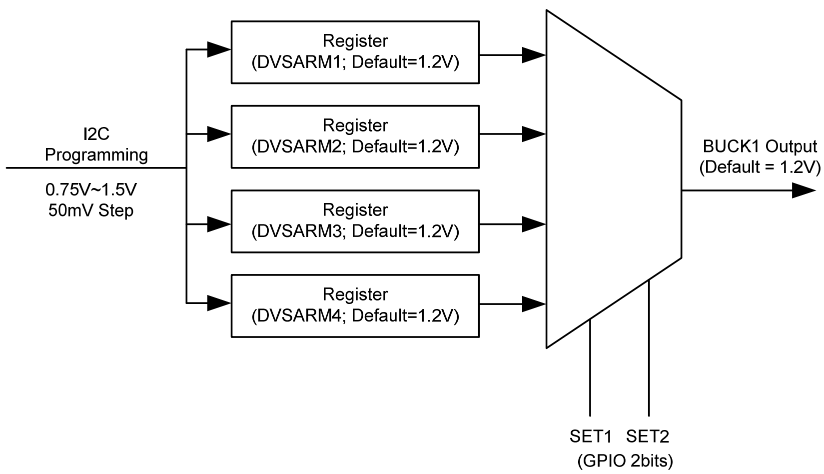


Figure 2. Dynamic Voltage Scaling for Buck1

Table 1. SET1, SET2, and BUCK1 Truth Table

SET2	SET1	BUCK1
0	0	DVSARM1
0	1	DVSARM2
1	0	DVSARM3
1	1	DVSARM4

BUCK2 DVS Modes

In normal operation, Buck2 output voltage is dynamically changed by setting 1 GPIO bit (SET3). As shown in the Figure below, I2C writes output voltages in the 2 registers. Each register can be any output voltage ranging from 0.75V to 1.5V with 100mV step. The Buck2 output voltage is selected by 1 bit of SET3. See the Table 2.

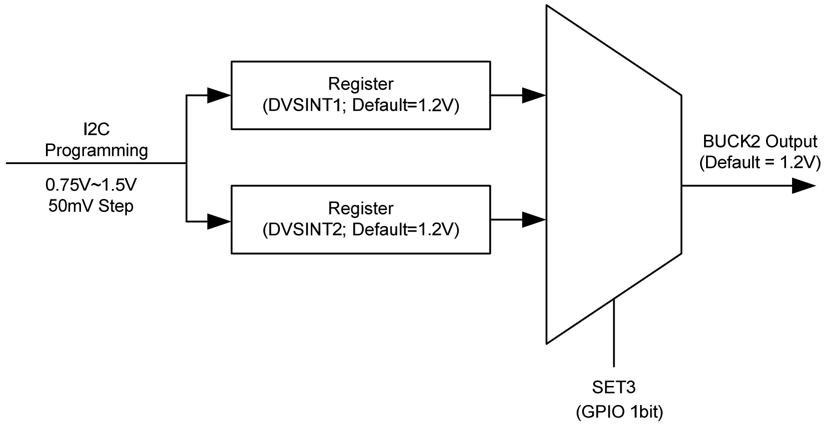


Figure 3. Dynamic Voltage Scaling for Buck2

Table 2. SET3 and BUCK2 Truth Table

SET3	BUCK2
0	DVSINT1
1	DVSINT2

Buck1 and Buck2 DVS Control with Ramp Rate (RAMP)
The output voltages of Buck1 and Buck2 have a variable ramp rate that is set by a register (RAMP). This register controls the output voltage ramp rate during a positive voltage-change (i.e. 1.0V to 1.1V), and a negative voltage-change (i.e. 1.1V to 1.0V). When Buck1 and Buck2 are disabled, the output voltage decays at a rate determined by the output capacitance, internal discharge resistance, and the external load.

In normal mode operation, the regulator output voltage ramps up/down at the rate set by RAMP. With small loads the regulator must sink current from the output capacitor to actively ramp down the output voltage. . the regulator output voltage ramps down at the rate determined by the output capacitance and the external load; small loads result in an output voltage decay that is slower than that specified by RAMP, large loads (> C_{OUT}*RAMPRATE) result in an output voltage decay that is no faster than that specified by RAMP.

BUCK1~BUCK3 and LDO1 ~ LDO9 have a fixed soft-start ramp that eliminates input current spikes when they are enabled.

Ramp Rate adjustment range is 1mV/us to 12mV/us. The RAMP step is 25mV.

Power Sequencing

Power On/OFF
The power management circuit must be able to handle all issues regarding power on/off the handset. The following pins and battery voltage determines the power on/off status of the handset.

PWRON
JIG_ON
PWRHOLD
PWREN

Logic high on PWRON pin is the normal way of powering up a handset. The PWRON signal is held high; default power supplies are turned on. When LDO9 reaches 87% of its final value, a 60 ms reset timer is started. The 60ms reset timer allows the AP chipset to fully reset. At the completion of the 60ms reset timer, RESET\ is allowed to rise (provided no other circuit pulls low on this WIRED-OR output). After RESET\ is asserted high; now the AP processor is initialized and will asserts PWRHOLD high. PWRHOLD maintains the power on. This allows the PWRON key to be released (return to low state) and the power remains on. If, however, PWRON is released before the PWRHOLD signal is asserted then the default power supplies are turned off. The default power supplies can be turned off by the AP processor asserting PWRHOLD low.

Enable Signals (*PWREN,* I^2C)

As shown in Table3, the MAX8698C feature numerous enable signals for flexibility in many applications. PWREN typically connects to S5PC100 GPIO. Alternatively, Buck1 and Buck2 may be activated via the I^2C interface (see the Figure 4). LDO1 and Backup Charger have no enable input and always remains on as long the MAX8698C is powered above UVLO. All regulators are forced off during UVLO. See the Under-voltage Lockout section for more information.

Table 3. Enable Signals

Power Domain	Maxim Enable Signal		ENABLE PIN from SAMSUNG AP
	Hardware	**Software**	
BUCK1 (VCC_ARM)	PWREN	EN1	*GPIOs & I^2C*
BUCK2 (*VCC_INTERNAL*)	PWREN	EN2	
BUCK3(VCC_MEM)	N/A	EN3	*I^2C*
LDO1 (VCC_RTC)	Always-On		*N/A*
LDO2 (*VCC_ALIVE*)	N/A	ELDO2	*I^2C*
LDO3		ELDO3	
LDO4		ELDO4	
LDO5		ELDO5	
LDO6		ELDO6	
LDO7		ELDO7	
LDO8		ELDO8	
LDO9		ELDO9	
Battery Monitor	N/A	ELBCNFG	
Backup Battery Charger (VCC_COIN)	Always-On ($V_{IN5} > V_{UVLO}$ and $V_{IN5} > V_{RTC}$)		N/A

Buck1 and Buck2 Enable (PWREN and I2C)

Buck1 and Buck2 have independent I^2C enable bits (EN1, EN2) and a shared hardware enable input (PWREN). As shown in Figure 4, the PWREN hardware enable input is logically ORed with the I^2C enable bits. Table 4 is the truth table for the Buck1and Buck2 enable logic. Note that to achieve a pure I^2C enable/disable, connect PWREN to ground. Similarly, to achieve a pure hardware enable/disable, leave the I^2C enable bits at their default value (EN1 = EN2 = 0 = off); Buck1 and Buck2 cannot be independently enabled/disabled using only hardware. Buck1 and Buck2 are default ON. In order to control Buck1 and Buck2 by PWREN hardware pin, the I2C control registers of Buck1 and Buck2 must be set to 0 after power up.

Note: a low /MR\ returns the I^2C registers to their default values: EN1 = 0 and EN2 = 0.

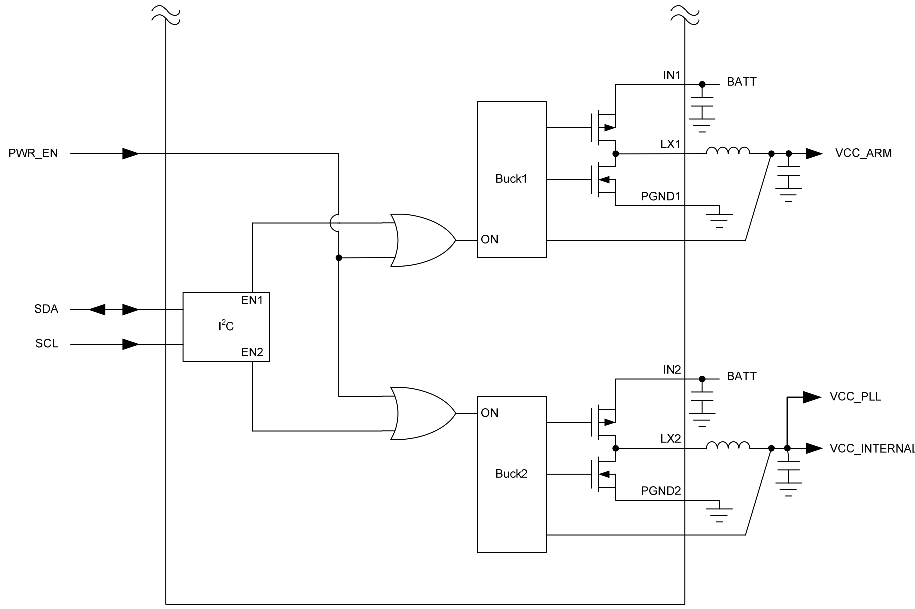


Figure 4. Buck1 and Buck2 Enable

Table 4. Truth Table for BUCK1 and BUCK2 Enable Logic

HARDWARE INPUT	I²C BITS		BUCK1	BUCK2
PWREN	EN1	EN2		
0	0 (default)	0 (default)	OFF	OFF
0	0	1	OFF	ON
0	1	0	ON	OFF
0	1	1	ON	ON
1	X	X	ON	ON

X=don't care

Power-Up and Power-Down Timing

The power management circuit must be able to handle all issues regarding powering the handset on and off. There are several events that can cause the PMIC to power on and off:

PWRON (or JIGON) key triggering power on sequence

High level on the PWRON (or JIGON) input is the normal way of powering up a handset. This corresponds to the user pressing the power on key. When the power on key is pressed the PMIC will first look at the battery voltage, if the battery voltage is below the under voltage lockout point, the PMIC will ignore the key press since there isn't sufficient power to bring up the phone.

MAX8698C powers up in the following order;
LDO2(VCC_ALIVE) ➔ BUCK1 ➔ BUCK2 ➔ LDO3-> BUCK3 ➔ LDO9➔ LDO5 -> LDO6 -> LDO8 -> ➔ I2C Enabled➔LDO4/7

Note that the Samsung S5PC100 processor controls PWREN/SET1/SET2/SET3/PWRHOLD. Buck1/2 and LDO2 are logically connected to ensure Buck1/2 are powered up after LDO2. LDO2 can be enabled /disabled by only I2C during normal operation. See Figure 5 and Figure 6.

After I2C is enabled, all regulators can be enabled or disabled via I2C. In the figure6, LDO4/7 are turned on by I2C and can be turned off individually.

Note that OTGi (LDO3) is recommended to turn on before OTG(LDO8) according to Samsung S5PC100 power requirements. It is not recommended turning on both OTGi and OTG at same time.

PWRHOLD triggering power down sequence

The normal way of powering off MAX8698C is by PWRHOLD going low.
If PWRHOLD = logic low, the nRESET is pulled low and the power–down sequence is initiated.

The following will trigger the PMIC to transition from active condition to off condition

- Falling threshold level on PWRHOLD & Low level of PWRON switch (See Figure 5)
- Falling threshold level on PWRON & Low level of PWRHOLD (See Figure 6)
- Internal temperature exceeding thermal limit
- LDO9 going out of regulation
- UVLO

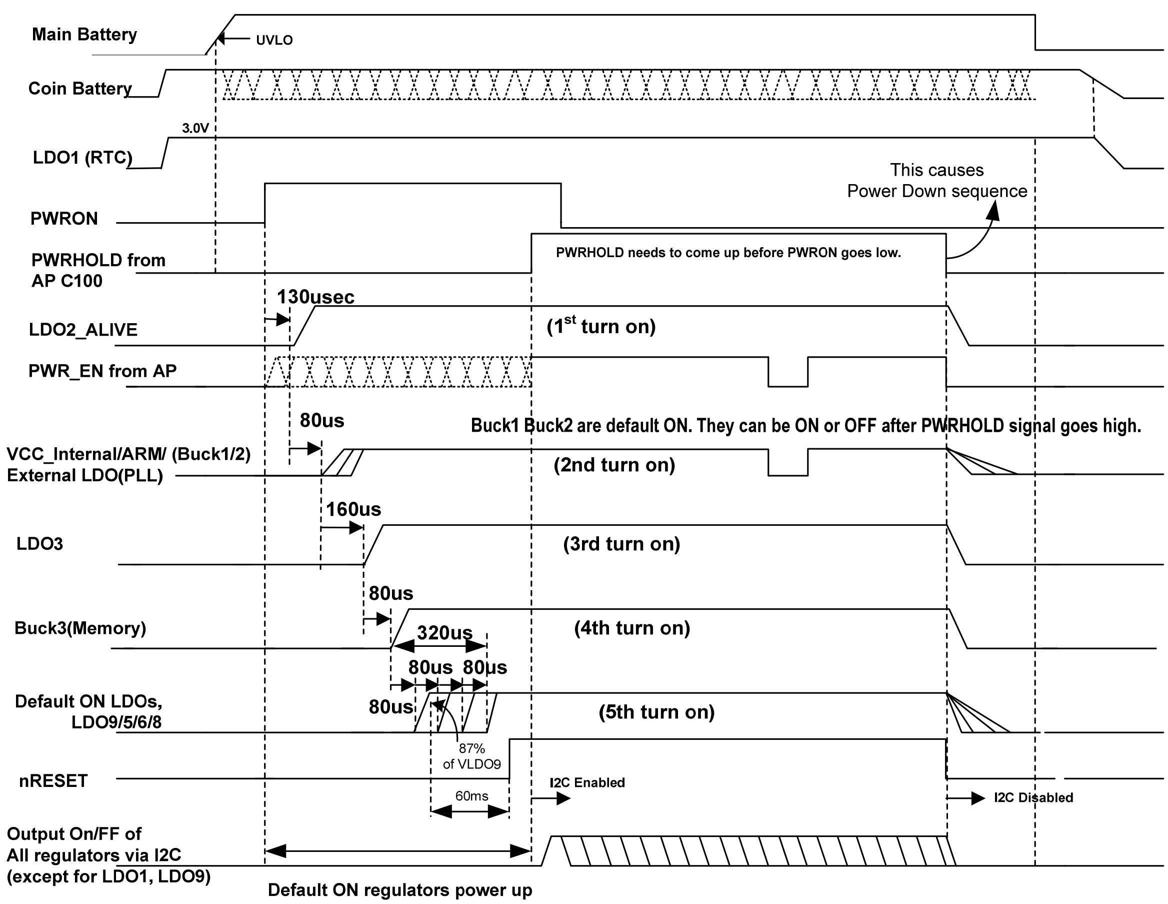


Figure 5. Power up/down sequence

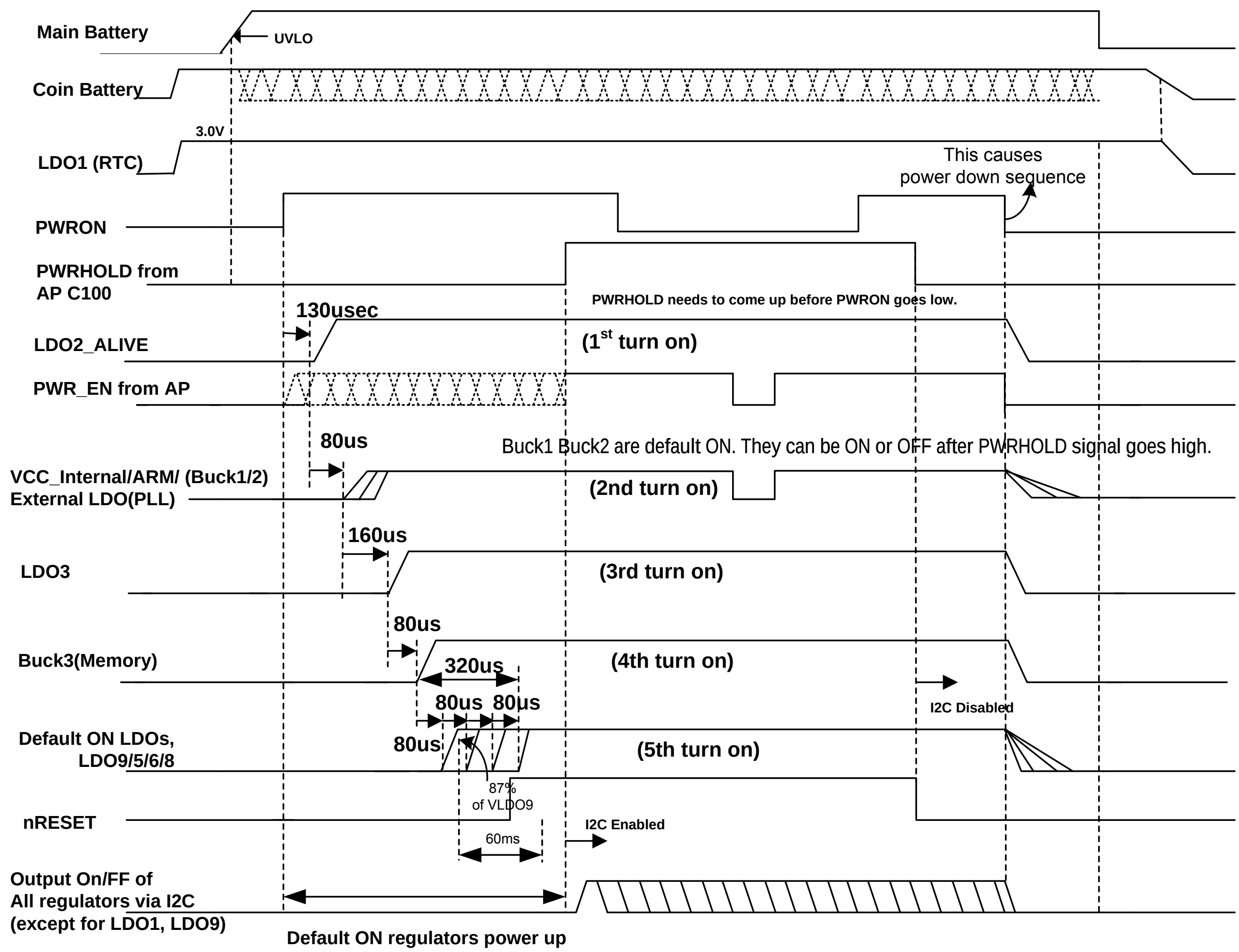


Figure 6. Power up/down sequence

If the die temperature goes above the maximum allowed threshold, the PMIC will enter thermal protection condition to reduce the risk of damaging the PMIC. This condition is a result of operating the PMIC at too high a load, too high a temperature or a fault condition.

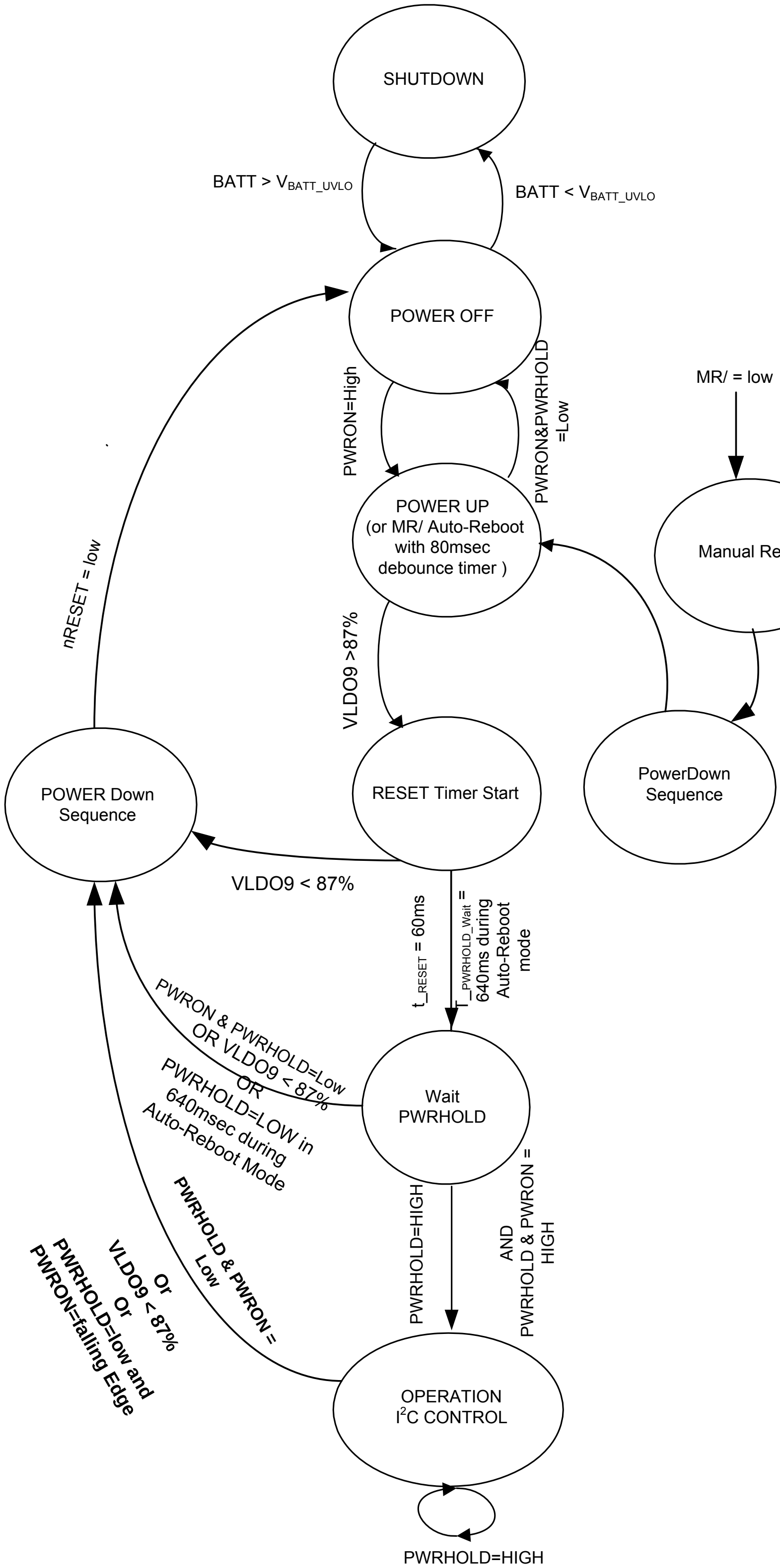


Figure 7. State Diagram

SHUTDOWN:
nRESET=low
nBATT_FAULT=low
All Supplies are powered OFF
LDO1 can be enabled by Backup battery

POWER OFF:
nRESET=low
nBATT_FAULT=high
VCC_COIN & VLDO1 are enabled
All other supplies are powered OFF

POWER UP:
nRESET=low
Buck1/2/3,LDO2/3/5/6/8/9 are enabled
All other power supplies are powered OFF

Auto-Reboot:
MAX8698 is automatically rebooted with 320ms delay when MR/ = low
.

Reset Timer Start:
nRESET=low
Reset timer starts (60msec)
PWRHOLD wait timer starts (640msec) during Auto-Reboot mode
Buck1/2/3,LDO2/3/5/6/8/9 are powered ON.
All other power supplies are powered OFF.

WaitPWRHOLD:
nRESET=high

OPERATION I^2C CONTROL:
nRESET=high
Buck1&2 are controlled by SET1,SET2,SET3, PWR_EN, and I^2C.
All other power supplies are controlled by EN logic signals or I^2C.

PowerDown Sequence:
See Figure 5 and 6

Voltage Monitors, Reset, and Under-voltage Lockout Functions

Under-voltage Lockout (UVLO)
When the IN input voltage is below V_{UVLO}, the MAX8698C enter its under-voltage lockout mode (UVLO). UVLO forces the device to a dormant state until the input voltage is high enough to allow the device to function reliably. In UVLO the input current is very low and all regulators are off. /RSO\ is forced low when the input voltage is between 1V (typ) and V_{UVLO}. The I^2C does not function in UVLO and the I^2C register contents are reset in UVLO.

Low-Battery Detector, (/LBO\ )
/LBO\ is an open drain output that typically connects to the *nBATT_FAULT* input of the Samsung S5PC100 processor to indicate that the battery has been removed or discharged. /LBO\ is typically pulled up to IN5 (*VCC_BATT*). When the main battery voltage falls below its low-battery threshold, /LBO\ is driven low. The low-battery detector is enabled by default. The Low Battery Detector can be disabled by Enable Low Battery Configuration register (ELBCNFG). When ELBCNFG=0, the Low Battery Detector is disabled and LBO/ stays High. When ELBCNFG=1, it is enabled.

The low battery threshold is configurable using LBTH (See LBCNFG register session).
The hysteresis is configurable using LBHYST in LBCNFG register session.

/LBO\ is a main battery monitor output signal. /LBO\ does not force MAX8698C to be turn off.

Reset Output (/RSO\) and /MR\ Input
/RSO\ is an open drain reset output. A low on *nRESET* causes the S5PC100 processor to enter its reset state.

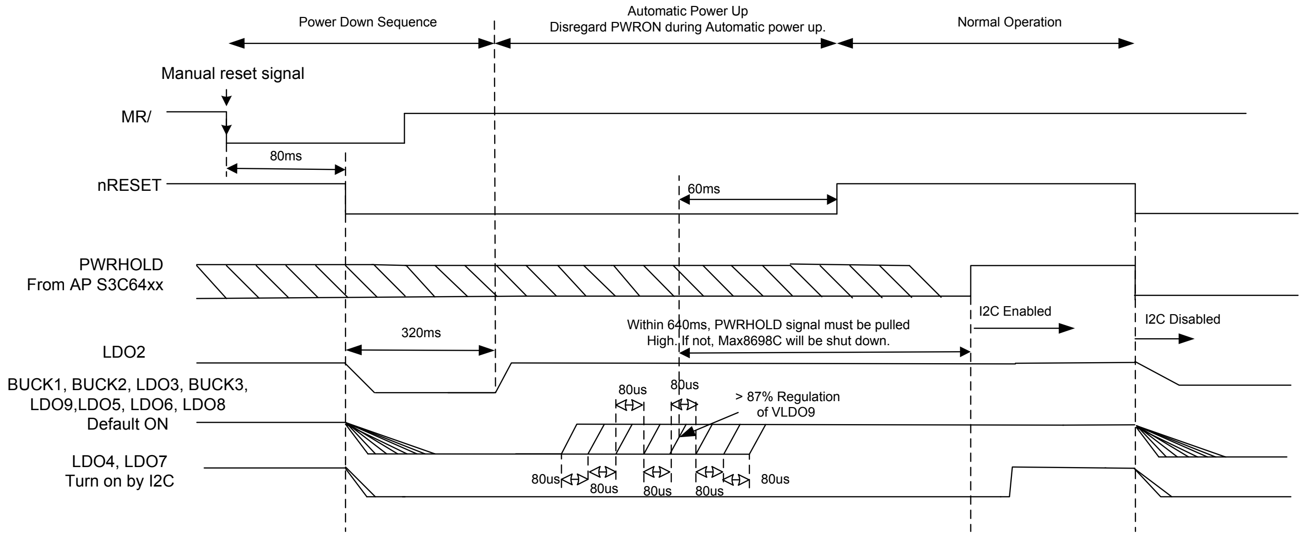
/RSO\ is forced low when one or more of the following conditions occur:
/MR\ is low
PWRHOLD goes to low.
LDO9 is below 87% of regulation
V_{IN} is below V_{UVLO} (2.35V typ)
When MAX8698C goes into power down sequence.

/RSO\ is high-impedance when all of the following conditions are satisfied:
/MR\ is high
LDO9 is above 87% of regulation
$V_{UVLO} < V_{IN}$
The reset delay 60ms has expired.
PWRHOLD is high

When RSO\ is low, all PMIC registers and serially set voltage settings return to their default values.

/MR\ is a manual reset input for hardware reset. Falling edge of MR/ and minimum 80msec low initiate the automatic power up. After the 80msec is expired, RSO\ asserts and all PMIC registers and serially-set voltage settings return to their default values. A low on /MR\ resets the MAX8698C I^2C registers to their default values. Once it enters the automatic power up sequence, MAX8698C disregard anther MR/ signals and completes the cycle of power up sequence. Refer to the timing diagram below for the automatic power up initiated by MR/.

If the /MR\ feature is not required, leave it open. If the /RSO\ feature is not required, connect /RSO\ low.



<Figure 8>; timing diagram of automatic power up caused by MR/>

Internal Off-Discharge Resistors

Each regulator on the MAX8698C has an internal resistor that discharges the output capacitor when the regulator is off (Table 5). The internal discharge resistors pull their respective output to ground when the regulator is off, ensuring that load circuitry always powers down completely. The internal off-discharge resistors are active when a regulator is disabled, and when the device is in UVLO with V_{IN} greater than 1.0V. With V_{IN} less than 1.0V the internal off-discharge resistors may not activate.

Table 5. Internal Off-Discharge Resistor Values

Regulator	Internal Off-Discharge Resistor Value
BUCK1	1k Ω ±30%
BUCK2	1k Ω ±30%
BUCK3	1k Ω ±30%
LDO2/3/4/5/6/7/8/9	1k Ω ±30%

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX8698C. When internal thermal sensors detect a die temperature in excess of +160°C, the corresponding regulator(s) are shut down, allowing the IC to cool. The regulators turn on again after the junction cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

A thermal overload on any of BUCK1 through BUCK2 only shuts down the overloaded regulator. During thermal overload, Backup Charger and LDO1 are not turned off, and the I^2C interface and voltage monitors remain active.

External Components

Suggested Inductors

Manufacturer	Series	Inductance (uH)	ESR (ohms)	Current Rating (mA)	Dimensions
FDK	MIPF	1.5 2.2 3.3	0.07 0.08 0.1	1.5 1.3 1.2	2.5x2.0x1.0
Murata	LQH32C_53	1.0 2.2	0.06 0.10	1000 790	3.2x2.5x2.0
TOKO	D312C	1.5 2.2 2.7 3.3	0.10 0.12 0.15 0.17	1290 1140 980 900	3.6x3.6x1.2
Hitachi Metals	KSLI-252012AG	1.0 2.2 3.3	0.08 0.10 0.11	2000 1500 600	2.5x2.0x1.2
Sumida	CDRH2D11	1.5 2.2 3.3	0.05 0.08 0.10	900 780 600	3.2x3.2x1.2

Table 4 Inductor selection guide

Output Capacitor Selection

The output capacitor, C_{BUCK}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{BUCK} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. For most applications a 4.7μF capacitor is sufficient. For optimum load-transient performance and very low output ripple, the output capacitor value in μF's should be equal or larger than the inductor value in μH's.

Input Capacitor Selection

The input capacitor, C_{IN3}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the MAX8698C step-down converter's fast soft-start, the input capacitance can be very low. For most applications a 4.7μF capacitor is sufficient.

PCB Layout Guide for the Buck Converters

For main current path from the input capacitor, LX_ pin, up to GND, use shorter and thicker trace. To minimize EMI, make C_{IN} - LX- PGND area shortest possible. The FB node is noise sensitive. Please make the trace of the FB_ as close and short as possible to the IC.

I2C

I^2C BIT TRANSFER

One data bit is transferred for each clock pulse. The data on DATA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

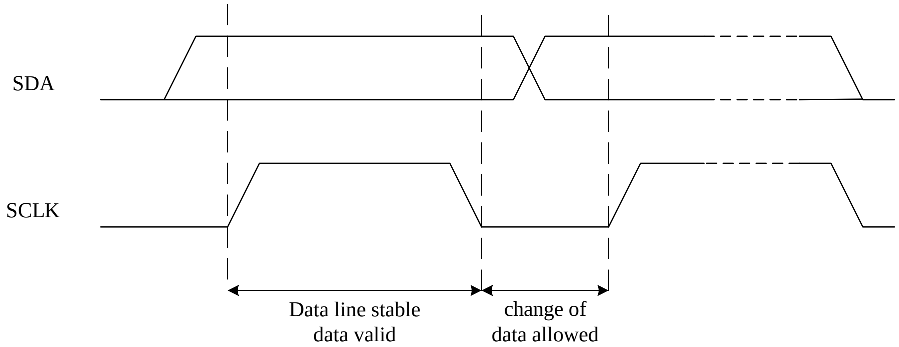


Figure 9 I²C bit transfer

I²C START AND STOP CONDITIONS

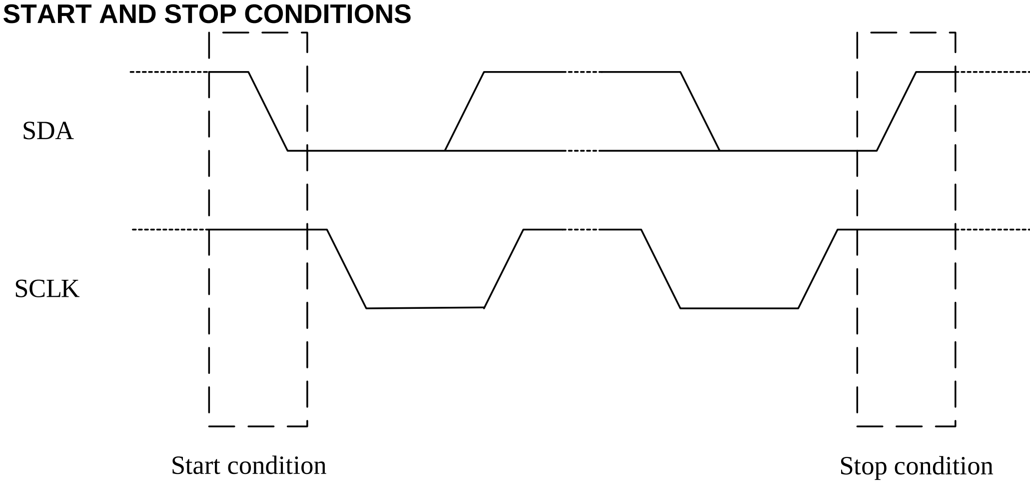


Figure 10 I²Cstart and stop conditions

Both DATA and CLK remain High when the bus is not busy. A high-to-low transition of DATA, while CLK is high is defined as the Start condition. A low-to-high transition of the data line while CLK is high is defined as the Stop condition.

I²C SYSTEM CONFIGURATION

A device on the I²C Bus who generates a "message" is called a "Transmitter" and a device that receives the message is a "Receiver". The device that controls the message is the "Master" and the devices that are controlled by the "Master" are called "Slaves"

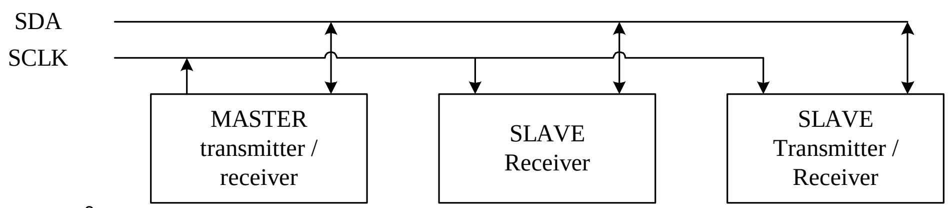


Figure 11 I²CMaster / Slave configuration

I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver are unlimited. Each 8-bit byte is followed by an Acknowledge bit. The Acknowledge Bit is a high level signal put on DATA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after each byte it receives. Also a master receiver must generate an Acknowledge after each byte it receives that has been clocked out of the slave transmitter.

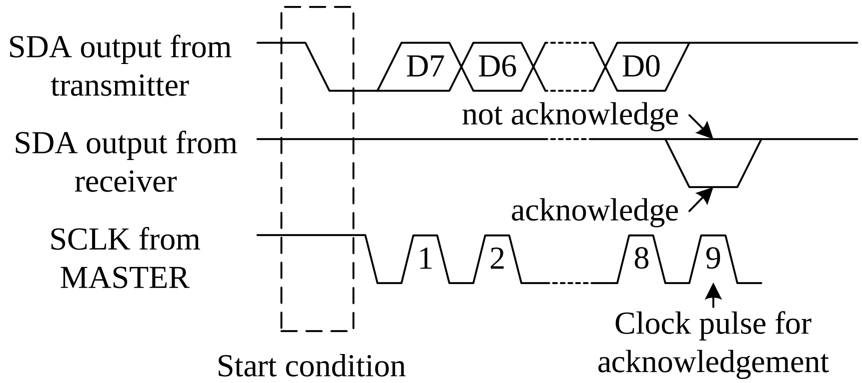


Figure 12 I^2C Acknowledge

The device that Acknowledges must pull down the DATA line during the acknowledge clock pulse, so that the DATA line is stable low during the high period of the Acknowledge clock pulse (set-up and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave DATA high to enable the master to generate a stop condition.

MAX8698C I^2C Address

The MAX8698C acts as a Slave Transmitter/Receiver. The slave address of the MAX8698C Power Management Section is
AC/ADh, BC/BDh, or CC/CDh selected by SRAD pin.

SRAD=1; AC/ADh is selected.
SRAD=floating; BC/BDh is selected.
SRAD=0; CC/CDh is selected.

ONOFF1 Register

ONOFF1 control register for Buck1, Buck2, Buck3, LDO2-LDO5.

Address (hex)	Default (hex)		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	FA		EN1	EN2	EN3	ELDO2	ELDO3	ELDO4	ELDO5	x
Name	Default		Description							
EN1	1	R/W	1: Turn Buck1 on (when PWREN=1 or EN1=1, Buck1 regulator is on). 0: Turn Buck1 off (When PWREN=0 and EN1=0, Buck1 regulator is off).							
EN2	1	R/W	1: Turn BUCK2 on (when PWREN=1 or EN2=1, Buck2 regulator is on). 0: Turn BUCK2 off (When PWREN=0 and EN2=0, Buck2 regulator is off).							
EN3	1	R/W	1: Turn BUCK3 on. 0: Turn BUCK3 off.							
ELDO2	1	R/W	1: Turn LDO2 on. 0: Turn LDO2 off.							
ELDO3	1	R/W	1: Turn LDO3 on. 0: Turn LDO3 off.							
ELDO4	0	R/W	1: Turn LDO4 on. 0: Turn LDO4 off.							
ELDO5	1	R/W	1: Turn LDO5 on. 0: Turn LDO5 off.							
x	x	x	x							

ONOFF2 Register

ON/OFF control register for LDO6-LDO9 and Low Battery Configuration (BLCNFG) of Battery Monitor.

Address (hex)	Default (hex)		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01	B1		ELDO6	ELDO7	ELDO8	ELDO9	x	x	x	x ELBCNFG
Name	Defa ult		Description							
ELDO6	1	R/W	1: Turn LDO6 on. 0: Turn LDO6 off.							
ELDO7	0	R/W	1: Turn LDO7 on. 0: Turn LDO7 off.							
ELDO8	1	R/W	1: Turn LDO8 on. 0: Turn LDO8 off.							
ELDO9	1	R/W	0: Turn LDO9 off. We can turn off only. Turning off LDO9 causes PMIC to shut down.							
X	x	x	x							
x	x	x	x							
X	x	x	X							
ELBCNFG	1	R/W	1: Turn Battery Monitor on, 0:Turn Battery Monitor off.							

ADISCHG_EN1
This register contains the active discharge enable for the BUCK's and LDO's

Address (hex)	Default (hex)		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02	FF		BUCK1 ADEN	BUCK2 ADEN	BUCK3 ADEN	LDO2 ADEN	LDO3 ADEN	LDO4 ADEN	LDO5 ADEN	LDO6 ADEN
Name	Defau lt		Description							
BUCK1 ADEN	1	R/W	0: Active discharge disabled 1: Active discharge enabled							
BUCK2 ADEN	1	R/W								
BUCK2 ADEN	1	R/W								
LDO2 ADEN	1	R/W								
LDO3 ADEN	1	R/W								
LDO4 ADEN	1	R/W								
LDO5 ADEN	1	R/W								
LDO6 ADEN	1	R/W								

ADISCHG_EN2
This register contains the active discharge enable for the LDO's

<table>
<tr><th>Address (hex)</th><th colspan="2">Default (hex)</th><th>Bit7</th><th>Bit6</th><th>Bit5</th><th>Bit4</th><th>Bit3</th><th>Bit2</th><th>Bit1</th><th>Bit0</th></tr>
<tr><td>03</td><td colspan="2">F9</td><td>LDO7 ADEN</td><td>LDO8 ADEN</td><td>x</td><td>x</td><td colspan="4">RAMP</td></tr>
<tr><td>Name</td><td>Default</td><td></td><td colspan="8">Description</td></tr>
<tr><td>LDO7 ADEN</td><td>1</td><td>R/W</td><td colspan="8" rowspan="4">0: Active discharge disabled
1: Active discharge enabled</td></tr>
<tr><td>LDO8 ADEN</td><td>1</td><td>R/W</td></tr>
<tr><td>x</td><td>x</td><td>x</td></tr>
<tr><td>x</td><td>x</td><td>x</td></tr>
<tr><td>RAMP</td><td>9h</td><td>R/W</td><td colspan="8">0h: 1mV/us
1h: 2mV/us
2h: 3mV/us
3h: 4mV/us
4h: 5mV/us
5h: 6mV/us
6h: 7mV/us
7h: 8mV/us
8h: 9mV/us
9h: 10mV/us (Default)
Ah: 11mV/us
Bh: 12mV/us</td></tr>
</table>

Serial Codes for Buck1 (VCC_ARM) output voltages
Output program registers for BUCK1 – DVSARM1 and DVSARM2

		Register Name							
		DVSARM2				DVSARM1			
Address (hex)	**Default (hex)**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
04	99	See below	See below	See below	See below	See below	See below	See below	See below

Output program registers for BUCK1 – DVSARM3 and DVSARM4

		Register Name							
		DVSARM4				DVSARM3			
Address (hex)	**Default (hex)**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
05	99	See below	See below	See below	See below	See below	See below	See below	See below

Data codes for DVSARM1, DVSARM2, DVSARM3, DVSARM

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
04 05	DVSARM1 DVSARM2 DVSARM3 DVSARM4	0	0.75
		1	0.80
		2	0.85
		3	0.90
		4	0.95
		5	1.00
		6	1.05
		7	1.10
		8	1.15
		9	**1.20(Default)**
		A	1.25
		B	1.30
		C	1.35
		D	1.40
		E	1.45
		F	1.50

Serial Codes for Buck2 (VCC_INTERNAL) output voltages
Output program registers for BUCK2 – DVSINT1 and DVSINT2

		Register Name							
		DVSINT2				DVSINT1			
Address (hex)	**Default (hex)**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
06	99	See below	See below	See below	See below	See below	See below	See below	See below

Data codes for DVSINT1, DVSINT2

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
06	DVSINT1 DVSINT2	0	0.75
		1	0.80
		2	0.85
		3	0.90
		4	0.95
		5	1.00
		6	1.05
		7	1.10
		8	1.15
		9	**1.20 (Default)**
		A	1.25
		B	1.30
		C	1.35
		D	1.40
		E	1.45
		F	1.50

Serial Codes for Buck3(VCC_MEM) output voltages (Default Datacode [hex] = 02)

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
07	Buck3	00	1.6
		01	1.7
		02	**1.8 (Default)**
		03	1.9
		04	2.0
		05	2.1
		06	2.2
		07	2.3
		08	2.4
		09	2.5
		0A	2.6
		0B	2.7
		0C	2.8
		0D	2.9
		0E	3.0
		0F	3.1
		10	3.2
		11	3.3
		12	3.4
		13	3.5
		14	3.6

Serial Codes for LDO2(VCC_ALIVE), LDO3output voltages

		Register Name							
		LDO3				LDO2			
Address (hex)	**Default (hex)**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
08	88	See below	See below	See below	See below	See below	See below	See below	See below

Output program registers for LDO2 and LDO3

Data Codes for LDO2, LDO3 output voltages

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
08	LDO2 LDO3	0	0.80
		1	0.85
		2	0.90
		3	0.95
		4	1.00
		5	1.05
		6	1.10
		7	1.15
		8	**1.20(Default for LDO2, LDO3)**
		9	1.25
		A	1.30

Serial Codes for LDO4 output voltages (Default datacode (hex) = 02)

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
09	LDO4	00	1.6
		01	1.7
		02	**1.8 (Default)**
		03	1.9
		04	2.0
		05	2.1
		06	2.2
		07	2.3
		08	2.4
		09	2.5
		0A	2.6
		0B	2.7
		0C	2.8
		0D	2.9
		0E	3.0
		0F	3.1
		10	3.2
		11	3.3
		12	3.4
		13	3.5
		14	3.6

Serial Codes for LDO5 output voltages (Default datacode (hex) = 0C)

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
0A	LDO5	00	1.6
		01	1.7
		02	1.8
		03	1.9
		04	2.0
		05	2.1
		06	2.2
		07	2.3
		08	2.4
		09	2.5
		0A	2.6
		0B	2.7
		0C	**2.8 (Default)**
		0D	2.9
		0E	3.0
		0F	3.1
		10	3.2
		11	3.3
		12	3.4
		13	3.5
		14	3.6

Serial Codes for LDO6 output voltages (Default datacode (hex) = 0A)

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
0B	LDO6	00	1.6
		01	1.7
		02	1.8
		03	1.9
		04	2.0
		05	2.1
		06	2.2
		07	2.3
		08	2.4
		09	2.5
		0A	**2.6 (Default)**
		0B	2.7
		0C	2.8
		0D	2.9
		0E	3.0
		0F	3.1
		10	3.2
		11	3.3
		12	3.4
		13	3.5
		14	3.6

Serial Codes for LDO7 output voltages (Default datacode (hex) = 0E)

Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
0C	LDO7	00	1.6
		01	1.7
		02	1.8
		03	1.9
		04	2.0
		05	2.1
		06	2.2
		07	2.3
		08	2.4
		09	2.5
		0A	2.6
		0B	2.7
		0C	2.8
		0D	2.9
		0E	**3.0 (Default)**
		0F	3.1
		10	3.2
		11	3.3
		12	3.4
		13	3.5
		14	3.6

Serial Codes for LDO8 and Backup Battery Charger (VCC_COIN) output voltages.

		Register Name							
		LDO8				BKCHR			
Address (hex)	**Default (hex)**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0D	33	See below	See below	See below	See below	See below	See below	See below	See below

Output program registers for LDO8 and Backup Charger (VCC_COIN) output voltages.

Data Codes for LDO8 output voltages

Register Address	**Register Name**	**Data Byte (hex)**	**Output Voltage (V)**
0D	LDO8	**0**	3.0
		1	3.1
		2	3.2
		3	**3.3 (Default)**
		4	3.4
		5	3.5
		6	3.6

Data Codes for Backup Battery Charger (VCC_COIN) output voltages

Register Address	**Register Name**	**Data Byte (hex)**	**Output Voltage (V)**
0D	BKCHR	0	2.9
		1	3.0
		2	3.1
		3	**3.2 (Default)**
		4	3.3

Serial Codes for LDO9 output voltages (Default datacode (hex) = 0E)

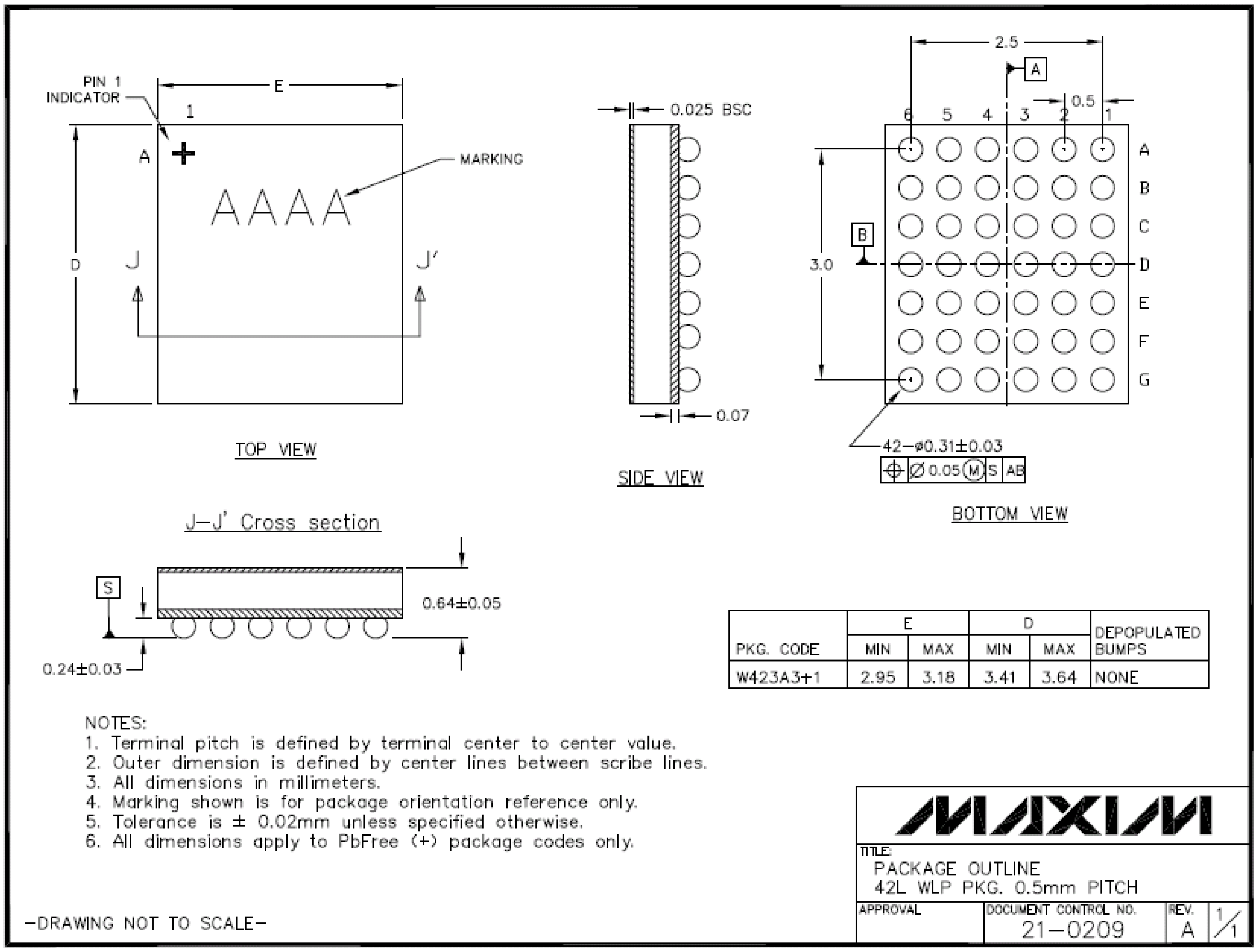
Register Address	Register Name	Data Byte (hex)	Output Voltage (V)
0E	LDO9	00	1.6
		01	1.7
		02	1.8
		03	1.9
		04	2.0
		05	2.1
		06	2.2
		07	2.3
		08	2.4
		09	2.5
		0A	2.6
		0B	2.7
		0C	2.8
		0D	2.9
		0E	**3.0 (Default)**
		0F	3.1
		10	3.2
		11	3.3
		12	3.4
		13	3.5
		14	3.6

Serial Codes for Low Battery Configuration (LBCNFG) (Default datacode (hex) =16)

Address (hex)	Default (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0F	16	x	x	LBHYST		LBTH			x

Name	Default		Description
Bit7	x	R/W	Reserved for future use
Bit6	x	R/W	Reserved for future use
LBHYST	1	R/W	Low Main-Battery Comparator Hysteresis 0b00=100mV **0b01=200mV (Default)** 0b10=300mV 0b11=400mV
LBTH	3	R/W	Low Main-Battery threshold voltage (V_{IN5}_falling) 0b000=2.8V 0b001=2.9V 0b010=3.0V **0b011=3.1V(Default)** 0b100=3.2V 0b101=3.3V 0b110=3.4V 0b111=3.5V
Bit0	x	x	Reserved for future use

Package Drawing



PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W423A3+1	2.95	3.18	3.41	3.64	NONE

Package Bump Drawing