



8-Chan JFET Analog Multiplexers (Overvoltage & Power Supply Loss Protected)

MUX-08

FEATURES

- JFET Switches Rather Than CMOS
- Low "ON" Resistance 220Ω Typ
- Highly Resistant to Static Discharge Damage
- No SCR Latch-Up Problems
- Digital Inputs Compatible With TTL and CMOS
- 125°C Temperature Tested Dice Available
- MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506
- MUX-24 is Obsolete and MUX08BRC/883 is Obsolete

ORDERING INFORMATION

See the updated Ordering Guide section at the end of this data sheet for ordering information.

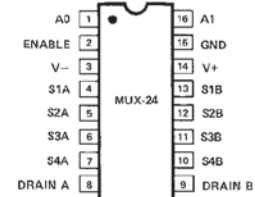
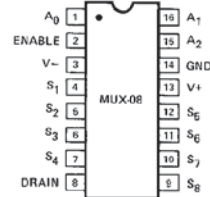
Several products are now obsolete, including the MUX-24 and MUX08BRC/883.

For products that are available as of the current revision of this data sheet, see the updated Outline Dimensions and Ordering Guide sections.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

The MUX-24 and MUX08BRC/883 are no longer available.

PIN CONNECTIONS

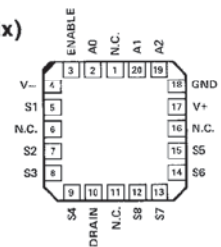


16-PIN CERDIP (Q-Suffix)

16-PIN PLASTIC DIP (P-Suffix)

16-PIN SO (S-Suffix)

20-CONTACT LCC (RC-Suffix)



GENERAL DESCRIPTION

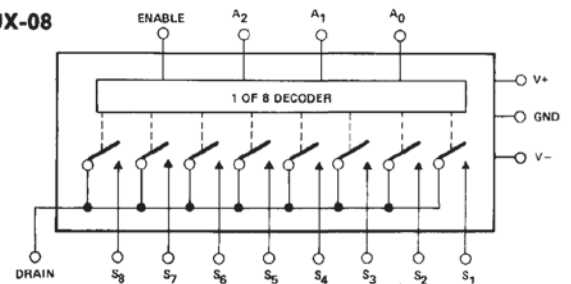
The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

FUNCTIONAL DIAGRAMS

MUX-08



Rev. C

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MUX-08

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range

MUX-08/24-AQ, BQ, BRC	-55°C to +125°C
MUX-02/24-EQ, FQ	-25°C to +85°C
MUX-08/24-EP	0°C to +70°C
MUX-08/24-FP, FS	-40°C to +85°C

Junction Temperature (T_J) -65°C to +150°C

Storage Temperature Range -65°C to +150°C

P-Suffix -65°C to +125°C

Lead Temperature (Soldering, 60 sec) 300°C

Maximum Junction Temperature 150°C

V+ Supply to V- Supply 36V

Logic Input Voltage (-4V or V-) to V+ Supply

Analog Input Voltage V- Supply -20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ _{JA} (Note 2)	Θ _{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V- = -15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/E			MUX-08B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R _{ON}	V _S ≤ 10V, I _S ≤ 200μA	—	220	300	—	300	400	Ω
ΔR _{ON} With Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 200μA	—	1	5	—	3	7	%
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 200μA	—	7	15	—	9	20	%
Analog Voltage Range	V _A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V
Source Current (Switch "OFF")	I _{S(OFF)}	V _S = 10V, V _D = -10V (Note 1)	—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	I _{D(OFF)}	V _S = 10V, V _D = -10V (Note 1)	MUX-08 MUX-24	— 0.05	0.1 1.0	—	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	I _{D(ON)} +I _{S(ON)}	V _D = 10V (Note 1)	MUX-08 MUX-24	— 0.05	0.1 1.0	—	0.1 0.05	2.0 2.0	nA
Digital Input Current	I _{IN}	V _{IN} = 0.4V to 15V	—	1	10	—	1	10	μA
Digital "0" Enable Current	I _{INL(EN)}	V _{EN} = 0.4V	—	4	10	—	4	10	μA
Digital Input Capacitance	C _{DIG}		—	3	—	—	3	—	pF
Switching Time (t _{TRAN})	t _{PHL} t _{PLH}	(Notes 2, 5) Figure 1 (Test Circuit)	—	1.5 1.0	2.1 1.3	—	1.5 1.0	2.1 1.3	μs
Output Settling Time	t _S	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%	—	2.2 2.7 3.4	— — —	—	2.2 2.7 3.4	— — —	μs
Break-Before-Make Delay	t _{OPEN}	Figure 3 (Test Circuit)	—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	t _{ON(EN)}	(Note 5) Figure 2 (Test Circuit)	—	1	2	—	1	2	μs
Enable Delay "OFF"	t _{OFF(EN)}	(Note 5) Figure 2 (Test Circuit)	MUX-08 MUX-24	— 0.2	0.1 0.5	0.4 0.6	— 0.3	0.2 0.6	μs
"OFF" Isolation	ISO _{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— 66	60 —	— —	60 66	— —	dB
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08 MUX-24	— 76	70 —	— —	70 76	— —	dB
Source Capacitance	C _{S(OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-08 MUX-24	— 2	2.5 —	— —	2.5 2	— —	pF
Drain Capacitance	C _{D(OFF)}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-08 MUX-24	— 4	7 —	— —	7 4	— —	pF
Input to Output Capacitance	C _{D(S,OFF)}	(Note 4)	MUX-08 MUX-24	— 0.15	0.3 —	— —	0.3 0.15	— —	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I ₊	V ₊ = 15V V ₊ = 5V	—	10 8	12 —	—	6 5	12 —	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I ₋	V ₊ = -15V V ₊ = -5V	—	3.0 2.5	3.8 —	—	2.0 1.8	3.8 —	mA

ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A			MUX-08B			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	—	425	—	—	500	Ω	
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%	
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V	
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	—	—	25	—	—	50	nA	
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	—	—	100 50	—	—	500 500	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	—	—	100 50	—	—	500 500	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V	
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.7	—	—	0.7	V	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA	
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA	
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA	
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA	

ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $-25^\circ C \leq T_A \leq +85^\circ C$ for MUX-08EQ/FQ and MUX-24EQ/FQ; $0^\circ C \leq T_A \leq +70^\circ C$ for MUX-08EP and MUX-24EP; $-40^\circ C \leq T_A \leq +85^\circ C$ for MUX-08FP/FS and MUX-24FP/FS, unless otherwise noted

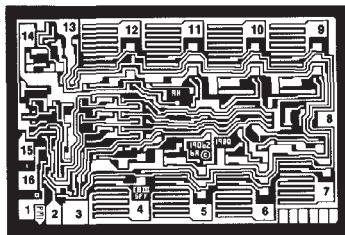
PARAMETER	SYMBOL	CONDITIONS	MUX-08E			MUX-08F			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	—	400	—	—	500	Ω	
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1.5	—	—	4.5	—	%	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	10	—	—	15	—	%	
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V	
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$ (Notes 1, 7)	—	—	10	—	—	10	nA	
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V, V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	—	—	100 50	—	—	100 50	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	—	—	100 50	—	—	100 50	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V	
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	—	—	0.8	V	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA	
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA	
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA	
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA	

NOTES:

- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
- $R_L = 10M\Omega$, $C_L = 10pF$.
- Crosstalk is measured by driving channel 8 with channel 4 "ON". $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$.
- "OFF" isolation is measured by driving channel 8 with ALL channels "OFF". $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$. C_{DS} is computed from the OFF isolation measurement.
- Sample tested.
- Guaranteed by leakage current and R_{ON} tests.
- Leakage tests are performed only on military temperature grades at 125°C.

MUX-08

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



MUX-08

DIE SIZE 0.093 × 0.059 inch, 5487 sq. mil
(2.362 × 1.500 mm, 3543 sq. mm)

- | | |
|-------------------|---------|
| 1. A0 | 9. S8 |
| 2. ENABLE | 10. S7 |
| 3. V- (SUBSTRATE) | 11. S6 |
| 4. S1 | 12. S5 |
| 5. S2 | 13. V+ |
| 6. S3 | 14. GND |
| 7. S4 | 15. A2 |
| 8. DRAIN | 16. A1 |

WAFER TEST LIMITS at $V+ = 15V$, $V- = -15V$, $T_A = 25^\circ C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 200\mu A$ $T_A = 125^\circ C$	300 400	300 —	400 —	Ω MAX
Digital "1" Input Voltage	V_{INH}	(Note 2)	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}	(Note 2)	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$ $T_A = 125^\circ C$	10 20	10 —	10 —	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{IN} = 0.4V$ $T_A = 125^\circ C$	10 20	10 —	10 —	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	$I+$	$T_A = 125^\circ C$	12 15	12 —	12 —	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	$I-$	$T_A = 125^\circ C$	3.8 5	3.8 —	3.8 —	mA MAX
Analog Input Range	V_A	(Note 2)	± 10	± 10	± 10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V+ = 15V$, $V- = -15V$ and $T_A = 25^\circ C$ for MUX-08/24N & G, $T_A = 125^\circ C$ for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL}	(Note 1)	1.7	1.3	2.1	μS
	t_{PLH}		1.1	0.9	1.3	
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	μS
Break-Before-Make Delay	t_{OPEN}	(Note 1)	0.8	0.8	1.0	μS
Crosstalk	CT	(Note 1)	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	2	2	6	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	$V_D = 10V$ (Note 1)	20	0.5	0.5	nA
Analog Input Range	V_A		+10.4/-15	+10.4/-15	+10.4/-15	V

NOTES:

1. The data shown is extrapolated from measurements made on the packaged devices.

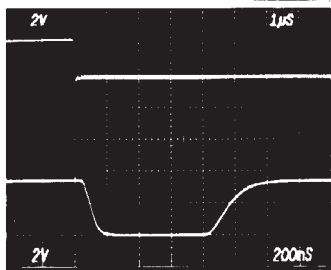
2. Guaranteed by leakage current and R_{ON} tests.

MUX-08
LOGIC STATE

A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

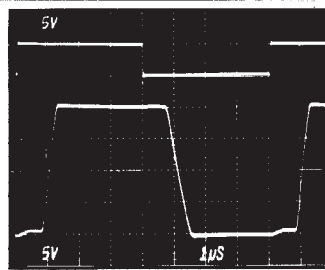
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

MUX-08
BREAK-BEFORE-MAKE
SWITCHING



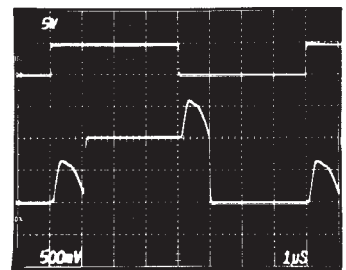
R_L = 1kΩ, C_L = 10pF, V₁, 8 = 10V
VOLTAGE = 2V/DIV
TIME = 200ns/DIV

MUX-08
LARGE-SIGNAL SWITCHING



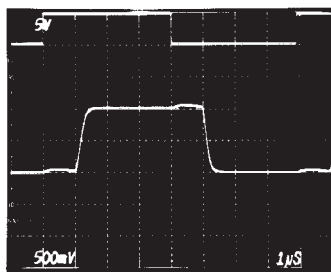
R_L = 1MΩ, C_L = 10pF, V₁ = -10V, V₈ = +10V
VOLTAGE = 5V/DIV
TIME = 1µs/DIV

MUX-08
SMALL-SIGNAL SWITCHING



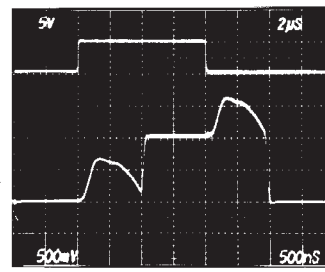
R_L = 1MΩ, C_L = 10pF, V₁ = -500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 1µs/DIV

MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING



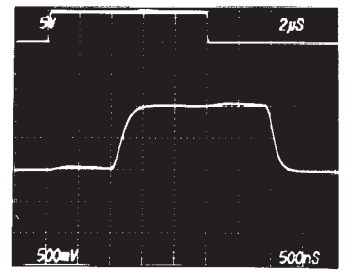
R_L = 1MΩ, C_L = 500pF, V₁ = 500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 1µs/DIV

MUX-08
SMALL-SIGNAL SWITCHING
WITH 2µs SAMPLE TIME



R_L = 1MΩ, C_L = 10pF, V₁ = -500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING AND
2.5µs SAMPLE TIME



R_L = 1MΩ, C_L = 500pF, V₁ = -500mV, V₈ = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

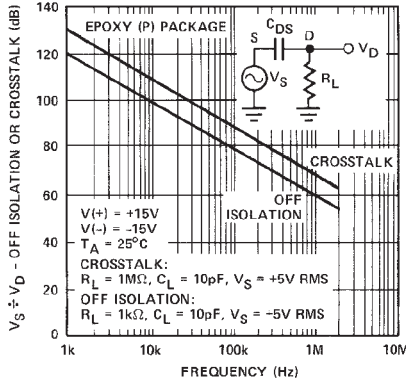
NOTE:

Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

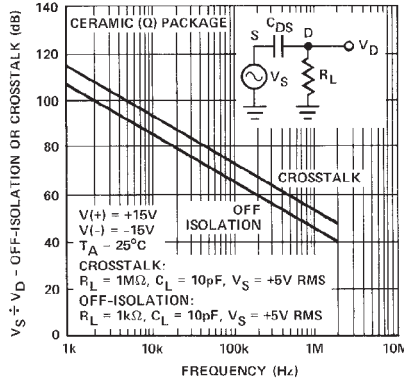
MUX-08

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

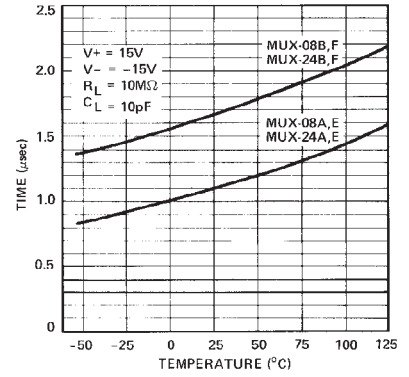
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



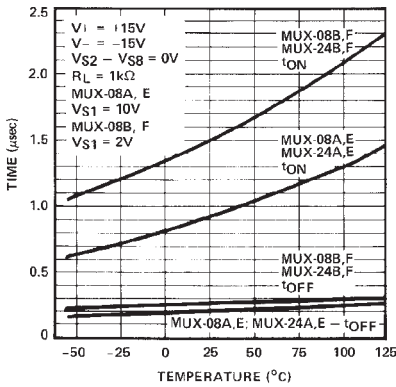
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



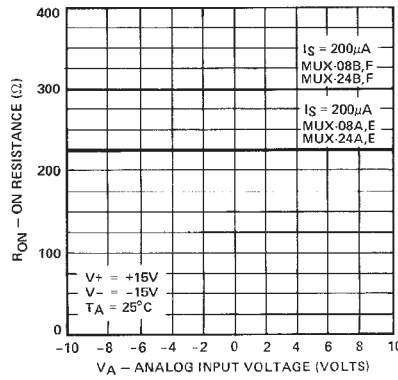
TRANSITION TIMES vs TEMPERATURE



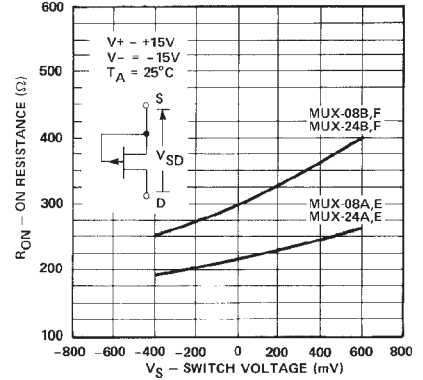
ENABLE DELAY TIMES vs TEMPERATURE



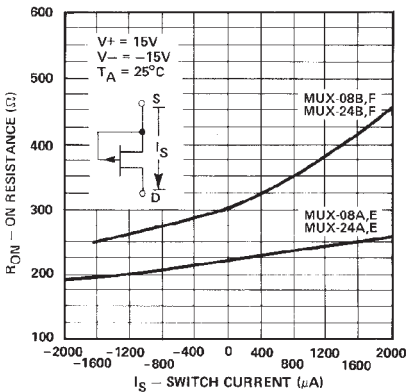
"ON" RESISTANCE (R_ON) vs ANALOG VOLTAGE (V_A)



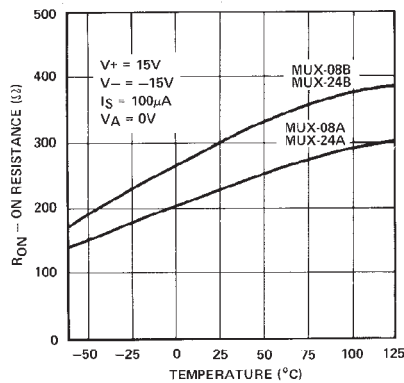
R_ON vs SWITCH VOLTAGE (V_SD)



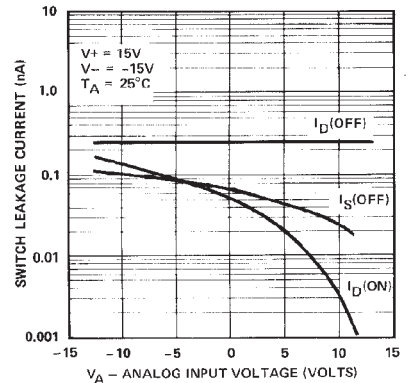
R_ON vs SWITCH CURRENT (I_S)



R_ON vs TEMPERATURE

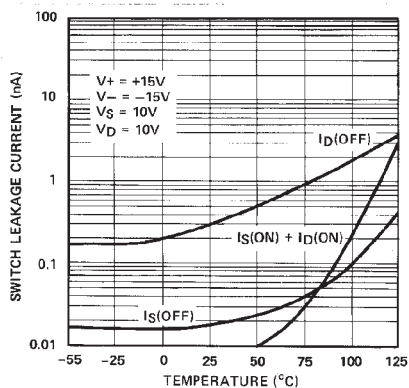


SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

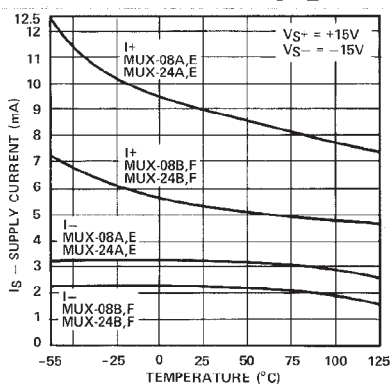


TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

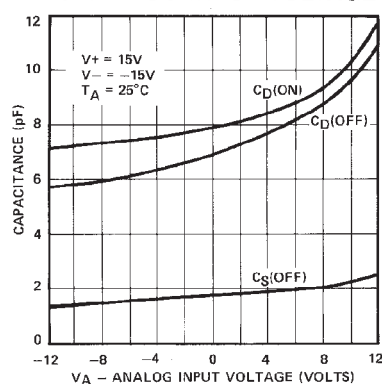
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



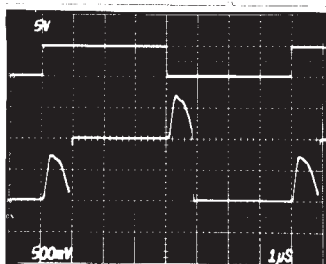
SUPPLY CURRENTS vs TEMPERATURE



MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

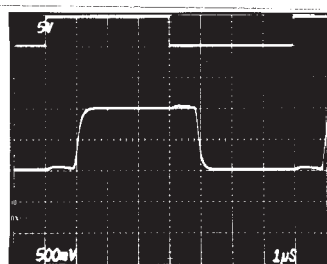


MUX-24 SMALL-SIGNAL SWITCHING



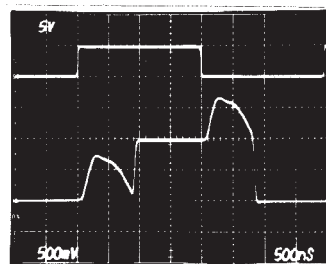
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING



$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



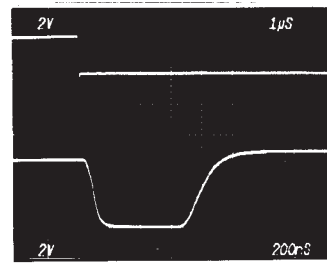
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME



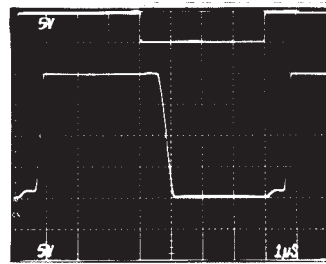
$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
 VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING



$R_L = 1k\Omega$, $C_L = 10pF$, $V_1 = 10V$
 VOLTAGE = 2V/DIV, TIME = 200ns/DIV

MUX-24 LARGE-SIGNAL SWITCHING



$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_4 = +10V$
 VOLTAGE = 5V/DIV, TIME = 1µs/DIV

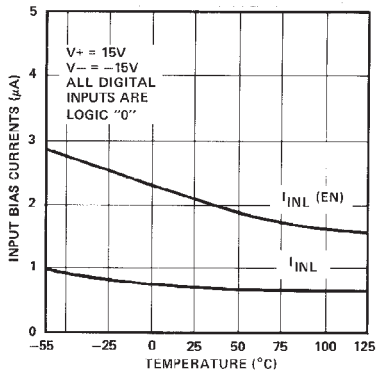
NOTE:

Top waveforms: Digital Input 5V/DIV
 Bottom waveforms: Multiplexer Output

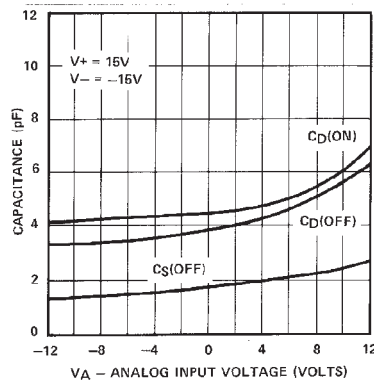
MUX-08

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

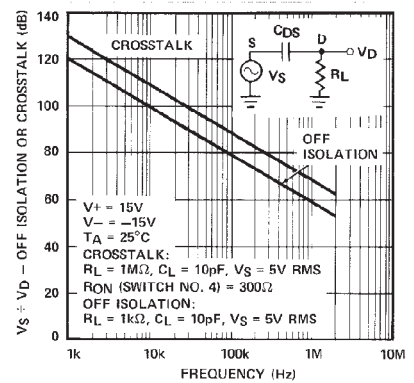
DIGITAL INPUT CURRENTS vs TEMPERATURE



MUX-24 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

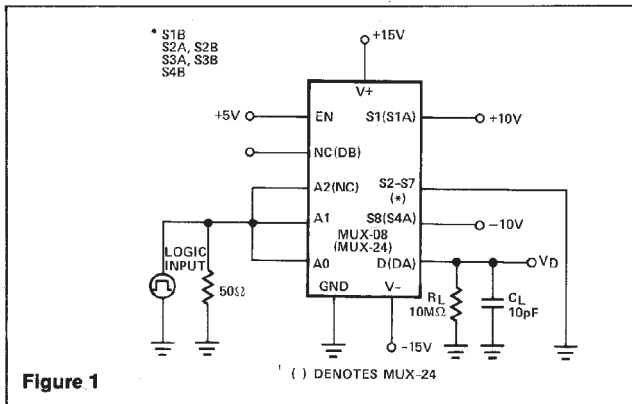


MUX-24 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 3A

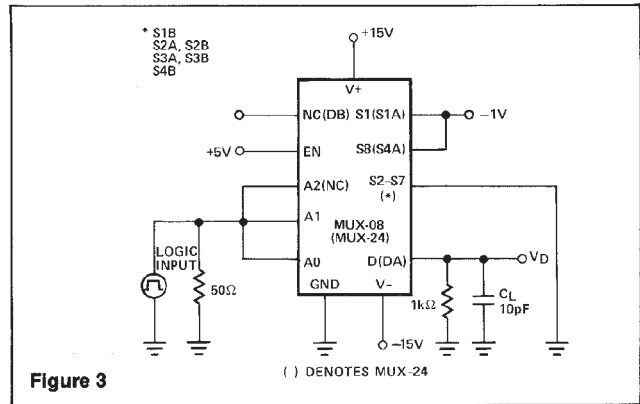


A.C. TEST CIRCUITS

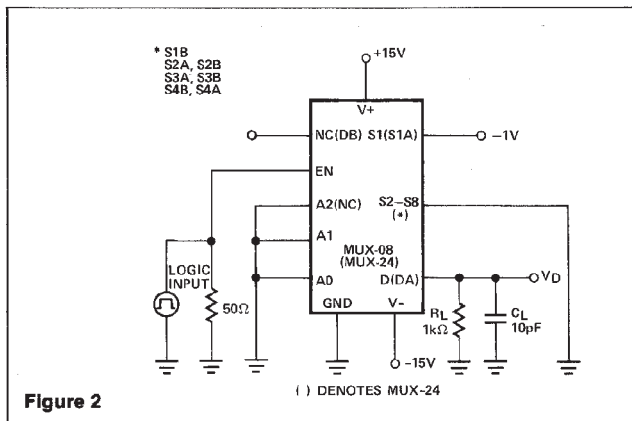
TRANSITION TIME TEST CIRCUIT



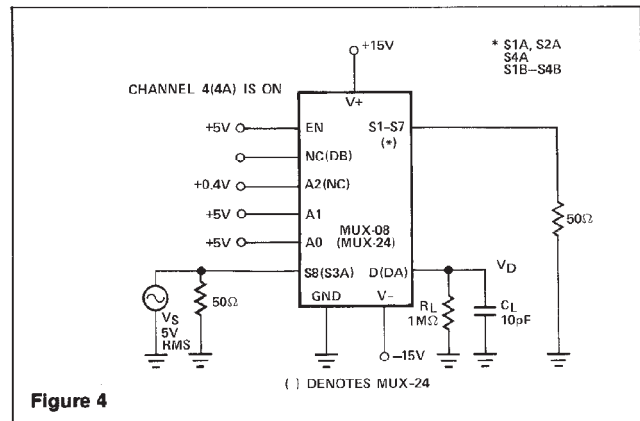
BREAK-BEFORE-MAKE TEST CIRCUIT



ENABLE DELAY TIME TEST CIRCUIT



CROSSTALK MEASUREMENT CIRCUIT



A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT

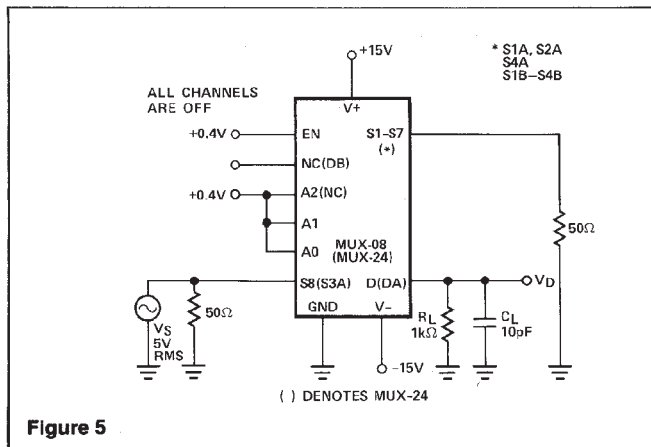
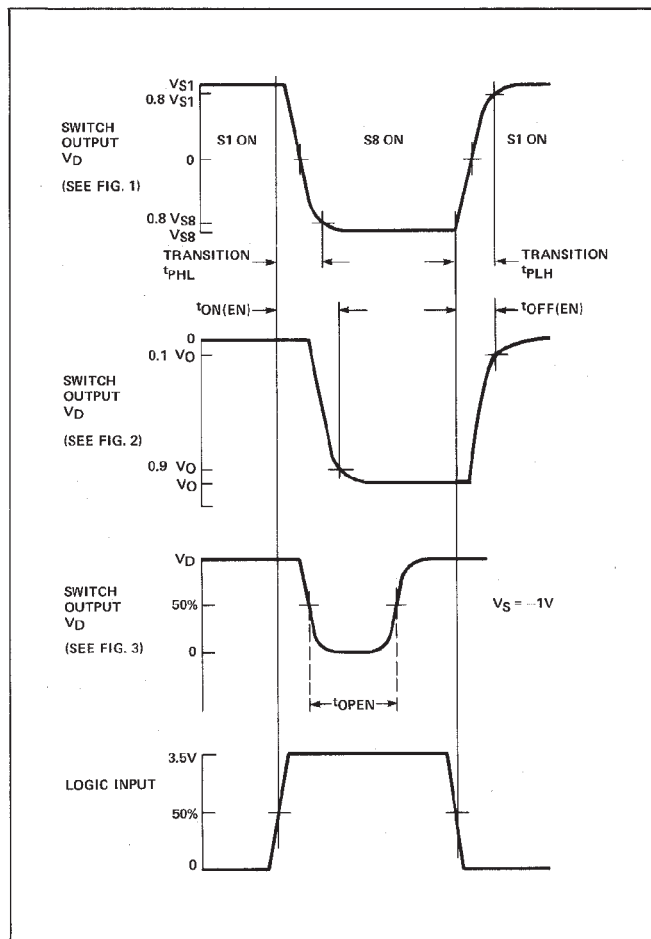


Figure 5

SWITCHING TIME WAVEFORMS



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p , and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a $0.01\mu F$ capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was $0.3V/\mu s$ which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was $0.7V/\mu s$ which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .

CROSSTALK AND OFF-ISOLATION

Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation ($f = 500kHz$) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk ($f = 500kHz$) performance when compared to ceramic (Q) packaged devices.

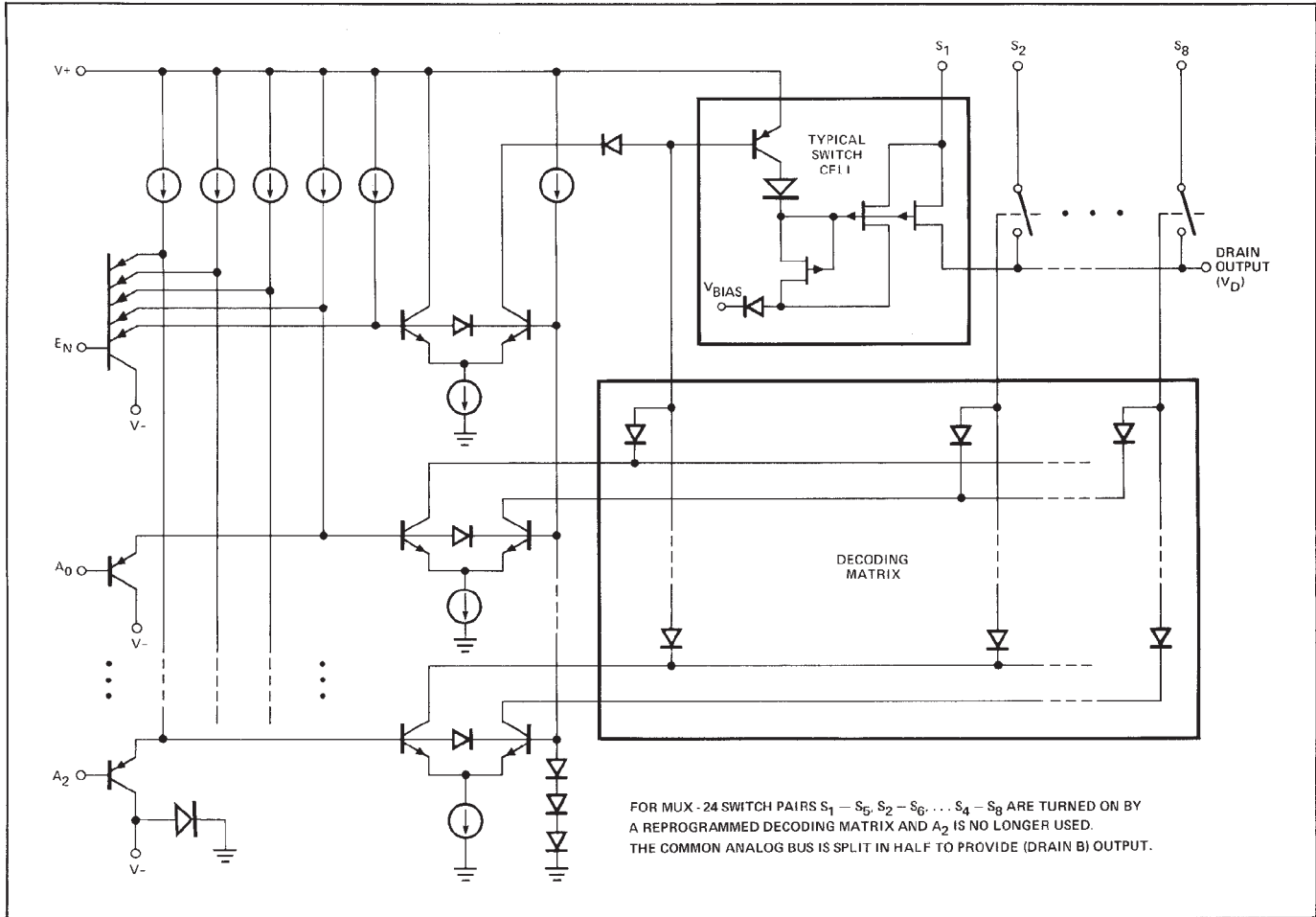
SINGLE SUPPLY OPERATION OF JFET MULTIPLEXERS

PMI's JFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer to application note, AN-32.

MUX-08

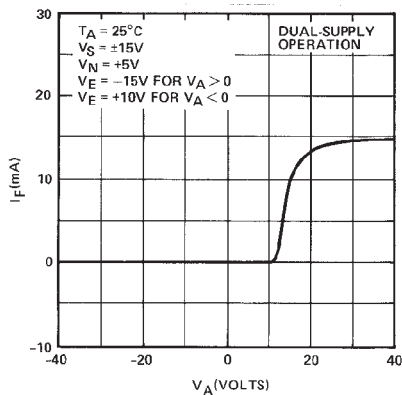
SIMPLIFIED MUX-08 SCHEMATIC



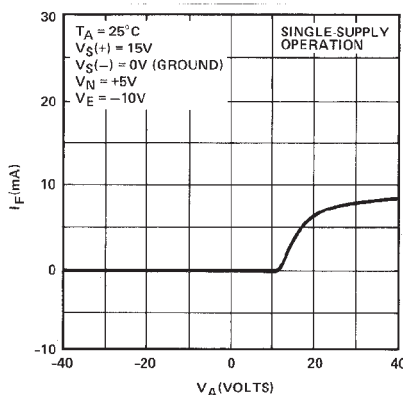
The simplified MUX-08/MUX-24 schematic shows that logic trip points are determined by two forward diode drops. An internal clamping diode between V^- and ground prevents excessive current flow between V^+ and ground in the event that V^- becomes open circuit. The decoding matrix is accomplished by a programmed diode array. The switch cell consists of P channel JFET's with appropriate blocking diodes which ruggedizes the circuit's overvoltage and supply loss characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

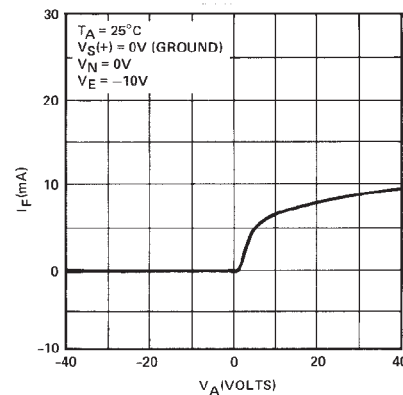
OVERVOLTAGE V-I CHARACTERISTIC



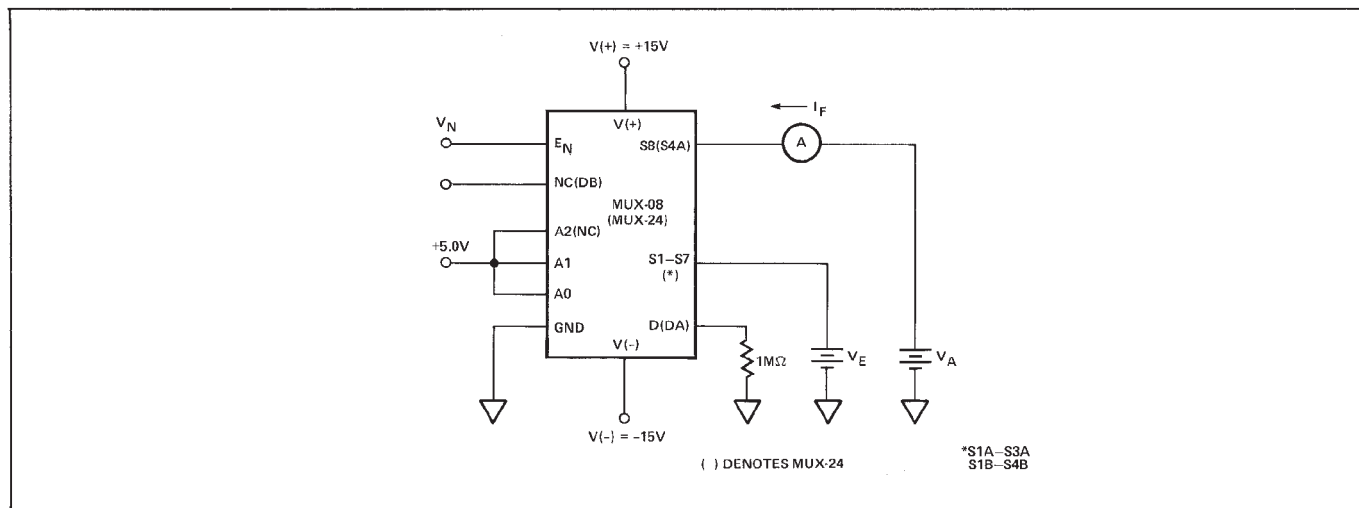
OVERVOLTAGE V-I CHARACTERISTIC



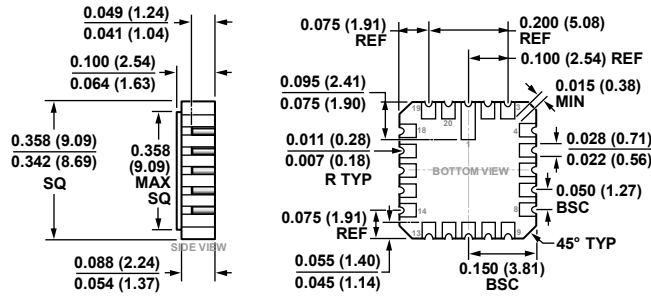
POWER-LOSS V-I CHARACTERISTIC



OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT



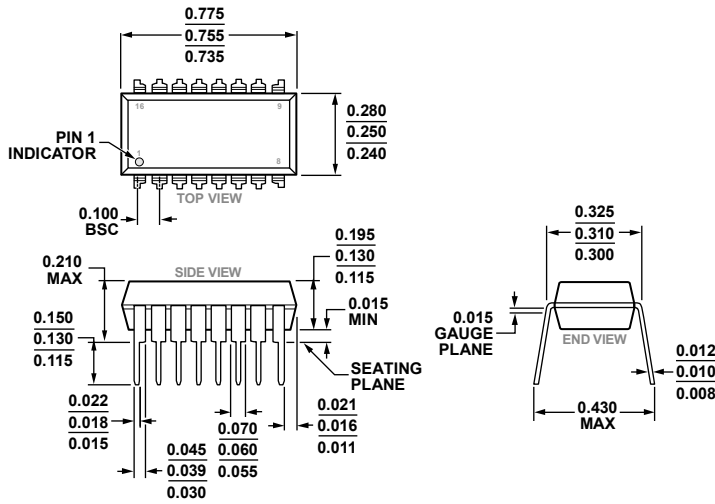
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 6. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20-1)

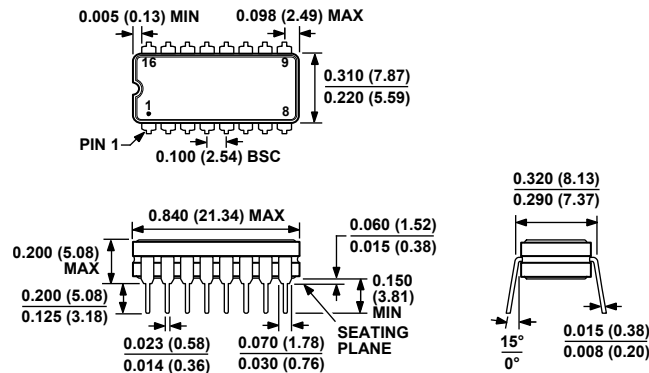
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 7. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)

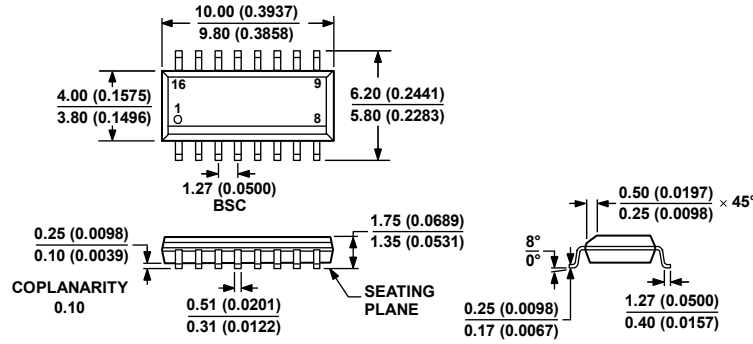
Dimensions shown in inches



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 8. 16-Lead Ceramic Dual In-Line Package [CERDIP] (Q-16)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

069606-A

Figure 9. 16-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-16)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
MUX08EPZ	0°C to 70°C	16-Lead PDIP	N-16
MUX08EQ	-25°C to +85°C	16-Lead CERDIP	Q-16
MUX08FPZ	-40°C to +85°C	16-Lead PDIP	N-16
MUX08FQ	-25°C to +85°C	16-Lead CERDIP	Q-16
MUX08FSZ	-40°C to +85°C	16-Lead SOIC_N	R-16
MUX08NBC	25°C	DIE	
5962-8771601EA	-55°C to +125°C	16-Lead CERDIP	Q-16
5962-87716022A	-55°C to +125°C	20-Terminal Ceramic LCC	E-20-1
5962-8771602EA	-55°C to +125°C	16-Lead CERDIP	Q-16
MUX08AQ/883C	-55°C to +125°C	16-Lead CERDIP	Q-16
MUX08BQ/883C	-55°C to +125°C	16-Lead CERDIP	Q-16

¹ Z = RoHS Compliant Part

REVISION HISTORY

5/2019—Rev. B to Rev C

Obsoluted MUX-24 and MUX08BRC/883 Universal
Deleted MUX-24 Functional Diagram..... 1
Changes to Features Section, Ordering information Section, and
General Description Section..... 1
Changed MUX-08A/E MUX-24A/E Column to MUX-08A/E
Column, Electrical Characteristics Table and MUX-08B/F
MUX-24B/F Column to MUX-08B/F Column, Electrical
Characteristics Table..... 2
Changed MUX-08A/MUX-24A Column to MUX-08A Column
and MUX-08B/MUX-24B Column to MUX-08B Column,

Electrical Characteristics Table, and MUX-08E/MUX-24E Column
to MUX-08E Column and MUX-08F/MUX-24F Column to
MUX-08F Column, Electrical Characteristics Table..... 3
Change to “ON” Resistance Parameter, MUX-08A..... 3
Deleted MUX-24 Dice Characteristics..... 4
Deleted MUX-24 Logic State Table 5
Deleted Differential Multiplexers and Figure 6 10
Added Outlines Dimension Section..... 12
Added Ordering Guide 13

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[MUX36S16IRSNR](#) [74LVC1G3157GM-Q10X](#) [TC7W53FK,LF](#) [CD4053BM96](#) [MC74HC4053ADWR2G](#) [SN74LV4051APWR](#)
[HEF4053BT.653](#) [ADG5408BRUZ-REEL7](#) [ADG1404YRUZ-REEL7](#) [ADG1208YRZ-REEL7](#) [MAX4704EUB+T](#) [ADG1406BRUZ-REEL7](#)
[LTC4305IDHD#PBF](#) [CD4053BPWRG4](#) [74HC4053D.653](#) [74HCT4052PW.118](#) [74LVC2G53DP.125](#) [74HC4052DB.112](#) [74HC4052PW.112](#)
[74HC4053DB.112](#) [74HC4067DB.112](#) [74HC4351DB.112](#) [74HCT4052D.112](#) [74HCT4052DB.112](#) [74HCT4053DB.112](#) [74HCT4067D.112](#)
[74HCT4351D.112](#) [74LV4051PW.112](#) [FSA1256L8X_F113](#) [PI5V330QE](#) [PI5V331QE](#) [5962-8771601EA](#) [5962-87716022A](#) [ADG5249FBRUZ](#)
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