Digital Input Stereo, 2 W, Class-D Audio Power Amplifier

Datasheet

SSM2518

FEATURES

- **Filterless, digital input Class-D amplifier**
- **Serial digital audio interface supports common formats**
  - **I²S, left justified, right justified, TDM1-16, and PCM**
- **2 channels × 2 W into 4 Ω and 2 channels × 1.4 W into 8 Ω with 1% THD+N, when using a 5 V supply**
- **I²C control interface or standalone operation**
- **91% efficiency at full scale into an 8 Ω load**
- **97 dB signal-to-noise ratio (SNR), A-weighted**
- **80 dB power supply rejection ratio (PSRR) at 217 Hz**
- **Digital volume control: −71.25 dB to +24 dB in 0.375 dB steps**
- **Supports a wide range of sample rates from 8 kHz to 96 kHz**
- **Automatic sample rate detection**
- **Can operate using 64 × f_S BCLK as the MCLK source**
- **2.5 V to 5.5 V speaker supply voltage (PVDD)**
- **1.62 V to 3.6 V digital supply voltage (DVDD)**
- **Pop-and-click suppression**
- **Short-circuit and thermal protection with programmable autorecovery**
- **Smart power-down when no input signal is detected**
- **Power-on reset**
- **Low power modes for performance/power trade-offs**
- **User selectable ultralow EMI emission mode**
- **Programmable dynamic range compression (DRC) with noise gate, expander, compressor, and limiter**
- **Available in two packages**
  - **16-bump, 2.2 mm × 2.2 mm, 0.5 mm pitch WLCSP**
  - **20-lead, 4.0 mm × 4.0 mm LFCSP**

APPLICATIONS

- **Mobile phones**
- **Portable media players**
- **Laptop PCs**
- **Wireless speakers**
- **Portable gaming**
- **Small LCD televisions**
- **Navigation systems**

GENERAL DESCRIPTION

The SSM2518 is a digital input, Class-D power amplifier that combines a digital-to-analog converter (DAC) and a sigma-delta (Σ-Δ) Class-D modulator. This unique architecture enables extremely low real-world power consumption from digital audio sources with excellent audio performance. The SSM2518 is ideal for power sensitive applications, such as mobile phones and portable media players, where system noise can corrupt small analog signals such as those sent to an analog input audio amplifier.

Using the SSM2518, audio data can be transmitted to the amplifier over a standard digital audio serial interface, thereby significantly reducing the effect of noise sources such as GSM interference or other digital signals on the transmitted audio. The closed-loop digital input design retains the benefits of an all digital amplifier, yet enables very good PSRR and audio performance. The three level, Σ-Δ Class-D modulator is designed to provide the least amount of EMI interference, the lowest quiescent power dissipation, and the highest audio efficiency without sacrificing audio quality.

Input is provided via a serial audio interface, programmable to accept all common audio formats including I²S and TDM. Control of the IC is provided via an I²C control interface. The SSM2518 can accept a variety of input MCLK frequencies and can use BCLK as the clock source in some configurations.

Additional features include a soft digital volume control, de-emphasis, and a programmable digital dynamic range compressor.

The architecture of the SSM2518 provides a solution that offers lower power and higher performance than existing DAC plus Class-D solutions. Its digital interface also offers a better system solution for other products whose sole audio source is digital, such as wireless speakers, laptop PCs, portable digital televisions, and navigation systems.

Rev. B Document Feedback

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REVISION HISTORY

1/2018—Rev. A to Rev. B

11/2011—Rev. 0 to Rev. A

10/2011—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

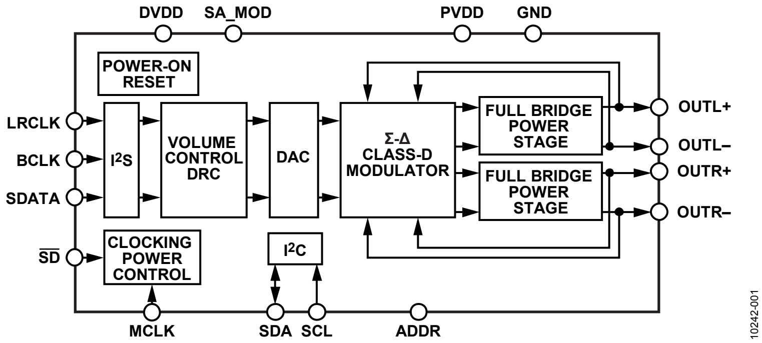

Figure 1.

SPECIFICATIONS

All specifications at PVDD = 5.0 V, DVDD = 1.8 V, f_S = 48 kHz, MCLK = 128 × f_S, T_A = 25°C, R_L = 8 Ω + 15 µH, LP_MODE = 0, volume control = 0 dB, unless otherwise noted.

PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
	P_O	f = 1 kHz, BW = 20 kHz				
Output Power		R_L = 4 Ω, THD = 1%, PVDD = 5.0 V		2		W
		R_L = 4 Ω, THD = 10%, PVDD = 5.0 V		2.5		W
		R_L = 8 Ω, THD = 1%, PVDD = 5.0 V		1.42		W
		R_L = 8 Ω, THD = 10%, PVDD = 5.0 V		1.8		W
		R_L = 4 Ω, THD = 1%, PVDD = 3.6 V		1.3		W
		R_L = 4 Ω, THD = 10%, PVDD = 3.6 V		1.7		W
		R_L = 8 Ω, THD = 1%, PVDD = 3.6 V		0.75		W
		R_L = 8 Ω, THD = 10%, PVDD = 3.6 V		0.94		W
		R_L = 4 Ω, THD = 1%, PVDD = 2.5 V		0.4		W
		R_L = 4 Ω, THD = 10%, PVDD = 2.5 V		0.45		W
		R_L = 8 Ω, THD = 1%, PVDD = 2.5 V		0.275		W
		R_L = 8 Ω, THD = 10%, PVDD = 2.5 V		0.35		W
Efficiency	η	P_O = 1.4 W, 8 Ω, PVDD = 5.0 V, normal operation		91		%
		P_O = 1.4 W, 8 Ω, PVDD = 5.0 V, ultralow EMI operation		86		%
Total Harmonic Distortion Plus Noise	THD + N	P_O = 0.5 W into 8 Ω each channel, f = 1 kHz, PVDD = 5 V		0.04		%
		P_O = 0.25 W into 8 Ω each channel, f = 1 kHz, PVDD = 3.6 V		0.03		%
Channel Separation	X_{TALK}	P_O = 1 W, f = 1 kHz, PVDD = 5 V		108		dB
Average Switching Frequency	f_{SW}			280		kHz
Differential Output Offset	V_{OOS}			2.0		mV
Power Supply Rejection Ratio	$PSRR_{DC}$	PVDD = 2.5 V to 5.0 V	70	80		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV rms at 217 Hz, dither input		80		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV rms at 217 Hz, no input		100		dB
Supply Current PVDD	I_{PVDD}	Dither input, no load, PVDD = 5.0 V		4.7		mA
		Dither input, no load, PVDD = 3.6 V		4.4		mA
		Dither input, no load, PVDD = 2.5 V		3.8		mA
		Software power-down, $\overline{SD}$ = 1.8 V, SPWDN = 1, PVDD = 3.6 V		4		µA
		Hardware power-down, $\overline{SD}$ = 0 V, PVDD = 3.6 V		100		nA
DVDD	I_{DVDD}	Dither input, no load, DVDD = 3.3 V		3.0		mA
		Dither input, no load, DVDD = 1.8 V		1.5		mA
		Dither input, no load, DVDD = 1.8 V, f_S = 8 kHz		0.25		mA
		Software power-down, $\overline{SD}$ = 1.8 V, SPWDN = 1, DVDD = 1.8 V		2.5		µA
		Hardware power-down, $\overline{SD}$ = 0 V, DVDD = 1.8 V		100		nA
Output Noise Voltage	e_n	PVDD = 5 V, f = 20 Hz to 20 kHz, dither input, A-weighted		50		µV
		PVDD = 3.6 V, f = 20 Hz to 20 kHz, dither input, A-weighted		40		µV
Signal-to-Noise Ratio	SNR	A-weighted, referred to 0 dBFS, PVDD = 3.6 V		97		dB
Mute Attenuation		Soft mute on	100			dB

POWER SUPPLY REQUIREMENTS

Table 2.

Parameter	Min	Typ	Max	Unit
PVDD	2.5	3.6	5.5	V
DVDD	1.62	1.8	3.6	V

DIGITAL INPUT/OUTPUT

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE					
High (V_{IH})	0.7 × DVDD		3.6	V	ADDR, MCLK, BCLK, LRCLK, SDATA, SAMOD
	1.35		5.5	V	$\overline{SD}$, SDA, SCL
Low (V_{IL})	−0.3		+0.3 × DVDD	V	ADDR, MCLK, BCLK, LRCLK, SDATA, SAMOD
	−0.3		+0.35	V	$\overline{SD}$, SDA, SCL
INPUT LEAKAGE CURRENT					
High (I_{IH})			1	µA	Excluding MCLK
Low (I_{IL})			1	µA	Excluding MCLK and bidirectional pin
MCLK INPUT LEAKAGE CURRENT					
High (I_{IH})			3	µA	
Low (I_{IL})			3	µA	
INPUT CAPACITANCE			5	pF	

DIGITAL INTERPOLATION FILTER

Table 4.

Parameter	Factor	Min	Typ[1]	Max	Unit
PASS BAND					
−3 dB	0.4535 × f_S		22		kHz
Ripple				±0.01	dB
TRANSITION BAND	0.5 × f_S		24		kHz
STOP BAND	0.5465 × f_S		26		kHz
Attenuation		70			dB
GROUP DELAY	25/f_S		521		µs

[1] Typical value given for 48 kHz sample rate.

DIGITAL TIMING

All timing specifications are given for the default setting (I^2S mode) of the serial input port.

Table 5.

Parameter	Limit Min	Limit Max	Unit	Description
MASTER CLOCK				
t_{MP}	74	136	ns	MCLK period, 256 × f_S mode (MCS = b0010)
t_{MP}	148	271	ns	MCLK period, 128 × f_S mode (MCS = b0001)
SERIAL PORT				
t_{BIL}	40		ns	BCLK low pulse width
t_{BIH}	40		ns	BCLK high pulse width
t_{LIS}	10		ns	Setup time from LRCLK or SDATA edge to BCLK rising edge
t_{LIH}	10		ns	Hold time from BCLK rising edge to LRCLK or SDATA edge
t_{SIS}	10		ns	SDATA setup time to BCLK rising
t_{SIH}	10		ns	SDATA hold time from BCLK rising
I^2C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period, the first clock is generated
t_{DS}	100		ns	Data setup time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	0.6		µs	Bus-free time (time between stop and start)

Digital Timing Diagrams

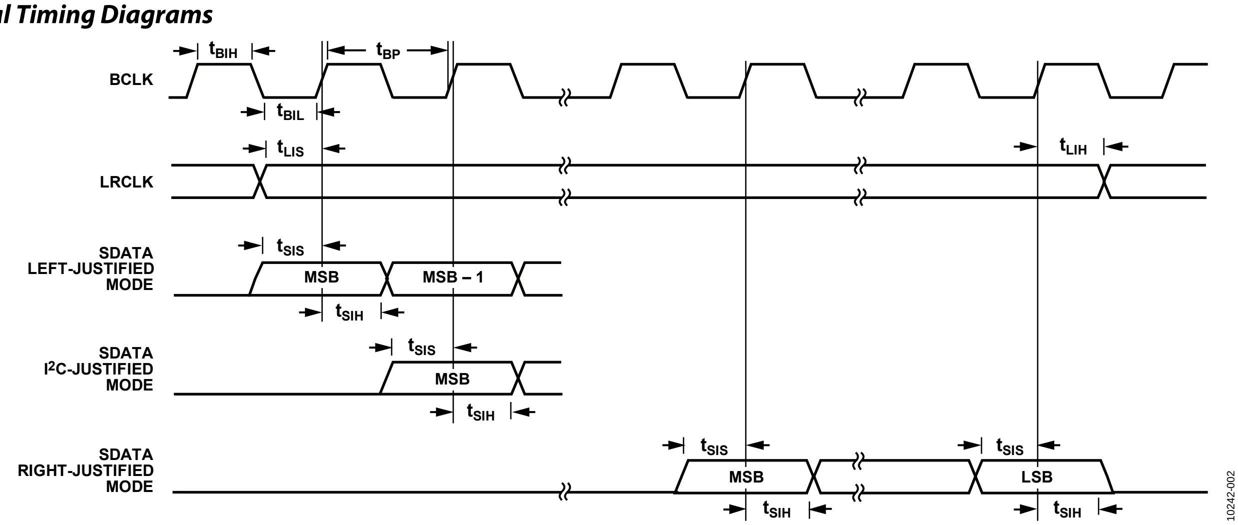

Figure 2. Serial Input Port Timing

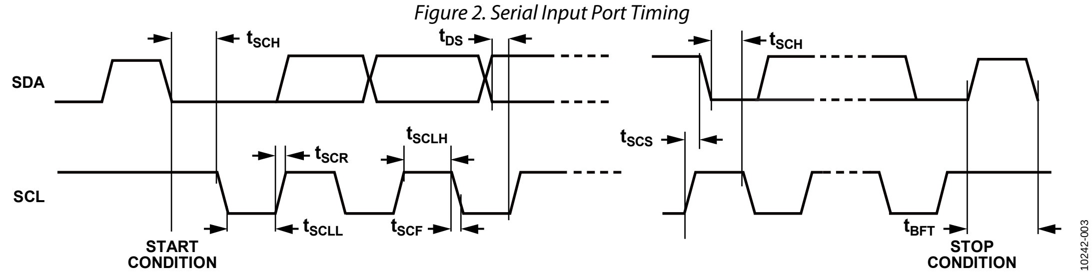

Figure 3. I^2C Port Timing

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
PVDD Supply Voltage	−0.3 V to +6 V
DVDD Supply Voltage	−0.3 V to +3.6 V
Input Voltage (ADDR, MCLK, BCLK, LRCLK, SDATA, SAMOD Pins)	−0.3 V to +3.6 V
Input Voltage ($\overline{SD}$, SDA, and SCL Pins)	−0.3 V to +6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
16-ball, 2 mm × 2 mm WLCSP	56	°C/W
20-lead, 4.0 mm × 4.0 mm LFCSP	54	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

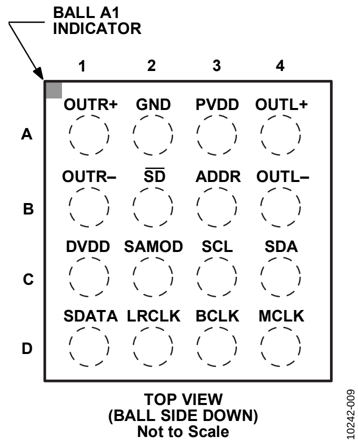

Figure 4. WLCSP Pin Configuration

Table 8. Pin Function Descriptions, WLCSP

Pin No.	Mnemonic	Function[1]	Description
A1	OUTR+	O	Right Channel Output Positive.
B1	OUTR−	O	Right Channel Output Negative.
A4	OUTL+	O	Left Channel Output Positive.
B4	OUTL−	O	Left Channel Output Negative.
A3	PVDD	P	2.5 V to 5.5 V Amplifier Power.
A2	GND	P	Amplifier Ground.
C1	DVDD	P	1.62 V to 3.6 V Digital and Analog Power.
B2	$\overline{\text{SD}}$	I	Power-Down Control, Active Low.
C3	SCL	I	I²C Clock.
C4	SDA	I/O	I²C Data.
D4	MCLK	I	Serial Audio Interface Master Clock.
D2	LRCLK	I	I²S Word Clock.
D3	BCLK	I	I²S Bit Clock.
D1	SDATA	I	I²S Serial Data.
C2	SAMOD	I	Standalone/I²C Mode Select. High = standalone mode, low = I²C mode.
B3	ADDR	I	I²C Address Select.

[1] I is input, O is output, I/O is input/output, and P is power.

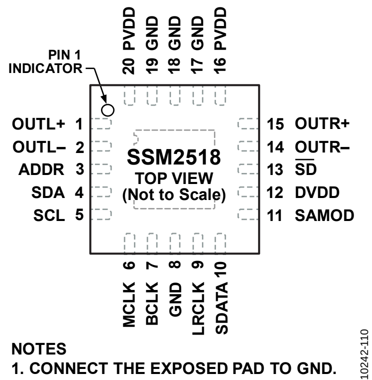

Figure 5. LFCSP Pin Configuration

Table 9. Pin Function Descriptions, LFCSP

Pin No.	Mnemonic	Function[1]	Description
1	OUTL+	O	Left Channel Output Positive.
2	OUTL−	O	Left Channel Output Negative.
3	ADDR	I	I^2C Address Select.
4	SDA	I/O	I^2C Data.
5	SCL	I	I^2C Clock.
6	MCLK	I	Serial Audio Interface Master Clock.
7	BCLK	I	I^2S Bit Clock.
8	GND	P	Amplifier Ground.
9	LRCLK	I	I^2S Word Clock.
10	SDATA	I	I^2S Serial Data.
11	SAMOD	I	Standalone/I^2C Mode Select. High = standalone mode, low = I^2C mode.
12	DVDD	P	1.62 V to 3.6 V Digital and Analog Power.
13	$\overline{SD}$	I	Power-Down Control, Active Low.
14	OUTR−	O	Right Channel Output Negative.
15	OUTR+	O	Right Channel Output Positive.
16	PVDD	P	2.5 V to 5.5 V Amplifier Power.
17	GND	P	Amplifier Ground.
18	GND	P	Amplifier Ground.
19	GND	P	Amplifier Ground.
20	PVDD	P	2.5 V to 5.5 V Amplifier Power.

[1] I is input, O is output, I/O is input/output, and P is power.

TYPICAL PERFORMANCE CHARACTERISTICS

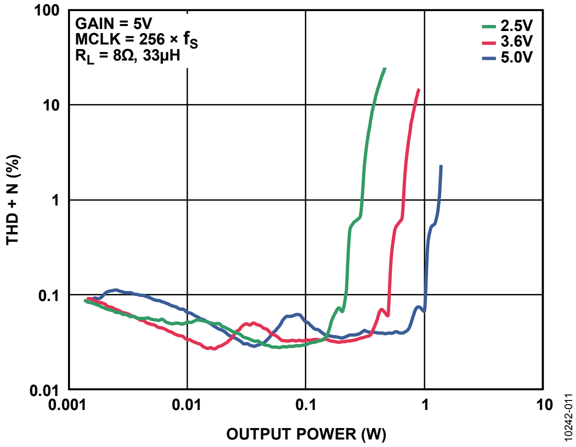

Figure 6. THD + N vs. Output Power into 8 Ω, 5.0 V Gain Setting

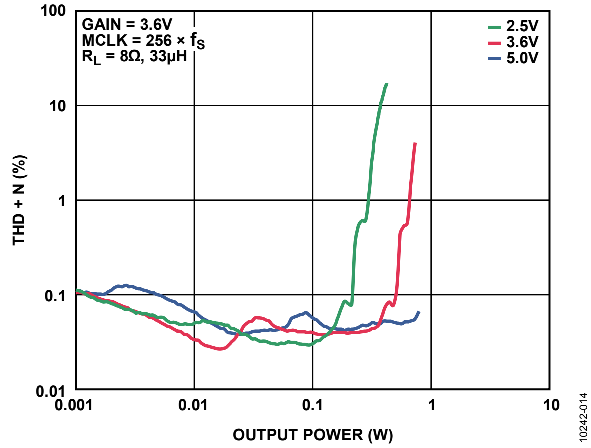

Figure 9. THD + N vs. Output Power into 8 Ω, 3.6 V Gain Setting

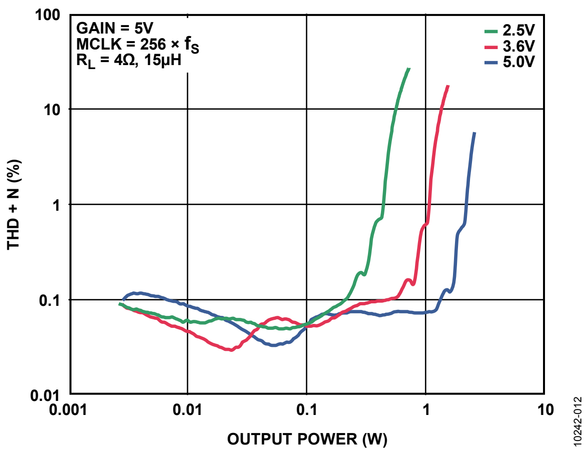

Figure 7. THD + N vs. Output Power into 4 Ω, 5.0 V Gain Setting

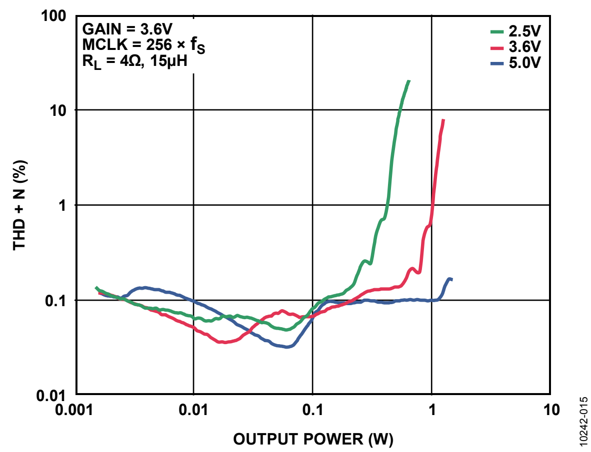

Figure 10. THD + N vs. Output Power into 4 Ω, 3.6 V Gain Setting

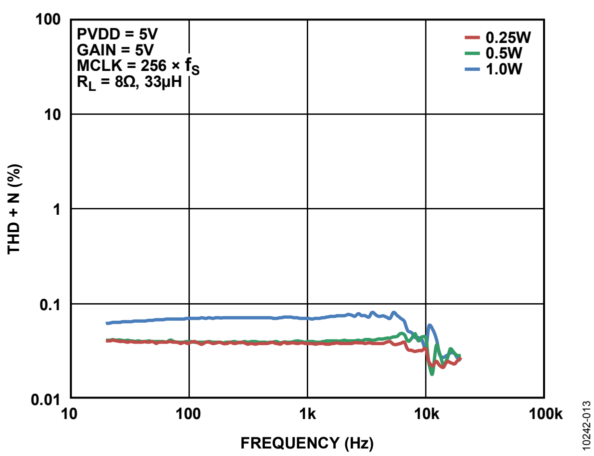

Figure 8. THD + N vs. Frequency, PVDD = 5 V, R_L = 8 Ω

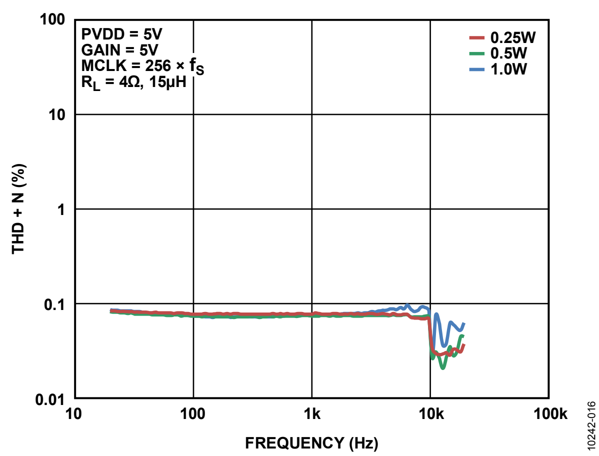

Figure 11. THD + N vs. Frequency, PVDD = 5 V, R_L = 4 Ω

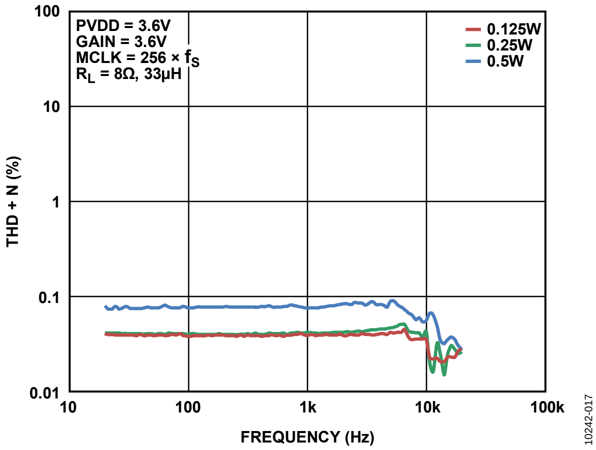

Figure 12. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 8 Ω

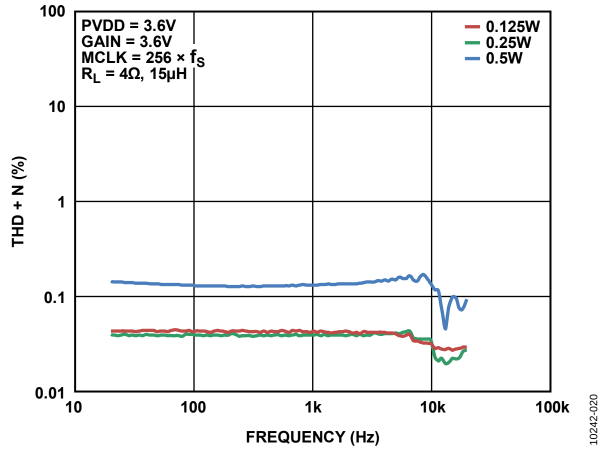

Figure 15. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 4 Ω

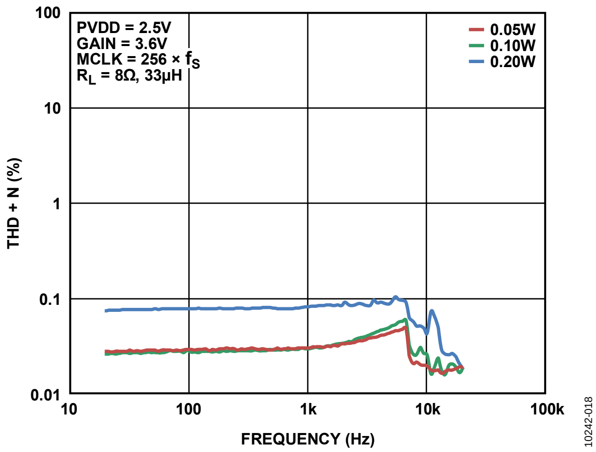

Figure 13. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 8 Ω

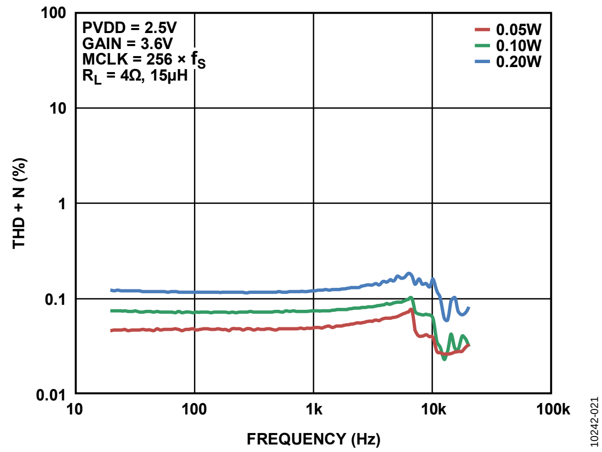

Figure 16. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 4 Ω

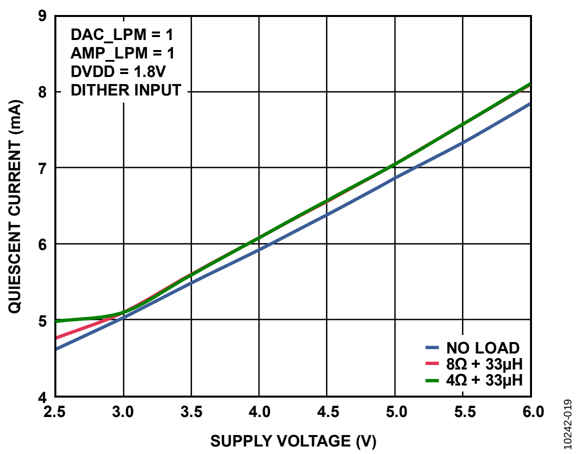

Figure 14. Quiescent Current (Power Stage) vs. Supply Voltage

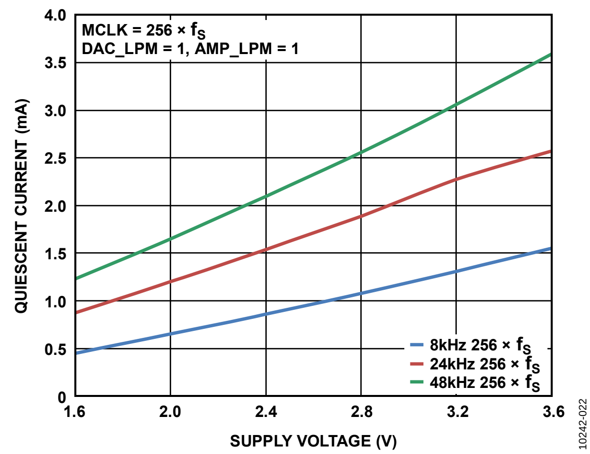

Figure 17. Quiescent Current (Digital Core) vs. Supply Voltage

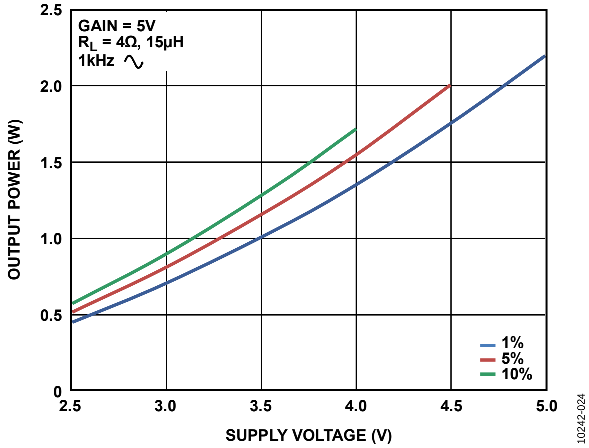

Figure 18. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω

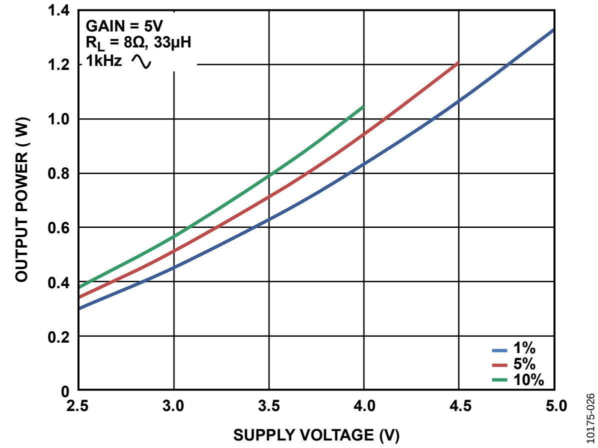

Figure 21. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω

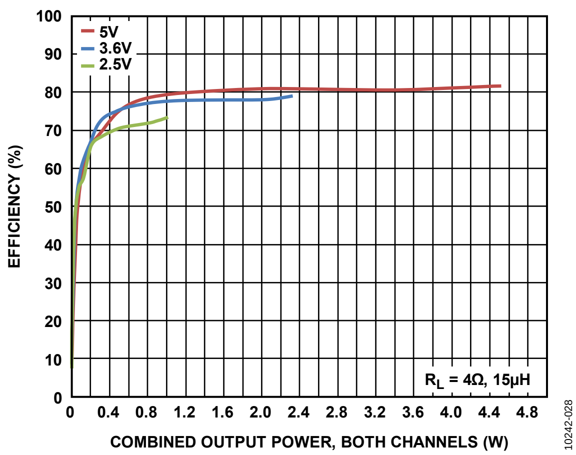

Figure 19. Efficiency vs. Output Power into 4 Ω

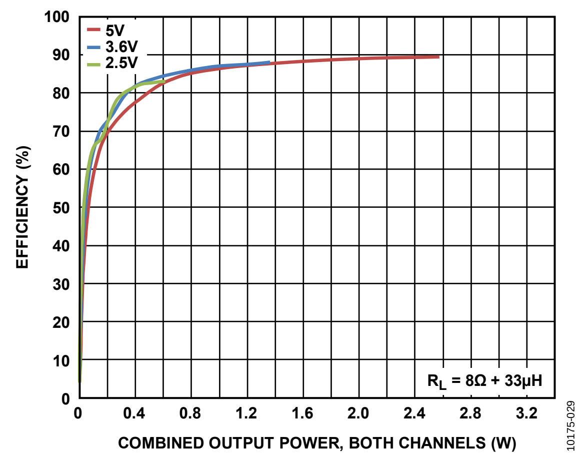

Figure 22. Efficiency vs. Output Power into 8 Ω

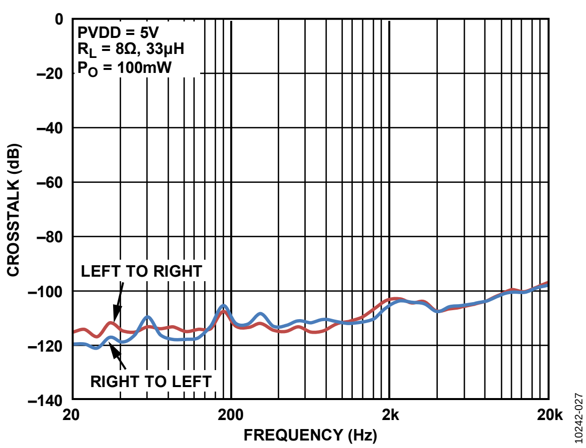

Figure 20. Crosstalk vs. Frequency

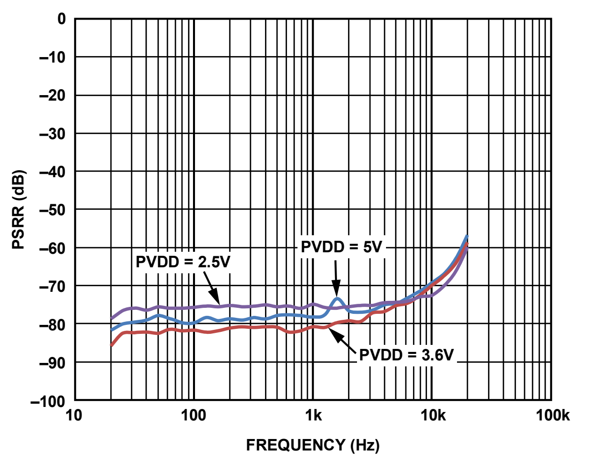

Figure 23. PSRR vs. Frequency

THEORY OF OPERATION

The SSM2518 is fully integrated 2-channel digital input, Class-D output audio amplifier. The SSM2518 receives digital audio input and produces the PDM differential switching outputs using the internal power stage. The part has built in protection for over-temperature as well as overcurrent conditions. The SSM2518 also has built in soft turn on and soft turn off for pop-and-click suppression. The part has programmable register control via the I^2C port.

POWER SUPPLIES

The SSM2518 requires two power supplies: PVDD and DVDD. Descriptions of each of these supplies follow.

PVDD

The PVDD pin supplies power to the full bridge power stage of a MOSFET and its associated drive, control, and protection circuitry. PVDD can operate from 2.5 V to 5.5 V and must be present to obtain audio output. Lowering the supply PVDD results in lower output power and, correspondingly, lower power consumption but does not degrade audio performance.

DVDD

The DVDD pin provides power to the digital logic circuitry and determines the input trip points. DVDD can operate from 1.62 V to 3.6 V and must be present to obtain audio output. Lowering the supply voltage of DVDD results in lower power consumption but does not affect audio performance.

POWER-DOWN MODES

The SSM2518 offers a hardware shutdown pin, $\overline{SD}$, which can be used to set the IC to its lowest power state, with all blocks disabled. This hardware shutdown mode is enabled when the $\overline{SD}$ pin is pulled low.

When the hardware shutdown is removed, the IC begins in software power-down mode, where all blocks except for the I^2C interface are disabled. To fully power up the amplifier, clear S_RST (Bit 7 of Register 0x00). In addition to the software power-down, the software master mute is enabled at the initial state of the amplifier; therefore, no audio is output until Bit 0 of Register 0x07 is cleared.

The left and right channels can be independently shut down by setting setting L_PWDN and R_PWDN (Bit 1 and Bit 2, respectively, in Register 0x09). Disabling a channel shuts down the channel specific digital processing, DAC, Class-D modulator, and power stage.

The SSM2518 also contains a smart power-down feature, which is enabled by default. This feature can be disabled by clearing APWDN_EN (Bit 0 in Register 0x09). When active, this feature monitors the incoming digital audio signal. If this is zero for 1024 consecutive samples, regardless of sample rate, it puts the IC in the smart power-down state wherein all blocks, except the I^2S and I^2C ports, are placed in a low power state. Once a single nonzero input is received on the I^2S interface, the SSM2518 leaves this state and resumes normal operation.

POWER-ON RESET/VOLTAGE SUPERVISOR

The SSM2518 includes an internal power-on reset and voltage supervisor circuit. This circuit provides an internal reset to all circuitry whenever PVDD or DVDD is substantially below the nominal operating threshold. This circuit simplifies supply sequencing during initial power-on.

The circuit also monitors the power supplies to the SSM2518. If the supply voltages fall below the nominal operating threshold, this circuit stops the output and issues a reset. This ensures that no damage occurs due to low voltage operation and that no pops can occur under nearly any power removal condition.

MASTER AND BIT CLOCK

The SSM2518 requires an internal master clock to operate. This clock must run at a frequency between 2.048 MHz and 6.144 MHz, depending on the input sample rate, and it must be fully synchronous with the incoming audio data. This clock signal can be derived from either the MCLK or BCLK pin, depending on the configuration used.

If the MCLK pin is used, the internal clock is derived by either dividing, passing through, or doubling the external clock signal as required. The clock supplied to the MCLK pin can range from 2.048 MHz to 38.864 MHz. In this case, the external MCLK pin signal can run at various multiples of the audio sample rate (f_S). The relationship between the MCLK rate and the audio sample rate is determined by the master clock select (MCS) register setting, Bits[4:1] in Register 0x00. Table 11 provides a summary of the available options.

In addition, a bit clock must run at the same rate as the incoming audio data on the SDATA pin. This clock can be supplied to the BCLK pin, or it can be generated internally by dividing MCLK. In this case, when BCLK_GEN (Bit 7 of Register 0x03) is set, the logic level of the BCLK pin is used to select the audio interface BCLK rate. Tie the BCLK pin to DVDD for 16 clock cycles per channel; tie it to ground for 32 cycles per channel.

If the system bit clock is in the range of acceptable internal master clock frequencies (between 2.048 MHz and 6.144 MHz), then it can serve as both master clock and bit clock. Setting NO_BCLK (Bit 5 of Register 0x00) routes the signal on the

MCLK pin to serve as the internal bit clock as well. In this case, tie the BCLK pin to ground.

Once the SSM2518 has entered its power-down state, it is possible to gate the clocks to conserve system power. However, a valid master clock must be present for the audio amplifier to operate. It is best to use a low jitter clock (less than 1 ns peak-to-peak) to ensure the specified audio performance.

TYPICAL APPLICATION CIRCUIT

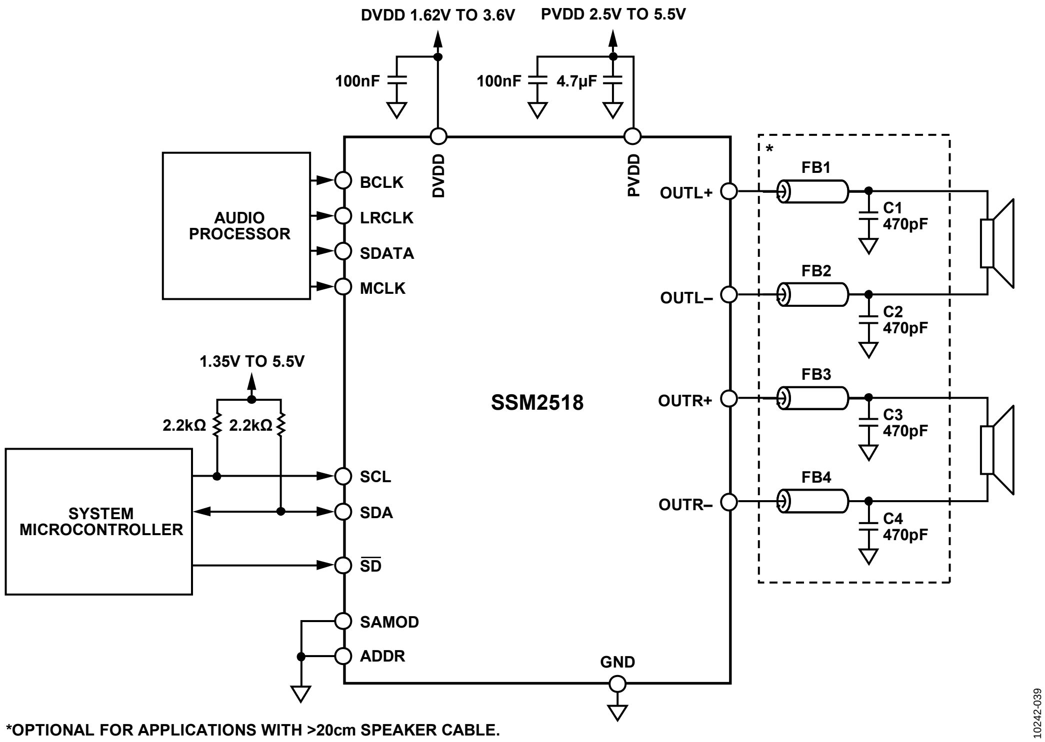

Figure 24. Typical Application Circuit Using I²C Configuration

DIGITAL AUDIO INTERFACE

The SSM2518 operates as a slave on the serial audio interface. It is capable of receiving stereo I²S-style, left justified, or right justified data. Mono, stereo, and multichannel PCM/TDM interface formats are available. The data format and interface style are selected by adjusting the SDATA_FMT and SAI fields in Register 0x02. Note that, when operating in right justified mode, the proper data width must be chosen. The function of the LRCLK pin varies depending on the data format. See Figure 26 through Figure 30 for the expected audio formats for various configurations.

CHANNEL MAPPING

Stereo audio formats and TDM formats with 2, 4, 8, or 16 channels are available. In these modes, the amplifier left and right audio can be independently chosen from any of the available channels using the two fields in Register 0x04. For most digital interface formats, many of these options are not present. For example, in stereo modes, only Channel 0 and Channel 1 are valid, and in four-slot TDM mode, only Channel 0, Channel 1, Channel 2, and Channel 3 are valid.

SAMPLE RATE DETECTION

The SSM2518 can be configured to automatically detect the sample rate, or the sample rate can be entered manually into the FS field (Bit 1 and Bit 0 of Register 0x02). The choice of automatic or manual sample rate detection is made by setting the ASR bit (Bit 0 of Register 0x01). Sample rate detection functions properly only when MCS (Bits[4:1] of Register 0x00) is set correctly.

STANDALONE MODE

When the SAMOD pin is pulled high, the SSM2518 can operate in several common stereo formats without any I²C control. Some details of the serial audio interface can be configured by tying the unused I²C pins to ground or DVDD, as shown in Table 10. In addition, the amplifier gain can be controlled via the ADDR pin.

Table 10. Standalone Mode Pin Functions

Pin	Standalone Function	Pin Options
SCL	FORMAT	Low: I²S
		High: left justified
SDA	MCLK_SEL	Low: MCLK = 256 × f_S
		High: MCLK = 384 × f_S
$\overline{SD}$	$\overline{SD}$	Low: shutdown/mute
		High: normal operation
ADDR	GAIN	Low: +12 dB digital gain
		High: 0 dB digital gain

In standalone mode, the volume control, dynamic range control, and EMI control features are disabled. Automatic sample rate detection and smart power-down are enabled. All other settings are set to their default values.

LOW POWER MODES

Two low power modes are available. If DAC_LPM (Bit 3 of Register 0x09) is set, the digital-to-analog converter (DAC) runs at half speed, reducing the quiescent current. This half speed mode is also active when the MCS setting (Bits[4:1] of Register 0x00) is set to its lowest value (MCS = 0000) because the slowest acceptable MCLK rates can only support half speed DAC operation.

If AMP_LPM (Bit 4 of Register 0x09) is set, the Σ-Δ modulator runs in a special mode that offers lower quiescent current when the output power is small, at the expense of slightly degraded audio performance.

DYNAMIC RANGE CONTROL

The dynamic range control, or DRC, can be used to reduce the dynamic range of the audio signal. A common DRC scheme involves applying a gain reduction to large output signals, along with a net increase in gain for moderate to small signals. The qualitative result is a louder speaker output for moderate output levels without the undesired effects of amplifier clipping or speaker overdrive at high levels.

To calculate the gain adjustment, an rms detector gives the average level of the input signal, based on the averaging time set by RMS_TAV (Bits[3:0] in Register 0x12). Based on this time averaged level, the overall gain is adjusted so that the input/output characteristic matches the specified compression curve. This curve can be represented by a log-to-log graph with five distinct regions, as shown in Figure 25.

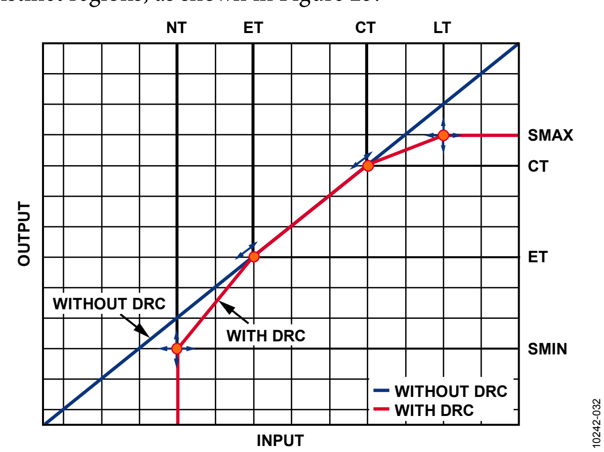

Figure 25. DRC Compression Curve: Log-to-Log Representation of the DRC Output Level vs. Input Level

From bottom left to top right, these regions (shown in red) are the noise gate, expander, linear region, compressor, and limiter. The control points between these regions can be set using the

DRC control registers (Register 0x0A through Register 0x12) using the variable names (CT, ET, and so forth) as shown on the plot axes in Figure 25. Each element can be individually enabled using the LIM_EN, COMP_EN, EXP_EN, and NG_EN bits in

Register 0x0A. The entire DRC function can be enabled or disabled using DRC_EN (Bits[1:0] of Register 0x0A).

Linear Region

For input amplitudes between the DRC_ET and DRC_CT thresholds, the DRC attenuation is set to zero, that is, the input is passed straight through to the output. This is the region in the center of the compression curve (see Figure 25) with a 1:1 slope, where the input and output amplitude are the same.

Compressor

Above the input level set by DRC_CT (Bits[3:0] of Register 0x0C), the output amplitude does not rise as quickly as the input. This provides a smooth transition to the limiter region, where the output stops increasing altogether at the input level set by DRC_LT (Bits[7:4] of Register 0x0C). At this point, the output level is DRC_SMAX (Bits[7:4] of Register 0x0E).

Limiter

When the input level is above the input level set by DRC_LT, the output level does not exceed the level given by DRC_SMAX (Bits[7:4] of Register 0x0E). Instead, the overall gain is reduced to maintain that level without clipping.

Expander

When the expander is enabled and the input level falls below the level set by DRC_ET (Bits[7:4] of Register 0x0D), the output level begins to decrease more rapidly than the input. This provides a smooth transition to the noise gate, where sufficiently small signals are blocked completely.

When the input signal falls to the level set by DRC_NT (Bits[3:0] of Register 0x0D), the output level is set by DRC_SMIN (Bits[3:0] of Register 0x0E).

Noise Gate

When the noise gate is enabled and the input signal level falls below the threshold set by DRC_NT for a period of time, the output is set to zero. Set this at a level lower than all signals of interest to block the output in periods of silence.

The period of time for which the input level must remain below the noise gate threshold prior to the output setting to zero is determined by HDT_NG, Bits[3:0] of Register 0x10.

Attack and Decay Rates

To prevent audible distortion effects as the gain changes, the time constants for the attack (gain reduction) and decay (gain increase) are adjustable. The attack time is set by DRC_ATT (Bits[7:4] of Register 0x0F), and the decay time is set by DRC_DEC (Bits[3:0] of Register 0x0F).

Between attack and decay, a hold time is used to prevent rapid switching between increased gain and decreased gain. The hold time is set by HDT_NOR (Bits[7:4] of Register 0x10).

Post-DRC Gain

Because the DRC feature may have an overall effect on the system gain, a separate digital gain option is provided to allow the user to compensate for this effect. This digital gain option is independent of the volume control feature, allowing an overall gain adjustment that remains separate from the volume settings. This level is set by DRC_POST_G (Bits[5:2] of Register 0x11).

Depending on the application, the entire DRC block can be placed before or after the volume controls (L_VOL and R_VOL). This option is set by PRE_VOL (Bit 6 of Register 0x0A).

MUTE OPTIONS

Several mute options are available. Each channel can be muted independently using the left channel mute (L_MUTE, Bit 1 of Register 0x07) or the right channel mute (R_MUTE, Bit 2 of Register 0x07). Alternatively, both channels can be muted simultaneously using the master mute option (M_MUTE, Bit 0 of Register 0x07).

The master mute is enabled at system startup; therefore, it must be disabled before any audio is produced.

The SSM2518 also contains an automatic mute feature. This feature is enabled by setting AMUTE (Bit 7 of Register 0x07). When active, this feature monitors the incoming digital audio signal. When the data stream is zero for 2048 consecutive frames (1024 stereo samples), the output is muted. When a single nonzero input is received on the I^2S interface, the SSM2518 is unmuted and resumes normal operation.

VOLUME CONTROL

The SSM2518 has a digital volume control that allows independent control of the left and right channels via Registers 0x05 and 0x06, respectively. 255 levels are available, providing a range from +24 dB to −71.25 dB in 0.375 dB increments. This is a soft volume control, meaning that the gain is adjusted continuously from one value to another. This continuously adjusted gain prevents the audible pop that occurs with an instantaneous gain adjustment.

When VOL_LINK (Bit 3 in Register 0x07) is set, both channels are linked to the left channel volume setting.

DE-EMPHASIS FILTER

A digital de-emphasis filter is provided to compensate for the standard compact disc style preemphasis, which occurs in some audio systems. This filter is designed for use with a 44.1 kHz sample rate only. To enable the de-emphasis filter, set DEEMP_EN (Bit 4 of Register 0x07).

ANALOG GAIN

The analog gain of the SSM2518 amplifier is set by ANA_GAIN (Bit 5 of Register 0x07). Each gain setting is designed to match the scaling needed for a specified PVDD voltage so that the digital full-scale values correspond to the clipping points of the amplifier at that voltage.

If PVDD is larger than the voltage specified in this register, the digital scale does not fill the output voltage range and maximum output power is reduced. Similarly, if PVDD is smaller than specified in this register, analog clipping may occur within the range of possible digital codes.

FAULT DETECTION AND RECOVERY

Three fault conditions are detected by the SSM2518 fault detection system: left channel overcurrent, right channel overcurrent, and overtemperature. When any of these is detected, the amplifier shuts down and a read-only I^2C bit is set to indicate the cause of the shutdown. The OC_L, OC_R, and OT fault indicators are Bit 7, Bit 6, and Bit 5 (respectively) of Register 0x08.

An autorecovery feature can be enabled for temperature faults, current faults, or both, depending on the state of ARCV (Bit 1 and Bit 0 of Register 0x08).

If autorecovery is enabled, the amplifier waits a short time (10 ms, 20 ms, 40 ms, or 80 ms) and attempts to recover. The recovery delay is set by AR_TIME (Bit 7 and Bit 6 of Register 0x09). The maximum number of consecutive recovery attempts can be set to one, three, seven, or unlimited attempts; this number is set by MAX_AR (Bit 3 and Bit 2 of Register 0x08).

If the autorecovery feature is disabled or the maximum number of attempts has been reached, the amplifier remains shut down until a software reset or manual fault recovery attempt occurs. The manual fault recovery is triggered by setting the write-only bit, MRCV (Bit 4 of Register 0x08).

DIGITAL AUDIO FORMATS

STEREO MODE

SAI = 0

SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)

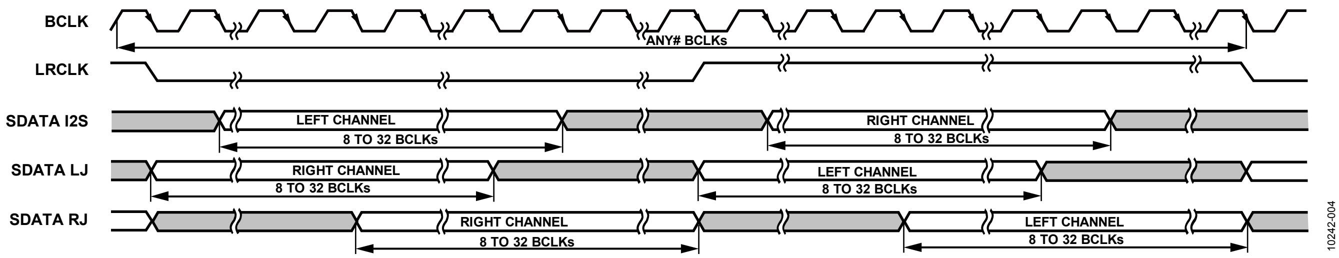

Figure 26. Stereo Modes: I^2S, Left Justified, and Right Justified

TDM, 50% DUTY CYCLE MODE

SAI = 1 (2 slots), 2 (4 slots), 3 (8 slots), 4 (16 slots)

SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)

BCLK_EDGE = 0

LRCLK_MODE = 0

SLOT_WIDTH = 0 (32 BCLKs), 1 (24 BCLKs), 2 (16 BCLKs)

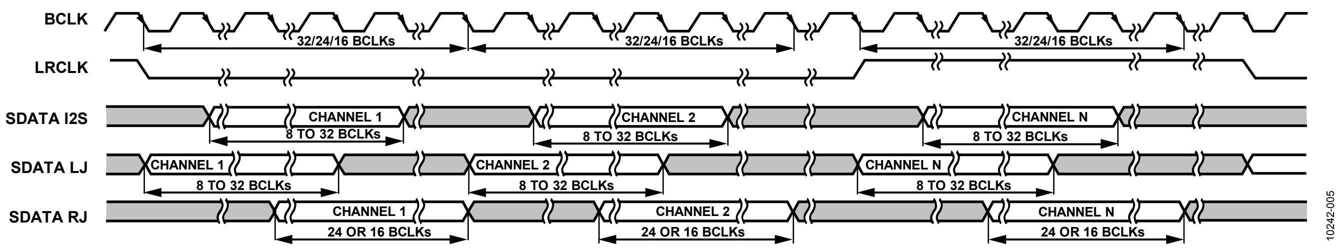

Figure 27. TDM Modes with 50% Duty Cycle LRCLK

TDM, PULSE MODE

SAI = 1 (2 slots), 2 (4 slots), 3 (8 slots), 4 (16 slots)

SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)

BCLK_EDGE = 0

LRCLK_MODE = 1

SLOT_WIDTH = 0 (32 BCLKs), 1 (24 BCLKs), 2 (16 BCLKs)

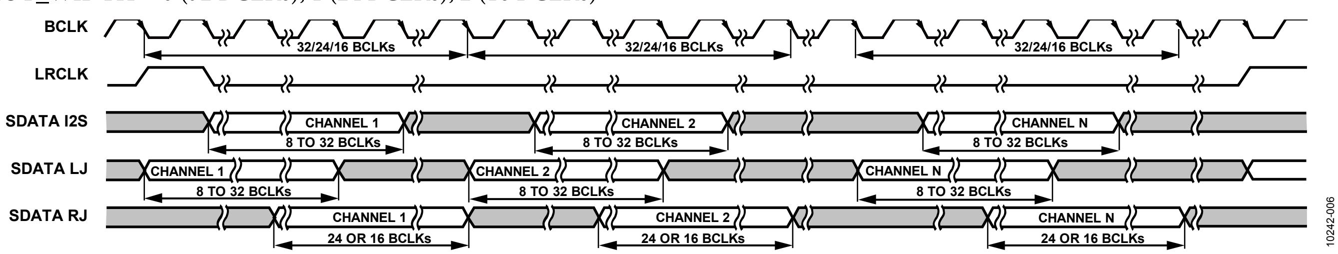

Figure 28. TDM Modes with Pulse Mode LRCLK

PCM, MULTICHANNEL MODE

SAI = 1 (2 channels), 2 (4 channels), 3 (8 channels), 4 (16 channels)
SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)
BCLK_EDGE = 1
LRCLK_MODE = 1
SLOT_WIDTH = 0 (32 BCLKs), 1 (24 BCLKs), 2 (16 BCLKs)

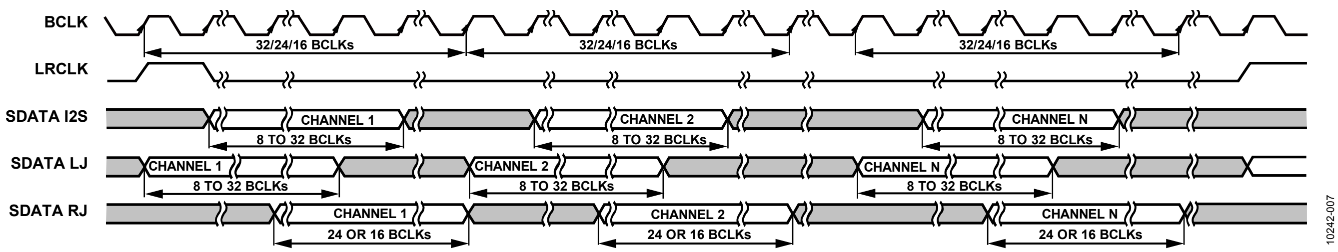

Figure 29. Multichannel PCM Modes

PCM MONO MODE

SAI = 5
SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)
BCLK_EDGE = 1
LRCLK_MODE = 1

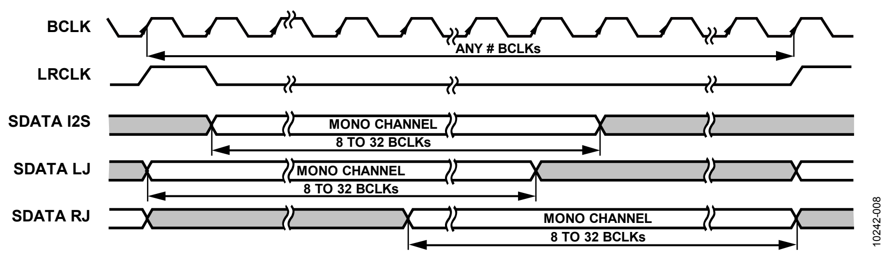

Figure 30. Mono PCM Modes

I²C CONFIGURATION INTERFACE

OVERVIEW

The SSM2518 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the SSM2518 and the system I²C master controller. The SSM2518 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique device address. The device address byte format is shown in Figure 31. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation.

Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. The full byte addresses are shown in Figure 3, where the subaddresses are automatically incremented at word boundaries and can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single word write unless a stop condition is encountered. A data transfer is always terminated by a stop condition.

Both SDA and SCL should have a 2.2 kΩ pull-up resistor on the lines connected to them.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
0	1	1	0	1	ADDR	0	$R/\overline{W}$

10242-033

Figure 31. I²C Device Address Byte Format

Addressing

Initially, each device on the I²C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the $R/\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. The device address is determined by the state of the ADDR pin. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The $R/\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I²C port is shown in Figure 3.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the SSM2518 immediately jumps to the idle condition. During a given SCL high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the SSM2518 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the SSM2518 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse of SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the SSM2518, and the part returns to the idle condition.

I²C Read and Write Operations

Figure 33 shows the timing of a single word write operation. Every ninth clock, the SSM2518 issues an acknowledge by pulling SDA low.

Figure 34 shows the timing of a burst mode write sequence. This figure shows an example where the target destination registers are two bytes. The SSM2518 knows to increment its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single word read operation is shown in Figure 35. Note that the first $R/\overline{W}$ bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the SSM2518 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the $R/\overline{W}$ bit set to 1 (read). This causes the SSM2518 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the SSM2518.

Figure 36 shows the timing of a burst mode read sequence. This figure shows an example where the target destination registers are two bytes. The SSM2518 knows to increment its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

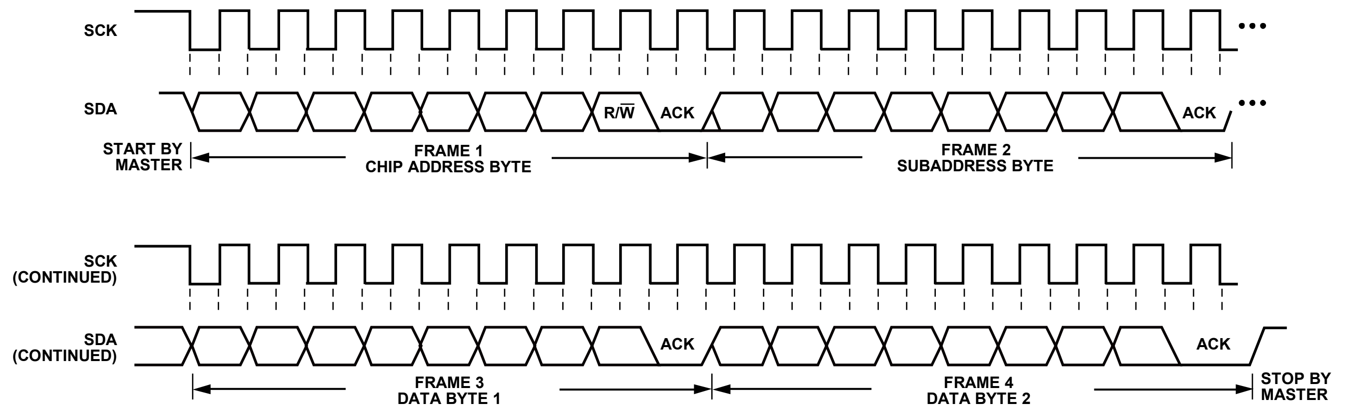

Figure 32. I²C Read/Write Timing

START BIT	CHIP ADDRESS (7 BITS)	R/$\overline{W}$ = 0	ACK BY SLAVE	SUBADDRESS (8 BITS)	ACK BY SLAVE	DATA BYTE 1 (8 BITS)	STOP BIT

10242-035

Figure 33. Single-Word I²C Write Format

START BIT	CHIP ADDRESS R/$\overline{W}$ = 0	ACK BY SLAVE	SUBADDRESS	ACK BY SLAVE	DATA-WORD 1	ACK BY SLAVE	DATA-WORD 2	ACK BY SLAVE	• • •	STOP BIT

10242-036

Figure 34. Burst Mode I²C Write Format

START BIT	CHIP ADDRESS R/$\overline{W}$ = 0	ACK BY SLAVE	SUBADDRESS	ACK BY SLAVE	START BIT	CHIP ADDRESS R/$\overline{W}$ = 1	ACK BY SLAVE	DATA BYTE 1	NO ACK	STOP BIT

10242-037

Figure 35. Single-Word I²C Read Format

START BIT	CHIP ADDRESS R/$\overline{W}$ = 0	ACK BY SLAVE	SUBADDRESS	ACK BY SLAVE	START BIT	CHIP ADDRESS R/$\overline{W}$ = 1	ACK BY SLAVE	DATA-WORD 1	ACK BY MASTER	• • •	STOP BIT

10242-038

Figure 36. Burst Mode I²C Read Format

MCLK Frequency Settings

Table 11. MCS Bit Field Setting: MCLK, Ratio, and Frequency

Input Sample Rate		Setting 0 b0000[1]	Setting 1 b0001	Setting 2 b0010	Setting 3 b0011	Setting 4 b0100	Setting 5 b0101	Setting 6 b0110	Setting 7 b0111	Setting 8 b1000
8 kHz	Ratio	$256 \times f_S$	$512 \times f_S$	$1024 \times f_S$	$1536 \times f_S$	$2048 \times f_S$	$3072 \times f_S$	$400 \times f_S$	$800 \times f_S$	$1600 \times f_S$
	MCLK	2.048 MHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	24.576 MHz	3.20 MHz	6.40 MHz	12.80 MHz
11.025 kHz	Ratio	$256 \times f_S$	$512 \times f_S$	$1024 \times f_S$	$1536 \times f_S$	$2048 \times f_S$	$3072 \times f_S$	$400 \times f_S$	$800 \times f_S$	$1600 \times f_S$
	MCLK	2.822 MHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz	4.41 MHz	8.82 MHz	17.64 MHz
12 kHz	Ratio	$256 \times f_S$	$512 \times f_S$	$1024 \times f_S$	$1536 \times f_S$	$2048 \times f_S$	$3072 \times f_S$	$400 \times f_S$	$800 \times f_S$	$1600 \times f_S$
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz
16 kHz	Ratio	$128 \times f_S$	$256 \times f_S$	$384 \times f_S$	$768 \times f_S$	$1024 \times f_S$	$1536 \times f_S$	$200 \times f_S$	$400 \times f_S$	$800 \times f_S$
	MCLK	2.048 MHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	24.576 MHz	3.20 MHz	6.40 MHz	12.80 MHz
22.05 kHz	Ratio	$128 \times f_S$	$256 \times f_S$	$512 \times f_S$	$768 \times f_S$	$1024 \times f_S$	$1536 \times f_S$	$200 \times f_S$	$400 \times f_S$	$800 \times f_S$
	MCLK	2.822 MHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz	4.41 MHz	8.82 MHz	17.64 MHz
24 kHz	Ratio	$128 \times f_S$	$256 \times f_S$	$512 \times f_S$	$768 \times f_S$	$1024 \times f_S$	$1536 \times f_S$	$200 \times f_S$	$400 \times f_S$	$800 \times f_S$
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz
32 kHz	Ratio	$64 \times f_S$	$128 \times f_S$	$256 \times f_S$	$384 \times f_S$	$512 \times f_S$	$768 \times f_S$	$100 \times f_S$	$200 \times f_S$	$400 \times f_S$
	MCLK	2.048 MHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	24.576 MHz	3.20 MHz	6.40 MHz	12.80 MHz
44.1 kHz	Ratio	$64 \times f_S$	$128 \times f_S$	$256 \times f_S$	$384 \times f_S$	$512 \times f_S$	$768 \times f_S$	$100 \times f_S$	$200 \times f_S$	$400 \times f_S$
	MCLK	2.822 MHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz	4.41 MHz	8.82 MHz	17.64 MHz
48 kHz	Ratio	$64 \times f_S$	$128 \times f_S$	$256 \times f_S$	$384 \times f_S$	$512 \times f_S$	$768 \times f_S$	$100 \times f_S$	$200 \times f_S$	$400 \times f_S$
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz
96 kHz	Ratio	$64 \times f_S$	$64 \times f_S$	$128 \times f_S$	$192 \times f_S$	$256 \times f_S$	$384 \times f_S$	$50 \times f_S$	$100 \times f_S$	$200 \times f_S$
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz

[1] When using MCS = 0000, the chip automatically operates in low power mode.

REGISTER SUMMARY (REG_MAP)

Table 12. REG_MAP Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	Reset_Power_Control	[7:0]	S_RST	RESERVED	NO_BCLK	MCS				SPWDN	0x05	RW
0x01	Edge_Clock_Control	[7:0]	RESERVED					EDGE		ASR	0x00	RW
0x02	Serial_Interface_Sample_Rate_Control	[7:0]	RESERVED	SDATA_FMT		SAI			FS		0x02	RW
0x03	Serial_Interface_Control	[7:0]	BCLK_GEN	LRCLK_MODE	LRCLK_POL	SAI_MSB	SLOT_WIDTH		BCLK_EDGE	RESERVED	0x00	RW
0x04	Channel_Mapping_Control	[7:0]	CH_SEL_R				CH_SEL_L				0x10	RW
0x05	Left_Volume_Control	[7:0]	L_VOL								0x40	RW
0x06	Right_Volume_Control	[7:0]	R_VOL								0x40	RW
0x07	Volume_Mute_Control	[7:0]	AMUTE	RESERVED	ANA_GAIN	DEEMP_EN	VOL_LINK	R_MUTE	L_MUTE	M_MUTE	0x81	RW
0x08	Fault_Control_1	[7:0]	OC_L	OC_R	OT	MRCV	MAX_AR		ARCV		0x0C	RW
0x09	Power_Fault_Control	[7:0]	AR_TIME		RESERVED	AMP_LPM	DAC_LPM	R_PWDN	L_PWDN	APWDN_EN	0x99	RW
0x0A	DRC_Control_1	[7:0]	RESERVED	PRE_VOL	LIM_EN	COMP_EN	EXP_EN	NG_EN	DRC_EN		0x7C	RW
0x0B	DRC_Control_2	[7:0]	PEAK_ATT				PEAK_REL				0x5B	RW
0x0C	DRC_Control_3	[7:0]	DRC_LT				DRC_CT				0x57	RW
0x0D	DRC_Control_4	[7:0]	DRC_ET				DRC_NT				0x89	RW
0x0E	DRC_Control_5	[7:0]	DRC_SMAX				DRC_SMIN				0x8C	RW
0x0F	DRC_Control_6	[7:0]	DRC_ATT				DRC_DEC				0x77	RW
0x10	DRC_Control_7	[7:0]	HDT_NOR				HDT_NG				0x26	RW
0x11	DRC_Control_8	[7:0]	RESERVED		DRC_POST_G				RESERVED		0x1C	RW
0x12	DRC_Control_9	[7:0]	RESERVED				RMS_TAV				0x07	RW

REGISTER (REG_MAP) DETAILS

SOFTWARE RESET AND MASTER SOFTWARE POWER-DOWN CONTROL REGISTER

Address: 0x00, Reset: 0x05, Name: Reset_Power_Control

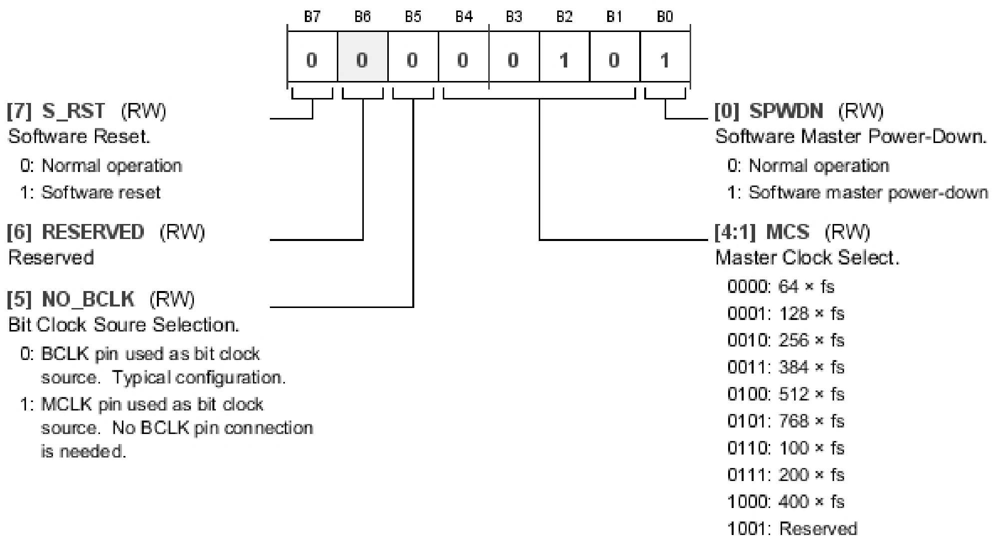

Table 13. Bit Descriptions for Reset_Power_Control

Bits	Bit Name	Settings	Description	Reset	Access
7	S_RST		Software Reset. Write 1 to reset all internal blocks, including I²C registers, to their initial state.	0x0	RW
		0	Normal operation		
		1	Software reset		
6	RESERVED		Reserved.	0x0	RW
5	NO_BCLK		Bit Clock Source Selection. Either the MCLK or BCLK pin can be routed internally to the bit clock.	0x0	RW
		0	BCLK pin used as bit clock source. Typical configuration.		
		1	MCLK pin used as bit clock source. No BCLK pin connection is needed.		
[4:1]	MCS		Master Clock Select. This must match the ratio between the input MCLK frequency and the audio sample rate, as shown in Table 11.	0x2	RW
		0000	$64 \times f_S$		
		0001	$128 \times f_S$		
		0010	$256 \times f_S$		
		0011	$384 \times f_S$		
		0100	$512 \times f_S$		
		0101	$768 \times f_S$		
		0110	$100 \times f_S$		
		0111	$200 \times f_S$		
		1000	$400 \times f_S$		
		1001	Reserved		
0	SPWDN		Software Master Power-Down. This places all blocks, except the I²C interface, into a low power state.	0x1	RW
		0	Normal operation		
		1	Software master power-down		

EDGE SPEED AND CLOCKING CONTROL REGISTER

Address: 0x01, Reset: 0x00, Name: Edge_Clock_Control

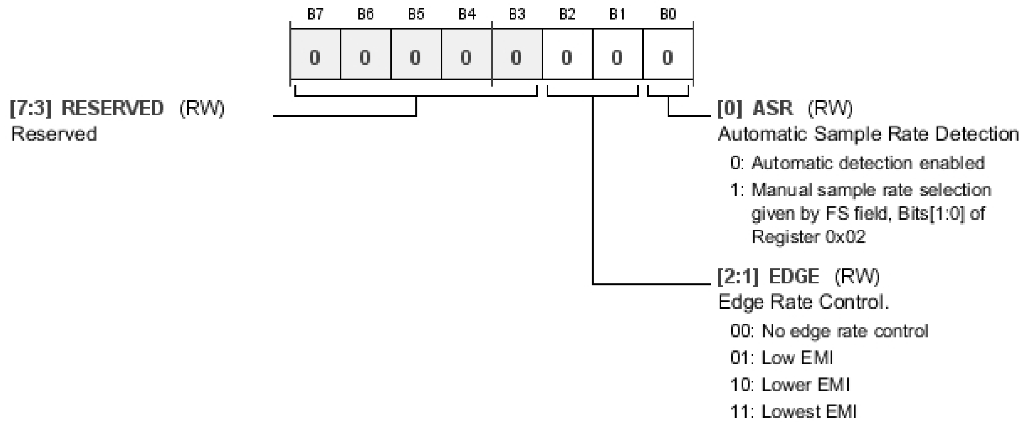

Table 14. Bit Descriptions for Edge_Clock_Control

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x00	RW
[2:1]	EDGE		Edge Rate Control. This limits the edge rate of the switching output stage. The low EMI operation modes reduce the edge speed, lowering EMI and power efficiency.	0x0	RW
		00	No edge rate control		
		01	Low EMI		
		10	Lower EMI		
		11	Lowest EMI		
0	ASR		Automatic Sample Rate Detection.	0x0	RW
		0	Automatic detection enabled		
		1	Manual sample rate selection given by FS field, Bits[1:0] of Register 0x02		

SERIAL AUDIO INTERFACE AND SAMPLE RATE CONTROL REGISTER

Address: 0x02, Reset: 0x02, Name: Serial_Interface_Sample_Rate_Control

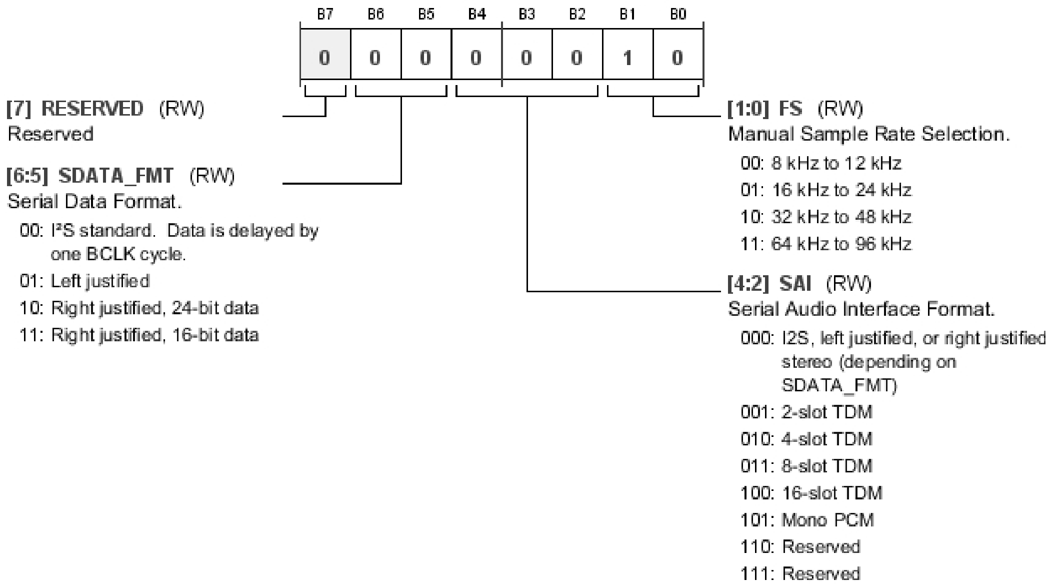

Table 15. Bit Descriptions for Serial_Interface_Sample_Rate_Control

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:5]	SDATA_FMT		Serial Data Format. Only required if SAI = 000.	0x0	RW
		00	I²S standard; data is delayed by one BCLK cycle		
		01	Left justified		
		10	Right justified, 24-bit data		
		11	Right justified, 16-bit data		
[4:2]	SAI		Serial Audio Interface Format.	0x0	RW
		000	I²S, left justified, or right justified stereo (depending on SDATA_FMT)		
		001	2-slot TDM		
		010	4-slot TDM		
		011	8-slot TDM		
		100	16-slot TDM		
		101	Mono PCM		
		110	Reserved		
		111	Reserved		
[1:0]	FS		Manual Sample Rate Selection. Only required if ASR = 1 in Register 0x01.	0x2	RW
		00	8 kHz to 12 kHz		
		01	16 kHz to 24 kHz		
		10	32 kHz to 48 kHz		
		11	64 kHz to 96 kHz		

SERIAL AUDIO INTERFACE CONTROL REGISTER

Address: 0x03, Reset: 0x00, Name: Serial_Interface_Control

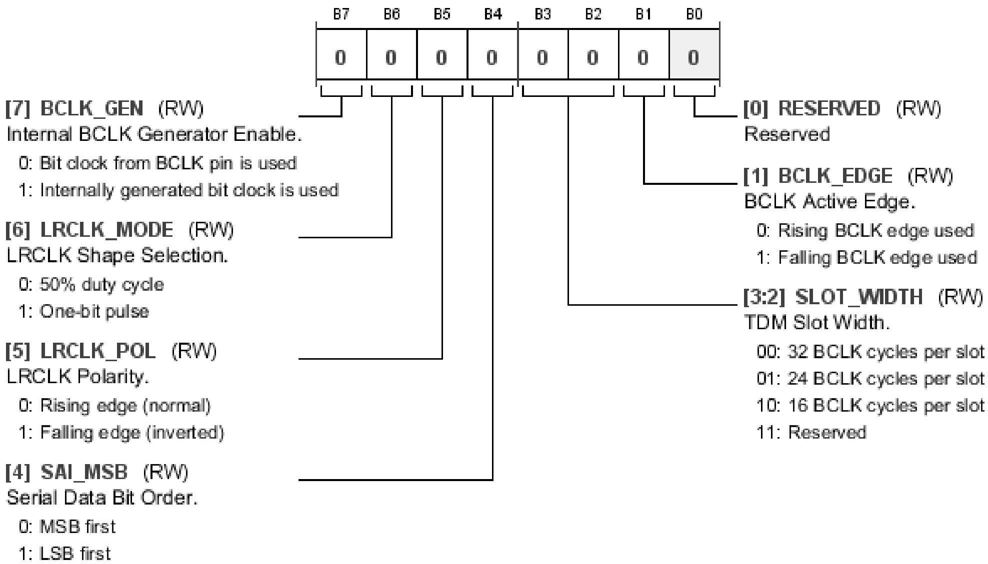

Table 16. Bit Descriptions for Serial_Interface_Control

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLK_GEN		Internal BCLK Generator Enable.	0x0	RW
		0	Bit clock from BCLK pin is used		
		1	Internally generated bit clock is used		
6	LRCLK_MODE		LRCLK Shape Selection. Required only for TDM modes.	0x0	RW
		0	50% duty cycle		
		1	1-bit pulse		
5	LRCLK_POL		LRCLK Polarity.	0x0	RW
		0	Rising edge (normal)		
		1	Falling edge (inverted)		
4	SAI_MSB		Serial Data Bit Order.	0x0	RW
		0	MSB first		
		1	LSB first		
[3:2]	SLOT_WIDTH		TDM Slot Width. Required only for TDM modes.	0x0	RW
		00	32 BCLK cycles per slot		
		01	24 BCLK cycles per slot		
		10	16 BCLK cycles per slot		
		11	Reserved		
1	BCLK_EDGE		BCLK Active Edge.	0x0	RW
		0	Rising BCLK edge used		
		1	Falling BCLK edge used		
0	RESERVED		Reserved.	0x0	RW

CHANNEL MAPPING CONTROL REGISTER

Address: 0x04, Reset: 0x10, Name: Channel_Mapping_Control

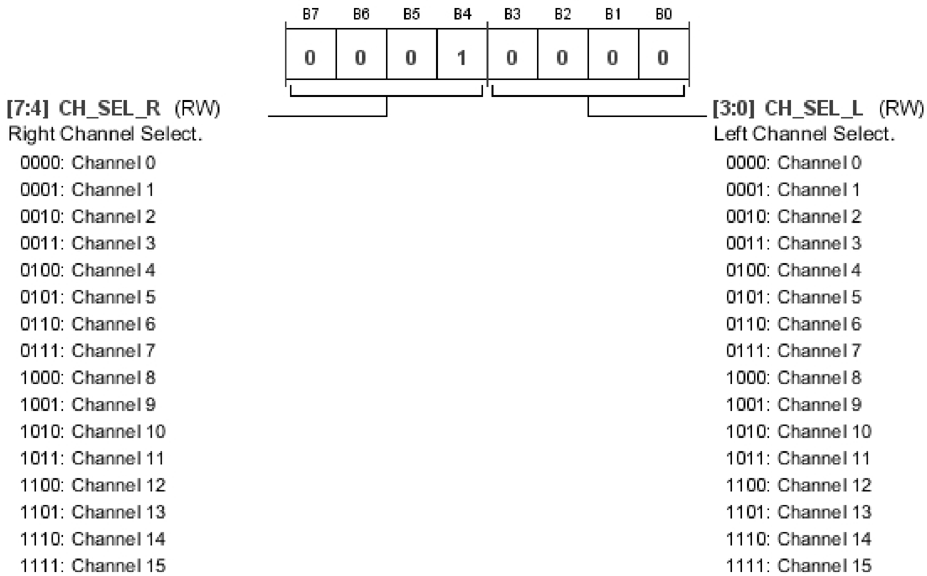

Table 17. Bit Descriptions for Channel_Mapping_Control

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CH_SEL_R		Right Channel Select. Channel 0 valid when running in mono (PCM) mode.	0x1	RW
			Channel 0 to Channel 1 valid when running in stereo and 2-slot TDM modes.		
			Channel 0 to Channel 3 valid when running in 4-slot TDM mode.		
			Channel 0 to Channel 7 valid when running in 8-slot TDM mode.		
			Channel 0 to Channel 15 valid when running in 16-slot TDM mode.		
		0000	Channel 0		
		0001	Channel 1		
		0010	Channel 2		
		0011	Channel 3		
		0100	Channel 4		
		0101	Channel 5		
		0110	Channel 6		
		0111	Channel 7		
		1000	Channel 8		
		1001	Channel 9		
		1010	Channel 10		
		1011	Channel 11		
		1100	Channel 12		
		1101	Channel 13		
		1110	Channel 14		
		1111	Channel 15		
[3:0]	CH_SEL_L		Left Channel Select. Channel 0 valid when running in mono (PCM) mode.	0x0	RW
			Channel 0 to Channel 1 valid when running in stereo and 2-slot TDM modes.		
			Channel 0 to Channel 3 valid when running in 4-slot TDM mode.		
			Channel 0 to Channel 7 valid when running in 8-slot TDM mode.		
			Channel 0 to Channel 15 valid when running in 16-slot TDM mode.		
		0000	Channel 0		
		0001	Channel 1		

Bits	Bit Name	Settings	Description	Reset	Access
		0010	Channel 2		
		0011	Channel 3		
		0100	Channel 4		
		0101	Channel 5		
		0110	Channel 6		
		0111	Channel 7		
		1000	Channel 8		
		1001	Channel 9		
		1010	Channel 10		
		1011	Channel 11		
		1100	Channel 12		
		1101	Channel 13		
		1110	Channel 14		
		1111	Channel 15		

LEFT CHANNEL VOLUME CONTROL REGISTER

Address: 0x05, Reset: 0x40, Name: Left_Volume_Control

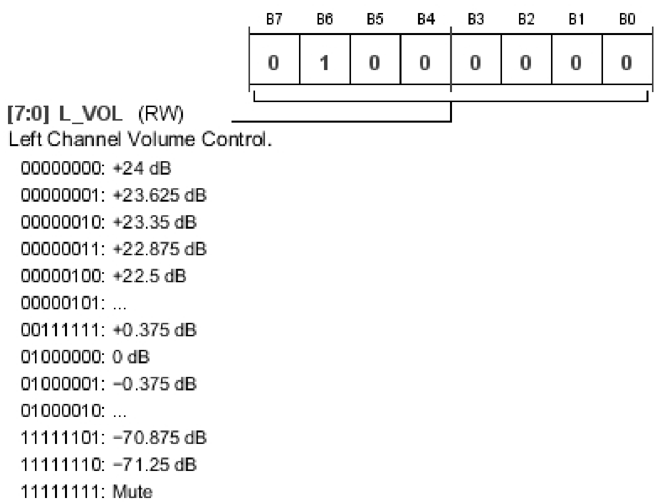

Table 18. Bit Descriptions for Left_Volume_Control

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	L_VOL		Left Channel Volume Control. Adjusts the digital gain in 0.375 dB increments.	0x40	RW
		00000000	+24 dB		
		00000001	+23.625 dB		
		00000010	+23.35 dB		
		00000011	+22.875 dB		
		00000100	+22.5 dB		
		00000101	+22.125 dB		
		…	…		
		00111111	+0.375 dB		
		01000000	0 dB		
		01000001	−0.375 dB		
		01000010	−0.750 dB		
		…	…		
		11111101	−70.875 dB		
		11111110	−71.25 dB		
		11111111	Mute		

RIGHT CHANNEL VOLUME CONTROL REGISTER

Address: 0x06, Reset: 0x40, Name: Right_Volume_Control

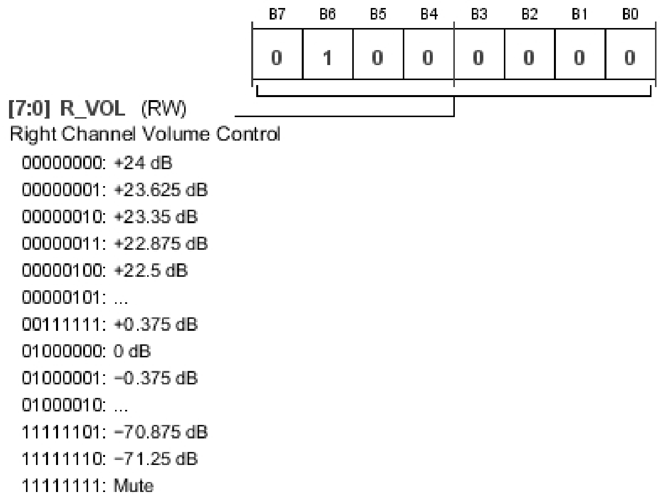

Table 19. Bit Descriptions for Right_Volume_Control

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	R_VOL		Right Channel Volume Control. Adjusts the digital gain in 0.375 dB increments.	0x40	RW
		00000000	+24 dB		
		00000001	+23.625 dB		
		00000010	+23.35 dB		
		00000011	+22.875 dB		
		00000100	+22.5 dB		
		00000101	+22.125 dB		
		…	…		
		00111111	+0.375 dB		
		01000000	0 dB		
		01000001	−0.375 dB		
		01000010	−0.750 dB		
		…	…		
		11111101	−70.875 dB		
		11111110	−71.25 dB		
		11111111	Mute		

VOLUME AND MUTE CONTROL REGISTER

Address: 0x07, Reset: 0x81, Name: Volume_Mute_Control

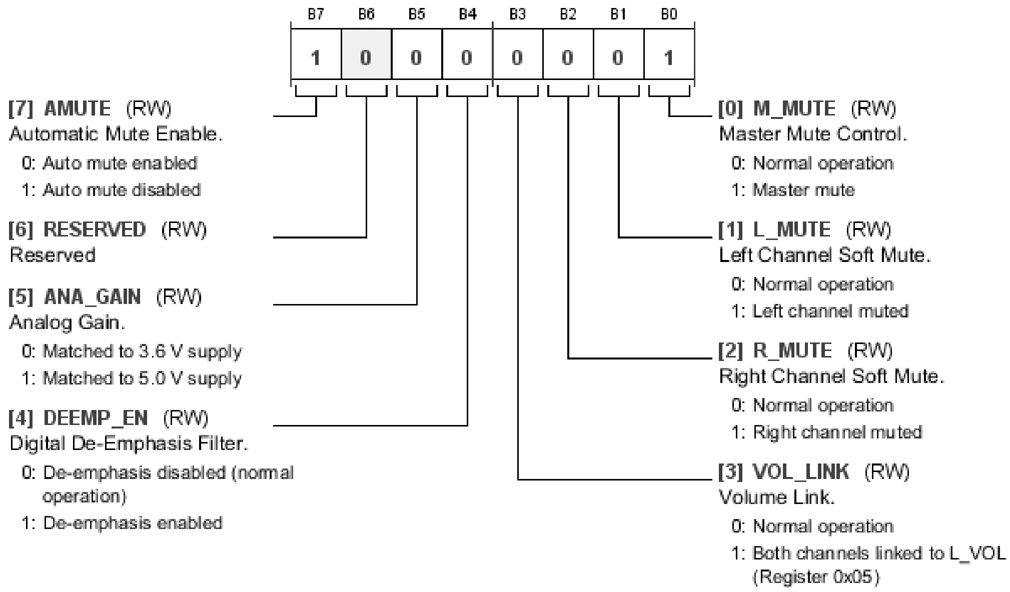

Table 20. Bit Descriptions for Volume_Mute_Control

Bits	Bit Name	Settings	Description	Reset	Access
7	AMUTE		Automatic Mute Enable. After 2048 slots (1024 stereo samples) have been received with zero data, the outputs mute until nonzero data arrives.	0x1	RW
		0	Automute enabled		
		1	Automute disabled		
6	RESERVED		Reserved.	0x0	RW
5	ANA_GAIN		Analog Gain. This sets the full-scale output level of the amplifier. The two settings are scaled appropriately for 3.6 V and 5.0 V nominal supply voltages.	0x0	RW
		0	Matched to 3.6 V supply		
		1	Matched to 5.0 V supply		
4	DEEMP_EN		Digital De-Emphasis Filter.	0x0	RW
		0	De-emphasis disabled (normal operation)		
		1	De-emphasis enabled		
3	VOL_LINK		Volume Link. When this bit is enabled, both channels respond to the left channel volume register.	0x0	RW
		0	Normal operation		
		1	Both channels linked to L_VOL (Register 0x05)		
2	R_MUTE		Right Channel Soft Mute.	0x0	RW
		0	Normal operation		
		1	Right channel muted		
1	L_MUTE		Left Channel Soft Mute.	0x0	RW
		0	Normal operation		
		1	Left channel muted		
0	M_MUTE		Master Mute Control. This bit soft mutes both channels.	0x1	RW
		0	Normal operation		
		1	Master mute		

FAULT CONTROL 1 REGISTER

Address: 0x08, Reset: 0x0C, Name: Fault_Control_1

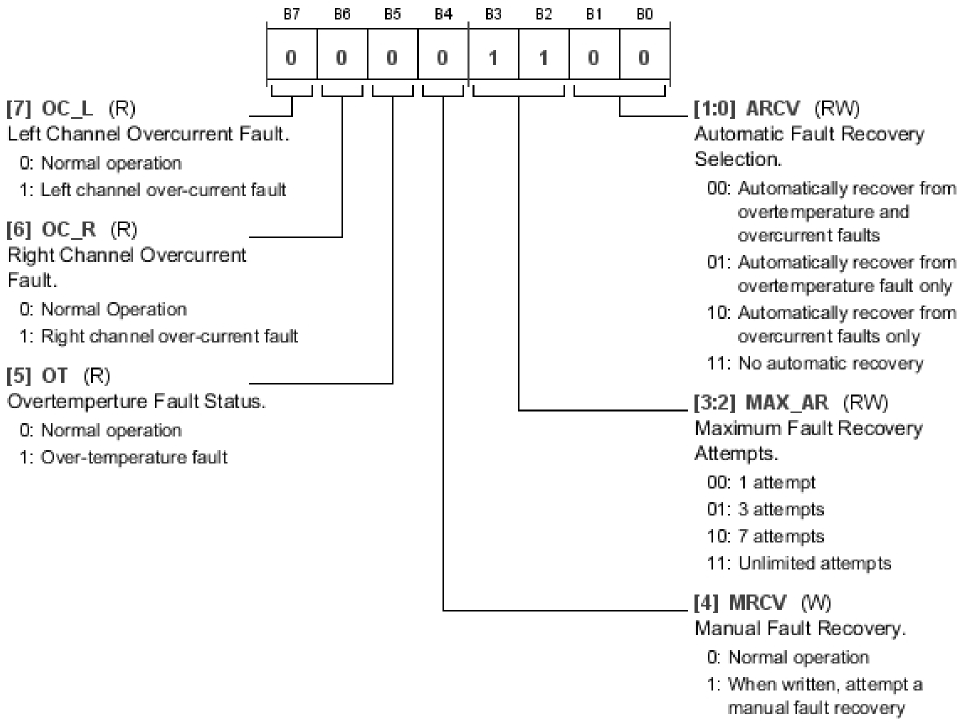

Table 21. Bit Descriptions for Fault_Control_1

Bits	Bit Name	Settings	Description	Reset	Access
7	OC_L		Left Channel Overcurrent Fault. Read only.	0x0	R
		0	Normal operation		
		1	Left channel overcurrent fault		
6	OC_R		Right Channel Overcurrent Fault. Read only.	0x0	R
		0	Normal operation		
		1	Right channel overcurrent fault		
5	OT		Overtemperature Fault Status. Read only.	0x0	R
		0	Normal operation		
		1	Overtemperature fault		
4	MRCV		Manual Fault Recovery. Available only when ARCV = 11. Write only.	0x0	W
		0	Normal operation		
		1	When written, attempt a manual fault recovery		
[3:2]	MAX_AR		Maximum Fault Recovery Attempts.	0x3	RW
		00	One attempt		
		01	Three attempts		
		10	Seven attempts		
		11	Unlimited attempts		
[1:0]	ARCV		Automatic Fault Recovery Selection.	0x0	RW
		00	Automatically recover from overtemperature and overcurrent faults		
		01	Automatically recover from overtemperature fault only		
		10	Automatically recover from overcurrent faults only		
		11	No automatic recovery		

POWER AND FAULT CONTROL REGISTER

Address: 0x09, Reset: 0x99, Name: Power_Fault_Control

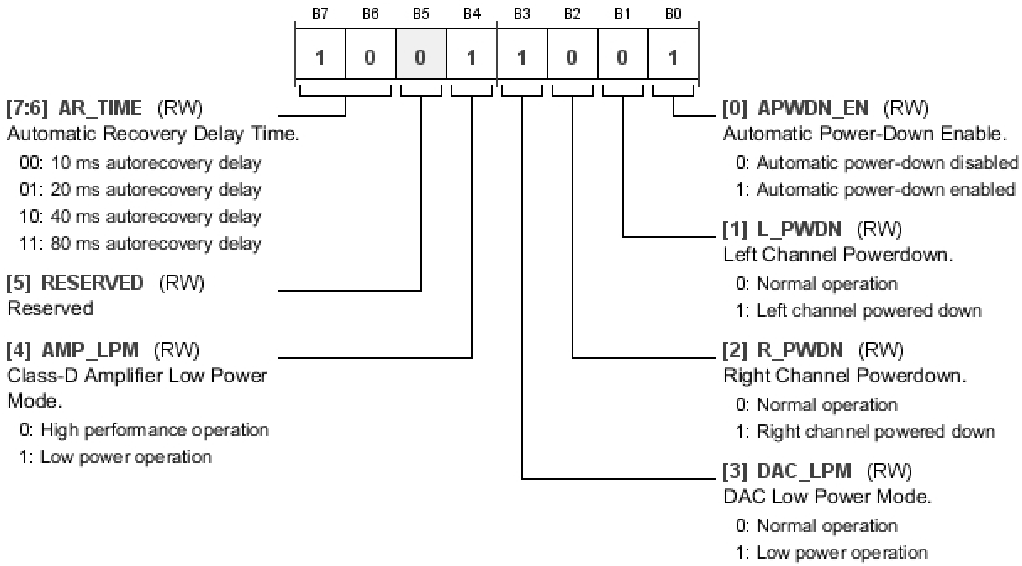

Table 22. Bit Descriptions for Power_Fault_Control

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	AR_TIME		Automatic Recovery Delay Time. This determines the amount of time delay between fault detection and an autorecovery attempt.	0x2	RW
		00	10 ms autorecovery delay		
		01	20 ms autorecovery delay		
		10	40 ms autorecovery delay		
		11	80 ms autorecovery delay		
5	RESERVED		Reserved.	0x0	RW
4	AMP_LPM		Class-D Amplifier Low Power Mode.	0x1	RW
		0	High performance operation		
		1	Low power operation		
3	DAC_LPM		DAC Low Power Mode. In low power mode, the DAC runs at half speed.	0x1	RW
		0	Normal operation		
		1	Low power operation		
2	R_PWDN		Right Channel Power-Down.	0x0	RW
		0	Normal operation		
		1	Right channel powered down		
1	L_PWDN		Left Channel Power-Down.	0x0	RW
		0	Normal operation		
		1	Left channel powered down		
0	APWDN_EN		Automatic Power-Down Enable. Automatic power-down automatically puts the IC in a low power state when 2048 consecutive zero input samples have been received.	0x1	RW
		0	Automatic power-down disabled		
		1	Automatic power-down enabled		

DRC CONTROL 1 REGISTER

Address: 0x0A, Reset: 0x7C, Name: DRC_Control_1

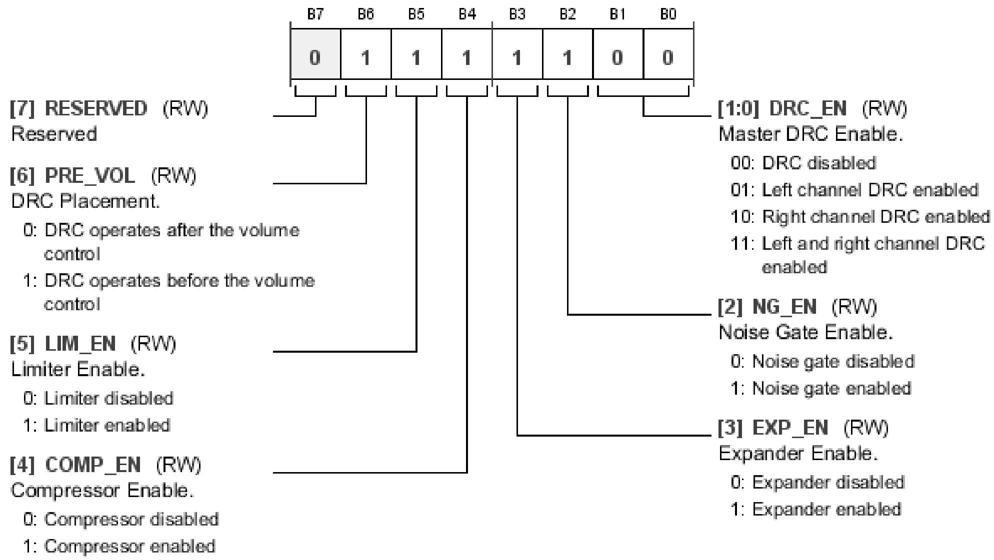

Table 23. Bit Descriptions for DRC_Control_1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	PRE_VOL		DRC Placement. This determines the placement of the DRC block in the signal chain. When placed before the volume control, the thresholds are relative to the input signal. When placed after the volume control, the thresholds are relative to the output signal level. All thresholds are 6 dB higher when placed after the volume control.	0x1	RW
		0	DRC operates after the volume control		
		1	DRC operates before the volume control		
5	LIM_EN		Limiter Enable. With the limiter enabled, the DRC_LT threshold (Bits[7:4] in Register 0x0C) must be set.	0x1	RW
		0	Limiter disabled		
		1	Limiter enabled		
4	COMP_EN		Compressor Enable. With the compressor enabled, the DRC_CT and DRC_SMAX thresholds (Bits[3:0] in Register 0x0C and Bits[7:4] in Register 0x0E) must be set.	0x1	RW
		0	Compressor disabled		
		1	Compressor enabled		
3	EXP_EN		Expander Enable. With the expander enabled, the DRC_ET and DRC_SMIN threshold values (Bits[7:4] in Register 0x0D and Bits[3:0] in Register 0x0E) must be set.	0x1	RW
		0	Expander disabled		
		1	Expander enabled		
2	NG_EN		Noise Gate Enable. With the noise gate enabled, the DRC_NT threshold value (Bits[3:0] in Register 0x0D) must be set.	0x1	RW
		0	Noise gate disabled		
		1	Noise gate enabled		
[1:0]	DRC_EN		Master DRC Enable. This must be enabled for any of the DRC features to function.	0x0	RW
		00	DRC disabled		
		01	Left channel DRC enabled		
		10	Right channel DRC enabled		
		11	Left and right channel DRC enabled		

DRC CONTROL 2 REGISTER

Address: 0x0B, Reset: 0x5B, Name: DRC_Control_2

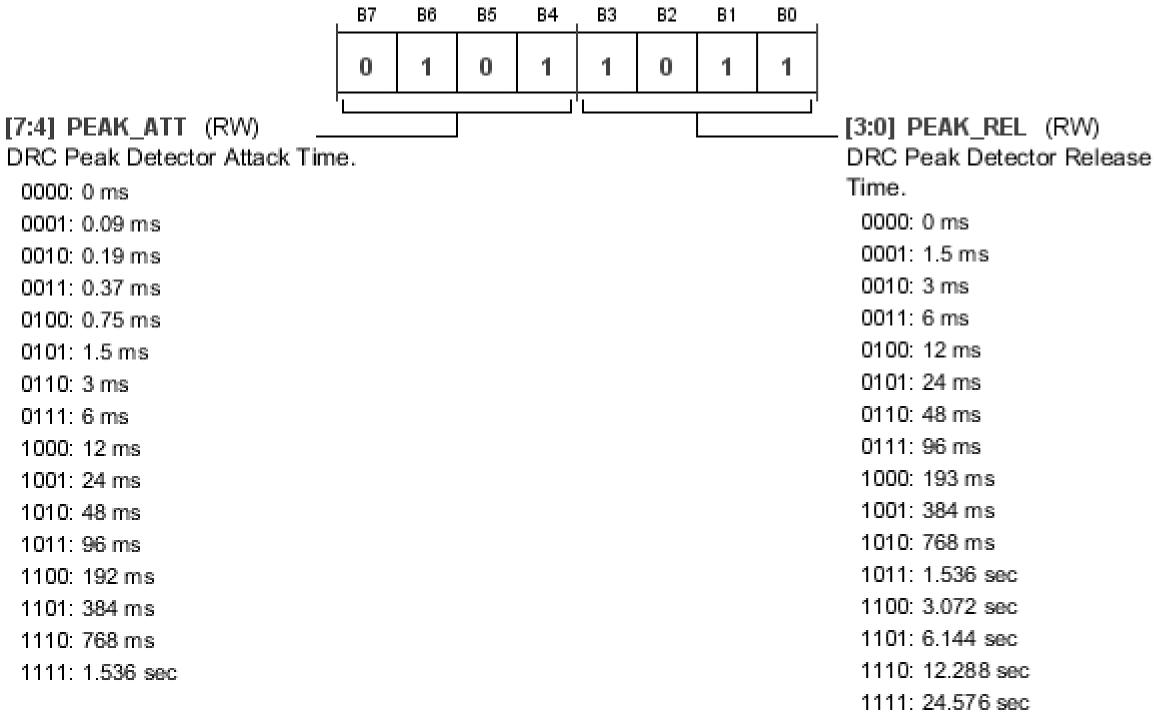

Table 24. Bit Descriptions for DRC_Control_2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	PEAK_ATT		DRC Peak Detector Attack Time.	0x5	RW
		0000	0 ms		
		0001	0.09 ms		
		0010	0.19 ms		
		0011	0.37 ms		
		0100	0.75 ms		
		0101	1.5 ms		
		0110	3 ms		
		0111	6 ms		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	PEAK_REL		DRC Peak Detector Release Time.	0xB	RW
		0000	0 ms		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		1000	193 ms		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC CONTROL 3 REGISTER

Address: 0x0C, Reset: 0x57, Name: DRC_Control_3

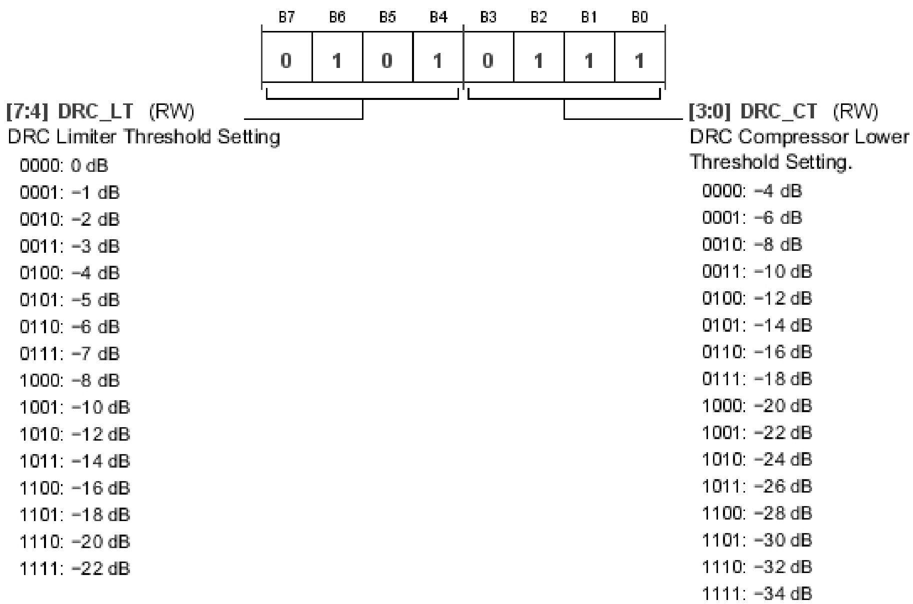

Table 25. Bit Descriptions for DRC_Control_3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRC_LT		DRC Limiter Threshold Setting. Relative to input.	0x5	RW
		0000	0 dB		
		0001	−1 dB		
		0010	−2 dB		
		0011	−3 dB		
		0100	−4 dB		
		0101	−5 dB		
		0110	−6 dB		
		0111	−7 dB		
		1000	−8 dB		
		1001	−10 dB		
		1010	−12 dB		
		1011	−14 dB		
		1100	−16 dB		
		1101	−18 dB		
		1110	−20 dB		
		1111	−22 dB		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DRC_CT		DRC Compressor Lower Threshold Setting. Relative to input.	0x7	RW
		0000	−4 dB		
		0001	−6 dB		
		0010	−8 dB		
		0011	−10 dB		
		0100	−12 dB		
		0101	−14 dB		
		0110	−16 dB		
		0111	−18 dB		
		1000	−20 dB		
		1001	−22 dB		
		1010	−24 dB		
		1011	−26 dB		
		1100	−28 dB		
		1101	−30 dB		
		1110	−32 dB		
		1111	−34 dB		

DRC CONTROL 4 REGISTER

Address: 0x0D, Reset: 0x89, Name: DRC_Control_4

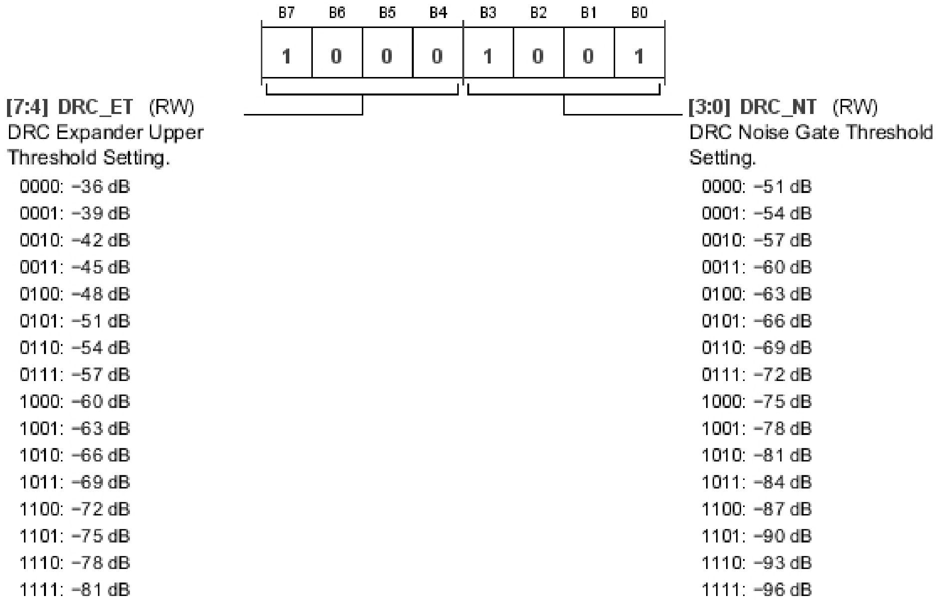

Table 26. Bit Descriptions for DRC_Control_4

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRC_ET		DRC Expander Upper Threshold Setting. Relative to input.	0x8	RW
		0000	−36 dB		
		0001	−39 dB		
		0010	−42 dB		
		0011	−45 dB		
		0100	−48 dB		
		0101	−51 dB		
		0110	−54 dB		
		0111	−57 dB		
		1000	−60 dB		
		1001	−63 dB		
		1010	−66 dB		
		1011	−69 dB		
		1100	−72 dB		
		1101	−75 dB		
		1110	−78 dB		
		1111	−81 dB		
[3:0]	DRC_NT		DRC Noise Gate Threshold Setting. Relative to input.	0x9	RW
		0000	−51 dB		
		0001	−54 dB		
		0010	−57 dB		
		0011	−60 dB		
		0100	−63 dB		
		0101	−66 dB		
		0110	−69 dB		
		0111	−72 dB		
		1000	−75 dB		
		1001	−78 dB		
		1010	−81 dB		
		1011	−84 dB		

Bits	Bit Name	Settings	Description	Reset	Access
		1100	−87 dB		
		1101	−90 dB		
		1110	−93 dB		
		1111	−96 dB		

DRC CONTROL 5 REGISTER

Address: 0x0E, Reset: 0x8C, Name: DRC_Control_5

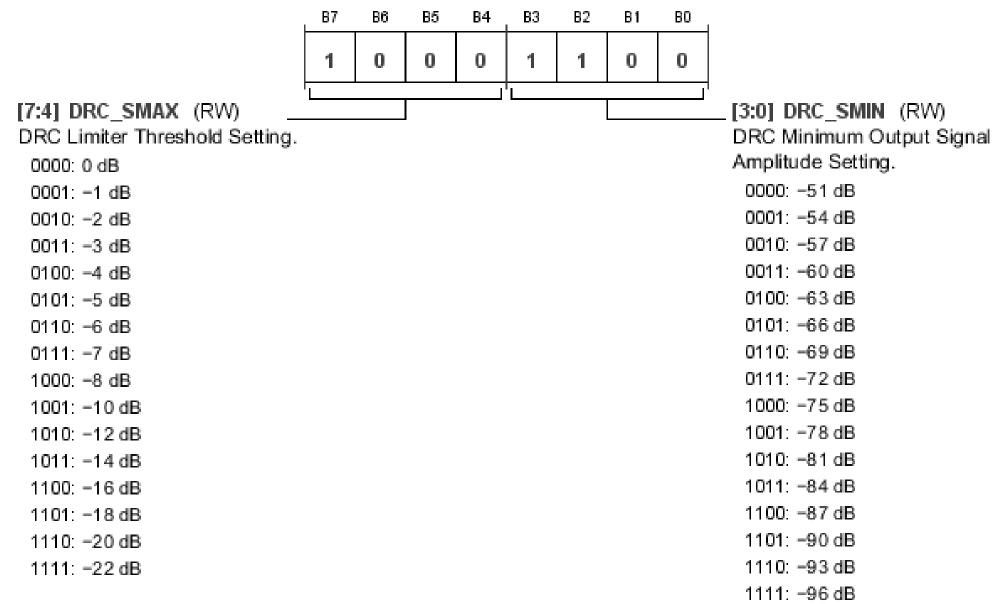

Table 27. Bit Descriptions for DRC_Control_5

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRC_SMAX		DRC Limiter Threshold Setting. Relative to input.	0x8	RW
		0000	0 dB		
		0001	−1 dB		
		0010	−2 dB		
		0011	−3 dB		
		0100	−4 dB		
		0101	−5 dB		
		0110	−6 dB		
		0111	−7 dB		
		1000	−8 dB		
		1001	−10 dB		
		1010	−12 dB		
		1011	−14 dB		
		1100	−16 dB		
		1101	−18 dB		
		1110	−20 dB		
		1111	−22 dB		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	DRC_SMIN		DRC Minimum Output Signal Amplitude Setting. This is the minimum output level produced by the DRC and is used to indicate the expander lower threshold, or output signal level when the input rises beyond the noise gate threshold.	0xC	RW
		0000	−51 dB		
		0001	−54 dB		
		0010	−57 dB		
		0011	−60 dB		
		0100	−63 dB		
		0101	−66 dB		
		0110	−69 dB		
		0111	−72 dB		
		1000	−75 dB		
		1001	−78 dB		
		1010	−81 dB		
		1011	−84 dB		
		1100	−87 dB		
		1101	−90 dB		
		1110	−93 dB		
		1111	−96 dB		

DRC CONTROL 6 REGISTER

Address: 0x0F, Reset: 0x77, Name: DRC_Control_6

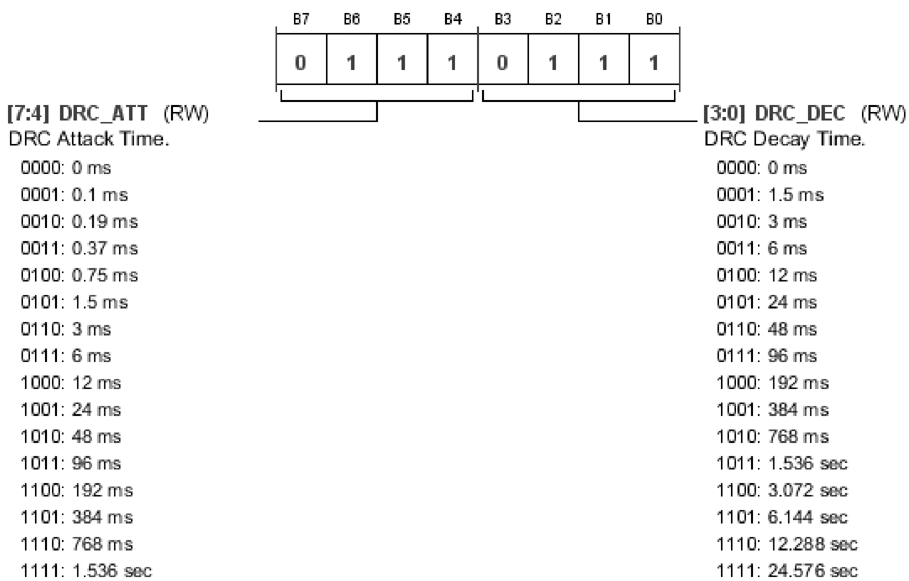

Table 28. Bit Descriptions for DRC_Control_6

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRC_ATT		DRC Attack Time. Used to smooth the gain curve at the thresholds (knees) of each DRC function.	0x7	RW
		0000	0 ms		
		0001	0.1 ms		
		0010	0.19 ms		
		0011	0.37 ms		
		0100	0.75 ms		
		0101	1.5 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		0110	3 ms		
		0111	6 ms		
		1000	12 ms		
		1001	24 ms		
		1010	48 ms		
		1011	96 ms		
		1100	192 ms		
		1101	384 ms		
		1110	768 ms		
		1111	1.536 sec		
[3:0]	DRC_DEC		DRC Decay Time. Used to smooth the gain curve at the thresholds (knees) of each DRC function.	0x7	RW
		0000	0 ms		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

DRC CONTROL 7 REGISTER

Address: 0x10, Reset: 0x26, Name: DRC_Control_7

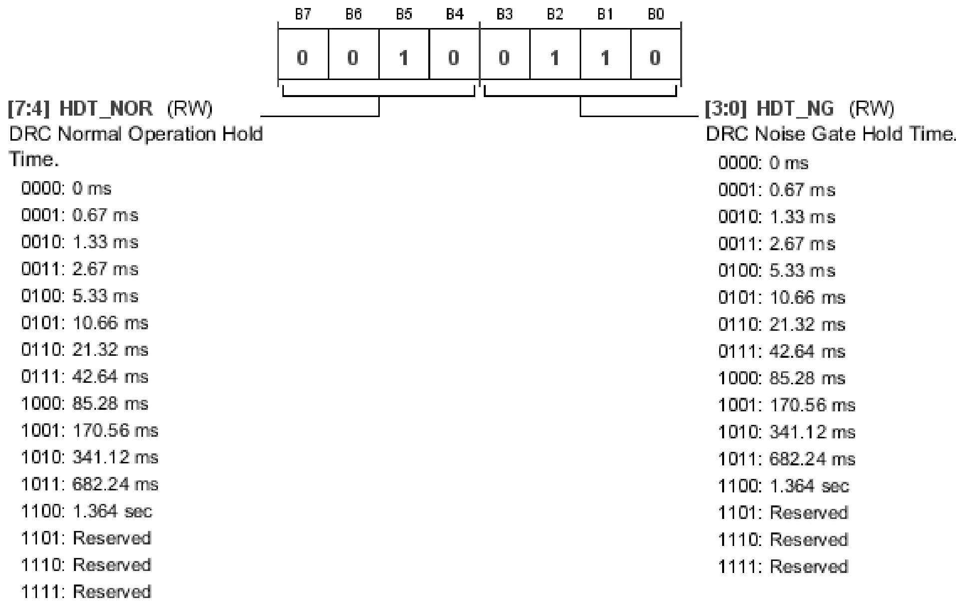

Table 29. Bit Descriptions for DRC_Control_7

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	HDT_NOR		DRC Normal Operation Hold Time. Used to prevent the gain curve calculation from increasing too quickly.	0x2	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.33 ms		
		0011	2.67 ms		
		0100	5.33 ms		
		0101	10.66 ms		
		0110	21.32 ms		
		0111	42.64 ms		
		1000	85.28 ms		
		1001	170.56 ms		
		1010	341.12 ms		
		1011	682.24 ms		
		1100	1.364 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		
[3:0]	HDT_NG		DRC Noise Gate Hold Time. Used to prevent the DRC from entering noise gate too quickly.	0x6	RW
		0000	0 ms		
		0001	0.67 ms		
		0010	1.33 ms		
		0011	2.67 ms		
		0100	5.33 ms		
		0101	10.66 ms		
		0110	21.32 ms		
		0111	42.64 ms		
		1000	85.28 ms		
		1001	170.56 ms		

Bits	Bit Name	Settings	Description	Reset	Access
		1010	341.12 ms		
		1011	682.24 ms		
		1100	1.364 sec		
		1101	Reserved		
		1110	Reserved		
		1111	Reserved		

DRC CONTROL 8 REGISTER

Address: 0x11, Reset: 0x1C, Name: DRC_Control_8

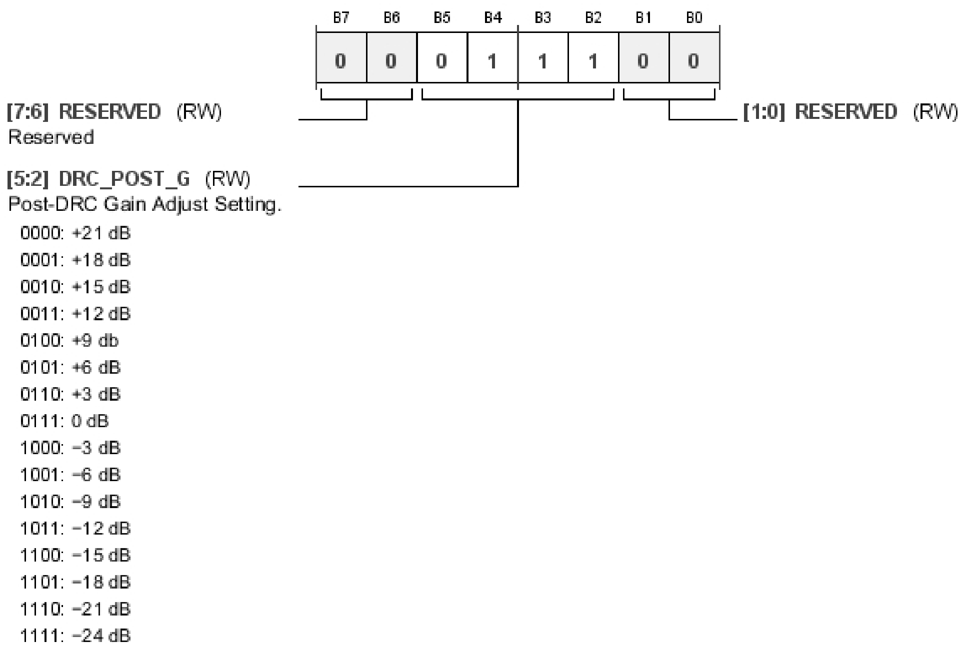

Table 30. Bit Descriptions for DRC_Control_8

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	RW
[5:2]	DRC_POST_G		Post-DRC Gain Adjust Setting. This can be used to add additional gain after the DRC function to compensate for the overall reduction of system gain due to the DRC.	0x7	RW
		0000	+21 dB		
		0001	+18 dB		
		0010	+15 dB		
		0011	+12 dB		
		0100	+9 db		
		0101	+6 dB		
		0110	+3 dB		
		0111	0 dB		
		1000	−3 dB		
		1001	−6 dB		
		1010	−9 dB		
		1011	−12 dB		
		1100	−15 dB		
		1101	−18 dB		
		1110	−21 dB		
		1111	−24 dB		
[1:0]	RESERVED		Reserved.	0x0	RW

DRC CONTROL 9 REGISTER

Address: 0x12, Reset: 0x07, Name: DRC_Control_9

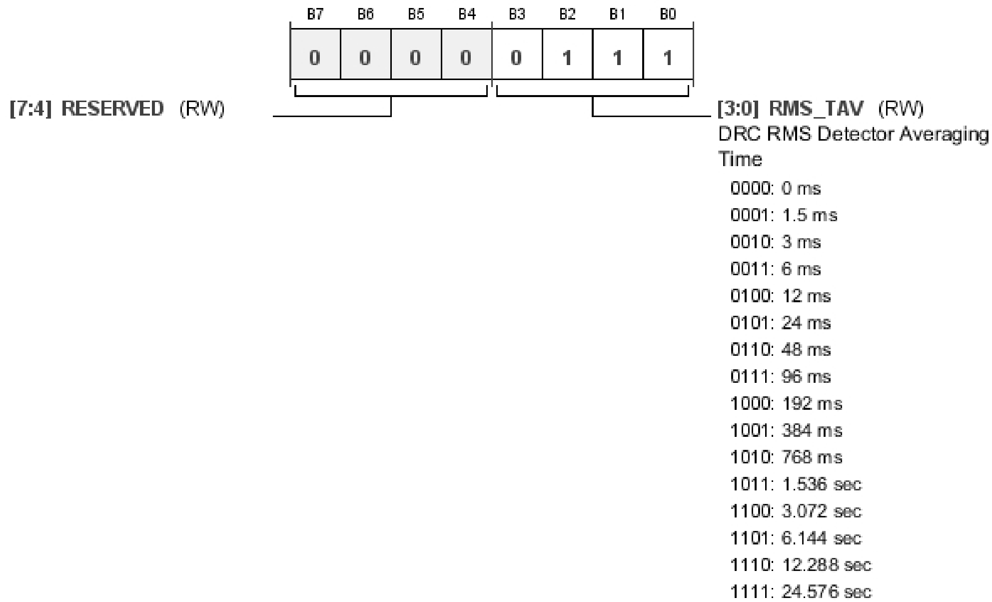

Table 31. Bit Descriptions for DRC_Control_9

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
[3:0]	RMS_TAV		DRC RMS Detector Averaging Time. This is the averaging time for the rms level that is compared to the DRC thresholds.	0x7	RW
		0000	0 ms		
		0001	1.5 ms		
		0010	3 ms		
		0011	6 ms		
		0100	12 ms		
		0101	24 ms		
		0110	48 ms		
		0111	96 ms		
		1000	192 ms		
		1001	384 ms		
		1010	768 ms		
		1011	1.536 sec		
		1100	3.072 sec		
		1101	6.144 sec		
		1110	12.288 sec		
		1111	24.576 sec		

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

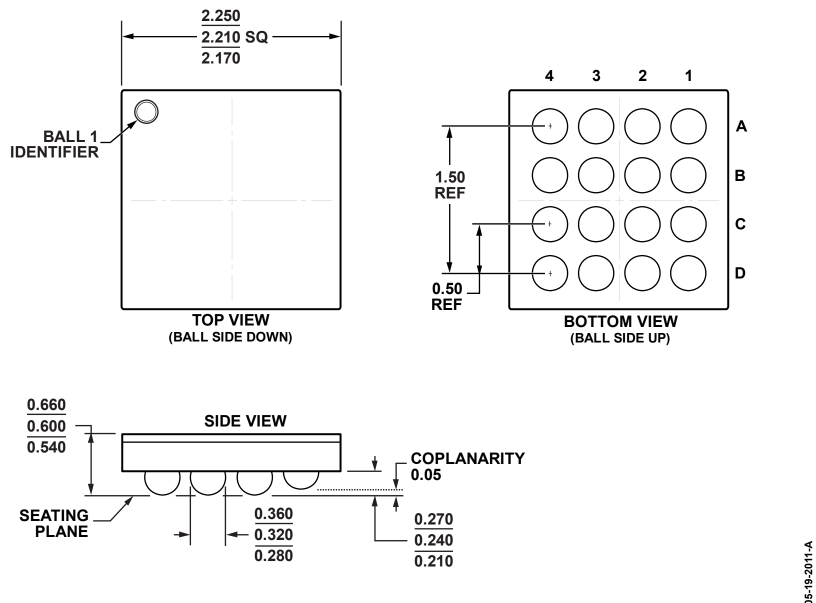

Figure 37.16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-13)
Dimensions shown in millimeters

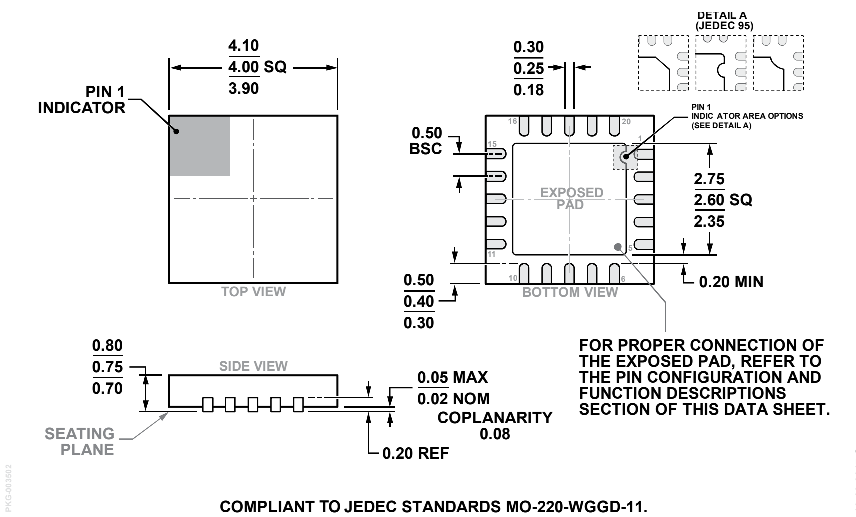

Figure 38. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2518CBZ-RL	−40°C to +85°C	16-Ball WLCSP	CB-16-13
SSM2518CBZ-R7	−40°C to +85°C	16-Ball WLCSP	CB-16-13
SSM2518CPZ	−40°C to +85°C	20-Lead LFCSP	CP-20-8
SSM2518CPZ-R7	−40°C to +85°C	20-Lead LFCSP	CP-20-8
SSM2518CPZ-RL	−40°C to +85°C	20-Lead LFCSP	CP-20-8
EVAL-SSM2518Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

D10242-0-1/18(B)