Mono 2.9 W Class-D Audio Amplifier with Digital Current and Voltage Output

Data Sheet **SSM4321**

FEATURES

Filterless Class-D amplifier with spread-spectrum Σ-Δ modulation
Digitized output of output voltage, output current, and PVDD supply voltage
72 dB signal-to-noise ratio (SNR) on output current sensing and 77 dB SNR on output voltage sensing
TDM or multichip I²S slave output interface
- **Up to 4 chips supported on a single bus**
- **8 kHz to 48 kHz operation**

I²S/left justified slave output interface
- **1 or 2 chips supported on a single bus**
- **8 kHz to 48 kHz operation**

PDM output interface operates from 1 MHz to 6.144 MHz
2.2 W into 4 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with <1% total harmonic distortion plus noise (THD + N)
89% efficiency at 5.0 V, 1.4 W into 8 Ω + 0.2 Ω R_{SENSE} speaker
>100 dB signal-to-noise ratio (SNR)
High PSRR at 217 Hz: 86 dB
Amplifier supply operation from 2.5 V to 5.5 V
Input/output supply operation from 1.42 V to 3.6 V
Flexible gain adjustment pin: 0 dB to 12 dB in 3 dB steps with fixed input impedance of 80 kΩ
<1 µA shutdown current
Smart power-down with loss of BCLK
Short-circuit and thermal protection with autorecovery
Available in a 16-ball, 0.4 mm pitch, 1.74 mm × 1.74 mm WLCSP
Pop-and-click suppression

APPLICATIONS

Mobile phones
MP3 players
Portable electronics

GENERAL DESCRIPTION

The SSM4321 is a fully integrated, high efficiency, Class-D audio amplifier with digitized output of output voltage, output current, and the PVDD supply voltage. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a 2.5 V to 5.5 V supply for the amplifier and a 1.42 V to 3.6 V supply for input/output. The SSM4321 is capable of delivering 2.2 W of continuous output power with <1% THD + N driving a 4 Ω load from a 5.0 V supply with a 0.1 Ω V/I sense resistor.

The SSM4321 features a high efficiency, low noise modulation scheme that requires no external LC output filters. The modulation scheme provides high efficiency even at low output power. The SSM4321 operates with 89% efficiency at 1.4 W into 8 Ω from a 5.0 V supply with an SNR of >100 dB.

The SSM4321 includes circuitry to sense output current, output voltage, and the PVDD supply voltage. Current sense is performed using an external sense resistor that is connected between an output pin and the load. The output current and voltage are sent to ADCs with 16-bit resolution; the PVDD supply voltage is sent to an ADC with 8-bit resolution.

The outputs of these ADCs are available on the TDM or I²S output serial port. The SLOT pin is used to determine which of four possible output slots is used on the TDM interface. A stereo I²S interface can be selected by reversing the pin connections for BCLK and FSYNC. Also, a direct PDM bit stream of voltage and current data can be selected via the SLOT pin.

Spread-spectrum pulse density modulation (PDM) is used to provide lower EMI-radiated emissions compared with other Class-D architectures. The inherent randomized nature of spread-spectrum PDM eliminates the clock intermodulation (beating effect) of several amplifiers in close proximity.

The SSM4321 produces ultralow EMI emissions that significantly reduce the radiated emissions at the Class-D outputs, particularly above 100 MHz. The ultralow EMI emissions of the SSM4321 are also helpful for antenna and RF sensitivity problems.

The device includes a highly flexible gain select pin that requires only one series resistor to select a gain setting of 0 dB, 3 dB, 6 dB, 9 dB, or 12 dB. Input impedance is fixed at 80 kΩ, independent of the selected gain.

The SSM4321 has a shutdown mode with a typical shutdown current of <1 µA. Shutdown is enabled by removing the BCLK input. A clock must be present on the BCLK pin for the part to operate.

The device also includes pop-and-click suppression circuitry, which minimizes voltage glitches at the output during turn-on and turn-off, reducing audible noise on activation and deactivation.

The SSM4321 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a halide-free, 16-ball, 0.4 mm pitch, 1.74 mm × 1.74 mm wafer level chip scale package (WLCSP).

Rev. 0 **Document Feedback**

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Technical Support www.analog.com

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REVISION HISTORY

10/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

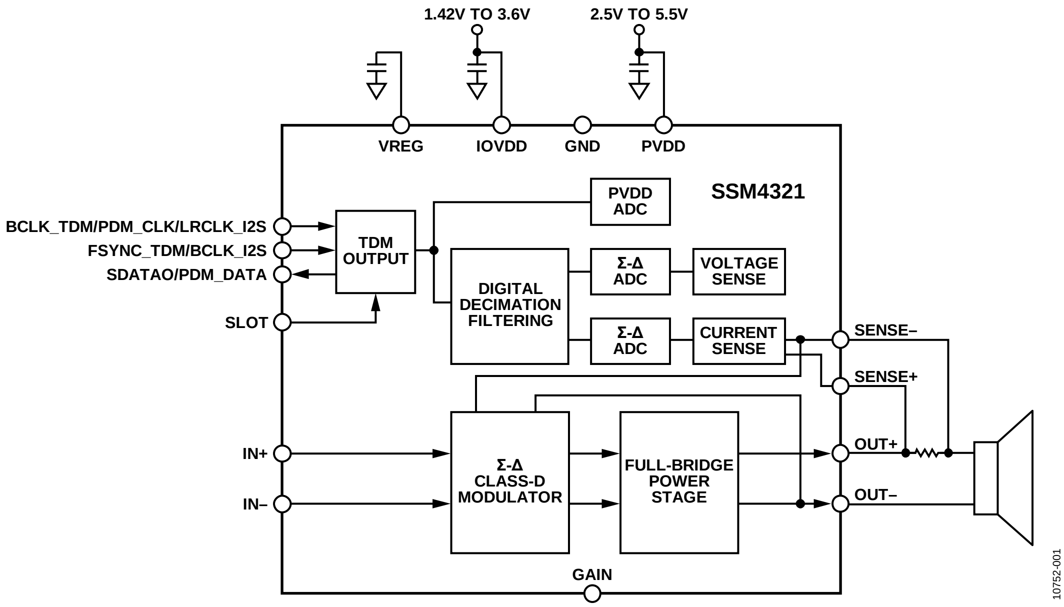


Figure 1.

SPECIFICATIONS

PVDD = 5.0 V, IOVDD = 1.8 V, f_S = 24 kHz with I^2S output, T_A = 25°C, R_L = 8 Ω +33 µH, unless otherwise noted. For R_L = 8 Ω, use a 200 mΩ V/I sense resistor; for R_L = 4 Ω, use a 100 mΩ V/I sense resistor; for R_L = 3 Ω, use a 75 mΩ V/I sense resistor.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power, RMS	P_{OUT}	f = 1 kHz, 20 kHz bandwidth				
		R_L = 8 Ω, THD = 1%, PVDD = 5.0 V		1.35		W
		R_L = 8 Ω, THD = 1%, PVDD = 3.6 V		0.70		W
		R_L = 8 Ω, THD = 1%, PVDD = 2.5 V		0.32		W
		R_L = 8 Ω, THD = 10%, PVDD = 5.0 V		1.70		W
		R_L = 8 Ω, THD = 10%, PVDD = 3.6 V		0.86		W
		R_L = 8 Ω, THD = 10%, PVDD = 2.5 V		0.4		W
		R_L = 4 Ω, THD = 1%, PVDD = 5.0 V		2.22		W
		R_L = 4 Ω, THD = 1%, PVDD = 3.6 V		1.12		W
		R_L = 4 Ω, THD = 1%, PVDD = 2.5 V		0.51		W
		R_L = 4 Ω, THD = 10%, PVDD = 5.0 V		2.8		W
		R_L = 4 Ω, THD = 10%, PVDD = 3.6 V		1.42		W
		R_L = 4 Ω, THD = 10%, PVDD = 2.5 V		0.64		W
		R_L = 3 Ω, THD = 1%, PVDD = 5.0 V		3.00		W
		R_L = 3 Ω, THD = 1%, PVDD = 3.6 V		1.51		W
		R_L = 3 Ω, THD = 1%, PVDD = 2.5 V		0.68		W
		R_L = 3 Ω, THD = 10%, PVDD = 5.0 V		3.77		W
		R_L = 3 Ω, THD = 10%, PVDD = 3.6 V		1.90		W
		R_L = 3 Ω, THD = 10%, PVDD = 2.5 V		0.86		W
Efficiency	η	P_{OUT} = 1.4 W into 8 Ω, PVDD = 5.0 V		89		%
		P_{OUT} = 2.8 W into 3 Ω, PVDD = 5.0 V		82		%
Total Harmonic Distortion Plus Noise	THD + N	P_{OUT} = 1 W into 8 Ω, f = 1 kHz, PVDD = 5.0 V		0.01		%
		P_{OUT} = 0.5 W into 8 Ω, f = 1 kHz, PVDD = 3.6 V		0.01		%
Input Common-Mode Voltage Range	V_{CM}		1.0		PVDD − 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 100 mV rms at 1 kHz		50		dB
Average Switching Frequency	f_{SW}			256		kHz
Clock Frequency	f_{OSC}			6.2		MHz
Differential Output Offset Voltage	V_{OOS}	Gain = 6 dB		0.3	5.0	mV
POWER SUPPLY						
Supply Voltage Range	PVDD	Guaranteed from PSRR test	2.5		5.5	V
	IOVDD		1.42		3.6	V
Power Supply Rejection Ratio	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs are ac-grounded, C_{IN} = 0.1 µF		86		dB
Supply Current, PVDD	I_{SYPVDD}	V_{IN} = 0 V				
		No load, PVDD = 5.0 V		3.7		mA
		No load, PVDD = 3.6 V		3.1		mA
		No load, PVDD = 2.5 V		2.9		mA
		R_L = 8 Ω, PVDD = 5.0 V		3.8		mA
		R_L = 8 Ω, PVDD = 3.6 V		3.2		mA
		R_L = 8 Ω, PVDD = 2.5 V		2.9		mA
Supply Current, IOVDD	$I_{SYIOVDD}$	IOVDD = 1.8 V		0.41		mA
Shutdown Current, PVDD	I_{SDPVDD}	No BCLK, PVDD = 5.0 V		0.1		µA
Shutdown Current, IOVDD	$I_{SDIOVDD}$	No BCLK, IOVDD = 1.8 V		0.77		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN CONTROL						
Closed-Loop Gain	Gain		0		12	dB
Input Impedance	Z_{IN}	BCLK enabled, fixed input impedance (0 dB to 12 dB)		80		kΩ
SHUTDOWN CONTROL						
Turn-On Time	t_{WU}	From BCLK start		12.5		ms
Turn-Off Time	t_{SD}	From BCLK removal		5		µs
Output Impedance	Z_{OUT}	No BCLK		>100		kΩ
AMPLIFIER NOISE PERFORMANCE						
Output Voltage Noise	e_n	f = 20 Hz to 20 kHz, inputs are ac-grounded, gain = 6 dB, A-weighted				
		PVDD = 5.0 V		30		µV
		PVDD = 3.6 V		30		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 1.3 W, R_L = 8 Ω, A-weighted		101		dB
OUTPUT SENSING						
Output Sampling Rate, TDM	f_S	LRCLK/FSYNC pulse rate	8		48	kHz
BCLK Frequency, TDM	f_{BCLK}	1 to 4 slots used	0.512		6.144	MHz
Voltage Sense Signal-to-Noise Ratio	SNRV	A-weighted		77		dB
Voltage Sense Full-Scale Output Voltage	V_{FS}	Amplifier voltage with 0 dBFS ADC output		6		V_P
Voltage Sense Absolute Accuracy				1.5		%
Voltage Sense Gain Drift		T_A = 10°C to 60°C		1		%
Current Sense Signal-to-Noise Ratio	SNRI	A-weighted		72		dB
Current Sense Full-Scale Input Voltage	V_{IS}	I_{SENSE} converter voltage with 0 dBFS ADC output		0.150		V_P
Current Sense Absolute Accuracy				3		%
Current Sense Gain Drift		T_A = 10°C to 60°C, ideal R_{SENSE}		1		%
PVDD Sense Full-Scale Range	PV_{FS}	PVDD with full-scale ADC output	2		6	V
PVDD Sense Absolute Accuracy				3		%
Current and Voltage Sense Linearity		From −80 dBr to 0 dBr			1	dB
ADC −3 dB Corner Frequency	f_C	Digital high-pass filter				
		Output f_S = 48 kHz		3.75		Hz
		Output f_S = 24 kHz		1.875		Hz

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BCLK, FSYNC PINS		Ball D2 and Ball D3				
Input Voltage High	V_{IH}		0.7 × IOVDD		3.6	V
Input Voltage Low	V_{IL}		−0.3		0.3 × IOVDD	V
Input Leakage Current High	I_{IH}				1	µA
Input Leakage Current Low	I_{IL}				1	µA
Input Capacitance	C_{IN}				5	pF
SDATAO/PDM_DATA PIN		Ball D1				
Output Drive Strength		IOVDD = 1.5 V		3.5		mA
		IOVDD = 1.8 V		4.5		mA

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
PVDD Supply Voltage	6 V
IOVDD Supply Voltage	3.6 V
Input Voltage	PVDD
Common-Mode Input Voltage	PVDD
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Susceptibility	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

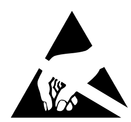
Junction-to-air thermal resistance (θ_{JA}) is specified for the worst-case conditions, that is, a device soldered in a printed circuit board (PCB) for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
16-Ball, 1.74 mm × 1.74 mm WLCSP	665	°C/W

[1] The θ_{JA} specification is measured on a JEDEC standard 4-layer PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

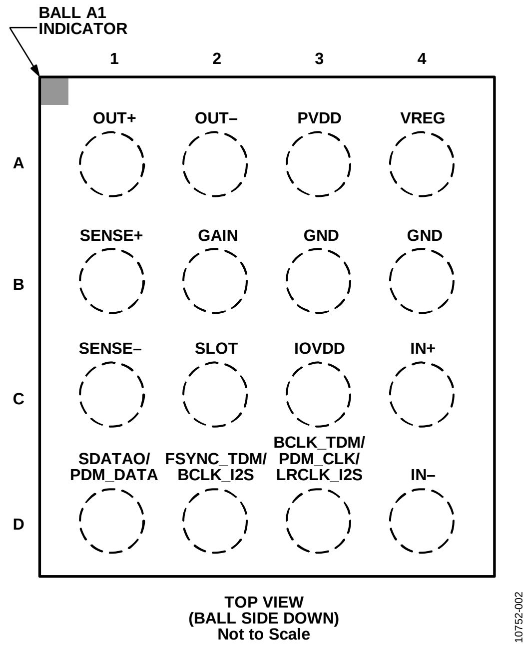


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	OUT+	Noninverting Output.
A2	OUT−	Inverting Output.
A3	PVDD	Amplifier Power Supply.
A4	VREG	Internal LDO Regulator Output.
B1	SENSE+	Current Sense Positive Input.
B2	GAIN	Gain Control Pin.
B3, B4	GND	Ground.
C1	SENSE−	Current Sense Negative Input.
C2	SLOT	TDM Slot Selection Input.
C3	IOVDD	Input/Output Digital Power Supply.
C4	IN+	Noninverting Input.
D1	SDATAO/PDM_DATA	TDM Serial Data Output/PDM Data Output.
D2	FSYNC_TDM/BCLK_I2S	TDM Frame Synchronization Input/I^2S Bit Clock Input.
D3	BCLK_TDM/PDM_CLK/ LRCLK_I2S	TDM Bit Clock Input/PDM Clock Input/I^2S LRCLK Input.
D4	IN−	Inverting Input.

TYPICAL PERFORMANCE CHARACTERISTICS

PVDD = 5.0 V, IOVDD = 1.8 V, f_S = 24 kHz with I²S output, gain = 6 dB, T_A = 25°C, unless otherwise noted. For R_L = 8 Ω, use a 200 mΩ V/I sense resistor; for R_L = 4 Ω, use a 100 mΩ V/I sense resistor; for R_L = 3 Ω, use a 75 mΩ V/I sense resistor.

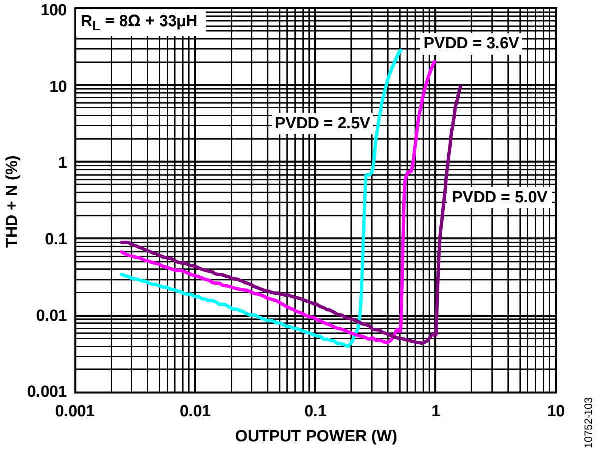


Figure 3. THD + N vs. Output Power into 8 Ω

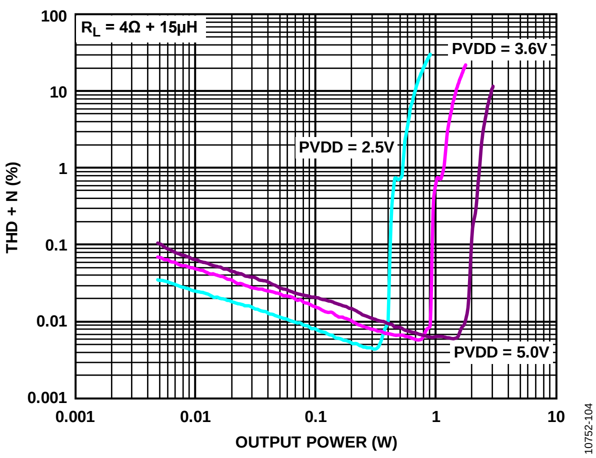


Figure 4. THD + N vs. Output Power into 4 Ω

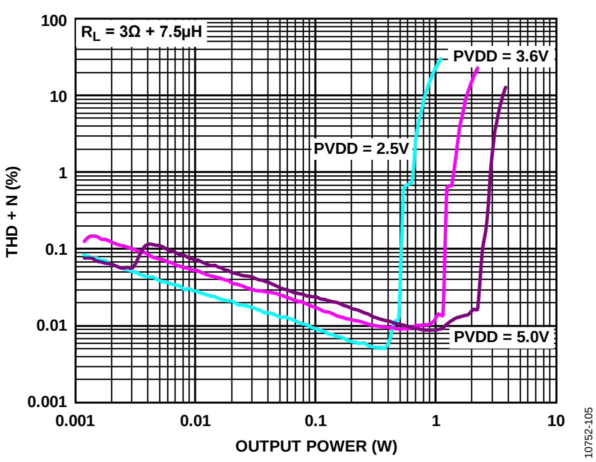


Figure 5. THD + N vs. Output Power into 3 Ω

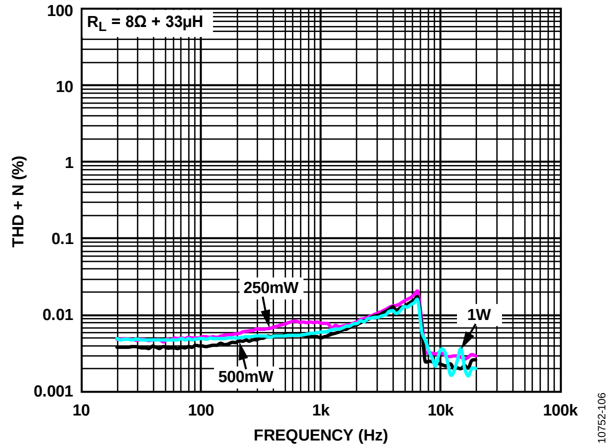


Figure 6. THD + N vs. Frequency, PVDD = 5 V, R_L = 8 Ω

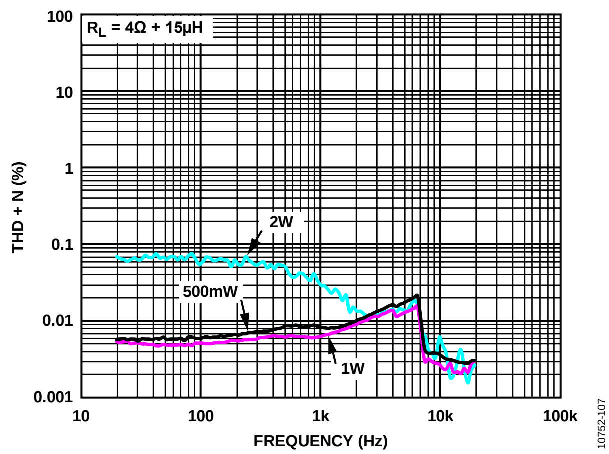


Figure 7. THD + N vs. Frequency, PVDD = 5 V, R_L = 4 Ω

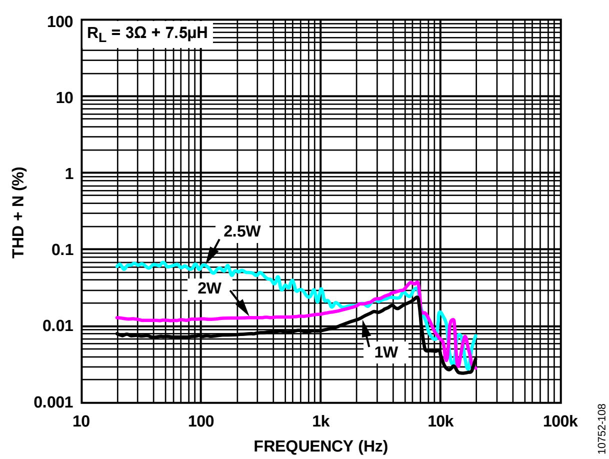


Figure 8. THD + N vs. Frequency, PVDD = 5 V, R_L = 3 Ω

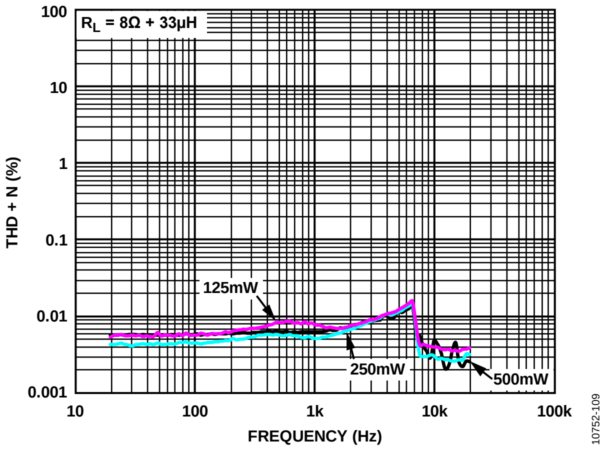


Figure 9. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 8 Ω

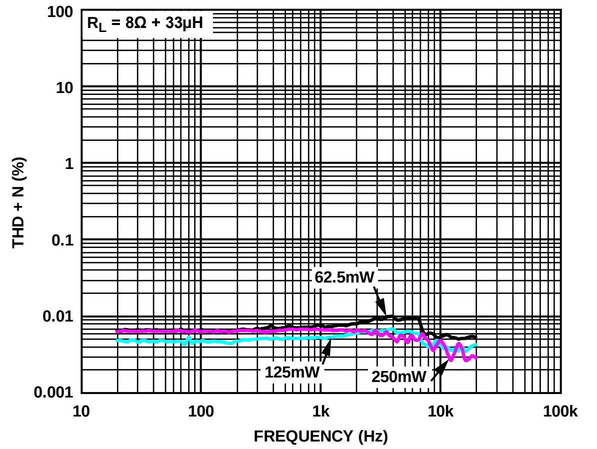


Figure 12. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 8 Ω

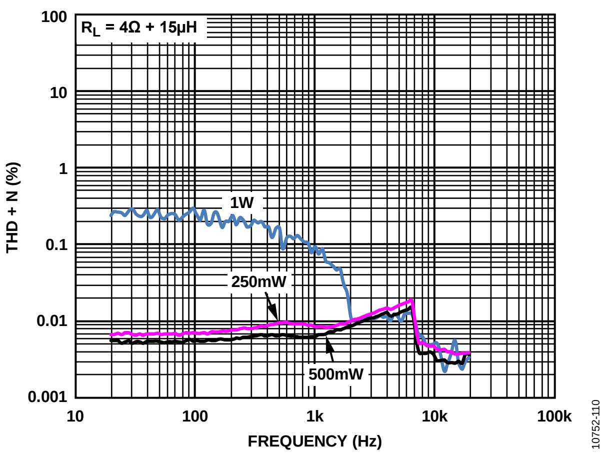


Figure 10. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 4 Ω

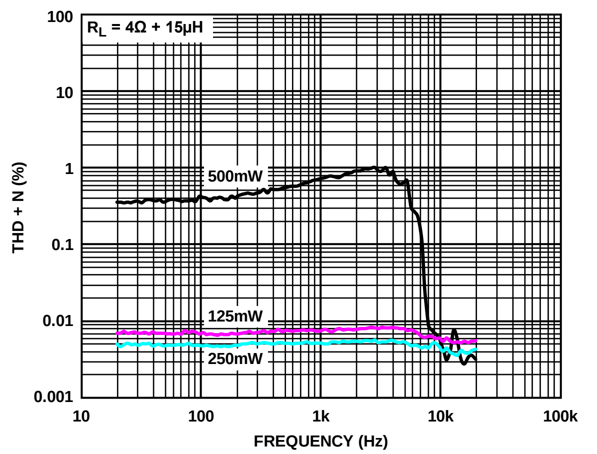


Figure 13. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 4 Ω

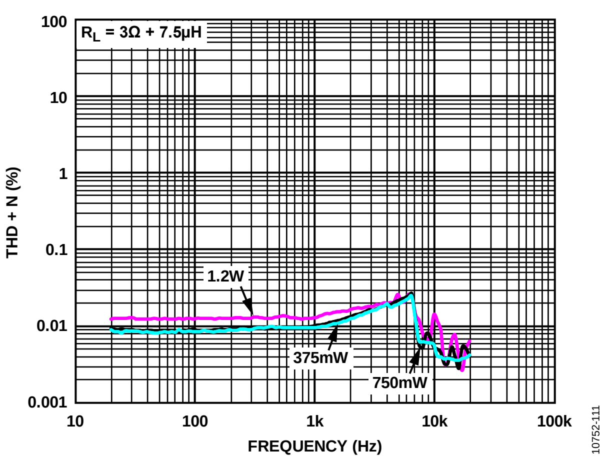


Figure 11. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 3 Ω

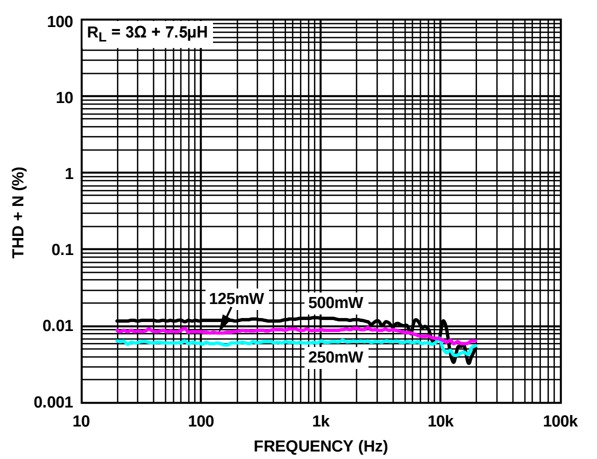


Figure 14. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 3 Ω

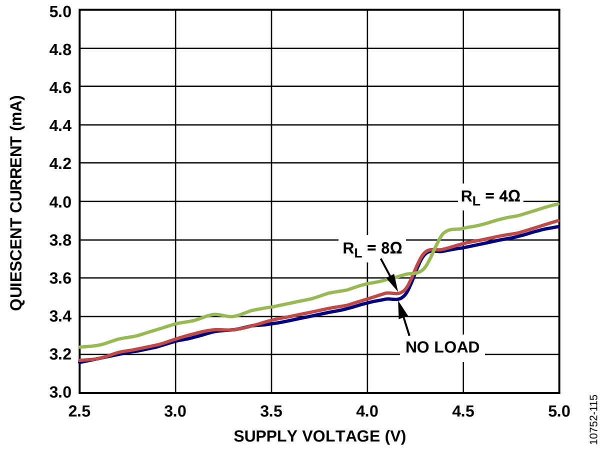


Figure 15. Quiescent Current vs. PVDD Supply Voltage, ADC Sense Enabled

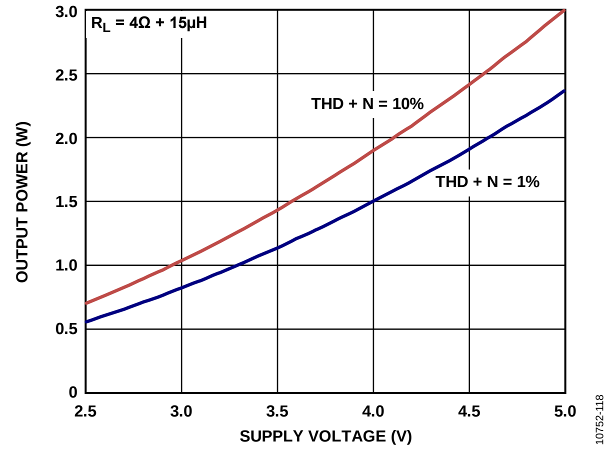


Figure 18. Maximum Output Power vs. PVDD Supply Voltage, $R_L = 4\ \Omega$

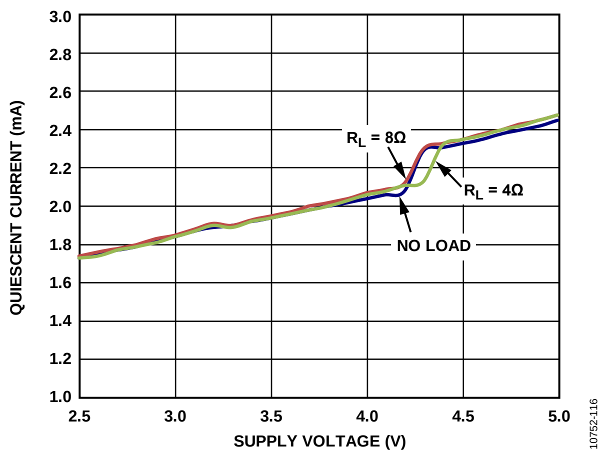


Figure 16. Quiescent Current vs. PVDD Supply Voltage, ADC Sense Disabled

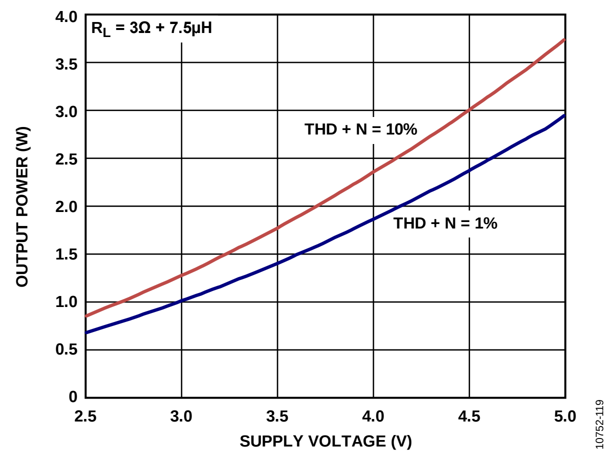


Figure 19. Maximum Output Power vs. PVDD Supply Voltage, $R_L = 3\ \Omega$

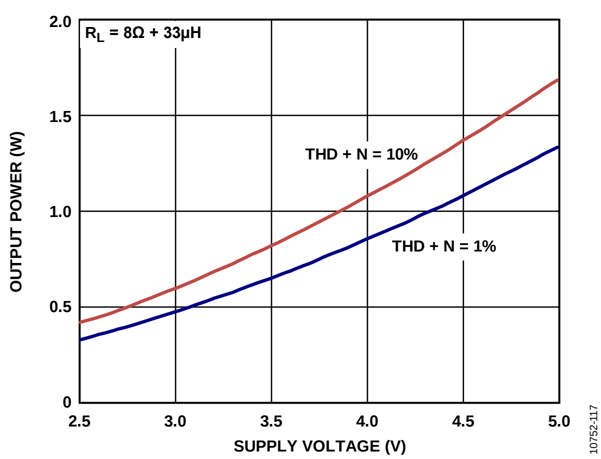


Figure 17. Maximum Output Power vs. PVDD Supply Voltage, $R_L = 8\ \Omega$

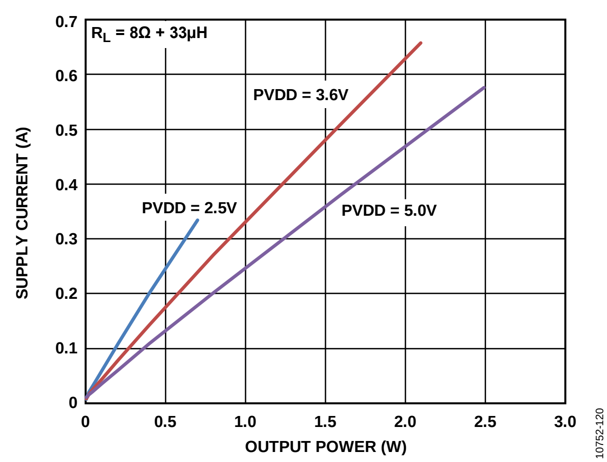


Figure 20. Supply Current vs. Output Power into 8 Ω

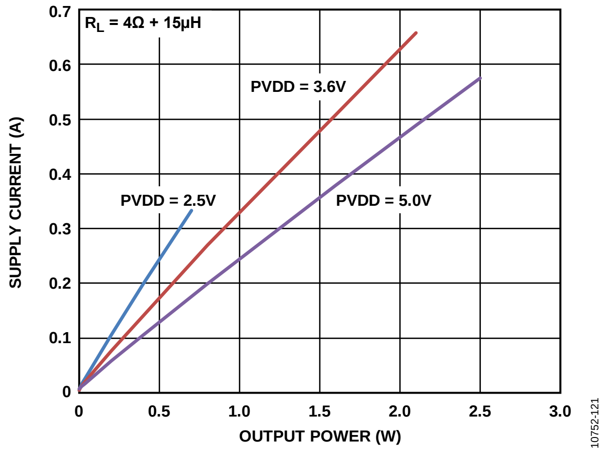


Figure 21. Supply Current vs. Output Power into 4 Ω

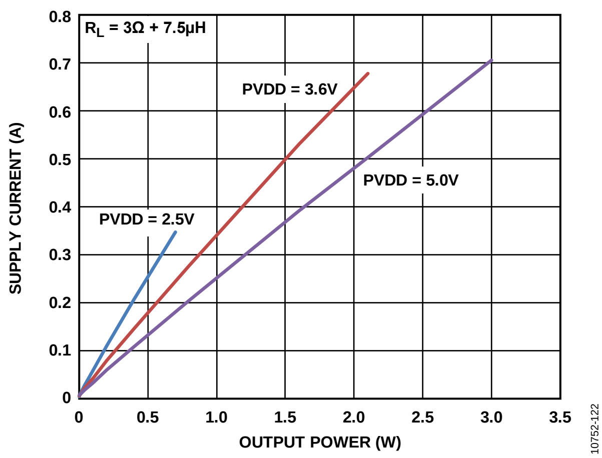


Figure 22. Supply Current vs. Output Power into 3 Ω

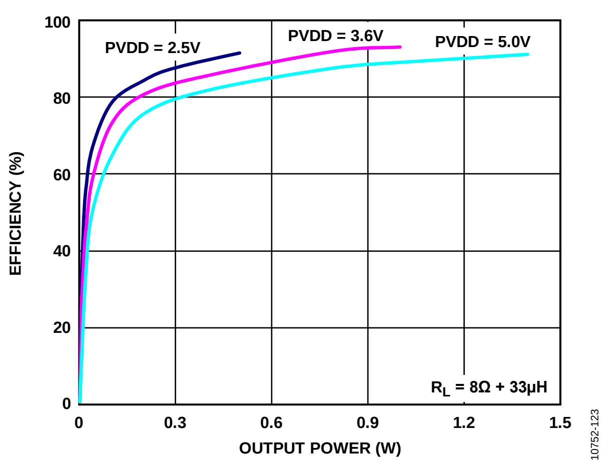


Figure 23. Efficiency vs. Output Power into 8 Ω

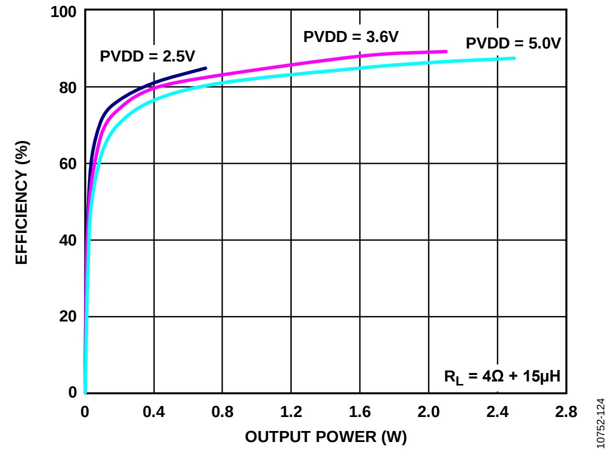


Figure 24. Efficiency vs. Output Power into 4 Ω

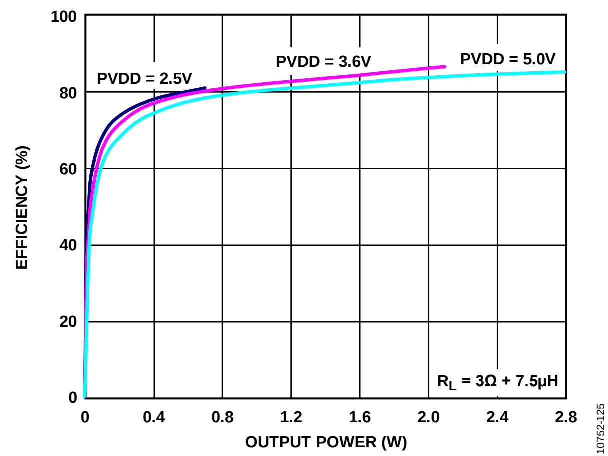


Figure 25. Efficiency vs. Output Power into 3 Ω

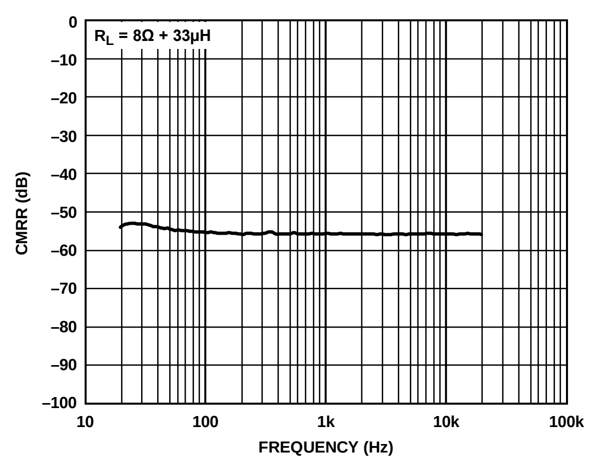


Figure 26. Common-Mode Rejection Ratio (CMRR) vs. Frequency, PVDD = 5 V, R_L = 8 Ω

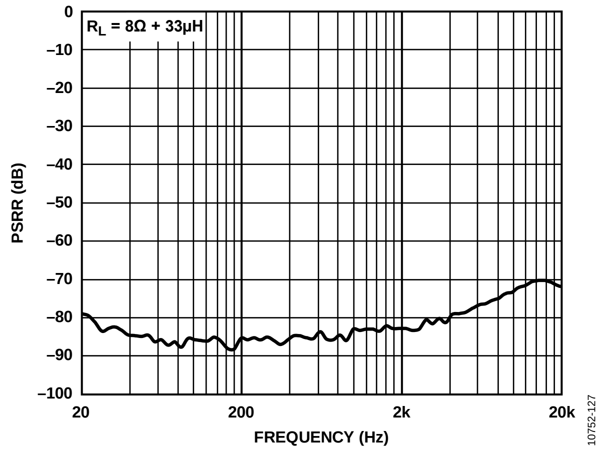


Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency, PVDD = 5 V, R_L = 8 Ω

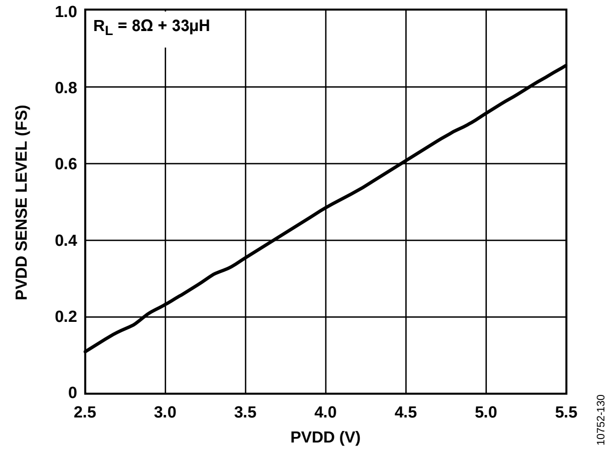


Figure 30. PVDD ADC Sense Level vs. PVDD Range, R_L = 8 Ω

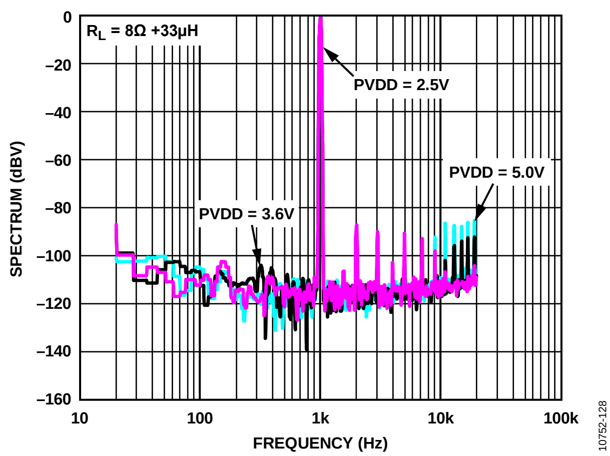


Figure 28. Output Spectrum vs. Frequency (FFT), P_{OUT} = 100 mW, R_L = 8 Ω

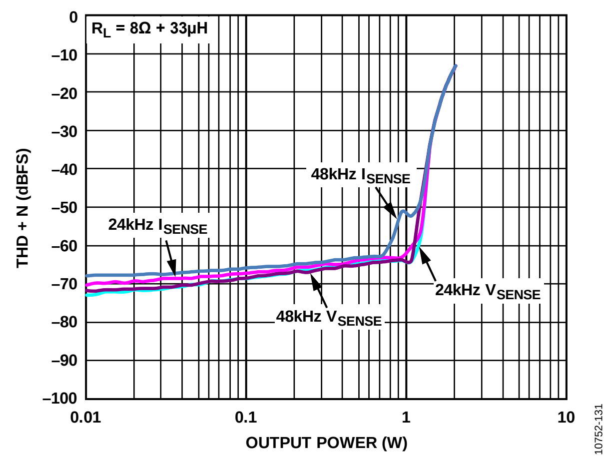


Figure 31. Sense ADC THD + N vs. Output Power into 8 Ω

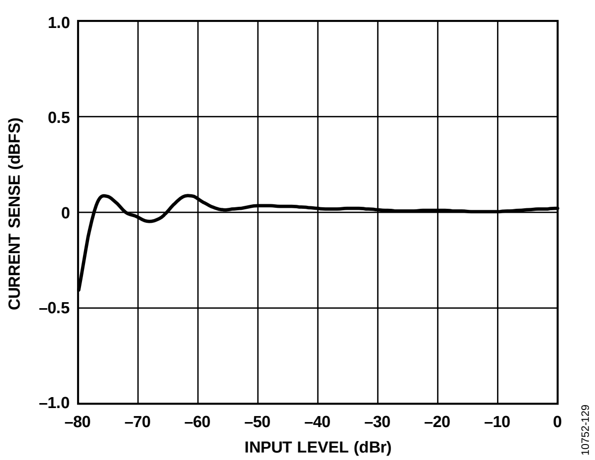


Figure 29. Current Sense Linearity

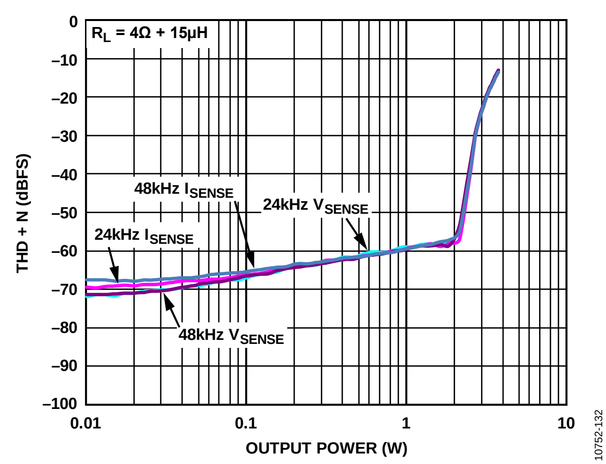


Figure 32. Sense ADC THD + N vs. Output Power into 4 Ω

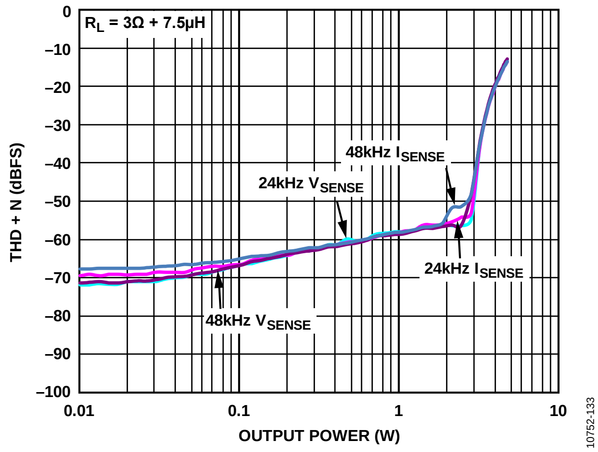


Figure 33. Sense ADC THD + N vs. Output Power into 3 Ω

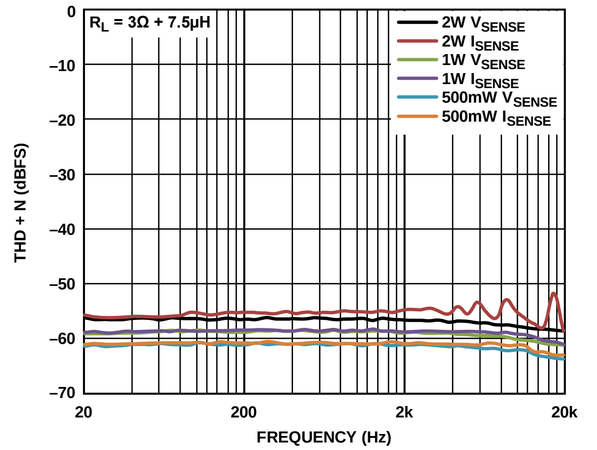


Figure 36. Sense ADC THD + N vs. Frequency, PVDD = 5 V, R_L = 3 Ω

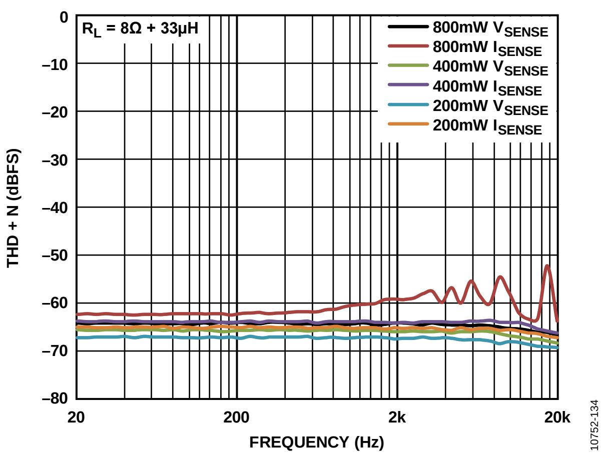


Figure 34. Sense ADC THD + N vs. Frequency, PVDD = 5 V, R_L = 8 Ω

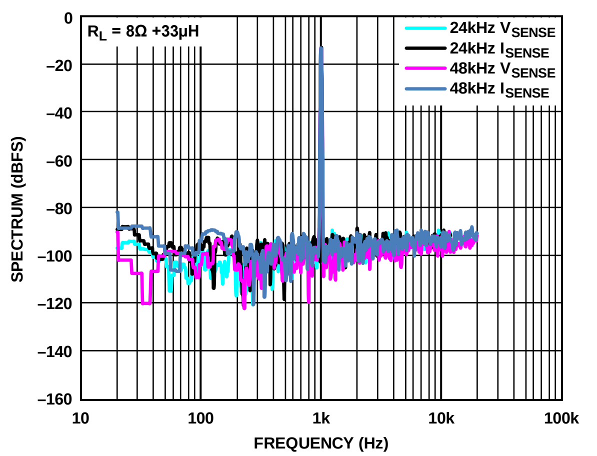


Figure 37. Output Spectrum of Sense ADC vs. Frequency (FFT), P_{OUT} = 100 mW, R_L = 8 Ω

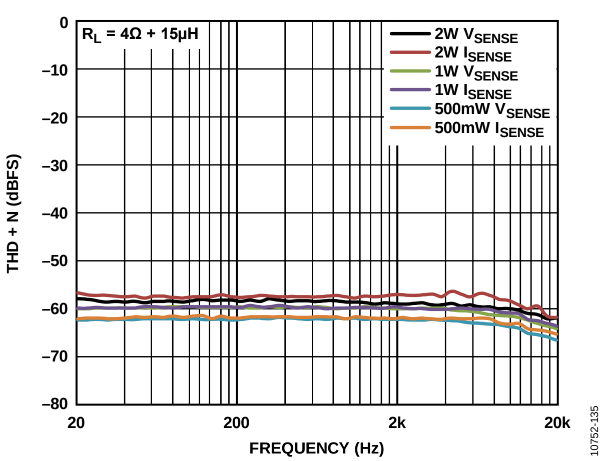


Figure 35. Sense ADC THD + N vs. Frequency, PVDD = 5 V, R_L = 4 Ω

THEORY OF OPERATION

OVERVIEW

The SSM4321 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing system cost. The SSM4321 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM4321 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits.

- Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do.
- Σ-Δ modulation reduces the amplitude of spectral components at high frequencies, thus reducing EMI emissions that might otherwise be radiated by speakers and long cable traces.
- Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs that incorporate multiple SSM4321 amplifiers.

The SSM4321 also integrates overcurrent and overtemperature protection.

POWER-DOWN OPERATION

The SSM4321 contains a clock loss detect circuit that works with the BCLK input clock. When no BCLK is present, the part automatically powers down all internal circuitry to its lowest power state. When a BCLK is returned, the part automatically powers up.

If BCLK is active but FSYNC or LRCLK is not present, the amplifier continues to operate, but the ADC, sense blocks, and digital processing are shut down, reducing quiescent current when the output sense data is not needed. The ADC shutdown feature is not available in PDM operating mode.

GAIN SELECTION

The gain of the SSM4321 can be set from 0 dB to 12 dB in 3 dB steps using the GAIN pin and one (optional) external resistor. The external resistor is used to select the 9 dB or 12 dB gain setting (see Table 6).

Table 6. Setting the Gain of the SSM4321 with the GAIN Pin

Gain Setting (dB)	GAIN Pin Configuration
0	Tie to GND
3	Open
6	Tie to PVDD
9	Tie to GND through a 47 kΩ resistor
12	Tie to PVDD through a 47 kΩ resistor

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audible pop in the speaker. Pops and clicks can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal.

The SSM4321 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM4321 uses three-level, Σ-Δ output modulation. Each output can swing from GND to PVDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to the constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUT+ and OUT−) is generated to follow the input voltage. The differential pulse density (V_{OUT}) is increased by raising the input signal level. Figure 38 depicts three-level, Σ-Δ output modulation with and without input stimulus.

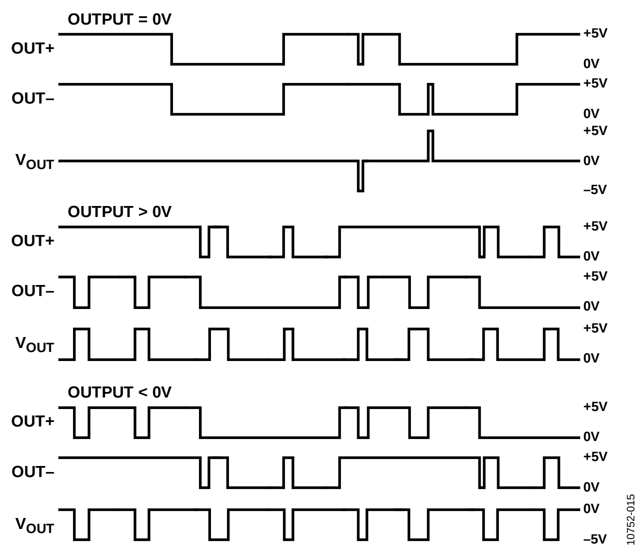


Figure 38. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

EMI NOISE

The SSM4321 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. For applications that have difficulty passing FCC Class B emission tests or experience antenna and RF sensitivity problems, the ultralow EMI architecture of the SSM4321 significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz.

EMI emission tests on the SSM4321 were performed in an FCC-certified EMI laboratory with a 1 kHz input signal, producing 0.5 W of output power into an 8 Ω load from a 5.0 V supply. The SSM4321 passed FCC Class B limits with 50 cm of unshielded twisted pair speaker cable. Note that reducing the power supply voltage greatly reduces radiated emissions.

OUTPUT CURRENT SENSING

The SSM4321 uses an external sense resistor to determine the output current flowing to the load. As shown in Figure 1, one end of the sense resistor is tied to one amplifier output pin (OUT+); the other end of the sense resistor is tied to the load, which is also connected to one sense input pin (SENSE−).

The voltage across the sense resistor is proportional to the load current and is sent to an analog-to-digital converter (ADC) running nominally at 128 f_S. The output of this ADC is downsampled using digital filtering. The downsampled signal is output at a rate of 8 kHz to 48 kHz on Slot 1 of the TDM bus. The 16-bit data is in signed fractional format.

The current sense output is scaled so that an output current of 0.75 A (6 V/8 Ω) with a 200 mΩ sense resistor results in full-scale output from the ADC. Table 7 lists the optimal sense resistor values for commonly used output loads.

Table 7. Optimal Sense Resistor for Typical Loads

Load Value (Ω)	Peak Current (A)	Sense Resistor (mΩ)
8	0.75	200
4	1.5	100
3	2	75

OUTPUT VOLTAGE SENSING

The output voltage level is monitored and sent to an ADC running nominally at 128 f_S. The output of this ADC is downsampled using digital filtering. The downsampled signal is output at a rate of 8 kHz to 48 kHz on Slot 2 of the TDM bus. The 16-bit data is in signed fractional format.

PVDD SENSING

The SSM4321 contains an 8-bit ADC that measures the voltage of the PVDD supply in real time. The output of the ADC is in 8-bit unsigned format and is presented on the 8 MSBs of Slot 3 on the TDM bus. The eight LSBs are driven low.

SERIAL DATA INPUT/OUTPUT

The SSM4321 includes circuitry to sense output current, output voltage, and the PVDD supply voltage. The output current, output voltage, and PVDD voltage are sent to ADCs. The output of these ADCs is available on the TDM or I^2S output serial port. A direct PDM bit stream of voltage and current data (or current and PVDD data) can also be selected.

TDM OPERATING MODE

The digitized output current, output voltage, and PVDD sense signals can be output on a TDM serial port. This serial port is always a slave and requires a bit clock (BCLK) and a frame synchronization signal (FSYNC) to operate. The output data is driven on the SDATAO/PDM_DATA pin at the IOVDD voltage. (See the Timing Diagrams, TDM Mode section.)

The FSYNC signal operates at the desired sample rate. A rising edge of the FSYNC signal indicates the start of a new frame. For proper operation, this signal should be one BCLK cycle wide, transitioning on a falling BCLK edge. The MSB of the Slot 1 data is output on the SDATAO/PDM_DATA pin one BCLK cycle later. The SDATAO signal should be latched on a rising edge of BCLK. Each slot is 64 BCLK cycles wide.

The SSM4321 can drive only four slots on its output, but it can work with 8 slots, 12 slots, or 16 slots. In this way, up to four SSM4321 devices can use the same TDM bus. At startup, the number of slots used is recognized automatically by the number of BCLK cycles between FSYNC pulses. Internal clocking is automatically generated from BCLK based on the determined BCLK rate.

The set of four TDM slots to be driven is determined by the configuration of the SLOT pin on the SSM4321 (see Table 8). The value of the SLOT pin must be stable at startup.

Table 8. TDM Slot Selection

Device Setting	SLOT Pin Configuration
TDM Slot 1 to Slot 4 used	Tie to IOVDD
TDM Slot 5 to Slot 8 used	Open
TDM Slot 9 to Slot 12 used	Tie to GND
TDM Slot 13 to Slot 16 used	Tie to IOVDD through a 47 kΩ resistor

The SSM4321 sets the SDATAO/PDM_DATA pin to a high impedance state when a slot is present that is not being driven. Connect a pull-down resistor to the SDATAO/PDM_DATA pin so that it is always in a known state.

With a single SSM4321 operating with four slots, Slot 1 is for the output current, Slot 2 is for the output voltage, Slot 3 is for the PVDD supply, and Slot 4 is not driven. With more than four slots, this pattern is repeated. Table 9 shows an example with three SSM4321 devices and 12 TDM slots.

Table 9. TDM Output Slot Example—Three SSM4321 Devices

TDM Slot	Data Present
1	Output current, Device 1
2	Output voltage, Device 1
3	PVDD voltage, Device 1
4	High-Z
5	Output current, Device 2
6	Output voltage, Device 2
7	PVDD voltage, Device 2
8	High-Z
9	Output current, Device 3
10	Output voltage, Device 3
11	PVDD voltage, Device 3
12	High-Z

I^2S AND LEFT JUSTIFIED OPERATING MODE

An I^2S or left justified output interface can be selected by reversing the pin connections for BCLK and FSYNC; that is, the I^2S LRCLK is connected to Ball D3 (BCLK_TDM/PDM_CLK/LRCLK_I2S), and the I^2S BCLK is connected to Ball D2 (FSYNC_TDM/ BCLK_I2S).

The I^2S interface requires 64 BCLK cycles per LRCLK cycle. The voltage information is sent when LRCLK is low, and the current information is sent when LRCLK is high. (See the Timing Diagrams, I^2S and Left Justified Modes section.)

The SLOT pin configures the I^2S or left justified output as follows (see Table 10).

- Selection of I^2S or left justified mode.
- Output of PVDD sense information. When PVDD data is output, eight bits are appended to the 16-bit voltage sense data to create a 24-bit output. The 16 MSBs represent the voltage data; the eight LSBs represent the PVDD data.
- Sample rate range. The sample rate ranges from 16 kHz to 48 kHz. A range of 32 kHz to 48 kHz is also allowed in low power I^2S mode.

Table 10. I^2S and Left Justified Slot Selection

Device Setting	BCLK Setting	SLOT Pin Configuration
I^2S mode at 16 kHz to 48 kHz; voltage and current data only	$64 \times f_S$	Tie to IOVDD
Left justified mode at 16 kHz to 48 kHz; voltage and current data only	$64 \times f_S$	Open
I^2S mode at 16 kHz to 48 kHz; PVDD data appended to voltage data	$64 \times f_S$	Tie to GND
Left justified mode at 16 kHz to 48 kHz; PVDD data appended to voltage data	$64 \times f_S$	Tie to IOVDD through a 47 kΩ resistor
Low power I^2S mode at 32 kHz to 48 kHz; voltage and current data only	$32 \times f_S$ or $64 \times f_S$	Tie to GND through a 47 kΩ resistor

MULTICHIP I²S OPERATING MODE

A special multichip I²S mode is enabled when the part is wired for TDM mode (BCLK and FSYNC not reversed) but the FSYNC signal has a 50% duty cycle. If the FSYNC signal consists of one-clock-cycle pulses, TDM operating mode is active instead.

The multichip I²S interface allows multiple chips to drive a single I²S bus. Each chip takes control of the bus every two or four frames (depending on the number of chips placed on the bus), allowing a maximum of four chips on the bus. The SLOT pin assignments determine the order of control. (See the Timing Diagrams, Multichip I²S Mode section.)

Each frame also contains a 1-bit ID code, which is appended to the current data in the frame. This code indicates the chip that sent the data for that frame. Table 11 provides the mapping of SLOT pin assignments to ID code.

Table 11. Multichip I²S Slot Selection

Chip No.	ID Code	SLOT Pin Configuration
1	0001	Tie to IOVDD
2	0010	Open
3	0100	Tie to GND
4	1000	Tie to IOVDD through a 47 kΩ resistor

The part is automatically configured for two-chip or four-chip operation, depending on the number of chips detected on the bus. The part starts up in four-chip operation, but after it detects that Slot 3 and Slot 4 are unused, the part switches to two-chip operation. For two-chip operation, the first and second slots must be used. If there are three chips on the bus, Slot 1 must be used along with any two other slots.

Table 12 lists the FSYNC and BCLK rates that are supported in multichip I²S mode.

Table 12. FSYNC and BCLK Rates in Multichip I²S Mode, f_S = 16 kHz to 48 kHz

Valid Slots	FSYNC Rate	BCLK Rate
1 and 2	$2 \times f_S$ (32 kHz to 96 kHz)	$128 \times f_S$ (2.048 MHz to 6.144 MHz)
1, 2, 3, 4	$4 \times f_S$ (64 kHz to 128 kHz)	$256 \times f_S$ (4.096 MHz to 12.288 MHz)

PDM OUTPUT MODE

By connecting the SLOT pin to GND through a 47 kΩ resistor, the 1-bit PDM data from the ADCs can be output directly. In PDM mode, a 1 MHz to 6.144 MHz clock must be provided on Ball D3 (BCLK_TDM/PDM_CLK/LRCLK_I2S). PDM data is sent on both edges of the clock and is output on Ball D1 (SDATAO/PDM_DATA). (See the Timing Diagrams, PDM Mode section.)

In PDM mode, Ball D2 (FSYNC_TDM/BCLK_I2S) is used to select the information that is output on the two possible channels (see Table 13).

Table 13. FSYNC_TDM Pin Settings for PDM Mode

Output Data	FSYNC_TDM Pin
Current data on rising edge; voltage data on falling edge	Tie to IOVDD
Current data on rising edge; PVDD data on falling edge	Tie to GND

TIMING DIAGRAMS, TDM MODE

TDM Mode, One Device

SLOT pin is tied to IOVDD.

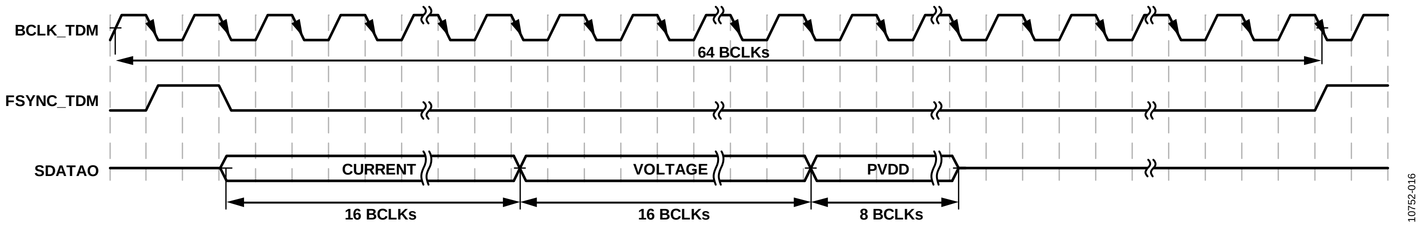


Figure 39. TDM Mode, One Device

TDM Mode, Two Devices

IC 1: SLOT pin is tied to IOVDD; IC 2: SLOT pin is open.

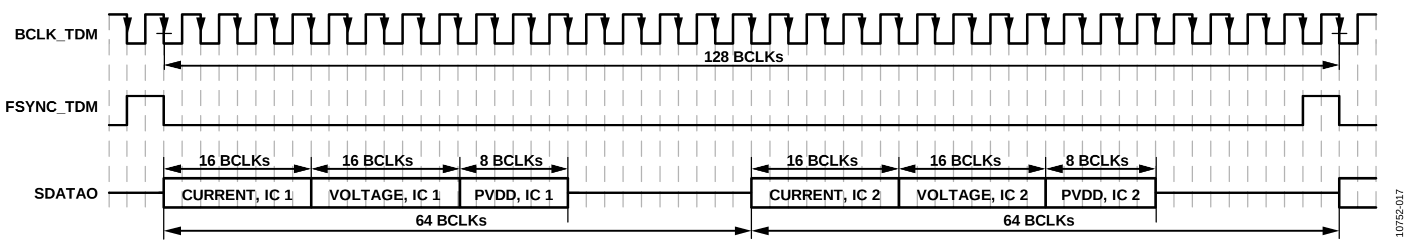


Figure 40. TDM Mode, Two Devices

TDM Mode, Three Devices

IC 1: SLOT pin is tied to IOVDD; IC 2: SLOT pin is open; IC 3: SLOT pin is tied to GND.

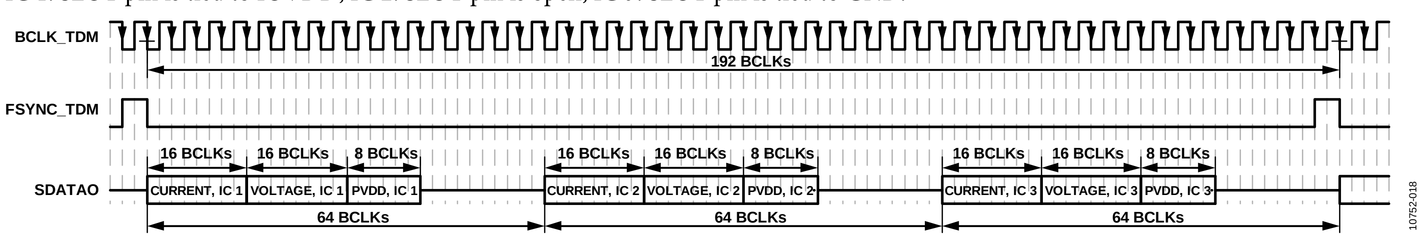


Figure 41. TDM Mode, Three Devices

TIMING DIAGRAMS, I²S AND LEFT JUSTIFIED MODES

I²S and Left Justified Modes with Voltage, Current, and PVDD Output, 64 × f_S

I²S output mode: SLOT pin is tied to GND.

Left justified output mode: SLOT pin is tied to IOVDD through a 47 kΩ resistor.

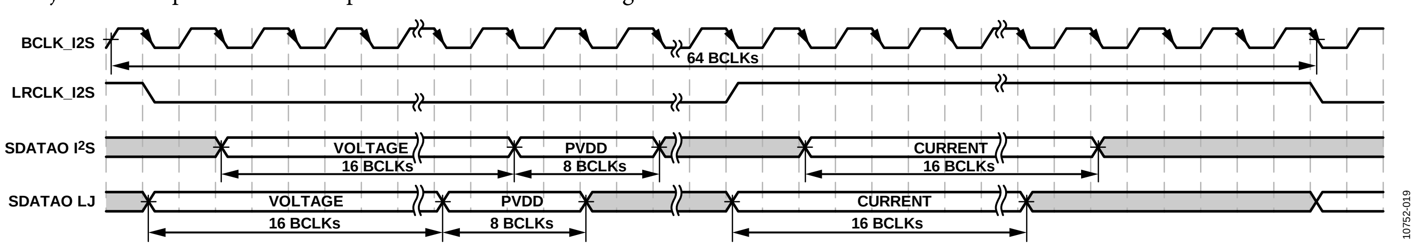


Figure 42. I²S and Left Justified Modes with Voltage, Current, and PVDD Output, 64 × f_S

I^2S and Left Justified Modes with Voltage and Current Output Only, 64 × f_S

I^2S output mode: SLOT pin is tied to IOVDD (or tied to GND through a 47 kΩ resistor for low power operation at 64 × f_S).
Left justified output mode: SLOT pin is open.

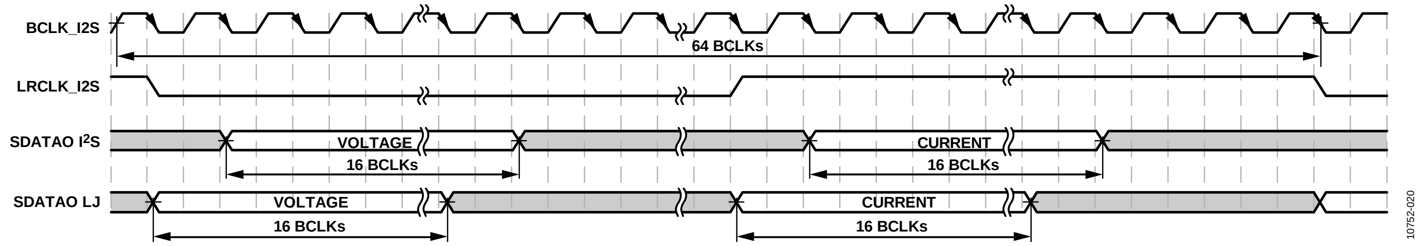


Figure 43. I^2S and Left Justified Modes with Voltage and Current Output Only, 64 × f_S

I^2S Low Power Mode with Voltage and Current Output Only, 32 × f_S

SLOT pin is tied to GND through a 47 kΩ resistor for low power operation at 32 × f_S.

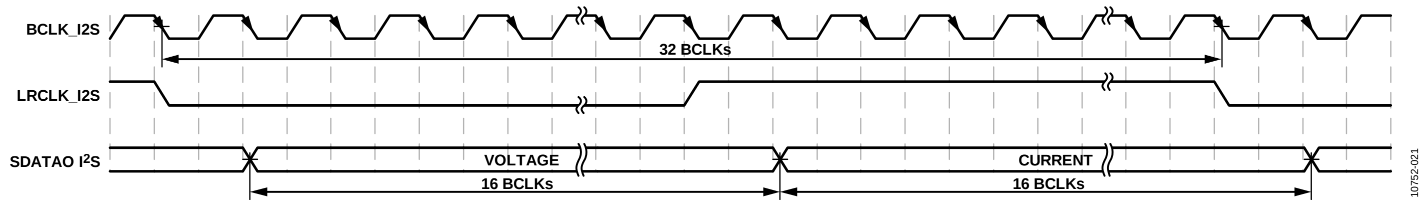


Figure 44. I^2S Low Power Mode with Voltage and Current Output Only, 32 × f_S

TIMING DIAGRAMS, MULTICHIP I^2S MODE

Multichip I^2S Mode with Two Devices on the Bus

IC 1: SLOT pin is tied to IOVDD; IC 2: SLOT pin is open.

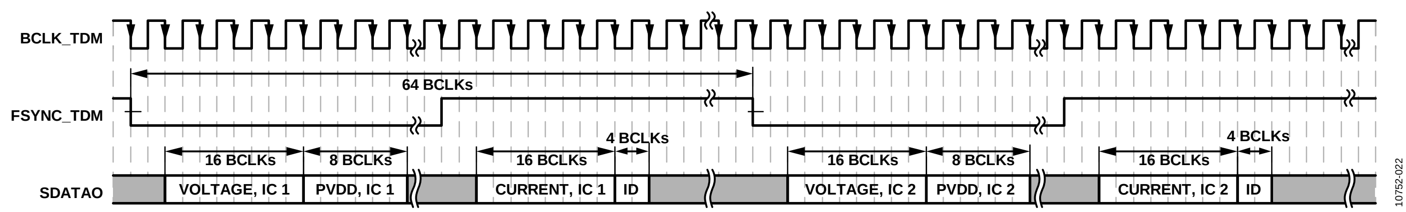


Figure 45. Multichip I^2S Mode with Two Devices on the Bus

Multichip I^2S Mode with Three or Four Devices on the Bus

IC 1: SLOT pin is tied to IOVDD; IC 2: SLOT pin is open; IC 3: SLOT pin is tied to GND; IC 4: SLOT pin is tied to IOVDD through a 47 kΩ resistor.

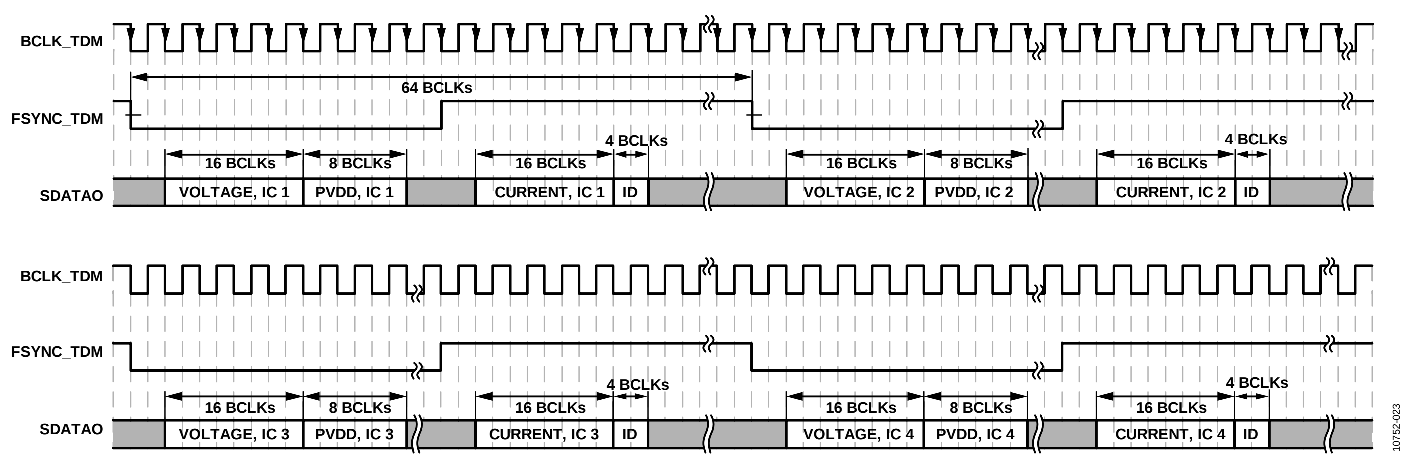


Figure 46. Multichip I^2S Mode with Three or Four Devices on the Bus

TIMING DIAGRAMS, PDM MODE

PDM Mode with Current and Voltage Output

SLOT pin is tied to GND through a 47 kΩ resistor; FSYNC_TDM pin is tied to IOVDD.

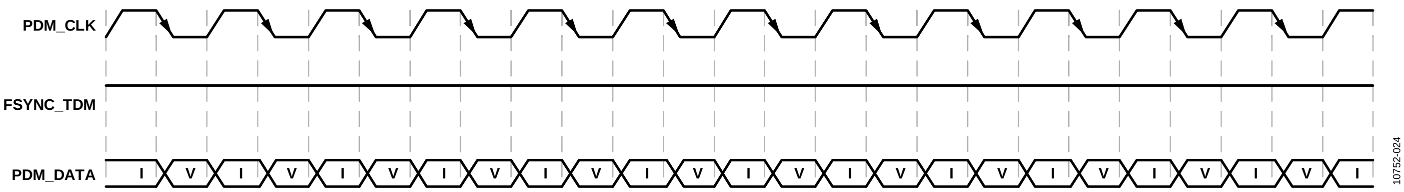


Figure 47. PDM Mode with Current and Voltage Output

PDM Mode with Current and PVDD Output

SLOT pin is tied to GND through a 47 kΩ resistor; FSYNC_TDM pin is tied to GND.

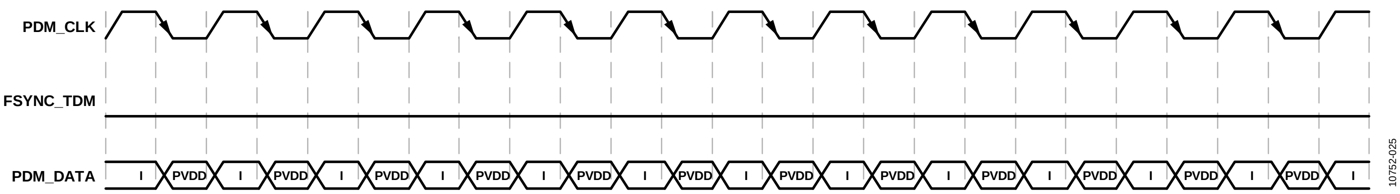


Figure 48. PDM Mode with Current and PVDD Output

APPLICATIONS INFORMATION

LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding helps to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layout isolates critical analog paths from sources of high interference. Separate high frequency circuits (analog and digital) from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be directly beneath the analog power plane, and, similarly, the digital ground plane should be directly beneath the digital power plane. There should be no overlap between the analog and digital ground planes or between the analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM4321 does not require input coupling capacitors if the input signal is biased from 1.0 V to PVDD − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor (C_{IN}) and the input impedance of the SSM4321 (80 kΩ) form a high-pass filter with a corner frequency determined by the following equation:

$$f_C = 1/(2\pi \times 80\ k\Omega \times C_{IN})$$

The input capacitor value and the dielectric material can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset voltage of the amplifier and the dc PSRR performance.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with a good quality, low ESL, low ESR capacitor, with a minimum value of 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1 µF capacitor as close as possible to the PVDD pin of the device. Placing the decoupling capacitors as close as possible to the SSM4321 helps to maintain efficient performance.

OUTLINE DIMENSIONS

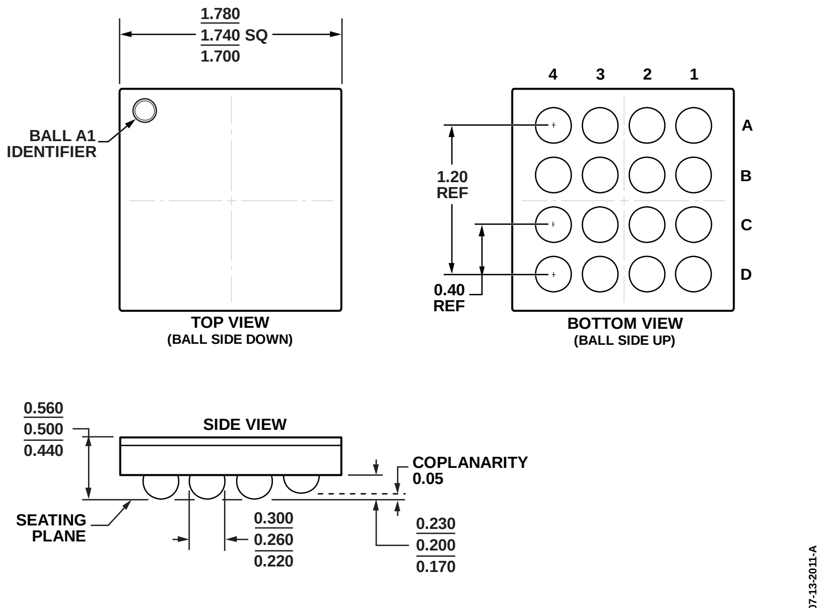


Figure 49. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]	Branding
SSM4321ACBZ-R7	−40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-15	Y4E
SSM4321ACBZ-RL	−40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-15	Y4E
EVAL-SSM4321Z		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] This package option is halide free.

NOTES

NOTES

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