1. FEATURES

- Small 3mm × 3mm MSOP package
- Ultra-small QFN package:
  2mm × 1.5mm × 0.4mm
- Wide supply range: 2.0V to 5.5V
- Low current consumption: 145μA
  (continuous-conversion mode)
- Programmable output data rate: 8SPS to 860SPS
- 50Hz and 60Hz rejection filter
- Single-cycle settling
- Internal low-drift voltage reference
- Internal oscillator
- I²C interface: four pin-selectable addresses
- Four single-ended or two differential inputs
- Programmable comparator
- Operating temperature range:
  –40°C to 125°C

2. APPLICATIONS

- Portable instrumentation
- Battery voltage and current monitoring
- Temperature measurement systems
- Consumer electronics
- Factory automation and process control

3. DESCRIPTION

The ADX113 device is precision, low-power, 16-bit, I²C-compatible, analog-to-digital converter (ADC) offered with MSOP-10 and QFN-10 packages. The ADX113 device incorporates a low-drift voltage reference and an oscillator. It also incorporates a programmable gain amplifier (PGA) and a digital comparator. These features, along with a wide operating supply range, make the ADX113 well suited for power- and space-constrained, sensor measurement applications.

The ADX113 performs conversions at data rates up to 860 samples per second (SPS). Internal digital filter provides flexible output data rate, from 8SPS to 860SPS. Additionally, it is optional to select 50Hz and 60Hz normal mode rejection filter. The PGA offers input ranges from ±256mV to ±6.144V, allowing precise large- and small-signal measurements. The ADX113 features an input multiplexer (MUX) that allows two differential or four single-ended input measurements. Use the digital comparator in the ADX113 for under- and overvoltage detection.

The ADX113 operates in either continuous-conversion mode or single-shot mode. The internal filter is single-cycle settling in both modes. The devices are automatically powered down after one conversion in single-shot mode; therefore, power consumption is significantly reduced during idle periods. See Table 1 for the order information.

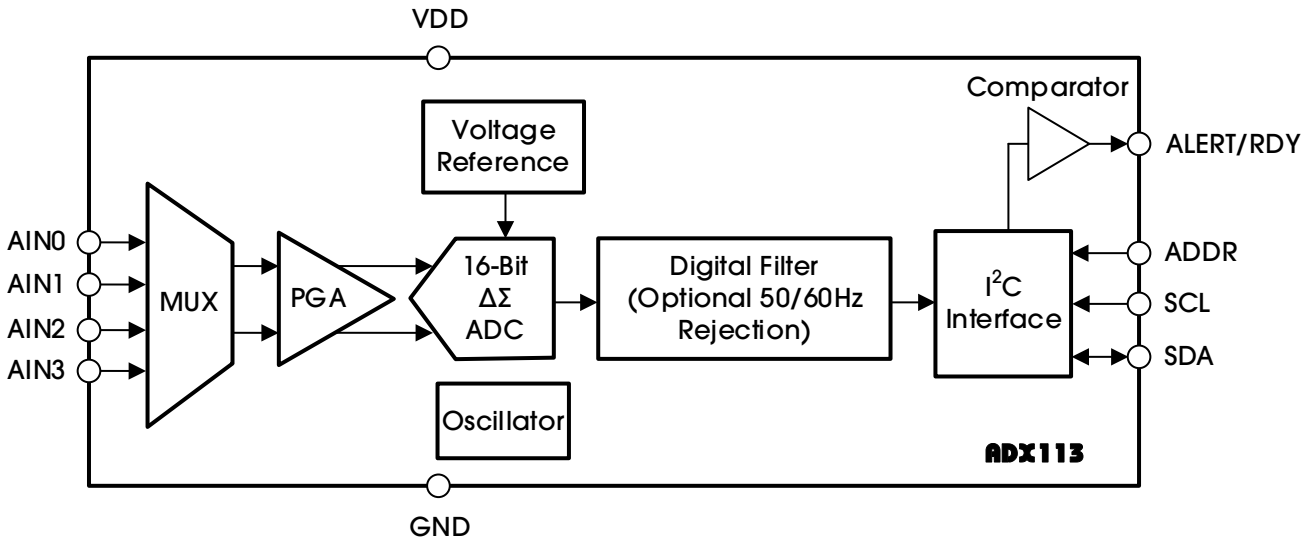

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Table 1 lists the order information.

Table 1. Order Information

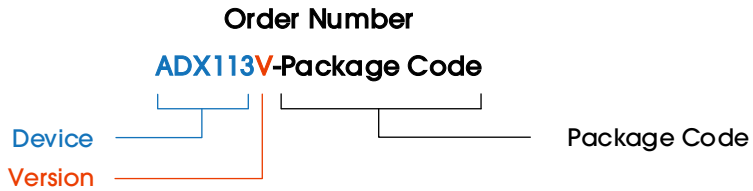
ORDER NUMBER[1]	CH (#)	BITS	PACKAGE	BODY SIZE (mm)	MARKING	ODR (SPS)	INTERFACE	COMPARATOR	TEMP SENSOR	50/60 REJECTION	OP. TEMP (°C)	PKG. OPTION
ADX113AMSOP10	2(4)	16	MSOP10	3 × 3	ADX113	860	I²C	Yes	No	Yes	–40-125	T/R-3000

Table 2. Family Selection Guide

ORDER NUMBER[1]	CH (#)	BITS	PACKAGE	BODY SIZE (mm)	MARKING	ODR (SPS)	INTERFACE	COMPARATOR	TEMP SENSOR	50/60 REJECTION	OP. TEMP (°C)	PKG. OPTION
ADX111AMSOP10	2(4)	16	MSOP10	3 × 3	ADX111	860	I²C	Yes	No	No	–40-125	T/R-3000
ADX111AQFN10	2(4)	16	QFN10	2 × 1.5	111	860	I²C	Yes	No	No	–40-125	T/R-4000
ADX112AMSOP10	2(4)	16	MSOP10	3 × 3	ADX112	860	SPI	No	Yes	No	–40-125	T/R-3000
ADX112AQFN10	2(4)	16	QFN10	2 × 1.5	112	860	SPI	No	Yes	No	–40-125	T/R-4000
ADX114AMSOP10	2(4)	16	MSOP10	3 × 3	ADX114	3571	SPI	No	Yes	Yes	–40-125	T/R-3000
ADX121AMSOP10	2(4)	20	MSOP10	3 × 3	ADX121	3571	I²C	Yes	No	Yes	–40-125	T/R-3000
ADX121AQFN10[2]	2(4)	20	QFN10	2 × 1.5	121	3571	I²C	Yes	No	Yes	–40-125	T/R-4000
ADX122AMSOP10	2(4)	20	MSOP10	3 × 3	ADX122	3571	SPI	No	No	Yes	–40-125	T/R-3000
ADX122AQFN10[2]	2(4)	20	QFN10	2 × 1.5	122	3571	SPI	No	No	Yes	–40-125	T/R-4000
ADX128AMSOP10[2]	2(4)	20	MSOP10	3 × 3	ADX128	7143	SPI	No	No	Yes	–40-125	T/R-3000
ADX128AQFN10[2]	2(4)	20	QFN10	2 × 1.5	128	7143	SPI	No	No	Yes	–40-125	T/R-4000
ADX125AMSOP10	2(4)	20	MSOP10	3 × 3	ADX125	3571	I²C	Yes	Yes	Yes	–40-125	T/R-3000
ADX126AMSOP10	2(4)	20	MSOP10	3 × 3	ADX126	3571	SPI	No	Yes	Yes	–40-125	T/R-3000
ADX125AQFN10[2]	2(4)	20	QFN10	2 × 1.5	125	3571	I²C	Yes	Yes	Yes	–40-125	T/R-4000
ADX126AQFN10[2]	2(4)	20	QFN10	2 × 1.5	126	3571	SPI	No	Yes	Yes	–40-125	T/R-4000
ADX131AQFN10[2]	2(4)	20	QFN10	2 × 1.5	131	440	I²C	Yes	No	Yes	–40-125	T/R-4000
ADX132AQFN10[2]	2(4)	20	QFN10	2 × 1.5	132	440	SPI	No	No	Yes	–40-125	T/R-4000
ADX123AMSOP10[2]	2(4)	20	MSOP10	3 × 3	ADX123	3571	Daisy Chain	No	No	Yes	–40-125	T/R-3000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: Available in the future.

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4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

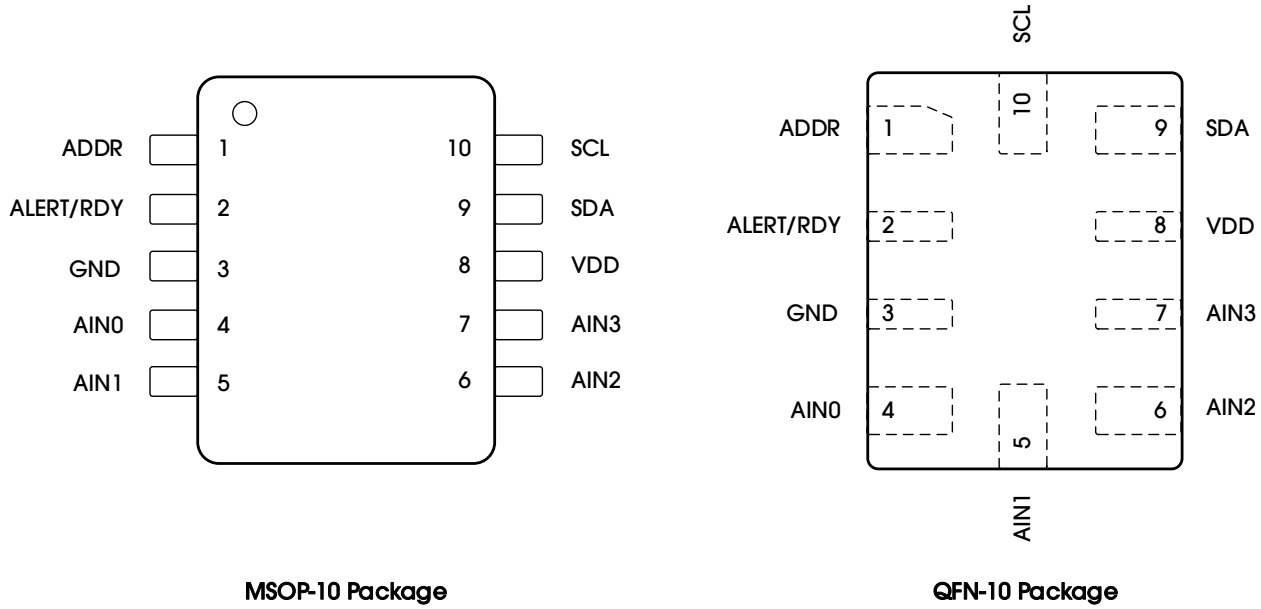

Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION	NAME	TYPE	DESCRIPTION
1	ADDR	Digital input	I²C slave address select
2	ALERT/RDY	Digital output	Comparator output or conversion ready, open drain, connected to a pull-up resistor
3	GND	Power	Ground
4	AIN0	Analog input	Analog input 0
5	AIN1	Analog input	Analog input 1
6	AIN2	Analog input	Analog input 2
7	AIN3	Analog input	Analog input 3
8	VDD	Power	Power supply. Connects a 0.1μF, power-supply decoupling capacitor to GND.
9	SDA	Digital I/O	Serial data. Transmits and receives data.
10	SCL	Digital input	Serial clock input. Locks data on SDA.

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5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the ADX113.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Power-Supply Voltage	VDD to GND	–0.3	7	V
Analog Input Voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital Input Voltage	SDA, SCL, ADDR, ALERT/RDY	GND – 0.3	5.5	V
Input Current, Continuous	Any pin except power supply pins	–10	10	mA
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–60	150	

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the ADX113.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the ADX113.

Table 6. Recommended Operating Conditions

PARAMETER	DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNITS
POWER SUPPLY						
Power Supply	VDD to GND		2		5.5	V
ANALOG INPUTS(1)						
Full-Scale Input Voltage Range(2)	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	FSR	±0.256		±6.144	V
Absolute Input Voltage		$V_{(AINx)}$	GND		VDD	V
DIGITAL INPUTS						
Digital Input Voltage		V_{DIG}	GND		5.5	V
TEMPERATURE RANGE						
Operating Ambient Temperature		T_A	–40		125	°C

Note 1: AIN_P and AIN_N denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.
Note 2: This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V must be applied to the analog inputs of the device. See Table 12 for more information.

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the ADX113.

Table 7. Thermal Information

PARAMETER	SYMBOL	MSOP-10	QFN-10	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	150	119	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	54	60	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	90	39	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	3	4	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	86	39	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	90	45	°C/W

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5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of ADX113. At VDD = 3.3V, data rate = 8SPS, and full-scale input voltage range (FSR) = ±2.048V (unless otherwise noted). Maximum and minimum specifications apply from T_A = –40°C to 125°C. Typical specifications are at T_A = 25°C.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Common-Mode Input Impedance		FSR = ±6.144V(1)		9		MΩ
		FSR = ±4.096V(1)		7		
		FSR = ±2.048V		6		
		FSR = ±1.024V		5		
		FSR = ±0.512V, FSR = ±0.256V		6		
Differential Input Impedance		FSR = ±6.144V(1)		26		MΩ
		FSR = ±4.096V(1)		17		
		FSR = ±2.048V		3		
		FSR = ±1.024V		1.5		
		FSR = ±0.512V, ±0.256V		0.9		MΩ
SYSTEM PERFORMANCE						
Resolution (No Missing Codes)			16			Bits
Data Rate	DR		8, 16 (20), 32, 64, 128, 250 (316), 475, 860			SPS
Data Rate Variation		All data rates	–7%		6%	
Output Noise			See NOISE PERFORMANCE section			
Integral Nonlinearity	INL	DR = 8SPS, FSR = ±2.048V(2)		0.5	1	LSB
Offset Error		FSR = ±2.048V, differential inputs	–2	0	2	LSB
		FSR = ±2.048V, single-ended inputs		±2		
Offset Drift Over Temperature		FSR = ±2.048V		0.005		LSB/°C
Long-Term Offset Drift		FSR = ±2.048V, T_A = 125°C, 1000 hrs		0.5		LSB
Offset Power-Supply Rejection		FSR = ±2.048V, DC supply variation		0.5		LSB/V
Offset Channel Match		Match between any two inputs		2		LSB
Gain Error(3)		FSR = ±2.048V, T_A = 25°C		0.01%	0.10%	
Gain Drift Over Temperature(3)		FSR = ±0.256V		8		ppm/°C
		FSR = ±2.048V		8	30	
		FSR = ±6.144V(1)		8		
Long-Term Gain Drift(3)		FSR = ±2.048V, T_A = 125°C, 1000 hrs		±0.05		%
Gain Power-Supply Rejection				70		ppm/V
Gain Match(3)		Match between any two gains		0.01%	0.05%	
Gain Channel Match		Match between any two inputs		0.03%	0.05%	
Common-Mode Rejection Ratio	CMRR	At DC, FSR = ±0.256V		>110		dB
		At DC, FSR = ±2.048V		>105		
		At DC, FSR = ±6.144V(1)		100		
		f_{CM} = 60Hz, DR = 8SPS		103		
		f_{CM} = 50Hz, DR = 8SPS		104		

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Normal-Mode Rejection Ratio	NMRR	ODR = 20SPS, Filter 50 = 1, Filter 60 = 0, 50Hz ± 1Hz		72	120		dB
		ODR = 20SPS, Filter 50 = 0, Filter 60 = 1, 60Hz ± 1Hz		73	128		dB
		ODR = 20SPS, Filter 50 = 1, Filter 60 = 1, 50Hz or 60Hz ± 1Hz		57	100		dB
DIGITAL INPUT/OUTPUT							
High-Level Input Voltage	V_{IH}			0.7 VDD		5.5	V
Low-Level Input Voltage	V_{IL}			GND		0.3 VDD	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 3mA		GND	0.15	0.4	V
Input Leakage Current		GND < V_{DIG} < VDD		–10		10	µA
POWER SUPPLY							
Supply Current	I_{VDD}	Power-down	T_A = 25°C		0.65	1	µA
						3.5	
		Operating	T_A = 25°C		145	170	
						300	
Power Dissipation	P_D	VDD = 5.0V			0.9		mW
		VDD = 3.3V			0.5		
		VDD = 2.0V			0.3		

Note 1: This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V must be applied to the analog inputs of the device. See Table 11 for more information.
Note 2: Best-fit INL; covers 98% of full-scale.
Note 3: Includes all errors from onboard PGA and voltage reference.

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5.6 TIMING REQUIREMENTS: I²C INTERFACE

Table 9 lists the timing requirements for the I²C interface. VDD = 2.0V to 5.5V, unless otherwise noted.

Table 9. Timing Requirements: I²C Interface

PARAMETER	SYMBOL	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0.01	0.4	0.01	3.4	MHz
Bus Free Time Between START and STOP Condition	t_{BUF}	600		160		ns
Hold Time After Repeated START Condition. (After this period, the first clock is generated.)	t_{HDSTA}	600		160		ns
Setup Time for A Repeated START Condition	t_{SUSTA}	600		160		ns
Setup Time for STOP Condition	t_{SUSTO}	600		160		ns
Data Hold Time	t_{HDDAT}	0		0		ns
Data Setup Time	t_{SUDAT}	100		10		ns
Low Period of the SCL Clock Pin	t_{LOW}	1300		160		ns
High Period for the SCL Clock Pin	t_{HIGH}	600		60		ns
Rise Time for Both SDA and SCL Signals(1)	t_F		300		160	ns
Fall Time for Both SDA and SCL Signals(1)	t_R		300		160	ns

Note: For high-speed mode maximum values, the capacitive load on the bus line must not exceed 400pF.

Figure 2 shows the I²C interface timing.

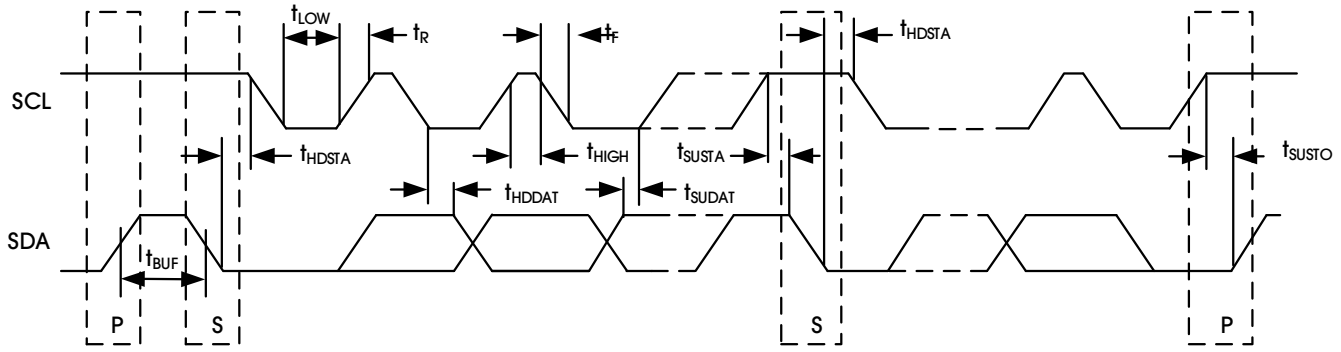

Figure 2. I²C Interface Timing

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5.7 TYPICAL CHARACTERISTICS

T_A = 25°C, VDD = 3.3V, FSR = ±2.048V, DR = 8SPS, unless otherwise noted.

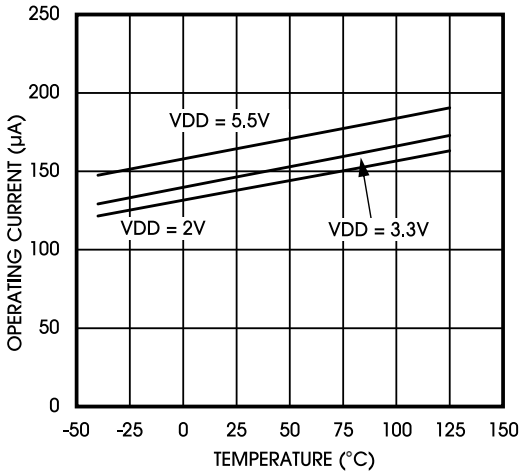

Figure 3. Operating Current vs Temperature

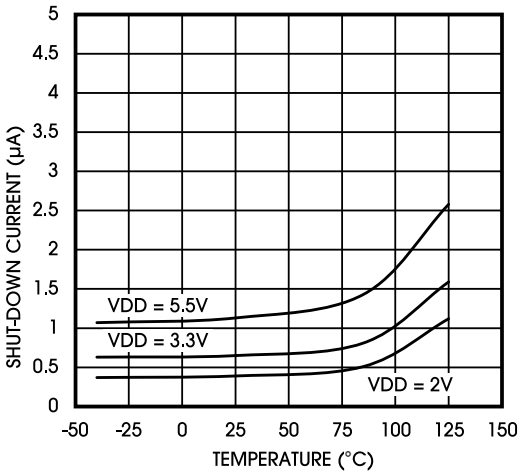

Figure 4. Power-Down Current vs Temperature

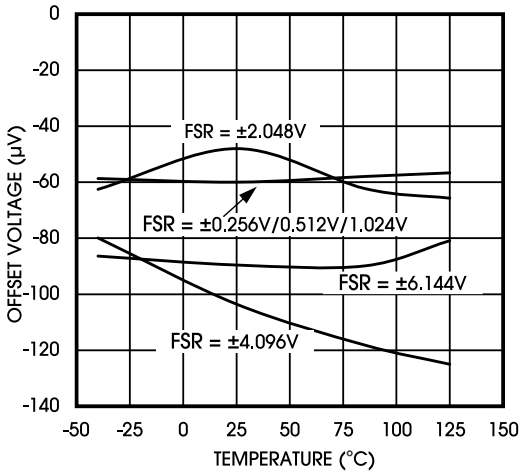

Figure 5. Single-Ended Offset Error vs Temperature

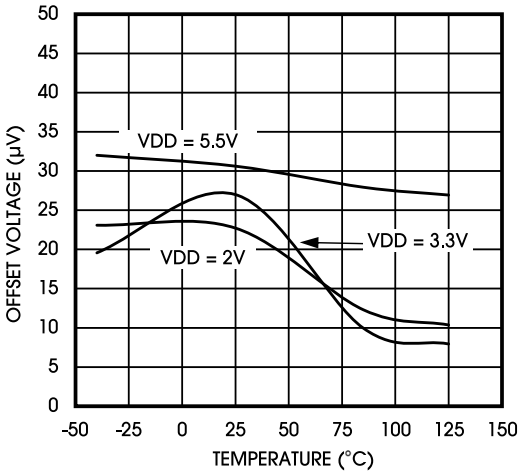

Figure 6. Differential Offset vs Temperature

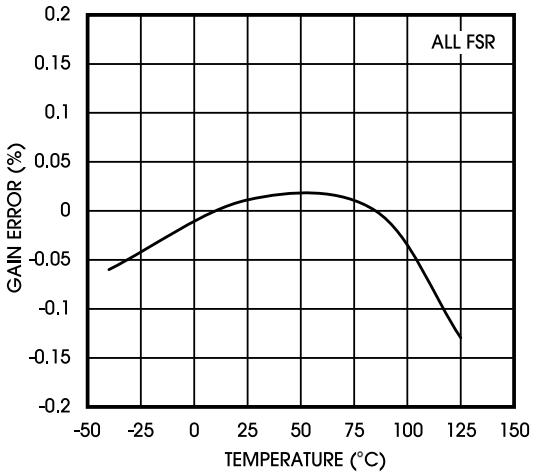

Figure 7. Gain Error vs Temperature

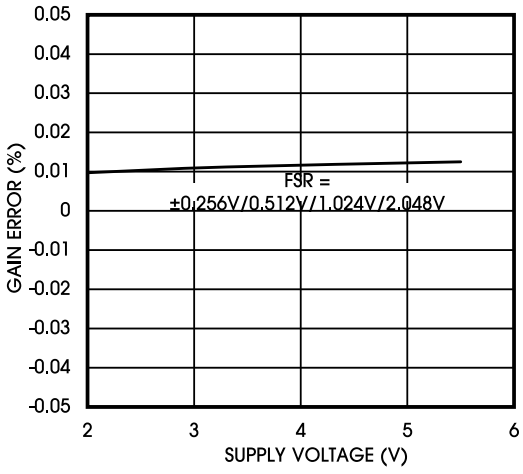

Figure 8. Gain Error vs Supply Voltage

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5.8 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, VDD = 3.3V, FSR = ±2.048V, DR = 8SPS, unless otherwise noted.

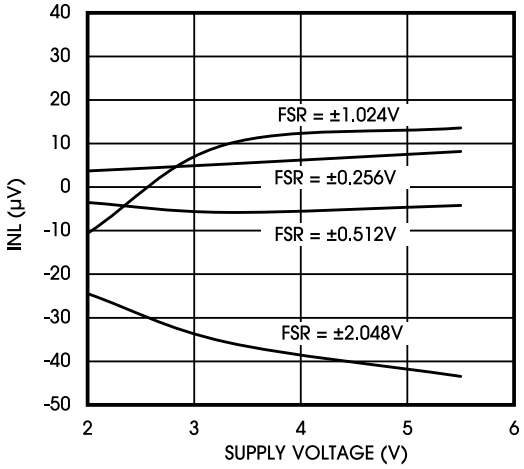

Figure 9. INL vs Supply Voltage

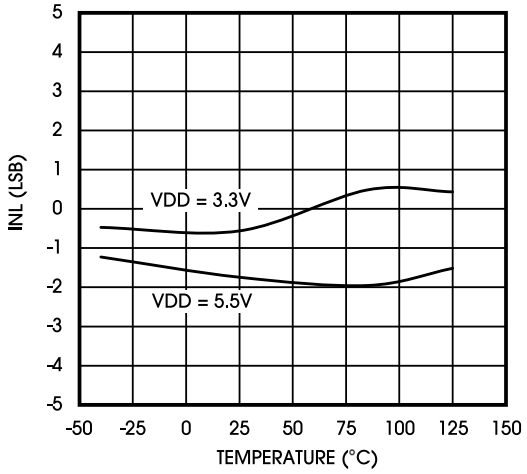

Figure 10. INL vs Temperature

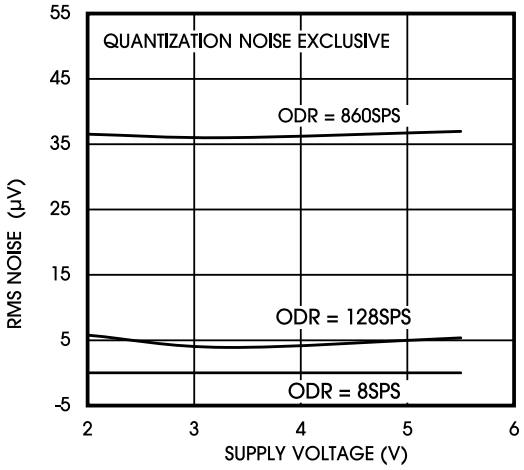

Figure 11. Noise vs Supply Voltage

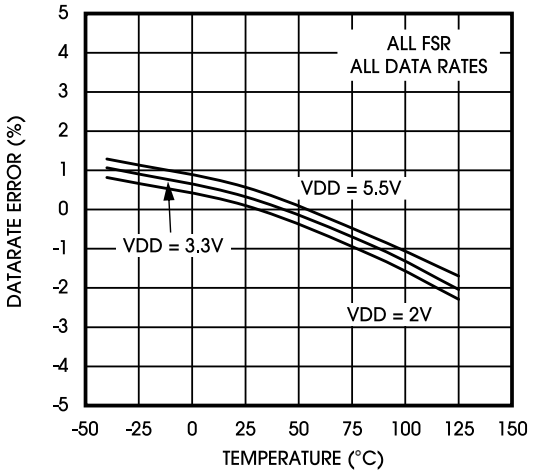

Figure 12. Data Rate vs Temperature

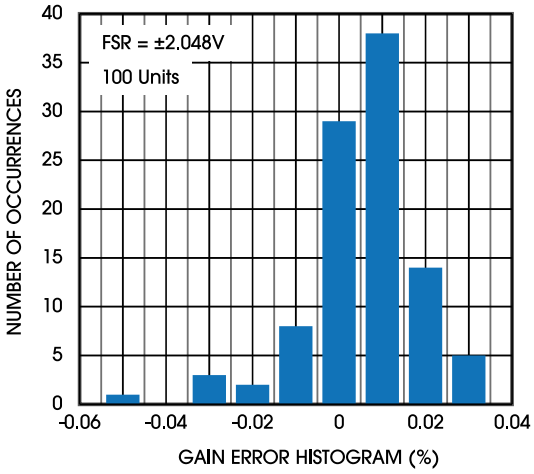

Figure 13. Gain Error Histogram

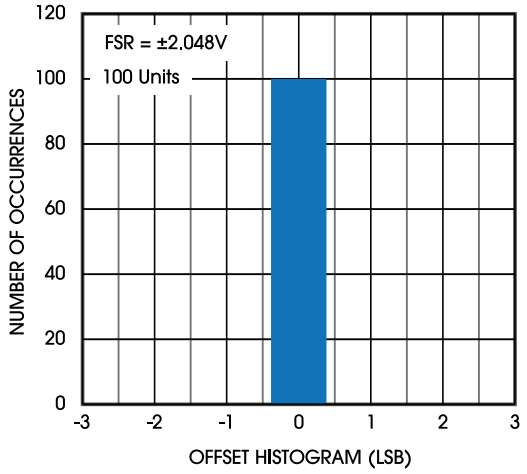

Figure 14. Offset Histogram

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5.9 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, VDD = 3.3V, FSR = ±2.048V, DR = 8SPS, unless otherwise noted.

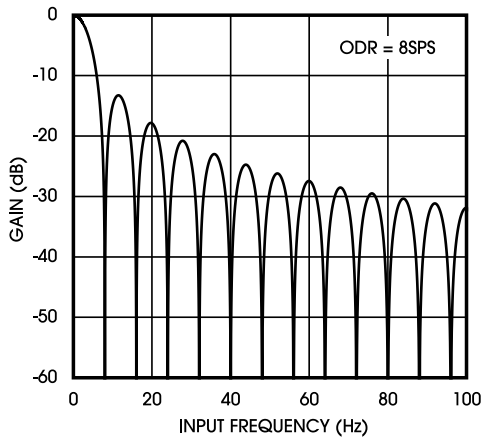

Figure 15. Digital Filter Frequency Response

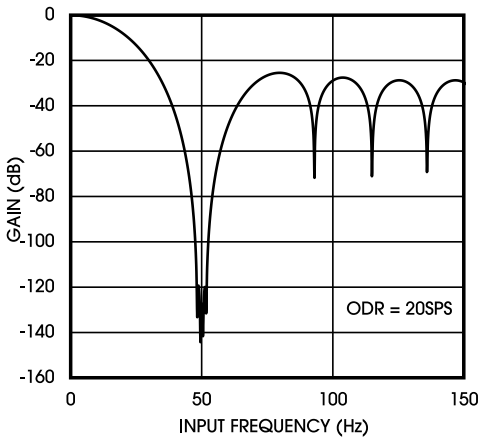

Figure 16. Digital Filter 50Hz Rejection Frequency Response

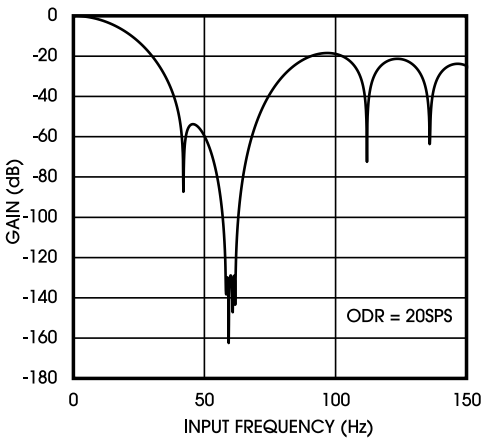

Figure 17. Digital Filter 60Hz Rejection Frequency Response

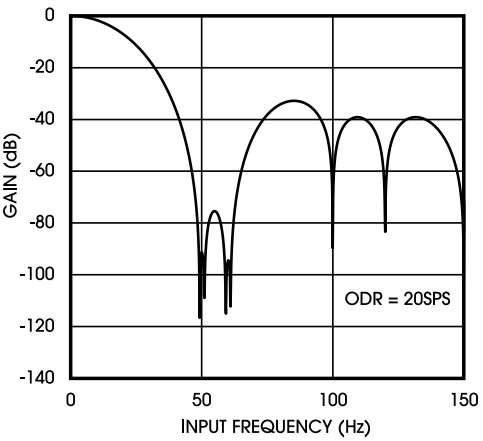

Figure 18. Digital Filter 50 & 60Hz Rejection Frequency Response

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6. PARAMETER MEASUREMENT INFORMATION

6.1 NOISE PERFORMANCE

Table 10 and Table 11 summarize the ADX113 noise performance, showing the RMS noise, peak-to-peak noise, effective resolution, and noise-free (peak-to-peak) resolution for various output data rates and gain settings. Data are representative of typical noise performance at T_A = 25°C with the differential inputs shorted together externally, when the ADC is continuously converting on a single channel. Table 10 shows the input-referred noise in units of μV_{RMS} for the conditions shown. Note that μV_{PP} values are shown in parenthesis. Table 11 shows the effective resolution calculated from μV_{RMS} values using Equation 1. The noise-free resolution calculated from peak-to-peak noise values using Equation 2 are shown in parenthesis.

$$\text{Effective Resolution} = \ln (\text{FSR} / V_{\text{RMS-Noise}}) / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln (\text{FSR} / V_{\text{PP-Noise}}) / \ln (2) \quad (2)$$

Table 10. Noise in μV_{RMS} (μV_{PP}) at VDD = 3.3V

DATA RATE (SPS)	FSR (Full-Scale Range)					
	±6.144V	±4.096V	±2.048V	±1.024V	±0.512V	±0.256V
8	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.625 (15.625)	7.8125 (7.8125)
16	187.5 (187.6)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.625 (15.625)	7.8125 (7.8125)
32	187.5 (187.7)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.625 (15.625)	7.8125 (7.8125)
64	187.5 (187.8)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.625 (15.625)	7.8125 (13.889)
128	187.5 (187.9)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.625 (17.333)	7.8125 (15.625)
250	187.5 (375)	125 (250)	62.5 (125)	31.25 (62.5)	15.625 (31.25)	7.8125 (23.4375)
475	187.5 (375)	125 (250)	62.5 (125)	31.25 (62.5)	15.625 (31.25)	7.8125 (32.986)
860	187.5 (520.8)	125 (319.4)	62.5 (152.7)	31.25 (90.2)	15.625 (38.19)	8.6799 (45.138)

Table 11. Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) at VDD = 3.3V

DATA RATE (SPS)	FSR (Full-Scale Range)					
	±6.144V	±4.096V	±2.048V	±1.024V	±0.512V	±0.256V
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
32	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
64	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.17)
128	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.85)	16 (15)
250	16 (15)	16 (15)	16 (15)	16 (15)	16 (15)	16 (14.41)
475	16 (15)	16 (15)	16 (15)	16 (15)	16 (15)	16 (13.92)
860	16 (14.52)	16 (14.64)	16 (14.7)	16 (14.47)	16 (14.71)	15.9 (13.47)

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7. DETAILED DESCRIPTION

7.1 OVERVIEW

The ADX113 is very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADX113 consists of a ΔΣ ADC core with an internal voltage reference, a clock oscillator and an I²C interface. It also integrates a programmable gain amplifier (PGA) and a programmable digital comparator. Figure 19 shows the functional block diagram of ADX113.

The ADX113 ADC core measures a differential signal, V_{IN}, that is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation of any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADX113 has two available conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request, stores the conversion value to an internal conversion register, and then enters a power-down state. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

7.2 FUNCTIONAL BLOCK DIAGRAM

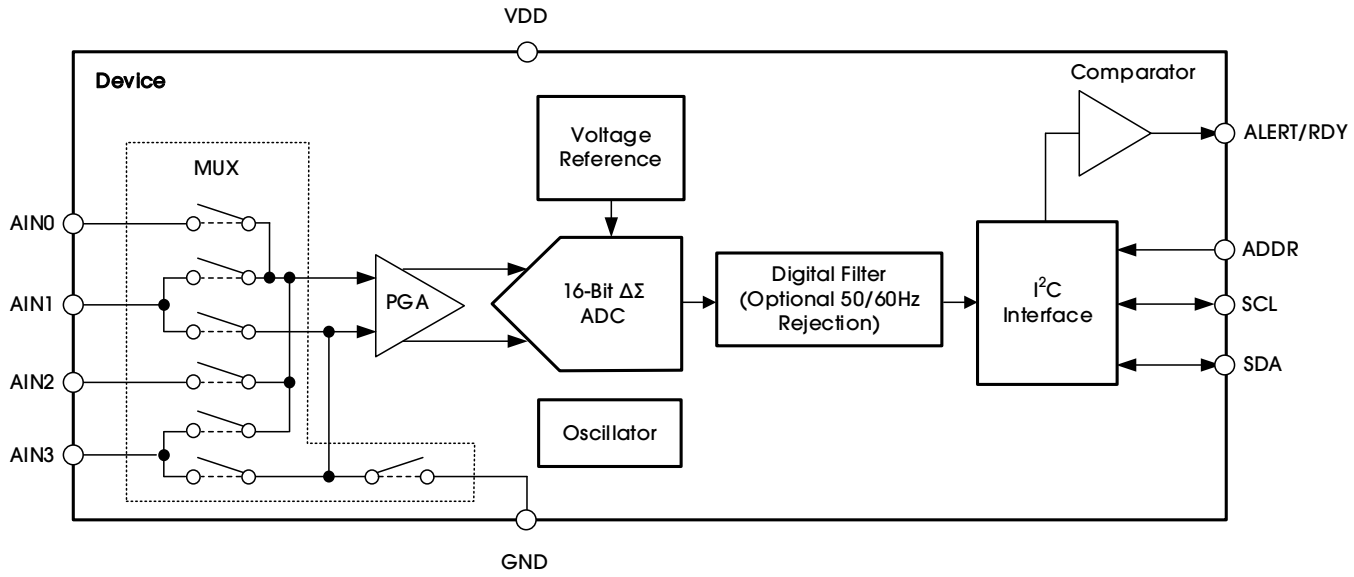

Figure 19. Functional Block Diagram

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7.3 FEATURE DESCRIPTION

7.3.1 MULTIPLEXER

The ADX113 contains an input multiplexer (MUX), as shown in Figure 20. Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 may be measured differentially to AIN3. The multiplexer is configured by bits MUX(2:0) in the CONFIG REGISTER. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

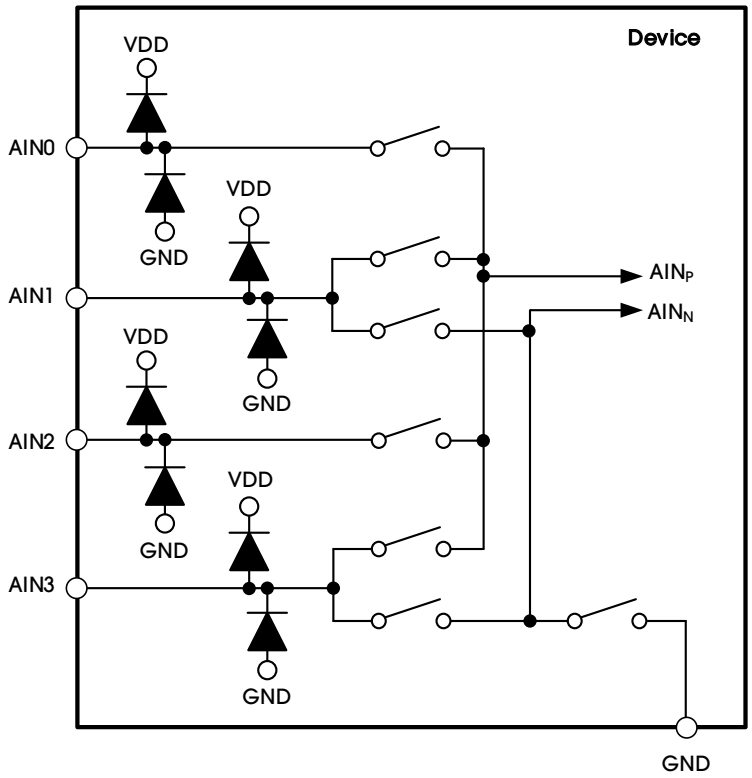

Figure 20. Input Multiplexer

Electrostatic discharge (ESD) diodes connected to VDD and GND protect the ADX113 analog inputs. Keep the absolute voltage of any input within the range shown in Equation 3 to prevent the ESD diodes from turning on.

$$GND - 0.3V < V_{(AINx)} < VDD + 0.3V \quad (3)$$

If the voltages on the input pins can potentially violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see Table 4).

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7.3.2 ANALOG INPUTS

The ADX113 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency (f_{MOD}). The ADX113 has a 1MHz internal oscillator that is further divided by a factor of 4 to generate f_{MOD} at 250kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. Figure 21 shows this structure. The capacitor values set the resistance and switching rate. Figure 22 shows the timing for the switches in Figure 21. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to $V_{(AINP)}$, C_{A2} to $V_{(AINN)}$, and C_B to ($V_{(AINP)}$ – $V_{(AINN)}$). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7V and C_B discharges to 0V. This charging draws a very small transient current from the source driving the ADX113 analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

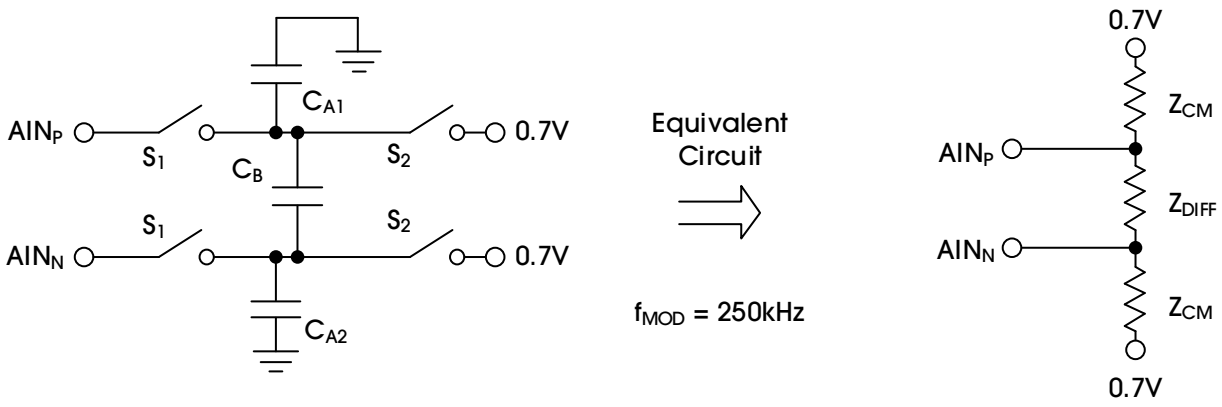

Figure 21. Simplified Analog Input Circuit

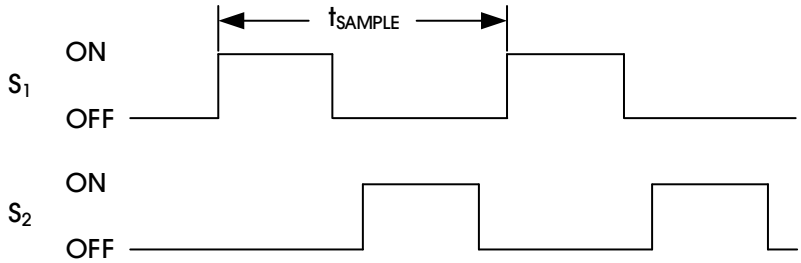

Figure 22. S_1 and S_2 Switch Timing

The common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6MΩ for the default full-scale range. In Figure 21, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the full-scale range. In Figure 21, the differential input impedance is Z_{DIFF}.

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Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADX113 input impedance may affect the measurement accuracy. For sources with high-output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.

7.3.3 FULL-SCALE RANGE (FSR) AND LSB SIZE

A programmable gain amplifier (PGA) is implemented before the ΔΣ ADC of the ADX113. The full-scale range is configured by bits PGA(2:0) in the CONFIG REGISTER and can be set to ±6.144V, ±4.096V, ±2.048V, ±1.024V, ±0.512V, ±0.256V. Table 12 shows the FSR together with the corresponding LSB size. Equation 4 shows how to calculate the LSB size from the selected full-scale range.

$$LSB = FSR / 2^{16} \quad (4)$$

Table 12. Full-Scale Range and Corresponding LSB Size

FSR	LSB SIZE
±6.144V(1)	187.5μV
±4.096V(1)	125μV
±2.048V	62.5μV
±1.024V	31.25μV
±0.512V	15.625μV
±0.256V	7.8125μV

Note: This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.

Analog input voltages must never exceed the analog input voltage limits given in the ABSOLUTE MAXIMUM RATINGS. If a VDD supply voltage is lower than the selected full-scale range, a full-scale ADC output code cannot be obtained. For example, with VDD = 3.3V and FSR = ±4.096V, only signals up to V_{IN} = ±3.3V can be measured. The code range that represents voltages of $|V_{IN}| > 3.3V$ is not used in this case.

It is highly recommended to use full-scale range one step higher than VDD supply voltage as the maximum full-scale range. For example, VDD = 2V, and ±2.048V are the best settings for a maximum full-scale range. Full-scale range larger than ±2.048V has no benefit.

7.3.4 VOLTAGE REFERENCE

The ADX113 has an integrated voltage reference. An external reference cannot be used with the device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the ELECTRICAL CHARACTERISTICS.

7.3.5 OSCILLATOR

The ADX113 has an integrated oscillator running at 1MHz. No external clock can be applied to operate the device. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

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7.3.6 OUTPUT DATA RATE AND CONVERSION TIME

The ADX113 offers programmable output data rates. Use the DR(2:0) bits in the CONFIG REGISTER to select output data rates of 8SPS, 16 (20) SPS, 32SPS, 64SPS, 128SPS, 250 (316) SPS, 475SPS, or 860SPS.

Furthermore, the ADX113 provides digital filter to reject 50Hz normal frequency and 60Hz normal frequency. Select one of the rejection filters or enable both 50Hz and 60Hz. If normal frequency rejection filter is enabled, the output data rate should be set to 20SPS, and any other output data rate is invalid.

Conversions in the ADX113 settle within a single cycle; thus, the conversion time is equal to 1 / DR.

7.3.7 DIGITAL COMPARATOR

The ADX113 features a programmable digital comparator that can issue an alert on the ALERT/RDY pin. The COMP_MODE bit in the CONFIG REGISTER configures the comparator as either a traditional comparator or a window comparator. In traditional comparator mode, the ALERT/RDY pin asserts (active low by default) when conversion data exceeds the limit set in the high-threshold register (Hi_thresh). The comparator then deasserts only when the conversion data falls below the limit set in the low-threshold register (Lo_thresh). In window comparator mode, the ALERT/RDY pin asserts when the conversion data exceed the Hi_thresh register or fall below the Lo_thresh register value.

In either window or traditional comparator mode, the comparator can be configured to latch after being asserted by the COMP_LAT bit in the CONFIG REGISTER. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can only be cleared by issuing an SMBus alert response or by reading the CONVERSION REGISTER. The ALERT/RDY pin can be configured as active high or active low by the COMP_POL bit in the CONFIG REGISTER. Operational diagrams for both the comparator modes are shown in Figure 23.

The comparator can also be configured to activate the ALERT/RDY pin only after a set number of successive readings exceed the threshold values set in the threshold registers (Hi_thresh and Lo_thresh). The COMP_QUE(1:0) bits in the CONFIG REGISTER configure the comparator to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin. The COMP_QUE(1:0) bits can also disable the comparator function, and put the ALERT/RDY pin into a high state.

7.3.8 CONVERSION READY PIN

The ALERT/RDY pin can also be configured as a conversion ready pin. Set the most-significant bit of the Hi_thresh register to 1 and the most-significant bit of Lo_thresh register to 0 to enable the pin as a conversion ready pin. The COMP_POL bit continues to function as expected. Set the COMP_QUE(1:0) bits to any 2-bit value other than 11 to keep the ALERT/RDY pin enabled, and allow the conversion ready signal to appear at the ALERT/RDY pin output. The COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion ready pin, ALERT/RDY continues to require a pullup resistor. The ADX113 provides an approximately 8μs conversion ready pulse on the ALERT/RDY pin at the end of each conversion in continuous-conversion mode, as shown in Figure 24. In single-shot mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to 0.

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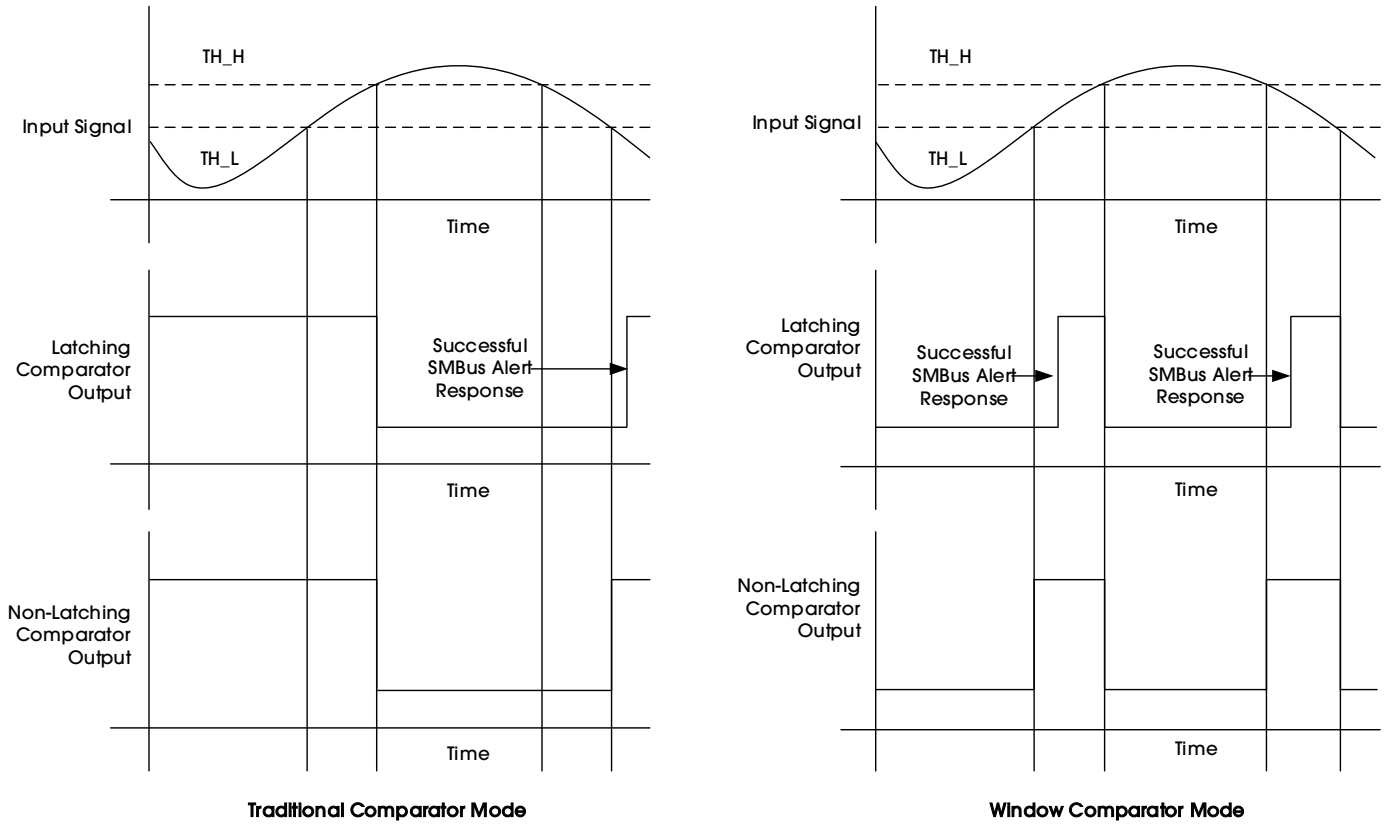

Figure 23. ALERT Pin Timing Diagram

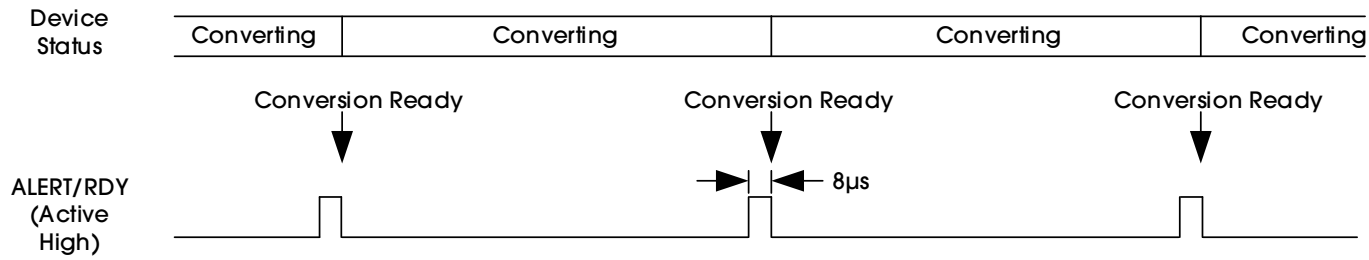

Figure 24. Conversion Ready Pulse in Continuous-Conversion Mode

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7.3.9 SMBus Alert Response

In latching comparator mode (COMP_LAT = 1), the ALERT/RDY pin asserts when the comparator detects a conversion that exceeds the upper or lower threshold value. This assertion is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I²C address. If conversion data exceed the upper or lower threshold values after being cleared, the pin reasserts. This assertion does not affect conversions that are already in progress. The ALERT/RDY pin is an open-drain output. This architecture allows several devices to share the same interface bus. When disabled, the pin holds a high state so that the pin does not interfere with other devices on the same bus line.

When the master senses that the ALERT/RDY pin has latched, the master issues an SMBus alert command (00011001) to the I²C bus. Any ADX113 data converters on the I²C bus with the ALERT/RDY pins asserted respond to the command with the slave address. If more than one ADX113 on the I²C bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert determines which device clears assertion. The device with the lowest I²C address always wins arbitration. If a device loses arbitration, the device does not clear the comparator output pin assertion. The master then repeats the SMBus alert response until all devices have the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a 1 if signals exceed the high threshold, and a 0 if signals exceed the low threshold.

7.4 Device Functional Modes

7.4.1 Reset and Power-Up

The ADX113 resets on power-up and sets all the bits in the CONFIG REGISTER to the respective default settings. The ADX113 enters a power-down state after completion of the reset process. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADX113 relieves systems with tight power-supply requirements from encountering a surge during power-up.

The ADX113 responds to the I²C general-call reset commands. When the ADX113 receives a general call reset command (06h), an internal reset is performed as if the device is powered-up.

7.4.2 Operating Modes

The ADX113 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the CONFIG REGISTER selects the respective operating mode.

7.4.2.1 Single-Shot Mode

When the MODE bit in the CONFIG REGISTER is set to 1, the ADX113 enters a power-down state, and operate in single-shot mode. This power-down state is the default state for the ADX113 when power is first applied. Although powered down, the devices still respond to commands. The ADX113 remains in this power-down state until a 1 is written to the operational status (OS) bit in the CONFIG REGISTER. When the OS bit is asserted, the device powers up in approximately 25μs, resets the OS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the OS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the CONFIG REGISTER.

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7.4.2.2 CONTINUOUS-CONVERSION MODE

In continuous-conversion mode (MODE bit set to 0), the ADX113 performs conversions continuously. When a conversion is complete, the ADX113 places the result in the CONVERSION REGISTER and immediately begin another conversion. When writing new configuration settings, the currently ongoing conversion completes with the previous configuration settings. Thereafter, continuous conversions with the new configuration settings start. To switch to single-shot conversion mode, write a 1 to the MODE bit in the CONFIG REGISTER or reset the device.

7.4.3 DUTY CYCLING FOR LOW POWER

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADX113 supports duty cycling that yields significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADX113 in power-down state with a data rate set to 860SPS can be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). A conversion at 860SPS only requires approximately 1.2ms, so the ADX113 enters power-down state for the remaining 123.8ms. In this configuration, the ADX113 consumes approximately 1/100th the power that is otherwise consumed in continuous-conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADX113 offers lower data rates that do not implement duty cycling and also offer improved noise performance if required.

7.5 PROGRAMMING

7.5.1 I²C INTERFACE

The ADX113 communicates through an I2C interface. I2C is a two-wire open-drain interface that supports multiple devices and masters on a single bus. Devices on the I2C bus only drive the bus lines low by connecting them to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors, so the bus wires are always high when no device is driving them low. As a result of this configuration, two devices cannot conflict. If two devices drive the bus simultaneously, there is no driver contention.

Communication on the I2C bus always takes place between two devices, one acting as the master and the other as the slave. Both the master and slave can read and write, but the slave can only do so under the direction of the master. Some I2C devices can act as a master or slave, but the ADX113 can only act as a slave device.

An I2C bus consists of two lines: SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I2C bus in groups of eight bits. To send a bit on the I2C bus, drive the SDA line to the appropriate level while SCL is low (a low on SDA indicates the bit is zero; a high indicates the bit is one). After the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I2C bus is held idle for more than 25ms, the bus times out.

The I2C bus is bidirectional; that is, the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The ADX113 cannot act as a master, and therefore can never drive SCL.

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Most of the time the bus is idle; no communication occurs, and both lines are high. When communication takes place, the bus is active. Only a master device can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high, and the data line goes from high to low. A STOP condition occurs when the clock line is high, and the data line goes from low to high.

After the master issues a START condition, the master sends a byte that indicates with which slave device to communicate. This byte is called the address byte. Each device on an I²C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether the master wishes to read from or write to the slave device.

Every byte (address and data) transmitted on the I²C bus is acknowledged with an acknowledge bit. When the master finishes sending a byte (eight data bits) to a slave, the master stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master completes reading a byte, the master pulls SDA low to acknowledge this completion to the slave. The master then sends a clock pulse to clock the bit. The master always drives the clock line.

If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low. A not-acknowledge is performed by simply leaving SDA high during an acknowledge cycle.

When the master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated start condition.

The TIMING REQUIREMENTS section shows a timing diagram for the ADX113 I²C communication.

7.5.1.1 I²C ADDRESS SELECTION

The ADX113 has one address pin, ADDR, that configures the I²C address of the device. This pin can be connected to GND, VDD, SDA, or SCL, allowing for four different addresses to be selected with one pin, as shown in Table 13. The state of address pin ADDR is sampled continuously. Use the GND, VDD, and SCL addresses first. If SDA is used as the device address, hold the SDA line low for at least 100ns after the SCL line goes low to make sure the device decodes the address correctly during I²C communication.

Table 13. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN CONNECTION	SLAVE ADDRESS
GND	1001000
VDD	1001001
SDA	1001010
SCL	1001011

7.5.1.2 I²C GENERAL CALL

The ADX113 responds to the I²C general call address (0000000) if the eighth bit is 0. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110 (06h), the ADX113 resets the internal registers and enter a power-down state.

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7.5.1.3 I²C SPEED MODES

The I²C bus operates at one of three speeds. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz; and high-speed mode (also called Hs mode) allows a clock frequency of up to 3.4MHz. The ADX113 is fully compatible with all three modes.

No special action is required to use the ADX113 in standard or fast mode, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of 00001xxx following the START condition, where xxx are bits unique to the Hs-capable master. This byte is called the Hs master code, and is different from normal address bytes; the eighth bit does not indicate read/write status. The ADX113 does not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. Upon receiving a master code, the ADX113 switches on Hs mode filters, and communicate at up to 3.4MHz. The ADX113 switches out of Hs mode with the next STOP condition.

For more information on high-speed mode, consult the I²C specification.

7.5.2 SLAVE MODE OPERATIONS

The ADX113 acts as slave receivers or slave transmitters. The ADX113 cannot drive the SCL line as slave devices.

7.5.2.1 RECEIVE MODE

In slave receive mode, the first byte transmitted from the master to the slave consists of the 7-bit device address followed by a low R/$\overline{W}$ bit. The next byte transmitted by the master is the ADDRESS POINTER REGISTER. The ADX113 then acknowledge receipt of the Address Pointer register byte. The next two bytes are written to the address given by the register address pointer bits, P(2:0). The ADX113 acknowledges each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

7.5.2.2 TRANSMIT MODE

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high R/$\overline{W}$ bit. This byte places the slave into transmit mode and indicates that the ADX113 is being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the register address pointer bits, P(2:0). This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master may terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

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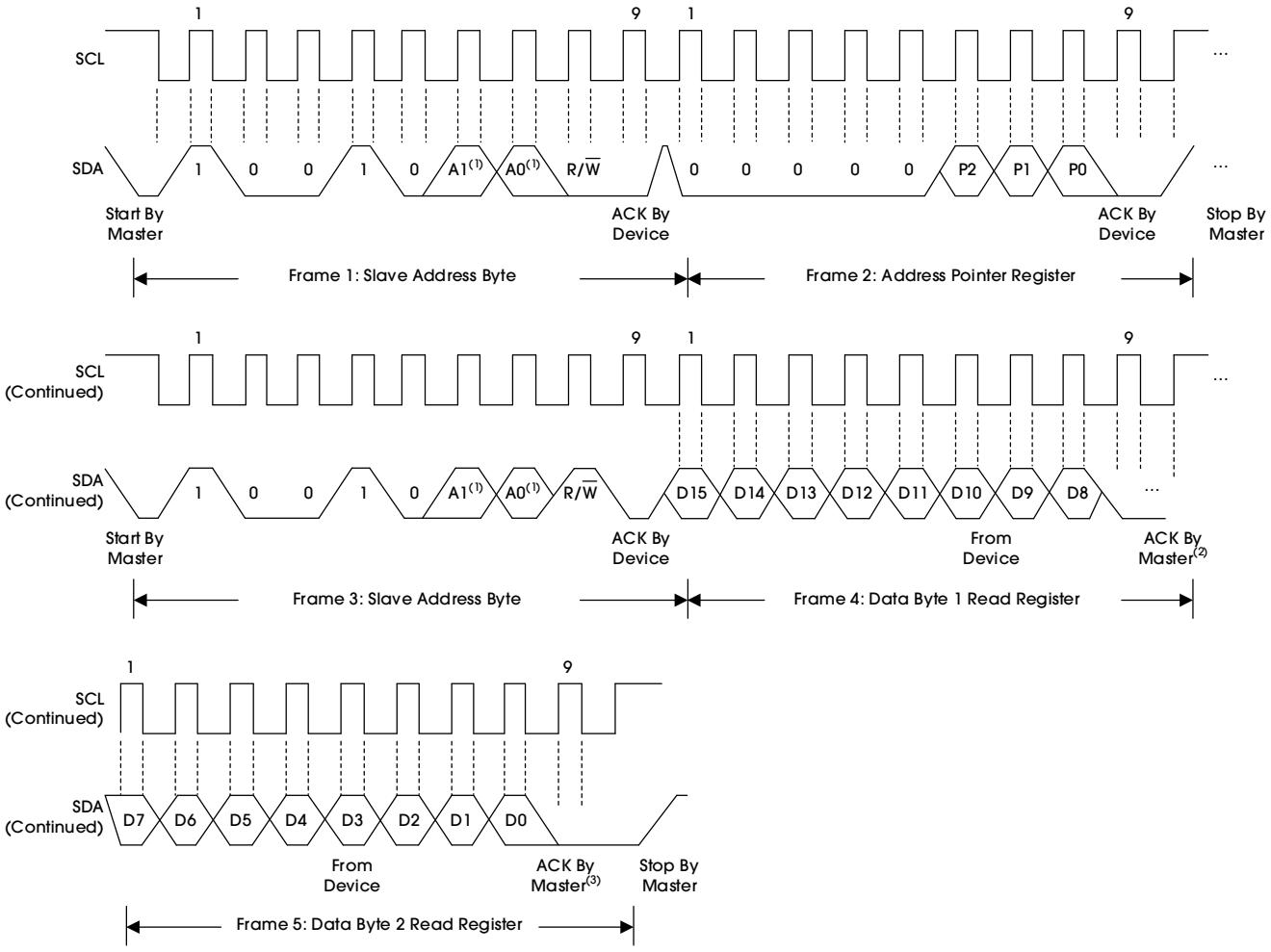
7.5.3 WRITING TO AND READING FROM THE REGISTERS

To access a specific register from the ADX113, the master must first write an appropriate value to register address pointer bits P(2:0) in the ADDRESS POINTER REGISTER. The Address Pointer register is written to directly after the slave address byte, low R/$\overline{W}$ bit, and a successful slave acknowledgment. After the Address Pointer register is written, the slave acknowledges, and the master issues a STOP or a repeated START condition.

When reading from the ADX113, the previous value written to bits P(2:0) determines the register that is read. To change which register is read, a new value must be written to P(2:0). To write a new value to P(2:0), the master issues a slave address byte with the R/$\overline{W}$ bit low, followed by the Address Pointer register byte. No additional data has to be transmitted, and a STOP condition can be issued by the master. The master can now issue a START condition and send the slave address byte with the R/$\overline{W}$ bit high to begin the read. Figure 25 details this sequence. If repeated reads from the same register are desired, there is no need to continually send the Address Pointer register, because the ADX113 stores the value of P(2:0) until it is modified by a write operation. However, for every write operation, the Address Pointer register must be written with the appropriate values.



(1) The values of A0 and A1 are determined by the ADDR pin.
(2) Master can leave SDA high to terminate a single-byte read operation.
(3) Master can leave SDA high to terminate a two-byte read operation.

Figure 25. Timing Diagram for Reading from ADX113

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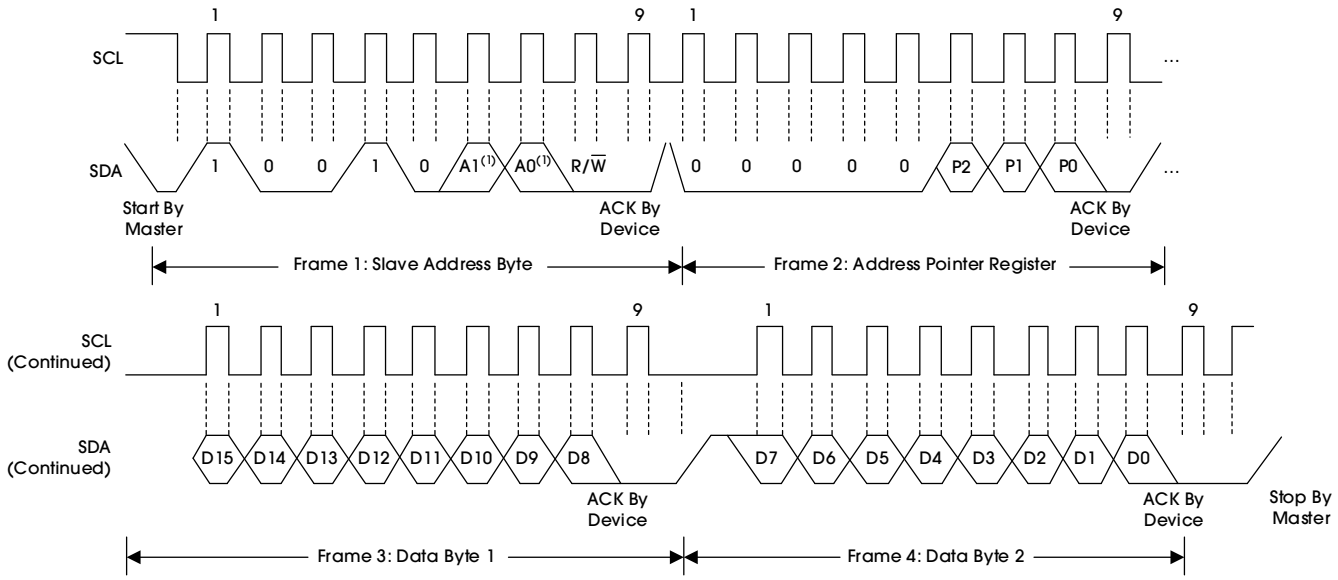
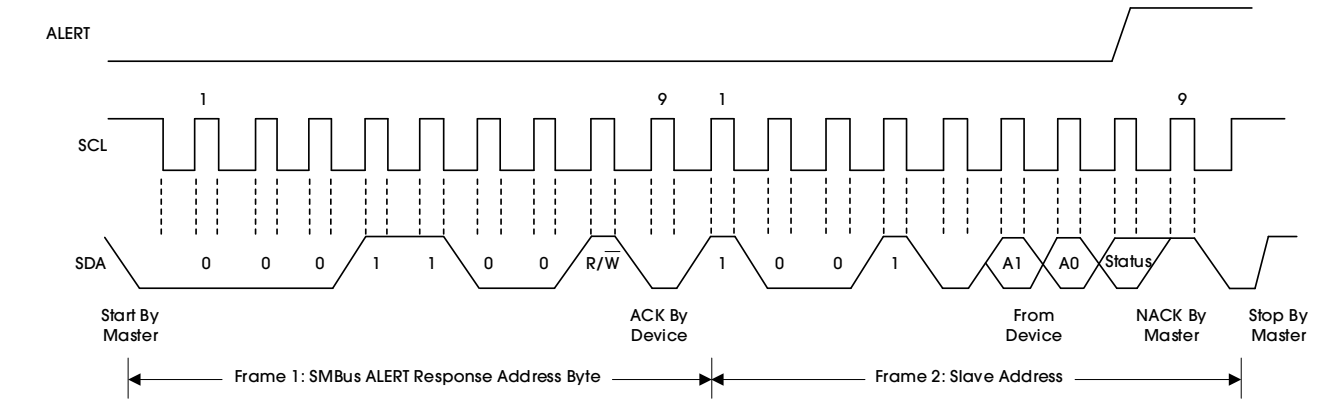


(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 26. Timing Diagram for Writing to ADX113



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 27. Timing Diagram for SMBus Alert Response

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7.5.4 DATA FORMAT

The ADX113 provides 16 bits of data in binary two's complement format. A positive full-scale (+FS) input produces an output code of 7FFFh and a negative full-scale (–FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 14 summarizes the ideal output codes for different input signals.

Table 14. Input Signal versus Ideal Output Code

INPUT SIGNAL $V_{IN} = (V_{AINP} - V_{AINN})$	IDEAL OUTPUT CODE (EXCLUDES THE EFFECTS OF NOISE, INL, OFFSET, AND GAIN ERRORS)
≥ +FS ($2^{15} - 1$) / 2^{15}	7FFFh
+FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

Figure 28 shows code transitions versus input voltage.

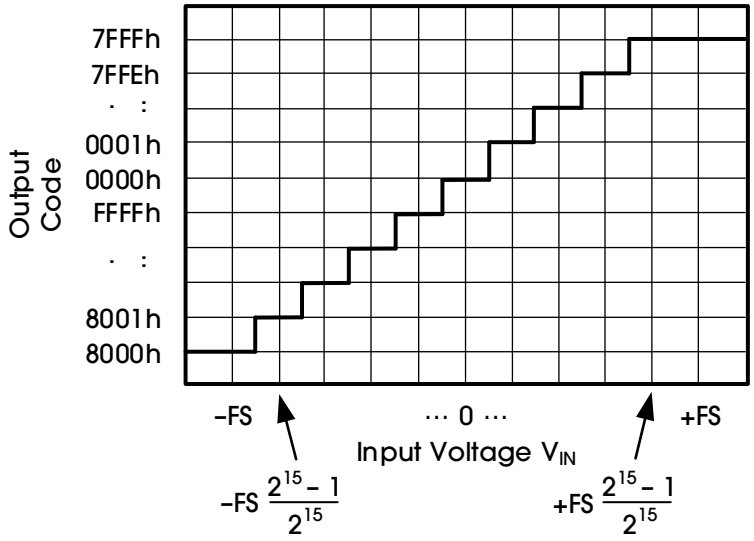

Figure 28. Code Transition Diagram

Note: Single-ended signal measurements, where V_{AINN} = 0V and V_{AINP} = 0V to +FS, only use the positive code range from 0000h to 7FFFh. However, because of device offset, the ADX113 can still output negative codes in case V_{AINP} is close to 0V.

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8. REGISTER MAPS

The ADX113 has 6 registers that are accessible through the I²C interface using the ADDRESS POINTERREGISTER. The CONVERSION REGISTER contains the result of the last conversion. The CONFIG REGISTER and CONFIG_EXTRA are used to change the ADX113 operating modes and query the status of the device. Device ID shows the ID. The other two registers, Lo_thresh and Hi_thresh, set the threshold values used for the comparator function.

Table 15. Register Map

ADDRESS	REGISTER	DEFAULT VALUE	READ/WRITE	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	CONVERSION	0000h	Read only	D15	D14	D13	D12	D11	D10	D9	D8
				D7	D6	D5	D4	D3	D2	D1	D0
0x01	CONFIG	8583h	Read/Write	OS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
				CR2	CR1	CR0	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE1	COMP_QUE0
0x02	CMP_TL	8000h	Read/Write	TL15	TL14	TL13	TL12	TL11	TL10	TL9	TL8
				TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
0x03	CMP_TH	7FFFh	Read/Write	TH15	TH14	TH13	TH12	TH11	TH10	TH9	TH8
				TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
0x06	CONFIG_EXTRA	0800h	Read/Write	FILT50	FILT60	RSV	RSV	RSV	RSV	RSV	RSV
				RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
0x07	DEVICE_ID	3000h	Read only	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
				RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV

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8.1.1 ADDRESS POINTER REGISTER (ADDRESS = N/A) [RESET = N/A]

All four registers are accessed by writing to the Address Pointer register; see Figure 25.

Table 16. Address Pointer Register

7	6	5	4	3	2	1	0
0	0	0	0	0	P(2:0)		
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Address Pointer Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:2	Reserved	W	0h	Always write 0h
1:0	P(2:0)	W	0h	Register address pointer 000: Conversion register 001: Config register 010: Lo_thresh register 011: Hi_thresh register 101: CONFIG_EXTRA 110: DEVICE_ID Others: Reserved

8.1.2 CONVERSION REGISTER (P[2:0] = 0H) [RESET = 0000H]

The 16-bit Conversion register contains the result of the last conversion in binary two's complement format. Following power-up, the Conversion register is cleared to 0, and remains 0 until the first conversion is completed.

Table 18. Conversion Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Conversion Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	D(15:0)	R	0000h	16-bit conversion result

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8.1.3 CONFIG REGISTER (P[2:0] = 1H) [RESET = 8583H]

The 16-bit Config register is used to control the operating mode, input selection, data rate, full-scale range, and comparator modes.

Table 20. Config Register

15	14	13	12	11	10	9	8
OS	MUX(2:0)			PGA(2:0)			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR(2:0)			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE(1:0)	
R/W-4h			R/W-0h	R/W-0h	R/W-0h	R/W-3h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Config Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	OS	R/W	1h	Operational status or single-shot conversion start This bit determines the operational status of the device. OS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0: No effect 1: Start a single conversion (when in power-down state) When reading: 0: Device is currently performing a conversion. 1: Device is not currently performing a conversion.
14:12	MUX(2:0)	R/W	0h	Input multiplexer configuration These bits configure the input multiplexer. 000: AIN_P = AIN0 and AIN_N = AIN1 (default) 001: AIN_P = AIN0 and AIN_N = AIN3 010: AIN_P = AIN1 and AIN_N = AIN3 011: AIN_P = AIN2 and AIN_N = AIN3 100: AIN_P = AIN0 and AIN_N = GND 101: AIN_P = AIN1 and AIN_N = GND 110: AIN_P = AIN2 and AIN_N = GND 111: AIN_P = AIN3 and AIN_N = GND
11:9	PGA(2:0)	R/W	2h	Programmable gain amplifier configuration These bits set the FSR of the programmable gain amplifier. 000: FSR = ±6.144V(1) 001: FSR = ±4.096V(1) 010: FSR = ±2.048V (default) 011: FSR = ±1.024V 100: FSR = ±0.512V 101: FSR = ±0.256V 110: FSR = ±0.256V 111: FSR = ±0.256V Note: This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.
8	MODE	R/W	1h	Device operating mode This bit controls the operating mode. 0: Continuous-conversion mode 1: Single-shot mode or power-down state (default)

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BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	DR(2:0)	R/W	4h	Data rate These bits control the data rate setting. 000: 8SPS 001: 16SPS (20SPS when 50/60 filter is enabled) 010: 32SPS 011: 64SPS 100: 128SPS (default) 101 : 250SPS (316SPS when 50/60 filter is enabled) 110: 475SPS 111 : 860SPS
4	COMP_MODE	R/W	0h	Comparator mode This bit configures the comparator operating mode. 0: Traditional comparator (default) 1: Window comparator
3	COMP_POL	R/W	0h	Comparator polarity This bit controls the polarity of the ALERT/RDY pin. 0: Active low (default) 1: Active high
2	COMP_LAT	R/W	0h	Latching comparator This bit controls whether the ALERT/RDY pin latches after being asserted or clears after conversions are within the margin of the upper and lower threshold values. 0: Nonlatching comparator. The ALERT/RDY pin does not latch when asserted (default). 1: Latching comparator. The asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master. The device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line.
1:0	COMP_QUE(1:0)	R/W	3h	Comparator queue and disable These bits perform two functions. When set to 11, the comparator is disabled and the ALERT/RDY pin is set to a high-impedance state. When set to any other value, the ALERT/RDY pin and the comparator function are enabled, and the set value determines the number of successive conversions exceeding the upper or lower threshold required before asserting the ALERT/RDY pin. 00: Assert after one conversion 01: Assert after two conversions 10: Assert after four conversions 11: Disable comparator and set ALERT/RDY pin to high-impedance (default)

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8.1.4 LO_THRESH (P[2:0] = 2H) [RESET = 8000H] AND HI_THRESH (P[2:0] = 3H) [RESET = 7FFFH] REGISTERS

The upper and lower threshold values used by the comparator are stored in two 16-bit registers in two's complement format. The comparator is implemented as a digital comparator; therefore, the values in these registers must be updated whenever the PGA settings are changed.

The conversion-ready function of the ALERT/RDY pin is enabled by setting the Hi_thresh register MSB to 1 and the Lo_thresh register MSB to 0. To use the comparator function of the ALERT/RDY pin, the Hi_thresh register value must always be greater than the Lo_thresh register value. The threshold register formats are shown in Table 22. When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode, and provides a continuous-conversion ready pulse when in continuous-conversion mode.

Table 22. Lo_thresh Register

15	14	13	12	11	10	9	8
Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset							

Table 23. Hi _thresh Register

15	14	13	12	11	10	9	8
Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset							

Table 24. Lo_thresh and Hi_thresh Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:0	Lo_thresh(15:0)	R/W	8000h	Low threshold value
15:0	Hi_thresh(15:0)	R/W	7FFFh	High threshold value

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8.1.5 CONFIG_EXTRA REGISTER (P[2:0] = 6H) [RESET = 0080H]

The 16-bit CONFIG_EXTRA register is used to control the 50Hz and 60Hz rejection digital filter.

Table 25. CONFIG_EXTRA Register

15	14	13	12	11	10	9	8
FILT50	FILT60	RSV	RSV	RSV	RSV	RSV	RSV
R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h
7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
R/W -1h	R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h	R/W -0h
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset							

Table 26. CONFIG_EXTRA Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	FILT_50HZ	R/W	0h	50Hz Normal mode rejection 0: Disable 1: Enable
14	FILT_60HZ	R/W	0h	60Hz Normal mode rejection 0: Disable 1: Enable
13:0	RSV(13:0)	R/W	0080h	Reserved bit, must write 0080h.

8.1.6 DEVICE_ID REGISTER (P[2:0] = 7H) [RESET = 3000H]

The 16-bit DEVICE_ID register is used to recognize device and test communication.

Table 27. DEVICE_ID Register

15	14	13	12	11	10	9	8
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h
7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset							

Table 28. DEVICE_ID Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15:8	D(15:8)	R	30h	DEVICE_ID value
7:0	RSV(7:0)	R	00h	Reserved

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9. APPLICATION AND IMPLEMENTATION

NOTE

The information provided in this section is not part of the AnalogySemi component specification. Hence, AnalogySemi does not warrant its completeness or accuracy. Customers are responsible for determining suitability of components and system functionality for their applications. Validation and testing should be performed prior to design implementation.

9.1 APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADX113 in various situations.

9.1.1 BASIC CONNECTIONS

The principle I²C connections for the ADX113 are shown in Figure 29.

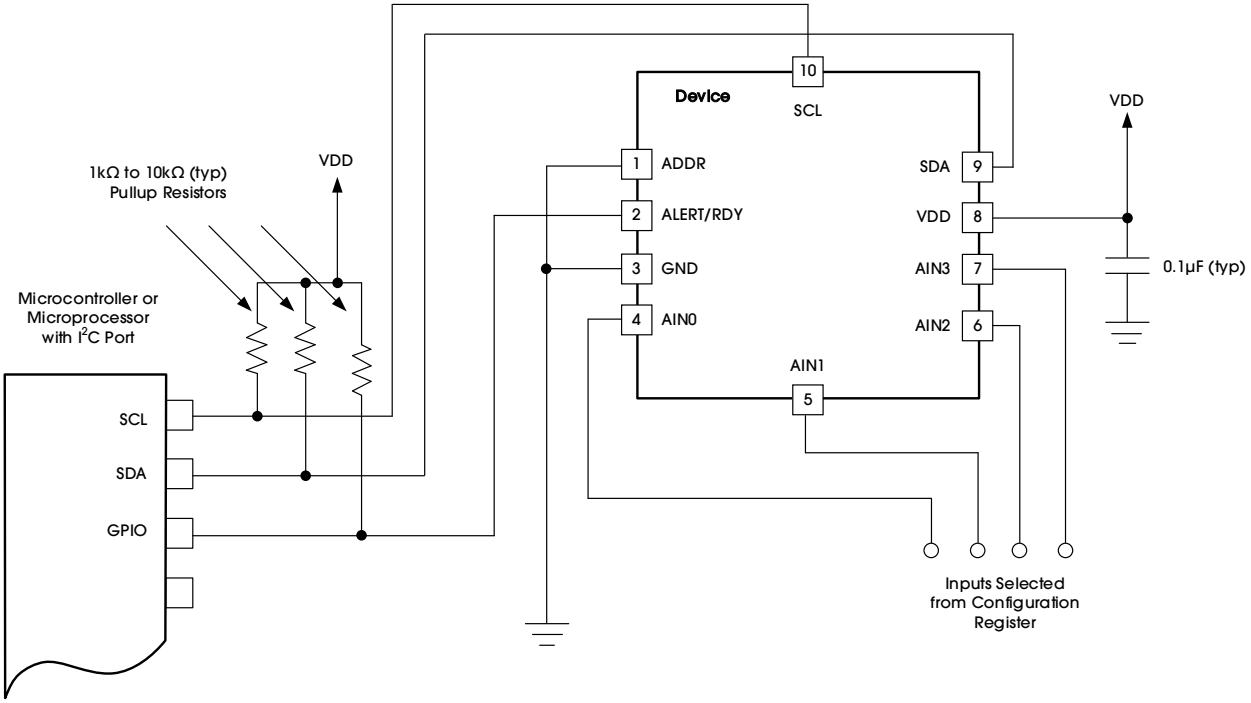

Figure 29. Typical Connections of the ADX113

The fully-differential voltage input of the ADX113 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADX113 can read bipolar differential signals, these devices cannot accept negative voltages on either input.

The ADX113 draws transient currents during conversion. A 0.1µF power-supply bypass capacitor supplies the momentary bursts of extra current required from the supply.

The ADX113 interfaces directly to standard mode, fast mode, and high-speed mode I²C controllers. Any microcontroller I²C peripheral, including master-only and single-master I²C peripherals, operates with the ADX113. The ADX113 does not perform clock-stretching (that is, the device never pulls the clock line low), so it is not necessary to provide for this function unless other clock-stretching devices are on the same I²C bus.

Pullup resistors are required on both the SDA and SCL lines because I²C bus drivers are open drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, thus limiting the bus speed. Lower-value resistors allow higher speed, but at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. Do not use resistors that are too small because the bus drivers may not be able to pull the bus lines low.

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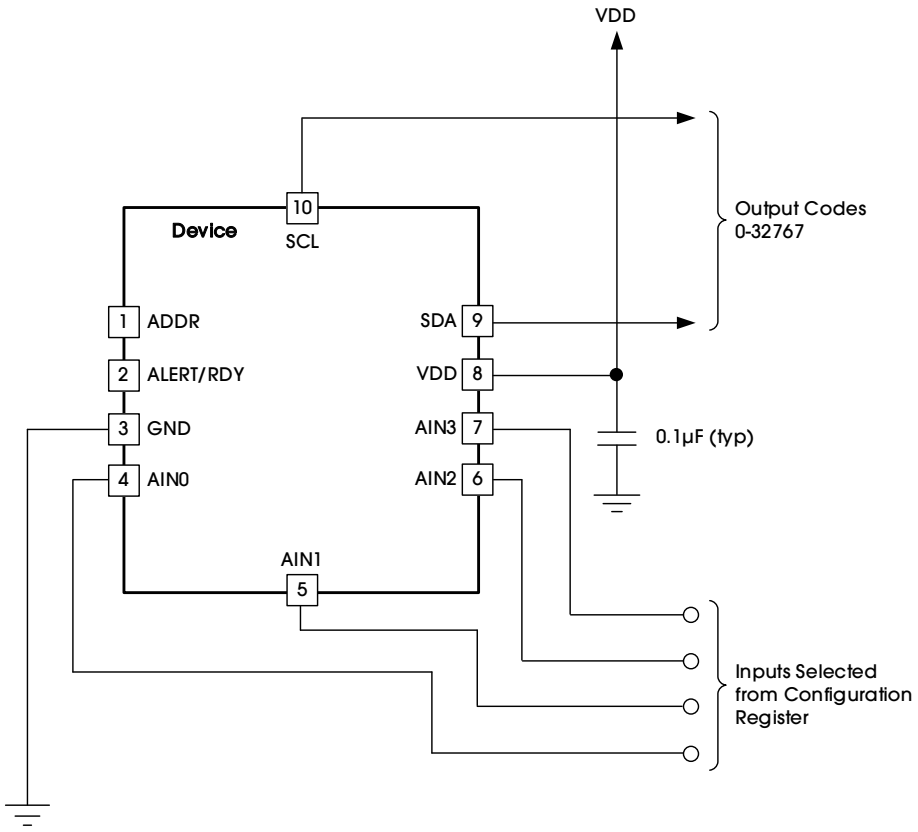
9.1.2 SINGLE-ENDED INPUTS

The ADX113 can measure up to four, single-ended signals. The ADX113 measures single-ended signals by appropriate configuration of the MUX(2:0) bits in the CONFIG REGISTER. Figure 30 shows a single-ended connection scheme for ADX113. The single-ended signal ranges from 0V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the ADX113 can only accept positive voltages with respect to ground. The ADX113 does not lose linearity within the input range.

The ADX113 offers a differential input voltage range of ±FSR. Single-ended configurations use only one-half of the full-scale input voltage range. Differential configurations maximize the dynamic range of the ADC, and provide better common-mode noise rejection than single-ended configurations.



NOTE: Digital pin connections omitted for clarity.

Figure 30. Measuring Single-Ended Inputs

The ADX113 also allows AIN3 to serve as a common point for measurements by appropriate setting of the MUX(2:0) bits. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADX113 operates with inputs, where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD; however, common-mode noise attenuation is not offered.

9.1.3 INPUT PROTECTION

The ADX113 is fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADX113 can be permanently damaged by analog input voltages that exceed approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADX113 analog inputs can withstand continuous currents as large as 10mA.

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9.1.4 UNUSED INPUTS AND OUTPUTS

Either float unused analog inputs, or tie the unused analog inputs to midsupply or VDD. Connecting unused analog inputs to GND is possible, but may yield higher leakage currents than the previous options.

If the ALERT/RDY output pin is not used, leave the pin unconnected or tie the pin to VDD using a weak pullup resistor.

9.1.5 ANALOG INPUT FILTERING

Analog input filtering serves two purposes:
1. Limits the effect of aliasing during the sampling process
2. Reduces external noise from being a part of the measurement

Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as the modulator frequency (f_{MOD}), as shown in Figure 31. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency, or multiples thereof, are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

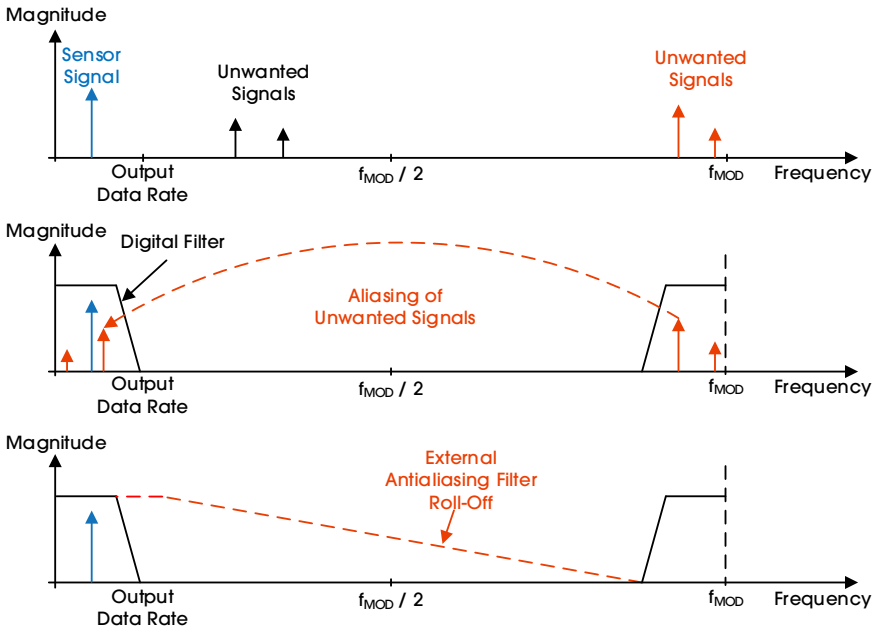

Figure 31. Effect of Aliasing

Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADX113 attenuate signals to a certain degree. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, use a first-order RC filter with a cutoff frequency set at the output data rate or 10x higher as a generally good starting point for a system design.

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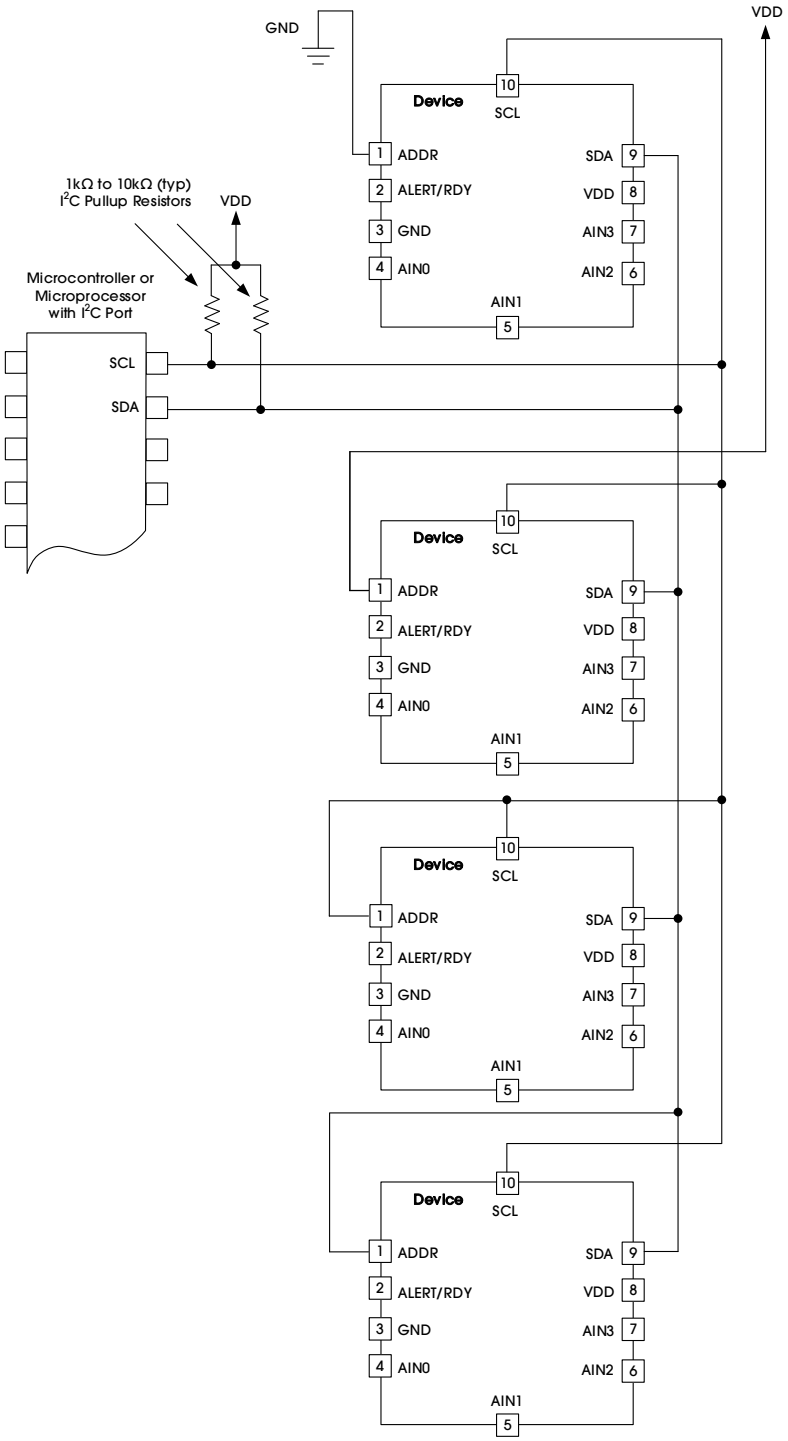
9.1.6 CONNECTING MULTIPLE DEVICES

It is possible to connect up to four ADX113 devices to a single I²C bus using different address pin configurations for each device. Use the address pin to set the ADX113 to one of four different I²C addresses. Use the GND, VDD, and SCL addresses first. If SDA is used as the device address, hold the SDA line low for at least 100ns after the SCL line goes low to make sure the device decodes the address correctly during I²C communication. An example showing four ADX113 devices on the same I²C bus is shown in Figure 32. One set of pullup resistors is required per bus. The pullup resistor values may need to be lowered to compensate for the additional bus capacitance presented by multiple devices and increased line length.



NOTE: Device power and input connections omitted for clarity. The ADDR pin selects the I²C address.

Figure 32. Connecting Multiple ADX113 Devices

9.1.7 COMMUNICATION GUIDE

This section provides a brief example of ADX113 communications. See subsequent sections of this datasheet for more detailed explanations. Hardware for this design includes: one ADX113 configured with an I²C address of 1001000; a microcontroller with an I²C interface; discrete components such as resistors, capacitors, and serial connectors; and a 2V to 5V power supply. Figure 33 shows the basic hardware configuration.

The ADX113 communicates with the master (microcontroller) through an I²C interface. The master provides a clock signal on the SCL pin and data are transferred using the SDA pin. The ADX113 never drives the SCL pin. For information on programming and debugging the microcontroller being used, see the device-specific product datasheet.

The first byte sent by the master is the ADX113 address, followed by the R/$\overline{W}$ bit that instructs the ADX113 to listen for a subsequent byte. The second byte is the ADDRESS POINTER REGISTER byte. The third and fourth bytes sent from the master are written to the register indicated in register address pointer bits P(2:0). See Figure 25 and Figure 26 for read and write operation timing diagrams, respectively. All read and write transactions with the ADX113 must be preceded by a START condition, and followed by a STOP condition.

For example, to write to the configuration register to set the ADX113 to continuous-conversion mode and then read the conversion result, send the following bytes in this order:

1. Write to Config register:
   - First byte: 0b10010000 (first 7-bit I²C address followed by a low R/$\overline{W}$ bit)
   - Second byte: 0b00000001 (points to Config register)
   - Third byte: 0b10000100 (MSB of the Config register to be written)
   - Fourth byte: 0b10000011 (LSB of the Config register to be written)
2. Write to Address Pointer register:
   - First byte: 0b10010000 (first 7-bit I²C address followed by a low R/$\overline{W}$ bit)
   - Second byte: 0b00000000 (points to Conversion register)
3. Read Conversion register:
   - First byte: 0b10010001 (first 7-bit I²C address followed by a high R/$\overline{W}$ bit)
   - Second byte: the ADX113 responds with the MSB of the Conversion register
   - Third byte: the ADX113 response with the LSB of the Conversion register

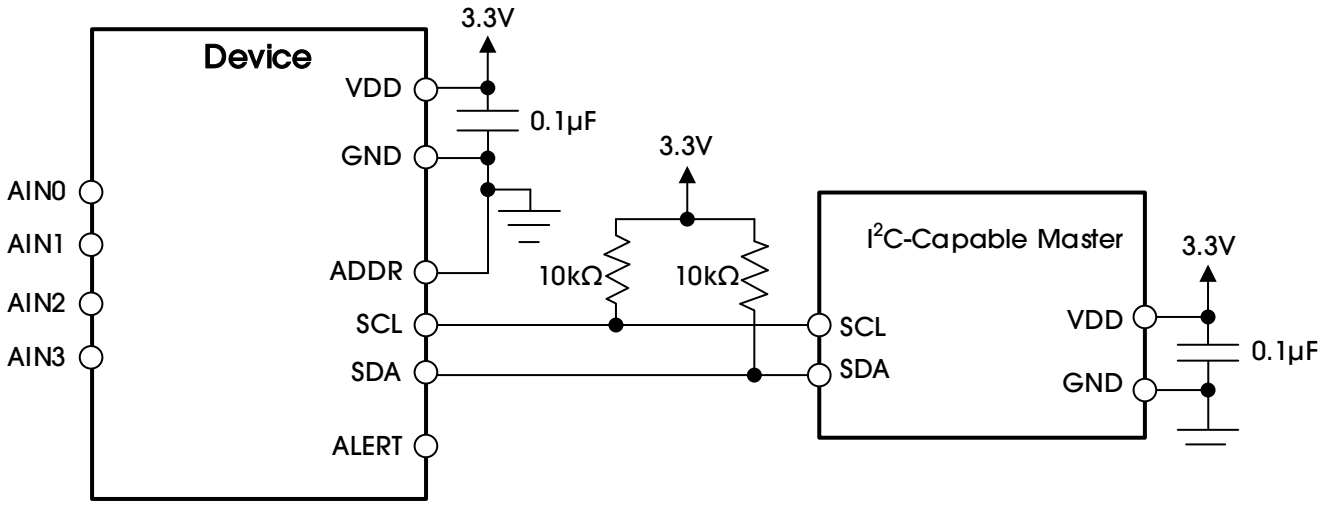


Figure 33. Basic Hardware Configuration

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10. POWER SUPPLY RECOMMENDATIONS

The device requires a single unipolar supply, VDD, to power both the analog and digital circuitry of the device.

10.1 POWER-SUPPLY SEQUENCING

Wait approximately 50μs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

10.2 POWER-SUPPLY DECOUPLING

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a 0.1μF capacitor, as shown in Figure 34. The 0.1μF bypass capacitor supplies the momentary bursts of extra current required from the supply when the device is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoid the use of vias for connecting the capacitors to the device pins for better noise immunity. The use of multiple vias in parallel lowers the overall inductance, and is beneficial for connections to ground planes.

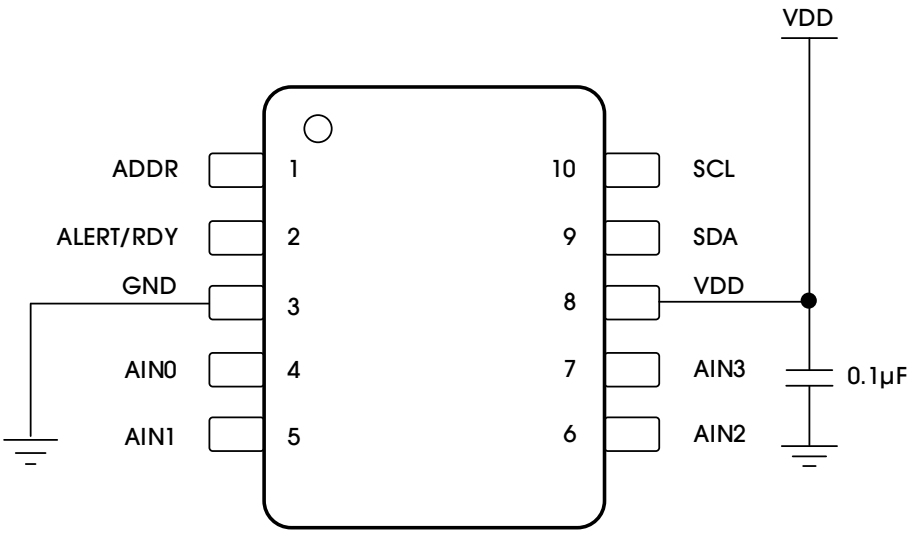

Figure 34. ADX113 Power-Supply Decoupling

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11. LAYOUT

11.1 LAYOUT GUIDELINES

The following outlines some basic recommendations for the layout of the ADX113 to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines such as AIN0, AIN1 and AIN2, AIN3. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low-noise characteristics.

11.2 LAYOUT EXAMPLE

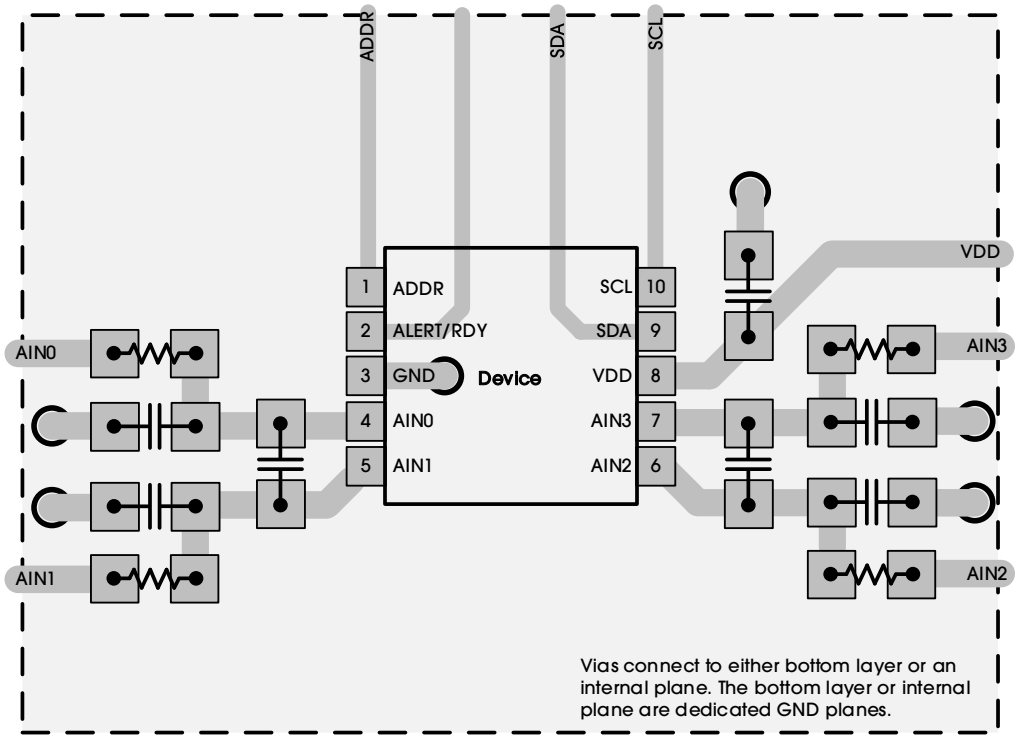

Figure 35. Layout Example

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12. PACKAGE INFORMATION

The ADX113 is available in the MSOP-10 and QFN-10 packages.

12.1 MSOP-10 PACKAGE

Figure 36 shows the MSOP-10 package view.

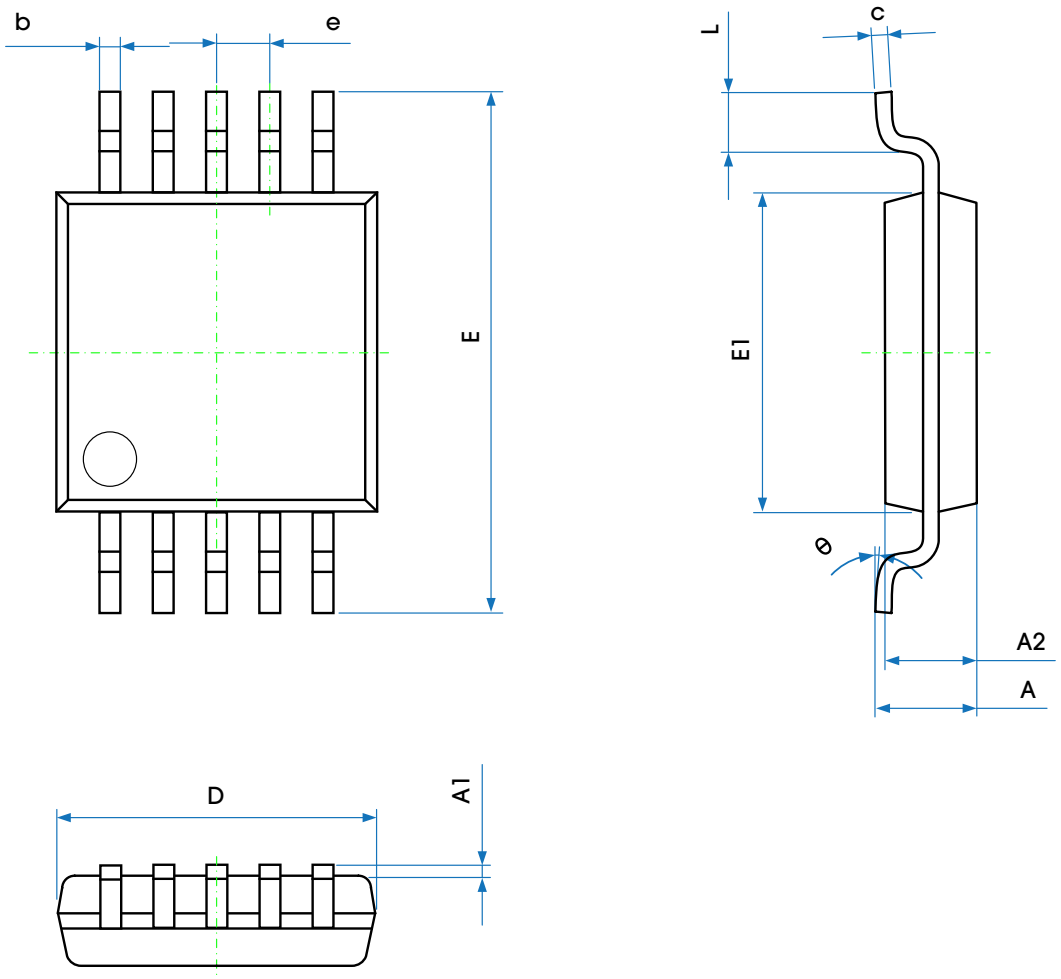

Figure 36. MSOP-10 Package View

Table 29 provides detailed information about the dimensions of the MSOP-10 package.

Table 29. Dimensions of the MSOP-10 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	—	1.100	—	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.330	0.007	0.013
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.500 (BSC)		0.020 (BSC)	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

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12.2 QFN-10 PACKAGE

Figure 37 shows the QFN-10 package view.

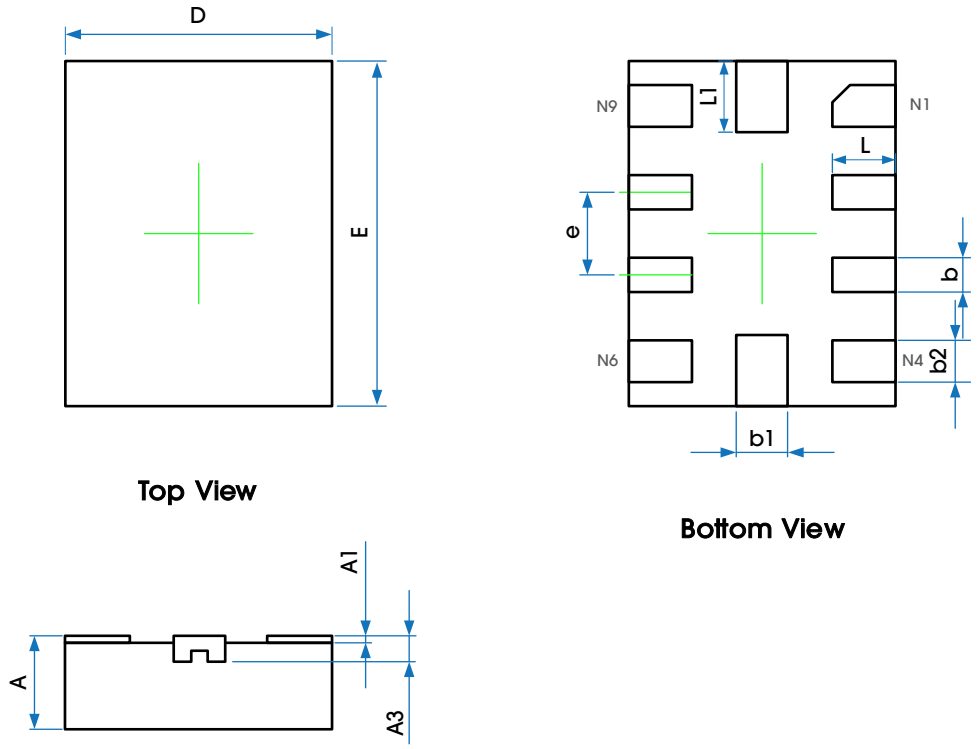

Figure 37. QFN-10 Package View

Table 30 provides detailed information about the dimensions of the QFN-10 package.

Table 30. Dimensions of the QFN-10 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
b	0.150	0.250	0.006	0.010
b1	0.250	0.350	0.010	0.014
b2	0.200	0.300	0.008	0.012
D	1.450	1.550	0.057	0.061
E	1.950	2.050	0.077	0.081
e	0.500TYP.		0.020TYP.	
L	0.300	0.400	0.012	0.016
L1	0.350	0.450	0.014	0.018

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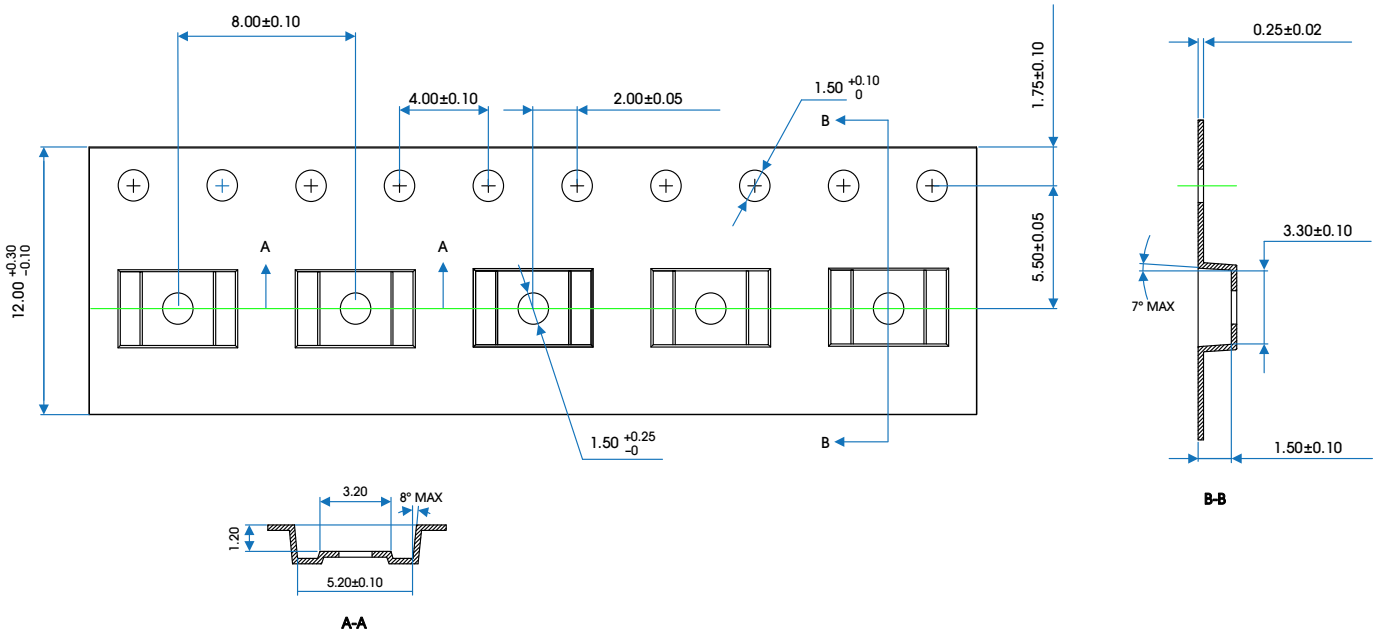
13. TAPE AND REEL INFORMATION

13.1 MSOP-10 PACKAGE

Figure 38 illustrates the carrier tape of the MSOP-10 package.



Notes:
1. Cover tape width: 9.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: MSOP-10 (3*3).
5. All dimensions: mm.
6. Direction of view:

Figure 38. Carrier Tape Drawing (MSOP-10 Package)

Table 31 provides information about tape and reel (MSOP-10 package).

Table 31. Tape and Reel Information (MSOP-10 Package)

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
MSOP-10 3*3	13''	3000	1	8	24000	358*340*50	430*380*390

Figure 39 shows the product loading orientation—pin 1 is assigned on the upper left corner.

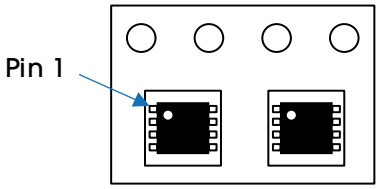


Figure 39. Product Loading Orientation (MSOP-10 Package)

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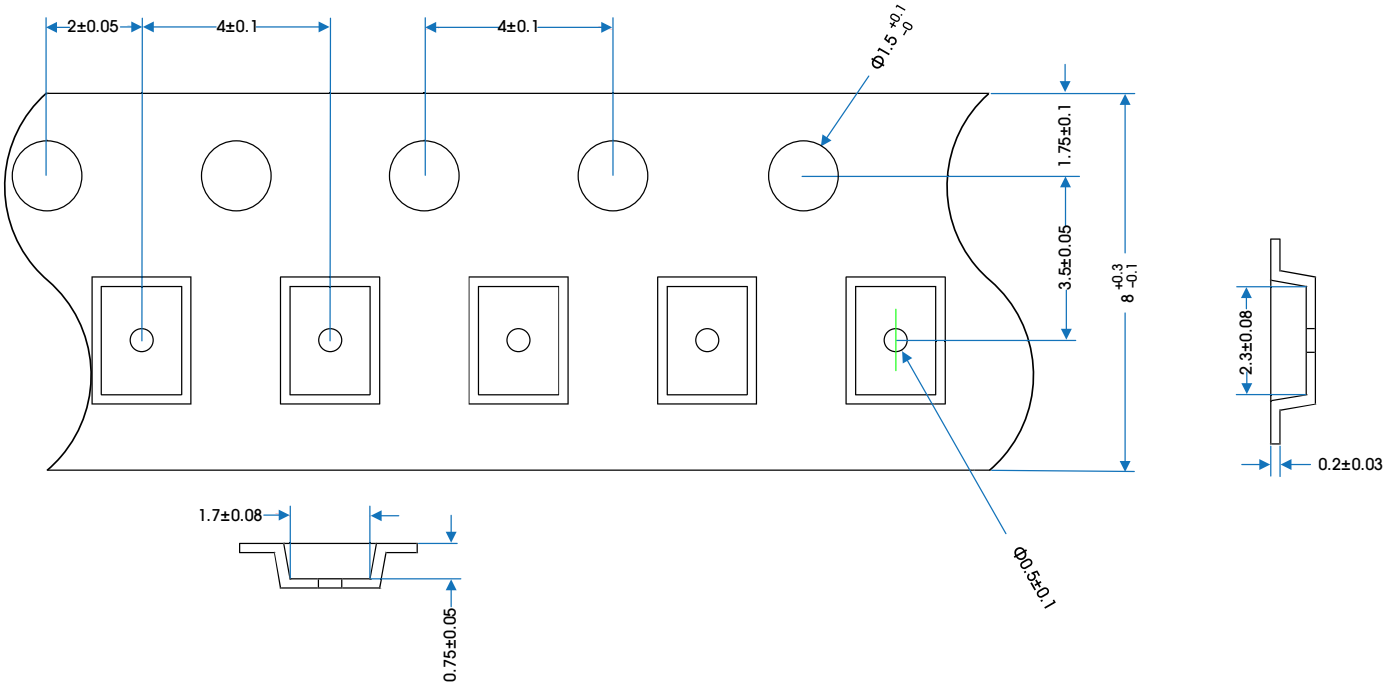
13.2 QFN-10 PACKAGE

Figure 40 illustrates the carrier tape (QFN-10 package).



Notes:
1. Cover tape width: 5.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: QFN-10 (1.5*2).
5. All dimensions: mm.
6. Direction of view:

Figure 40. Carrier Tape Drawing (QFN-10 Package)

Table 32 provides information about tape and reel (QFN-10 package).

Table 32. Tape and Reel Information (QFN-10 Package)

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
QFN-10 1.5*2	7''	4000	10	4	160000	210*208*203	440*440*230

Figure 41 shows the product loading orientation—pin 1 is assigned on the upper left corner.

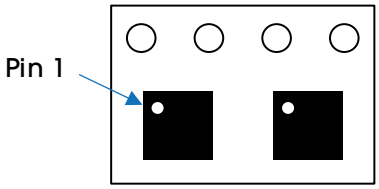


Figure 41. Product Loading Orientation (QFN-10 Package)

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REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	09 August 2022	Rev A release.

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