Low-Power, 2-Channel, 24-Bit Analog Front-End for Biopotential Measurements

1. FEATURES

- Three low-noise (ADX923) PGAs and two high-resolution ADCs (ADX922/3)
- Input-referred noise: 8.6μV_{PP} (G = 6)
- Input bias current: 100pA
- Data rate: 125SPS to 8kSPS
- CMRR: 117dB; THD: –107dB
- Programmable gain: 1, 2, 3, 4, 6, 8, or 12
- Supplies: unipolar or bipolar
  - Analog: 2.7V to 5.5V
  - Digital: 1.65V to 3.6V
- Built-in right leg drive amplifier, lead-off detection, test signals
- Integrated respiration impedance measurement (ADX922/3)
- Electrode Rotation mode (ERM) to implement time-division multiplexing LEAD-I, LEAD-II, and LEAD-III measurements (ADX923)
- Integrated digital AC lead-off measurement and software AC lead-off measurement (ADX922/3)
- Integrated analog PACE measurement (ADX921/2/3)
- Flexible power mode
  - High Resolution mode
  - High Speed mode (ADX921/2/3)
- Built-in oscillator and reference
- Supply monitor, internal temp sensor, OSC fault detection, overrange detection
- Flexible power-down, standby mode
- SPI™-compatible serial interface, timeout reset
- Cyclic redundancy check (CRC) on communications, checksum
- Support ADC data FIFO for reducing polling time of the external device to save power
- Functional safety
- Support systems meeting IEC 60601-2-47
- Operating temperature range: –40°C to 85°C

2. APPLICATIONS

- Medical instrumentation (ECG) including:
  - Patient monitoring: Holter, event, stress, and vital signs including ECG, AED, and telemedicine
  - Personal care and fitness monitors (heart rate, respiration, and ECG)
- High-precision, simultaneous, multichannel data acquisition

3. DESCRIPTION

The ADX920/1/2/3 devices are multichannel, simultaneous sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator.

The ADX920/1/2/3 devices incorporate all features commonly required in portable, low-power medical electrocardiogram (ECG), sports, and fitness applications.

With high levels of integration and exceptional performance, the ADX920/1/2/3 devices enable the creation of scalable medical instrumentation systems at significantly reduced size, power, and overall cost.

The ADX920/1/2/3 devices have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and lead-off detection. Additionally, any configuration of input channels can be selected for derivation of the right leg drive (RLD) output signal. The ADX920/1/2/3 devices operate at data rates up to 8kSPS. Lead-off detection can be implemented internal to the device, using the device internal excitation current sink or source. The ADX922/3 devices include a fully integrated respiration impedance measurement function. Operating temperature is specified from –40°C to 85°C. See Table 1 for the order information.

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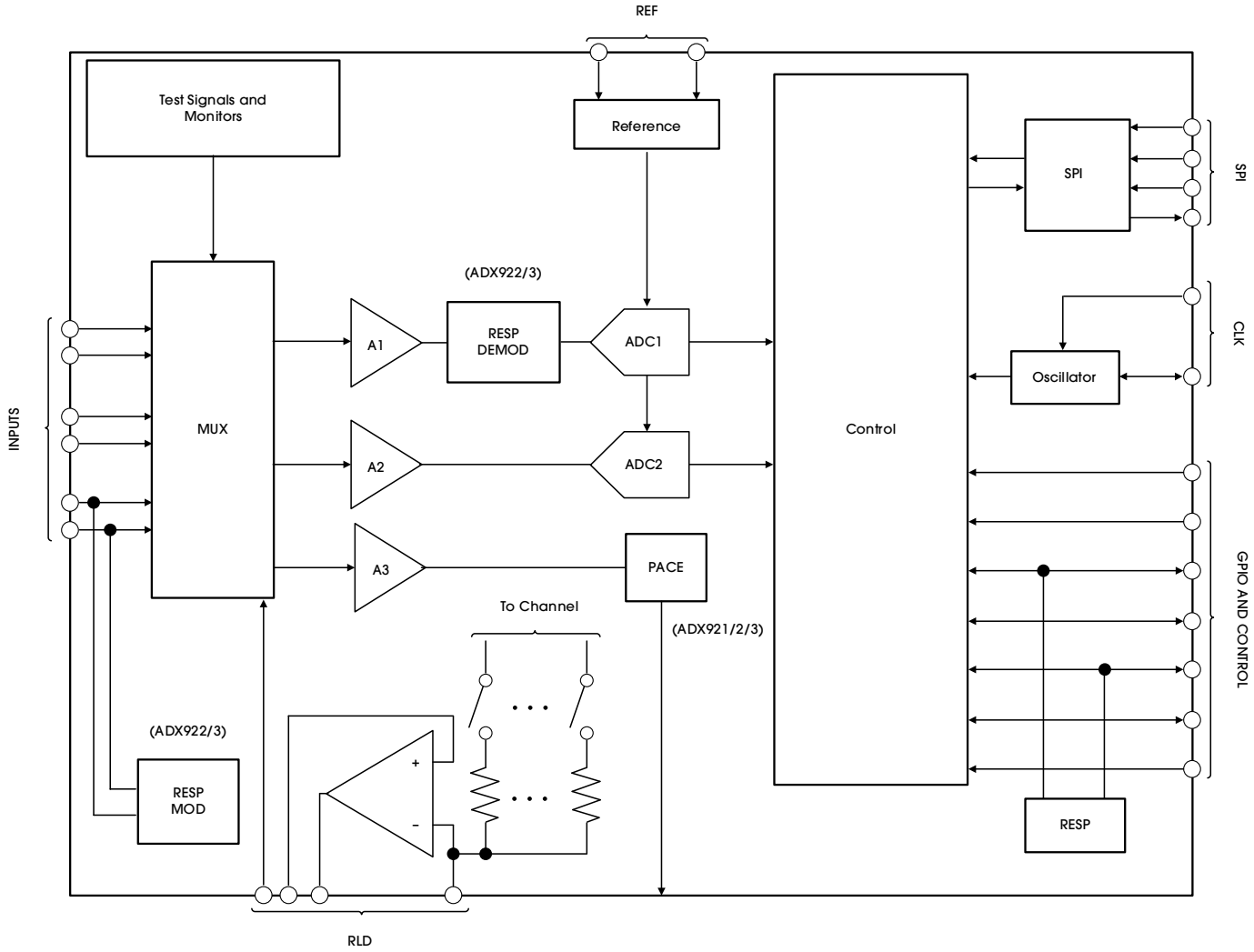

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Table 1 lists the order information.

Table 1. Order Information

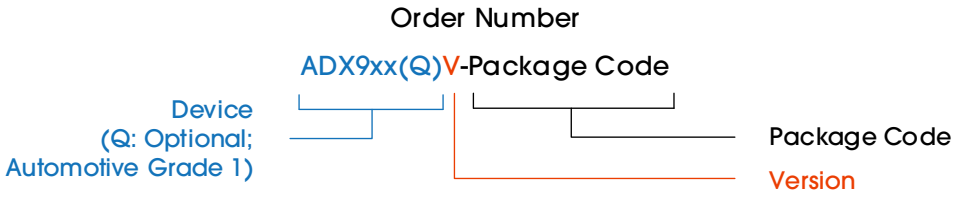
ORDER NUMBER[1]	CH (#)	MARK	PACKAGE	RESOLUTION (BIT)	RESPIRATION	ANALOG PACE	AC LEAD-OFF	ERM	DIGITAL HIGH-PASS FILTER	FIFO	OP. TEMP. (°C)	RATING	PKG. OPTION
ADX923AQFN32	2	ADX923	QFN-32	24	Y	Y	Y	Y	Y	Y	–40-85	Industry	T/R-1500
ADX922AQFN32	2	ADX922	QFN-32	24	Y	Y	Y				–40-85	Industry	T/R-1500
ADX921AQFN32	2	ADX921	QFN-32	24		Y	Y				–40-85	Industry	T/R-1500
ADX920AQFN32	1	ADX920	QFN-32	24			Y			Y	–40-85	Industry	T/R-1500

Table 2. Family Selection Guide

ORDER NUMBER[1]	CH (#)	MARK	PACKAGE	RESOLUTION (BIT)	RESPIRATION	ANALOG PACE	AC LEAD-OFF	ERM	DIGITAL HIGH-PASS FILTER	FIFO	OP. TEMP. (°C)	RATING	PKG. OPTION
ADX923QAQFN32	2	ADX923Q	QFN-32	24	Y	Y	Y	Y	Y	Y	–40-125	Auto	T/R-1500
ADX922QAQFN32	2	ADX922Q	QFN-32	24	Y	Y	Y				–40-125	Auto	T/R-1500
ADX921QAQFN32	2	ADX921Q	QFN-32	24		Y	Y				–40-125	Auto	T/R-1500
ADX920QAQFN32[2]	1	ADX920Q	QFN-32	24			Y			Y	–40-125	Auto	T/R-1500
ADX912QAQFN32[2]	2	ADX912Q	QFN-32	16			Y				–40-125	Auto	T/R-1500
ADX912AQFN32[2]	2	ADX912	QFN-32	16							–40-85	Industry	T/R-1500
ADX911QAQFN32[2]	1	ADX911Q	QFN-32	16			Y				–40-125	Auto	T/R-1500
ADX911AQFN32[2]	1	ADX911	QFN-32	16							–40-85	Industry	T/R-1500

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or,
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: Available in the future.

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4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration (ADX921/2/3).

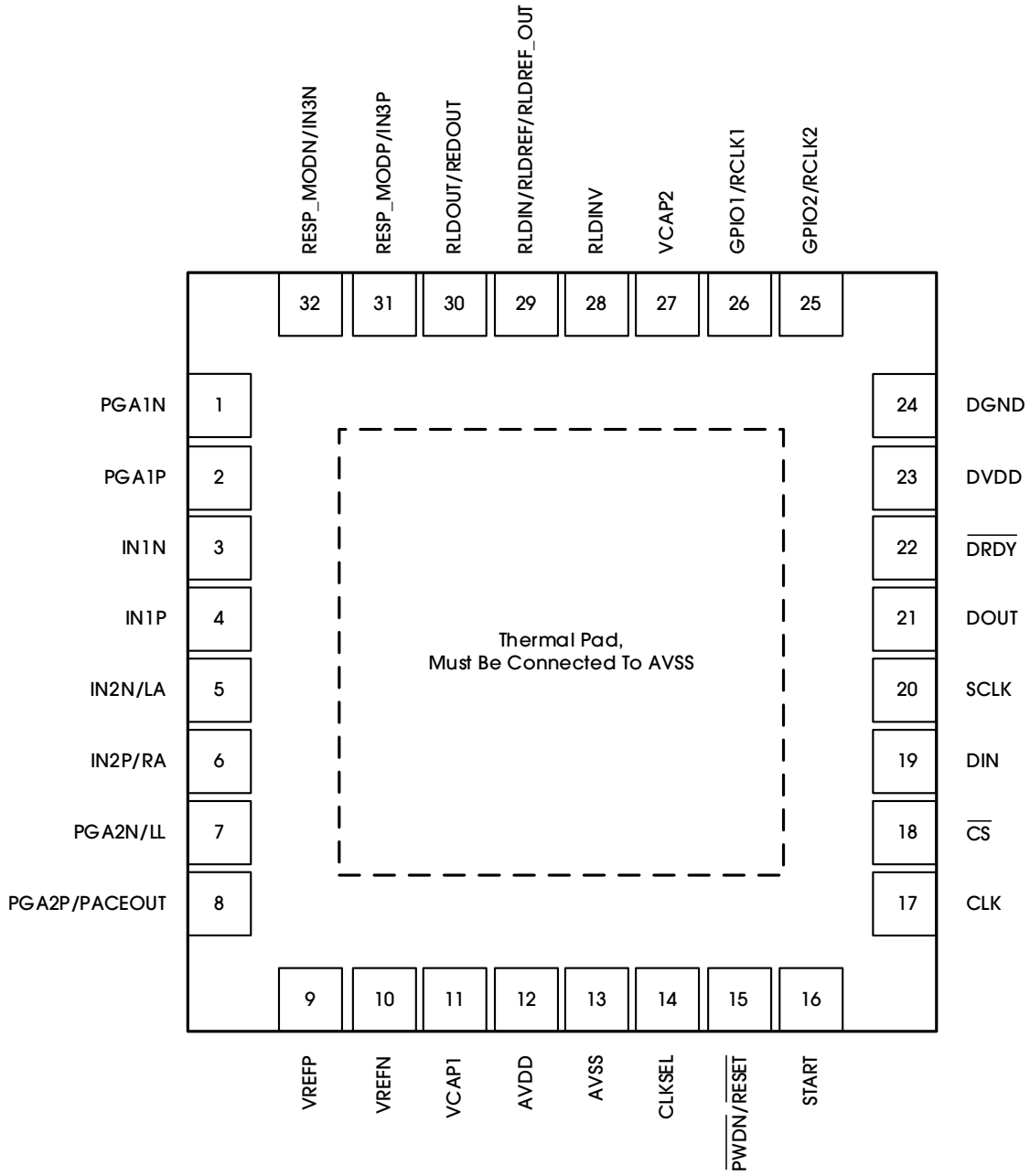

Figure 1. Pin Configuration (ADX921/2/3)

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Table 3 lists the pin functions (ADX921/2/3).

Table 3. Pin Functions (ADX921/2/3)

PIN	POSITION	FUNCTION	DESCRIPTION
PGA1N	1	Analog output	PGA1 inverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1P.
PGA1P	2	Analog output	PGA1 noninverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1N.
IN1N(1)	3	Analog input	Differential analog negative input 1
IN1P(1)	4	Analog input	Differential analog positive input 1
IN2N(1)/LA	5	Analog input	Differential analog negative input 2, Left arm in electrode rotation mode
IN2P(1)/RA	6	Analog input	Differential analog positive input 2, right arm in electrode rotation mode
PGA2N/LL	7	Analog output/input	PGA2 inverting output, left leg in electrode rotation mode
PGA2P/PACEOUT	8	Analog output	PGA2 noninverting output, pace output in analog pace mode
VREFP	9	Analog input/output	Positive reference voltage
VREFN	10	Supply	Negative reference voltage, must be connected to AVSS, Analog ground
VCAP1	11	—	Analog bypass capacitor, bandgap output
AVDD	12	Supply	Analog supply
AVSS	13	Supply	Analog ground
CLKSEL	14	Digital input	Master clock select
$\overline{\text{PWDN}}$/$\overline{\text{RESET}}$	15	Digital input	Power-down or system reset, active low
START	16	Digital input	Start conversion
CLK	17	Digital input	Master clock input
$\overline{\text{CS}}$	18	Digital input	Chip select
DIN	19	Digital input	SPI data in
SCLK	20	Digital input	SPI clock
DOUT	21	Digital output	SPI data out
$\overline{\text{DRDY}}$	22	Digital output	Data ready, active low
DVDD	23	Supply	Digital power supply
DGND	24	Supply	Digital ground
GPIO2/RCLK2	25	Digital input/output	General-purpose I/O 2 or respiration clock 2 (ADX922/3)
GPIO1/RCLK1	26	Digital input/output	General-purpose I/O 1 or respiration clock 1 (ADX922/3)
VCAP2	27	Supply	Analog bypass capacitor, AVDD + 2V
RLDINV	28	Analog input	Right leg drive inverting input, connect to AVDD if not used
RLDIN/RLDREF/RLDREF_OUT	29	Analog input/output	RLDIN/RLDREF: Right leg drive input to MUX or RLD amplifier noninverting input; also connects to pace reference buffer noninverting input internally. Connect to AVDD if not used. RLDREF_OUT: Build an external bandpass filter on PACE_OUT and RLDREF_OUT.
RLDOUT/REDOUT	30	Analog output	Right leg drive output, reference electrode driver output in electrode rotation mode
RESP_MODP/IN3P(1)	31	Analog output/input	P-side respiration excitation signal for respiration (analog output) or auxiliary input 3P (analog input)
RESP_MODN/IN3N(1)	32	Analog output/input	N-side respiration excitation signal for respiration (analog output) or auxiliary input 3N (analog input)
Pad	Power Pad	—	Thermal pad, must be connected to AVSS

Note: Connect unused analog pins to AVDD.

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Figure 2 illustrates the pin configuration (ADX920).

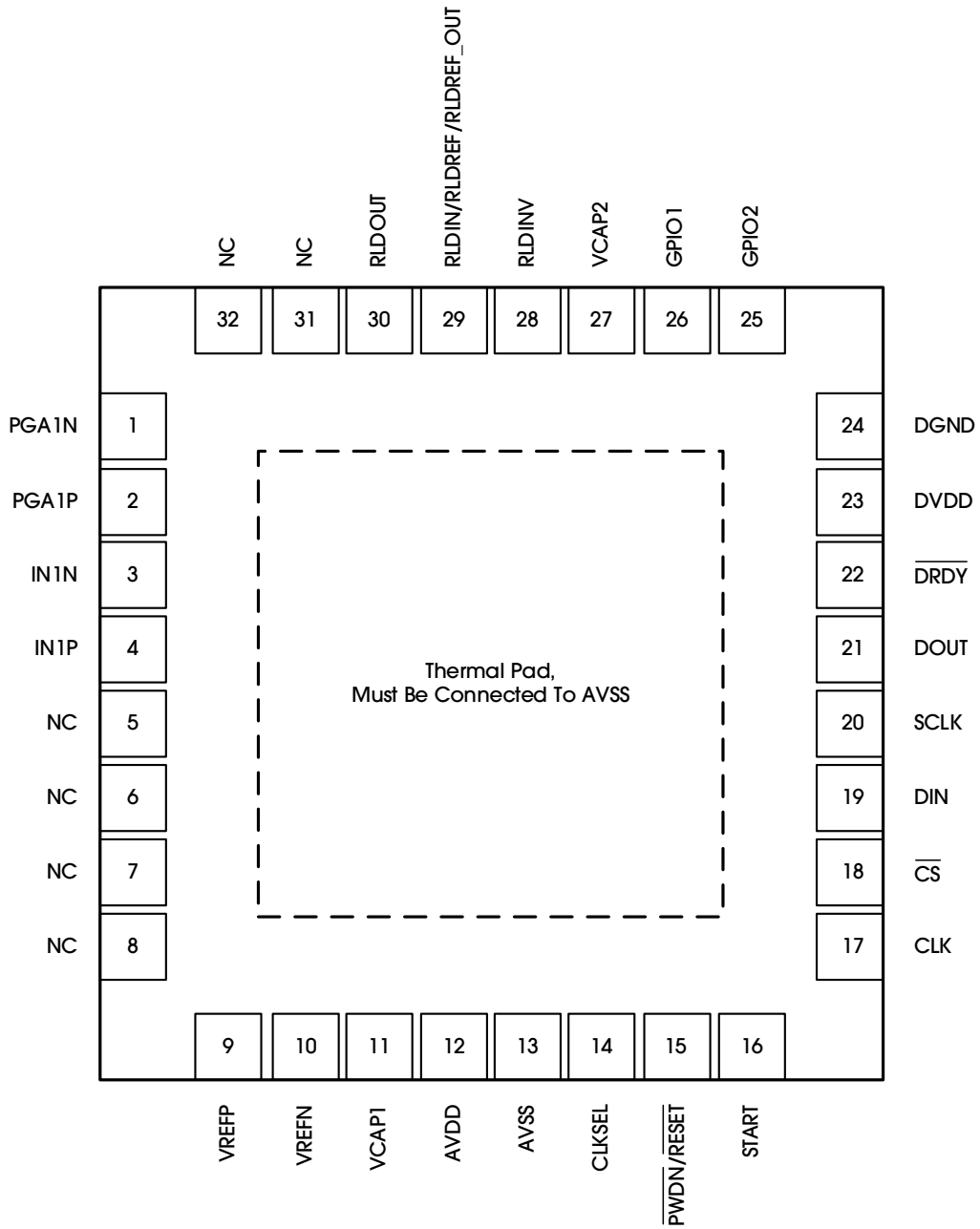

Figure 2. Pin Configuration (ADX920)

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Table 4 lists the pin functions (ADX920).

Table 4. Pin Functions (ADX920)

PIN	POSITION	FUNCTION	DESCRIPTION
PGA1N	1	Analog output	PGA1 inverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1P.
PGA1P	2	Analog output	PGA1 noninverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1N.
IN1N(1)	3	Analog input	Differential analog negative input 1
IN1P(1)	4	Analog input	Differential analog positive input 1
NC	5, 6, 7, 8, 31, 32	—	Do not connect
VREFP	9	Analog input/output	Positive reference voltage
VREFN	10	Supply	Negative reference voltage, must be connected to AVSS, analog ground
VCAP1	11	—	Analog bypass capacitor, bandgap output
AVDD	12	Supply	Analog supply
AVSS	13	Supply	Analog ground
CLKSEL	14	Digital input	Master clock select
$\overline{\text{PWDN}}$/$\overline{\text{RESET}}$	15	Digital input	Power-down or system reset, active low
START	16	Digital input	Start conversion
CLK	17	Digital input	Master clock input
$\overline{\text{CS}}$	18	Digital input	Chip select
DIN	19	Digital input	SPI data input
SCLK	20	Digital input	SPI clock
DOUT	21	Digital output	SPI data output
$\overline{\text{DRDY}}$	22	Digital output	Data ready, active low
DVDD	23	Supply	Digital power supply
DGND	24	Supply	Digital ground
GPIO2	25	Digital input/output	General-purpose I/O 2
GPIO1	26	Digital input/output	General-purpose I/O 1
VCAP2	27	Supply	Analog bypass capacitor, AVDD + 2V
RLDINV	28	Analog input	Right leg drive inverting input, connect to AVDD if not used
RLDIN/RLDREF/RLDREF_OUT	29	Analog input/output	RLDIN/RLDREF: Right leg drive input to MUX or RLD amplifier noninverting input, connect to AVDD if not used. RLDREF_OUT: Build an external bandpass filter on RLDREF_OUT.
RLDOUT	30	Analog output	Right leg drive output
Pad	Power Pad	—	Thermal pad, must be connected to AVSS

Note: Connect unused analog pins to AVDD.

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5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 5 lists the absolute maximum ratings of the ADX920/1/2/3. Over operating free-air temperature range, unless otherwise noted.

Table 5. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Power-Supply Voltage	AVDD to AVSS	–0.3	7.0	V
	AVSS to DGND	–3	0.2	
	DVDD to DGND	–0.3	5.0	
	Analog input to AVSS	AVSS – 0.3	AVDD + 0.3	
	Digital input to DVDD	DVSS – 0.3	DVDD + 0.3	
Input Current	To any pin except supply pins	–10	10	mA
	Momentary	–100	100	
	Continuous	–10	10	
Temperature	Operating, T_A	–40	85	°C
	Junction, T_J		105	
	Storage, T_{stg}	–60	150	

Note: Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 7. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 6 lists the ESD ratings of the ADX920/1/2/3.

Table 6. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per AEC Q100-002(1)	±3500	V
		Charged device model (CDM), per AEC Q100-011	±2000	

Note: AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 RECOMMENDED OPERATING CONDITIONS

Table 7 lists the recommended operating conditions for the ADX920/1/2/3. Over operating free-air temperature range, unless otherwise noted.

Table 7. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
POWER SUPPLY					
Analog Power Supply, AVDD to AVSS	AVDD	2.7	3	5.5	V
Digital Power Supply, DVDD to DGND	DVDD	1.65	1.8	3.6	V
ANALOG INPUTS					
Voltage		AVSS		AVDD	V
DIGITAL INPUTS					
Voltage		DVSS		DVDD	V
TEMPERATURE RANGE					
Operating Ambient Temperature	T_A	–40		85	°C

5.4 THERMAL INFORMATION

Table 8 lists the thermal information for the ADX920/1/2/3.

Table 8. Thermal Information

PARAMETER	SYMBOL	QFN-32	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	42.2	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	16.7	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	14.9	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	0.3	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	14.2	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	8.2	°C/W

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5.5 ELECTRICAL CHARACTERISTICS

Table 9 lists the electrical characteristics of ADX920/1/2/3. Minimum and maximum specifications apply from –40°C to 85°C, typical specifications are at 25°C, all specifications are at DVDD = 1.8V, AVDD – AVSS = 3V(1), V_{REF} = 2.4V, external f_{CLK} = 512kHz, data rate = 500SPS, C_{FILTER} = 4.7nF(2), and gain = 6, unless otherwise noted.

Table 9. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Full-Scale Differential Input Voltage (AINP – AINN)			±V_{REF} / gain			V
Input Common-Mode Range			See the INPUT COMMON-MODE RANGE section			
Input Capacitance to GND				15		pF
Input Capacitance Differential Input Pair				1		pF
Input Bias Current (PGA Chop = 8kHz)		T_A = 25°C, input = 1.5V			±100	pA
		T_A = –40°C to 85°C, input = 1.5V		±3		pA
DC Input Impedance		No pull-up or pull-down current source	15			GΩ
		Current source lead-off detection (nA), AVSS + 0.3V < AIN < AVDD – 0.3V		> 10		GΩ
PGA PERFORMANCE						
Gain Settings			1, 2, 3, 4, 6, 8, 12			
Bandwidth (Channel 1)		With a 4.7nF capacitor on PGA output (see the PGA SETTINGS AND INPUT RANGE section for details)		6.8		kHz
ANALOG PACE CHANNEL						
Gain			0.67, 1.33, 2, 2.67, 4, 5.3, 8			V/V
–3dB Bandwidth	BW	Gain = 4		160		kHz
Output Reference				RLDREF		V
Input-Referred Offset Voltage	V_{OS}			±1.2		mV
Differential Input Voltage Range	DIVR	2.7V ≤ VDD < 3.3V	–330		330	mV
		3.3V ≤ VDD	–400		400	mV
Common-Mode Voltage Range for Full DIVR	CMVR		0.95		VDD – 1.2	V
Common-Mode Rejection Ratio	CMRR	0.5V ≤ VCM ≤ VDD – 1.5V		95		dB
Power Supply Rejection Ratio	PSRR	3V ≤ VDD ≤ 5V, VCM = RLDREF		113		dB
Slew Rate	SR			324		mV/µs
Overload Recovery				10		µs
Input-Referred Noise for Analog Pace	V_e-APACE	VCM = RLDREF, 0.1kHz–20kHz		101		$µV_{PP}$
Current Consumption	IVDD			22		µA
ADC PERFORMANCE						
Resolution			24			Bits
Data Rate		f_{CLK} = 512kHz	125		8000	SPS

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHANNEL PERFORMANCE (DC PERFORMANCE)						
Input-Referred Noise		CH1, Gain = 6[3], 10 seconds of data		8.6		μV_{PP}
		CH2, Gain = 6[3], 10 seconds of data, HS mode		17.5		μV_{PP}
		CH1, Gain = 6,256 points, 0.5 seconds of data		6.3	11	μV_{PP}
		CH2, Gain = 6,256 points, 0.5 seconds of data, HS mode		11.4		μV_{PP}
		Gain settings other than 6, data rates other than 500SPS	See the NOISE MEASUREMENTS section			
Integral Nonlinearity		Full-scale with gain = 6, best fit		2		ppm
Offset Error		CH1		±27		µV
		CH2		±154		µV
Offset Error Drift		CH1		0.02		µV/°C
		CH2		2		µV/°C
Offset Error with Calibration		CH1		±1		µV
		CH2		±15		µV
Gain Error		Excluding voltage reference error, CH1		±0.06	±0.23	% of FS
		Excluding voltage reference error, CH2		±0.22	±0.9	% of FS
Gain Error with Calibration				At noise level		
Gain Drift		Excluding voltage reference drift		2.5		ppm/°C
Gain Match Between Channels				0.12		% of FS
CHANNEL PERFORMANCE (AC PERFORMANCE)						
Common-Mode Rejection Ratio	CMRR	f_{CM} = 50Hz and 60Hz[4]	103	117		dB
Power-Supply Rejection Ratio	PSRR	f_{PS} = 50Hz and 60Hz		95		dB
Crosstalk		f_{IN} = 50Hz and 60Hz		–117		dB
Signal-to-Noise Ratio	SNR	f_{IN} = 10Hz input, gain = 6, CH1		106		dB
Total Harmonic Distortion	THD	10Hz, –0.5dBFs, C_{FILTER} = 4.7nF		–107		dB
		100Hz, –0.5dBFs, C_{FILTER} = 4.7nF		–98		dB
DIGITAL FILTER						
SINC3 Digital Filter		–3dB bandwidth		0.262 f_{DR}		Hz
		Full digital filter setting timing		4		Conversions
HPF Digital Filter		Support f_{DR} setting with HPF_EN = 1		125		DR
				250		
		Cut-off frequency		0.5		Hz
				0.67		
				7		
RIGHT LEG DRIVE (RLD) AMPLIFIER						
RLD Integrated Noise		BW = 150Hz		0.89		μV_{RMS}
Gain Bandwidth Product	GBP	50kΩ || 10pF load, gain = 1		130		kHz
Slew Rate	SR	50kΩ || 10pF load, gain = 1		0.1		V/µs
Common-Mode Input Range	CMIR		AVSS + 0.3		AVDD – 0.3	V
Common-Mode Resistor Matching		Internal 200kΩ resistor matching		0.06		%
Short-Circuit Current	I_{SC}			2		mA
Quiescent Power Consumption				3		µA
LEAD-OFF DETECT						

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency		See the REGISTER MAPS section for settings		(0, 8)		kHz
Current		ILEAD_OFF (5:0) = 000000		0.02		nA
		Step size		2.2		nA
Current Accuracy				±20		%
Comparator Threshold Accuracy				±42		mV
RESPIRATION (ADX922/3)						
Frequency		Internal source		32, 64		kHz
		External source	32		64	kHz
Phase Shift		See the REGISTER MAPS section for settings	0	112.5	168.75	Degrees
Impedance Range		Configured as Figure 65		2000	10,000	Ω
Impedance Measurement Noise		0.05Hz to 2Hz brick wall filter, 32kHz modulation clock, phase = 112.5, with 2kΩ baseline load, gain = 4		46		$m\Omega_{PP}$
EXTERNAL REFERENCE						
Reference Input Voltage		3V supply V_{REF} = (VREFP – VREFN)	2	2.5	VDD – 0.3	V
		5V supply V_{REF} = (VREFP – VREFN)	2	4	VDD – 0.3	V
Negative Input	VREFN			AVSS		V
Positive Input	VREFP			AVSS + 2.5		V
Input Impedance				107		kΩ
INTERNAL REFERENCE						
Output Voltage		Register bit CONFIG2.VREF_4V = 0		2.43		V
		Register bit CONFIG2.VREF_4V = 1		4.037		V
Output Current Drive		Available for external use		100		µA
V_{REF} Accuracy				±0.2		%
V_{REF} Drift		–40°C ≤ T_A ≤ 85°C		7		ppm/°C
Start-Up Time		Settled to 0.2% with 10µF capacitor on VREFP pin		36		ms
Quiescent Current Consumption		Register bit CONFIG2.VREF_4V = 0		23		µA
		Register bit CONFIG2.VREF_4V = 1		36		µA
SYSTEM MONITORS						
Analog Supply Reading Error				0.4		%
Digital Supply Reading Error				0.6		%
Device Wakeup		From power-supply ramp after power-on reset (POR) to $\overline{DRDY}$ low		27		ms
		From power-down mode to $\overline{DRDY}$ low		25.9		ms
		From STANDBY mode to $\overline{DRDY}$ low		10		ms
VCAP1 Settling Time		1% accuracy		0.4		s
Temp. Sensor Reading Voltage		T_A = 25°C		144.31		mV
Temp. Sensor Reading Coefficient				309.37		µV/°C
TEST SIGNAL						
Signal Frequency		See the REGISTER MAPS section for settings		At DC and 1Hz		Hz
Signal Voltage		See the REGISTER MAPS section for settings		±1		mV
Accuracy				±2		%

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PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK							
Internal Oscillator Clock Frequency			Nominal frequency		512		kHz
Internal Clock Accuracy			T_A = 25°C			±1	%
			–40°C ≤ T_A ≤ 85°C			±1.5	%
Internal Oscillator Start-Up Time					35		µs
Internal Oscillator Power Consumption					12		µW
External Clock Input Frequency			CLKSEL pin = 0, CLK_DIV = 0	485	512	562.5	kHz
			CLKSEL pin = 0, CLK_DIV = 1	1.94	2.048	2.25	MHz
DIGITAL INPUT/OUTPUT							
Logic Level	DVDD = 1.8V to 3.6V	V_{IH}		0.8 DVDD		DVDD + 0.1	V
	DVDD = 1.8V to 3.6V	V_{IL}		–0.1		0.2 DVDD	V
	DVDD = 1.65V to 1.8V	V_{IH}		DVDD – 0.2			V
	DVDD = 1.65V to 1.8V	V_{IL}				0.2	V
	DVDD = 1.65V to 3.6V	V_{OH}	I_{OH} = –500µA	0.8 DVDD			V
	DVDD = 1.65V to 3.6V	V_{OL}	I_{OL} = +500µA			0.2 DVDD	V
	Input current	I_{IN}	0V < $V_{DigitalInput}$ < DVDD	–10		+10	µA
POWER SUPPLY REQUIREMENTS							
Analog Supply	AVDD – AVSS	AVDD		2.7	3	5.5	V
Digital Supply	DVDD – DGND	DVDD		1.65	1.8	3.6	V
AVDD – DVDD				–2.1		3.6	V
SUPPLY CURRENT (RLD AMPLIFIER TURNED OFF)							
I_{AVDD}	ADX921/2/3		AVDD – AVSS = 3V		272		µA
			AVDD – AVSS = 5V		307		µA
I_{DVDD}	ADX921/2/3		DVDD = 3.3V		49		µA
			DVDD = 1.8V		25		µA
POWER DISSIPATION (ANALOG SUPPLY = 3V, RLD AMPLIFIER TURNED OFF)							
Quiescent Power Dissipation	ADX921/2/3		Normal mode		860	946	µW
			Standby mode		150		µW
	ADX920		Normal mode		542	600	µW
			Standby mode		150		µW
Quiescent Power Dissipation, per Channel	ADX921/2/3		Normal mode		430		µW
	ADX920		Normal mode		542		µW

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PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DISSIPATION (ANALOG SUPPLY = 5V, RLD AMPLIFIER TURNED OFF)							
Quiescent Power Dissipation	ADX921/2/3		Normal mode		1583		µW
			Standby mode		271		µW
	ADX920		Normal mode		1015		µW
			Standby mode		271		µW
Quiescent Power Dissipation, per Channel	ADX921/2/3		Normal mode		791		µW
	ADX920		Normal mode		1015		µW
POWER DISSIPATION IN POWER-DOWN MODE							
Analog Supply = 3V	DVDD = 1.8V				3.3		µW
	DVDD = 3.3V				9.8		µW
Analog Supply = 5V	DVDD = 1.8V				8		µW
	DVDD = 3.3V				11		µW
TEMPERATURE							
Specified Temperature Range				–40		85	°C
Operating Temperature Range				–40		85	°C
Storage Temperature Range				–60		150	°C

Note 1: Performance is applicable for 5V operation as well. Production testing for limits is performed at 3V.
Note 2: C_{FILTER} is the capacitor across the PGA outputs, see the PGA SETTINGS AND INPUT RANGE section for details.
Note 3: Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted (without electrode resistance) over a 10-second interval.
Note 4: CMRR is measured with a common-mode signal of AVSS + 0.3V to AVDD – 0.3V. The values indicated are the minimum of the two channels.

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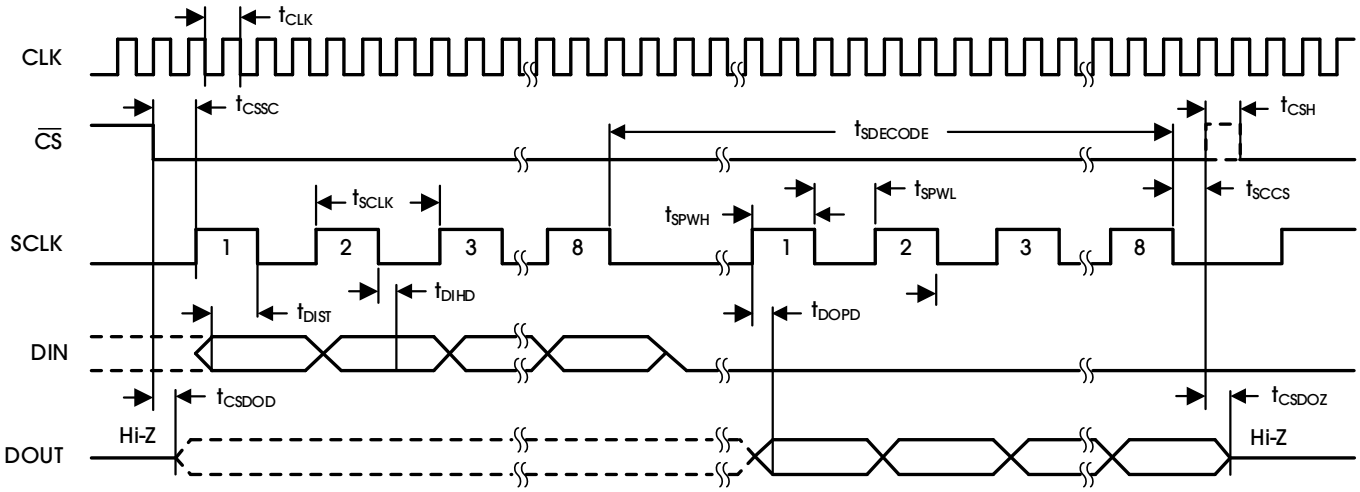
5.6 TIMING REQUIREMENTS

Table 10 lists the timing requirements. Specifications apply from –40°C to 85°C, load on DOUT = 20pF | | 100kΩ.

Table 10. Timing Requirements

PARAMETER	SYMBOL	2.7V ≤ DVDD ≤ 3.6V			1.65V ≤ DVDD < 2.7V			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
Master Clock Period (CLK_DIV Bit of LOFF_STAT Register = 0)	t_{CLK}	1775		2170	1775		2170	ns
Master Clock Period (CLK_DIV Bit of LOFF_STAT Register = 1)		444		542	444		542	ns
$\overline{CS}$ Low to First SCLK, Setup Time	t_{CSSC}	6			17			ns
SCLK Period	t_{SCLK}	50			66.6			ns
SCLK Pulse Width, High and Low	$t_{SPWH, L}$	15			25			ns
DIN Valid to SCLK Falling Edge: Setup Time	t_{DIST}	10			10			ns
Valid DIN after SCLK Falling Edge: Hold Time	t_{DIHD}	10			11			ns
SCLK Rising Edge to DOUT Valid	t_{DOPD}			12			22	ns
$\overline{CS}$ High Pulse	t_{CSH}	2			2			t_{CLK}s
$\overline{CS}$ Low to DOUT Driven	t_{CSDOD}	10			20			ns
Eighth SCLK Falling Edge to $\overline{CS}$ High	t_{SCCS}	3			3			t_{CLK}s
Command Decode Time	$t_{SDECODE}$	4			4			t_{CLK}s
$\overline{CS}$ High to DOUT Hi-Z	t_{CSDOZ}			10			20	ns

Figure 3 shows the serial interface timing.



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 3. Serial Interface Timing

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6. TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C, DVDD = 1.8V, AVDD – AVSS = 3V, V_{REF} = 2.42V, external f_{CLK} = 512kHz, data rate = 500SPS, C_{FILTER} = 4.7nF, and gain = 6, unless otherwise noted.

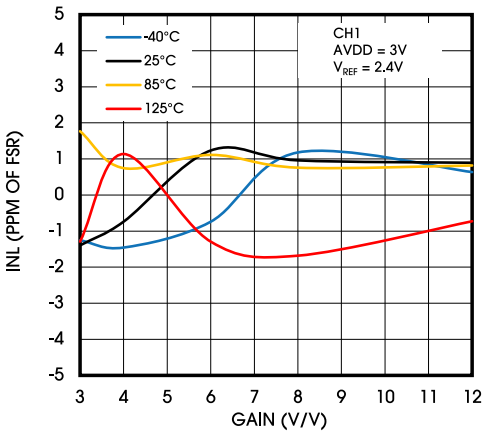

Figure 4. INL vs. Gain

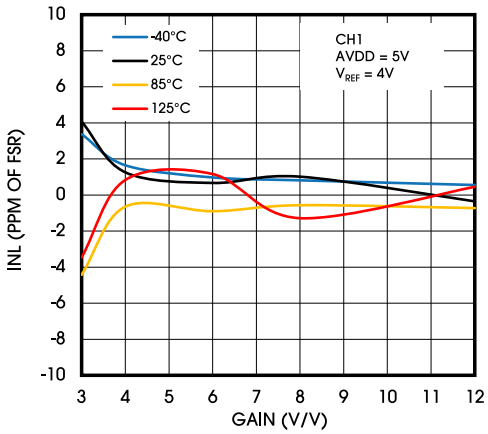

Figure 5. INL vs. Gain

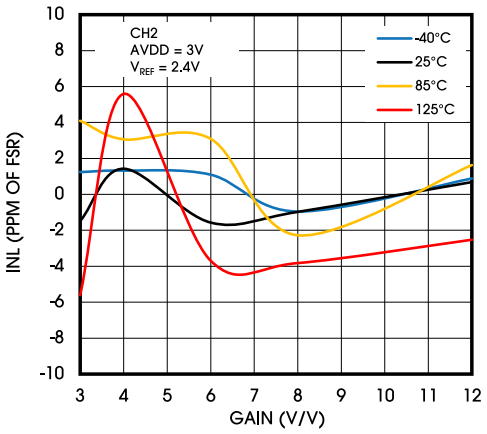

Figure 6. INL vs. Gain

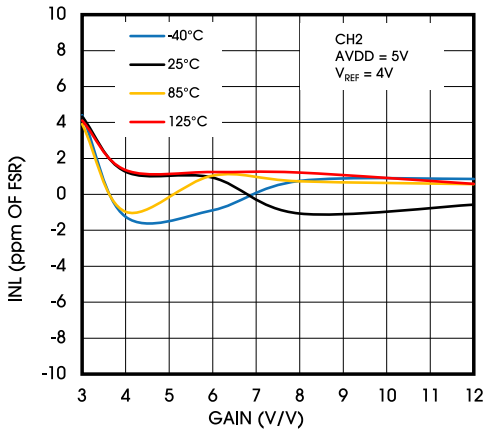

Figure 7. INL vs. Gain

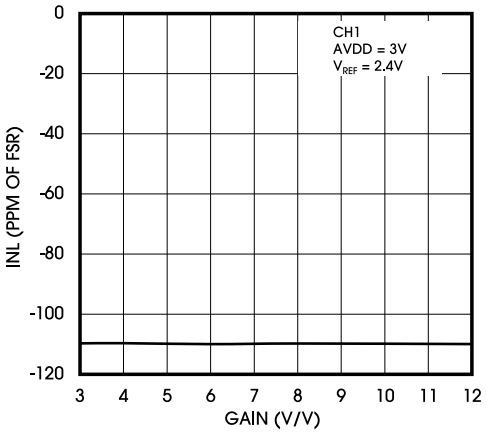

Figure 8. INL vs. Gain

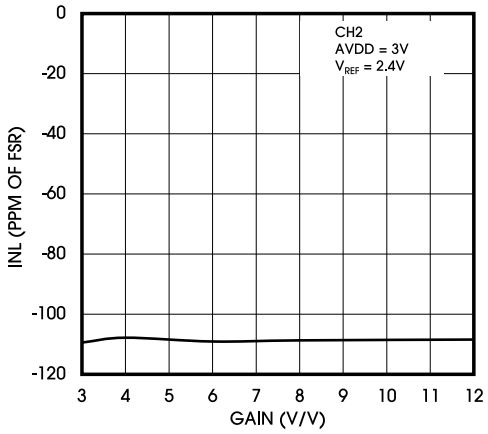

Figure 9. INL vs. Gain

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7. TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

T_A = 25°C, DVDD = 1.8V, AVDD – AVSS = 3V, V_{REF} = 2.42V, external f_{CLK} = 512kHz, data rate = 500SPS, C_{FILTER} = 4.7nF, and gain = 6, unless otherwise noted.

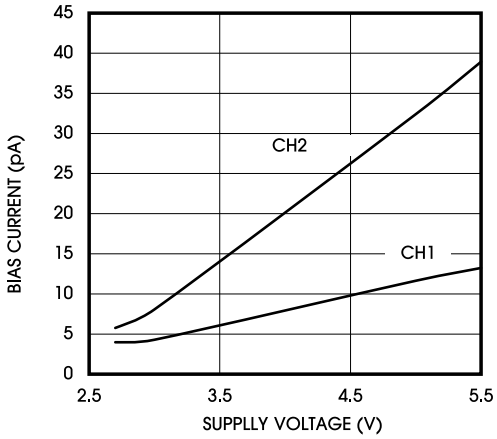

Figure 10. Bias Current vs. Supply Voltage

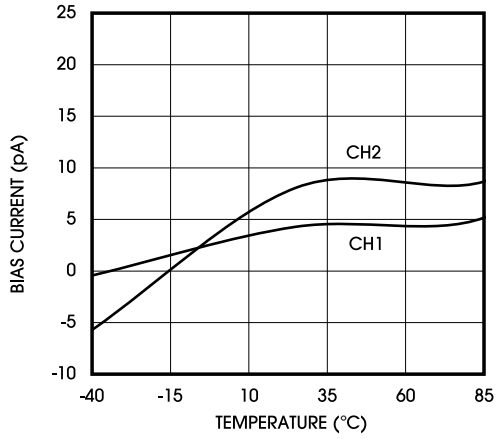

Figure 11. Bias Current vs. Temperature

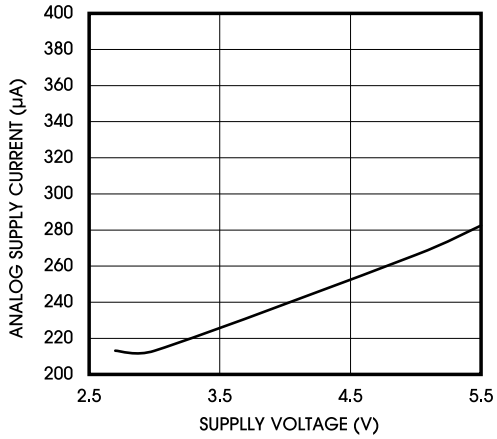

Figure 12. Analog Supply Current vs. Supply Voltage

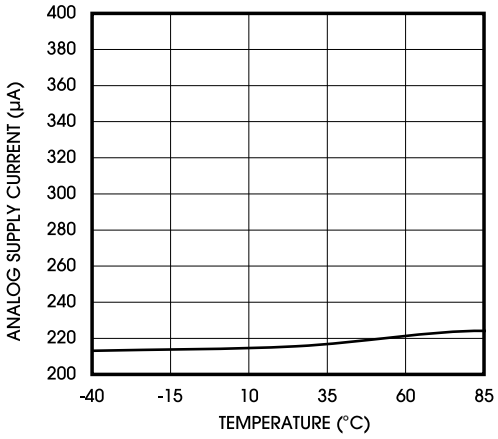

Figure 13. Analog Supply Current vs. Temperature

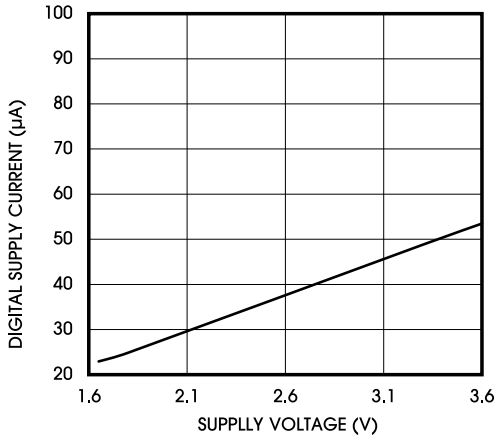

Figure 14. Digital Supply Current vs. Supply Voltage

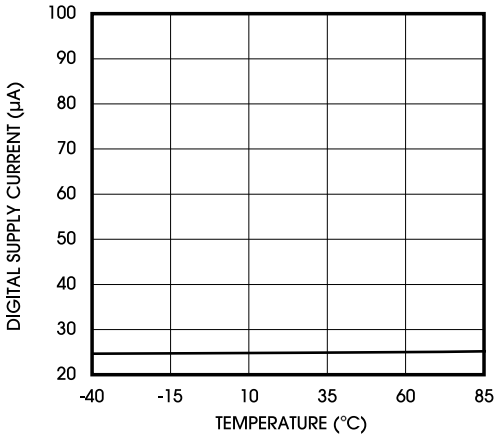

Figure 15. Digital Supply Current vs. Temperature

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8. TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

T_A = 25°C, DVDD = 1.8V, AVDD – AVSS = 3V, V_{REF} = 2.42V, external f_{CLK} = 512kHz, data rate = 500SPS, C_{FILTER} = 4.7nF, and gain = 6, unless otherwise noted.

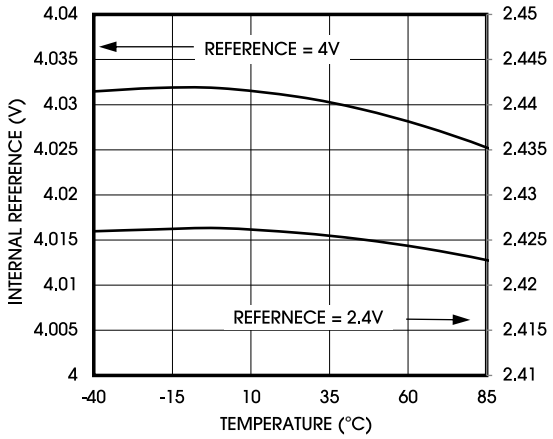

Figure 16. Internal Reference vs. Temperature

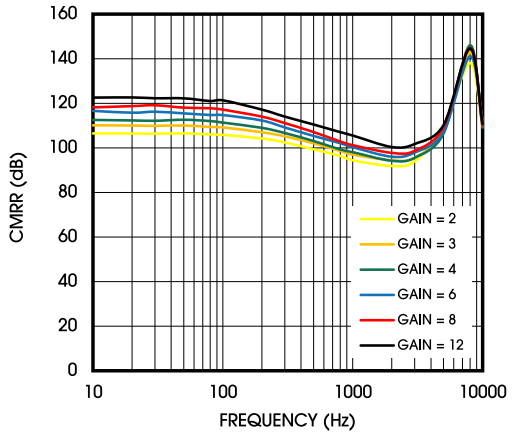

Figure 17. CMRR

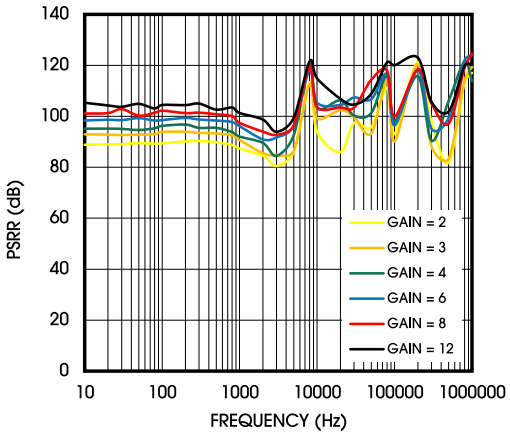

Figure 18. PSRR

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9. PARAMETER MEASUREMENT INFORMATION

9.1 NOISE PERFORMANCE

The ADX920/1/2/3 noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the programmable gain amplifier (PGA) value reduces the input-referred noise, which is particularly useful when measuring low-level biopotential signals. Table 11 through Table 21 summarize the ADX920/1/2/3 noise performance. The data are representative of typical noise performance at T_A = 25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. For the shown data rates, the ratio is approximately 6.6.

In Table 11 through Table 21, μV_{RMS} and μV_{PP} are measured values. Effective resolution (EFF RESOL) and dynamic range (DYN RANGE) are calculated with Equation 1 and Equation 2.

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \quad (1)$$

$$\text{Dynamic Range} = 20 \times \log_{10}\left|\frac{V_{REF}}{\sqrt{2} \times V_{RMS\_Noise} \times \text{Gain}}\right| \quad (2)$$

Table 11 through Table 18 show measurements taken with an internal reference on channel 1.

Table 11. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 1				PGA GAIN = 2			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	2.1	14.4	118.4	21.2	1.0	7.8	118.7	21.2
001	250	65.5	2.8	20.5	115.6	20.7	1.4	12.3	115.8	20.7
010	500	131	3.8	27.1	113.1	20.3	1.9	15.4	113.1	20.3
011	1000	262	5.5	46.7	109.9	19.7	2.8	25.4	109.7	19.7
100	2000	524	10.6	114.0	104.2	18.8	5.4	96.4	104.1	18.8
101	4000	1048	42.8	608.4	92.0	16.8	21.4	377.6	92.0	16.8
110	8000	2096	237.3	3860.5	77.2	14.3	118.3	1342.8	77.2	14.3

Table 12. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 3				PGA GAIN = 4			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.8	5.7	117.2	21.0	0.7	5.0	115.9	20.8
001	250	65.5	1.1	7.6	114.4	20.5	0.9	7.4	113.1	20.3
010	500	131	1.5	12.6	111.6	20.0	1.3	10.2	110.4	19.8
011	1000	262	2.1	17.9	108.6	19.5	1.8	15.1	107.4	19.3
100	2000	524	3.8	68.7	103.5	18.7	3.1	49.2	102.7	18.6
101	4000	1048	14.5	244.7	91.9	16.8	11.0	167.8	91.8	16.7
110	8000	2096	78.4	895.2	77.2	14.3	59.0	671.4	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

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Table 13. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 6				PGA GAIN = 8			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.6	5.0	112.9	20.3	0.6	4.3	111.2	20.0
001	250	65.5	0.8	6.8	110.9	19.9	0.8	6.2	108.7	19.6
010	500	131	1.1	9.0	108.0	19.4	1.0	8.5	106.2	19.1
011	1000	262	1.6	12.4	105.1	19.0	1.5	11.3	103.2	18.6
100	2000	524	2.5	33.4	101.1	18.3	2.3	26.4	99.5	18.0
101	4000	1048	7.7	104.9	91.4	16.7	5.9	77.4	91.2	16.6
110	8000	2096	39.5	447.6	77.2	14.3	29.7	335.7	77.1	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 14. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 12			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.6	4.0	108.2	19.5
001	250	65.5	0.7	5.4	106.0	19.1
010	500	131	1.0	8.7	103.1	18.6
011	1000	262	1.4	12.0	100.2	18.1
100	2000	524	2.0	17.3	96.9	17.6
101	4000	1048	4.4	48.1	90.2	16.5
110	8000	2096	18.5	195.8	77.7	14.4

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 15. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 1				PGA GAIN = 2			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	2.1	13.9	122.8	21.9	1.0	6.7	123.4	22.0
001	250	65.5	2.6	19.7	120.7	21.6	1.4	9.6	120.4	21.5
010	500	131	3.7	27.4	117.8	21.1	1.9	14.2	117.6	21.0
011	1000	262	5.5	55.8	114.2	20.5	2.8	30.3	114.1	20.4
100	2000	524	14.2	266.8	106.0	19.1	7.1	134.4	106.0	19.1
101	4000	1048	71.0	1468.3	92.1	16.8	34.9	681.7	92.2	16.8
110	8000	2096	392.7	4615.4	77.2	14.3	197.9	2307.7	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

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Table 16. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 3				PGA GAIN = 4			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.8	5.8	121.8	21.7	0.7	4.9	120.6	21.5
001	250	65.5	1.0	7.7	119.4	21.3	0.9	6.5	118.0	21.1
010	500	131	1.4	11.1	116.6	20.9	1.2	9.5	115.3	20.7
011	1000	262	2.1	21.6	113.0	20.3	1.8	16.6	112.0	20.1
100	2000	524	4.9	95.4	105.7	19.1	3.9	67.7	105.3	19.0
101	4000	1048	23.5	460.4	92.1	16.8	17.7	323.4	92.1	16.8
110	8000	2096	130.7	1491.8	77.2	14.3	98.1	1118.9	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 17. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 6				PGA GAIN = 8			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.6	4.1	118.2	21.1	0.5	3.8	117.1	20.9
001	250	65.5	0.8	6.1	115.9	20.8	0.7	5.5	113.8	20.4
010	500	131	1.0	8.4	113.2	20.3	1.0	8.0	111.3	20.0
011	1000	262	1.5	13.2	110.1	19.8	1.4	10.6	108.4	19.5
100	2000	524	2.9	49.1	104.4	18.8	2.4	36.1	103.4	18.7
101	4000	1048	11.9	198.1	92.0	16.8	9.0	135.5	91.9	16.8
110	8000	2096	65.4	745.9	77.2	14.3	49.3	559.4	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 18. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 12			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.5	3.5	113.2	20.3
001	250	65.5	0.7	5.2	111.0	19.9
010	500	131	0.9	8.6	108.3	19.5
011	1000	262	1.3	10.9	105.5	19.0
100	2000	524	2.0	24.8	101.4	18.3
101	4000	1048	6.2	84.5	91.6	16.7
110	8000	2096	32.6	373.0	77.3	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

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Table 19 through Table 21 show measurements taken with an internal reference on channel 2 in HS mode.

Table 19. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 3				PGA GAIN = 4			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	250	65.5	2.8	18.6	106.2	19.1	2.2	15.2	105.6	19.0
001	500	131	3.8	28.8	103.6	18.7	3.1	23.4	102.8	18.6
010	1000	262	5.2	38.8	100.8	18.2	4.3	34.0	99.9	18.1
011	2000	524	7.4	56.6	97.7	17.7	6.0	51.7	97.1	17.6
100	4000	1048	10.8	91.8	94.5	17.2	8.5	74.1	94.0	17.1
101	8000	2096	20.3	206.4	89.0	16.3	15.9	173.2	88.6	16.2
110	16000	4192	82.0	867.2	76.8	14.3	62.2	692.4	76.7	14.2

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 20. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 6				PGA GAIN = 8			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	250	65.5	1.7	12.4	104.5	18.9	1.4	9.8	103.8	18.7
001	500	131	2.3	17.9	101.7	18.4	1.9	14.1	100.9	18.3
010	1000	262	3.2	28.3	98.9	17.9	2.7	22.4	97.9	17.8
011	2000	524	4.5	36.5	95.9	17.4	3.8	36.9	94.9	17.3
100	4000	1048	6.5	53.9	92.8	16.9	5.5	43.3	91.9	16.8
101	8000	2096	11.5	106.6	87.9	16.1	9.2	93.1	87.3	16.0
110	16000	4192	41.9	461.6	76.6	14.2	31.7	356.7	76.6	14.2

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 21. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	-3dB BANDWIDTH (Hz)	PGA GAIN = 12			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	250	65.5	1.1	7.8	102.1	18.5
001	500	131	1.5	11.7	99.3	18.0
010	1000	262	2.2	17.1	96.4	17.5
011	2000	524	3.0	28.6	93.5	17.0
100	4000	1048	4.3	35.9	90.4	16.5
101	8000	2096	7.0	67.3	86.2	15.8
110	16000	4192	21.7	209.8	76.4	14.2

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

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10. DETAILED DESCRIPTION

10.1 OVERVIEW

The ADX920/1/2/3 devices are low-power, multichannel, simultaneously-sampling, 24-bit delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with integrated programmable gain amplifiers (PGAs). These devices integrate various electrocardiogram (ECG)-specific functions that make them well-suited for scalable ECG, sports, and fitness applications. The devices can also be used in high-performance, multichannel data acquisition systems by powering down the ECG-specific circuitry.

The ADX920/1/2/3 devices have a highly programmable multiplexer that allows for temperature, supply, input short, and RLD measurements. Additionally, the multiplexer allows any of the input electrodes to be programmed as the patient reference drive. The PGA gain can be chosen from one of seven settings (1, 2, 3, 4, 6, 8, and 12). The ADCs in the device offer data rates from 125SPS to 8kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides two general-purpose I/O (GPIO) pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to either 2.4V or 4V. The internal oscillator generates a 512kHz clock. The versatile right leg drive (RLD) block allows the user to choose the average of any combination of electrodes to generate the patient drive signal. Lead-off detection can be accomplished either by using an external pull-up or pull-down resistor or the device internal current source or sink. An internal AC lead-off detection feature is also available. Apart from the above features, the ADX922/3 provide options for internal respiration circuitry.

10.2 FUNCTIONAL BLOCK DIAGRAM

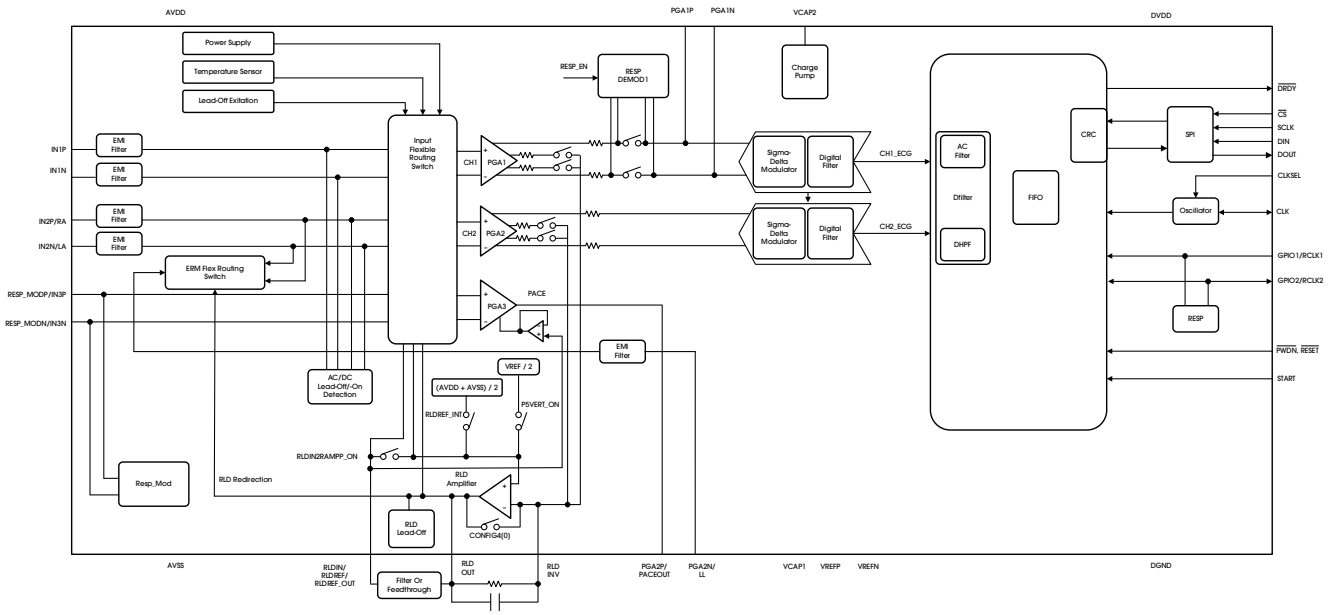

Figure 19. Functional Block Diagram

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10.3 FEATURE DESCRIPTION

10.3.1 MULTIPLEXER

This section contains details of the ADX920/1/2/3 internal functional elements. The analog blocks are discussed first followed by the digital interface. Blocks implementing ECG-specific functions are covered in the end.

Throughout this document, f_{CLK} denotes the signal frequency at the CLK pin, t_{CLK} denotes the signal period of the CLK pin, f_{DR} denotes the output data rate, t_{DR} denotes the output data time period, and f_{MOD} denotes the frequency at which the modulator samples the input.

10.3.2 EMI FILTER

An RC filter at the input acts as an electromagnetic interference (EMI) filter on channels 1 and 2. The –3dB filter bandwidth is approximately 6MHz.

10.3.3 INPUT MULTIPLEXER

The ADX920/1/2/3 input multiplexers are very flexible and provide many configurable signal-switching options. Figure 20 shows the multiplexer for the ADX920/1/2/3. Note that TESTP, TESTM, and RLDIN/RLDREF are common to both channels. INP and INN are separate for each of the three pins. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CH1SET or CH2SET register (see the CH1SET and CH2SET registers for details). More details of the ECG-specific features of the multiplexer are discussed in the INPUT MULTIPLEXER section.

10.3.4 DEVICE NOISE MEASUREMENTS

Setting CHnSET(3:0) = 0001 sets the common-mode voltage of (VREFP + VREFN) / 2 to both inputs of the channel. This setting can be used to test the inherent noise of the device in the user system.

10.3.5 TEST SIGNALS (TESTP AND TESTN)

Setting CHnSET(3:0) = 0101 provides internally-generated test signals for use in sub-system verification at power-up. This functionality allows the entire signal chain to be tested out. Although the test signals are similar to the CAL signals described in the IEC60601-2-51 specification, this feature is not intended for use in compliance testing.

Test signals are controlled through register settings (see the CONFIG2 register for details). INT_TEST enables the test signal and TEST_FREQ controls switching at the required frequency.

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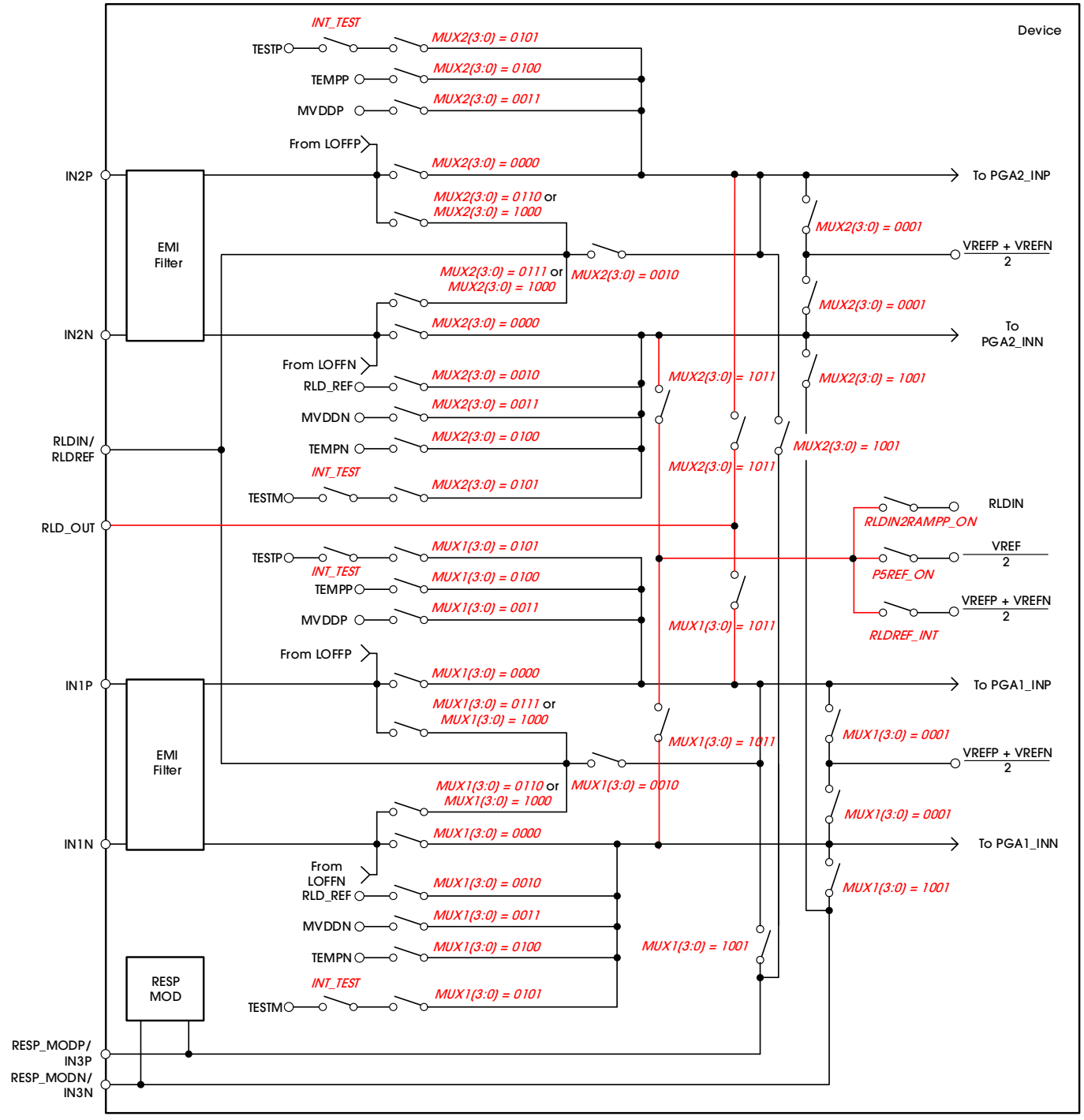

NOTE: MVDD monitor voltage supply depends on channel number; see the Supply Measurements (MVDDP, MVDDN) section.

Figure 20. Input Multiplexer Block for Both Channels

10.3.6 AUXILIARY DIFFERENTIAL INPUT (RESP_MODN/IN3N, RESP_MODP/IN3P)

In applications where the respiration modulator output is not used, the RESP_MODN/IN3N and RESP_MODP/IN3P signals can be used as a third multiplexed differential input channel. These inputs can be multiplexed to either of the ADC channels.

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10.3.7 TEMPERATURE SENSOR (TEMPP, TEMPN)

The ADX920/1/2/3 contain an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 21. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

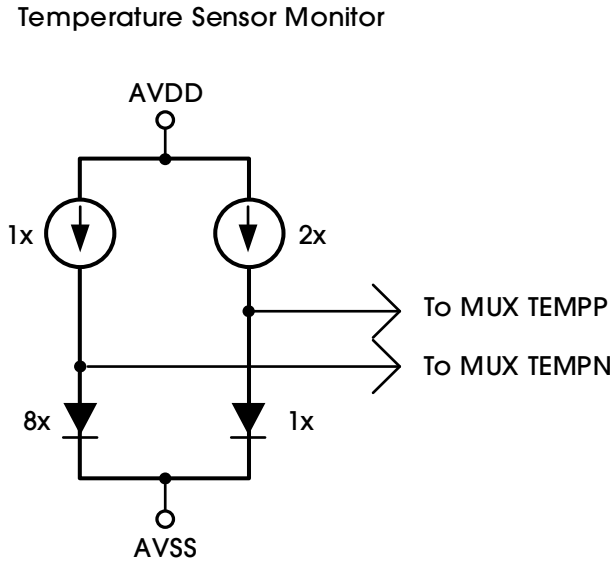

Figure 21. Temperature Sensor Measurement in the Input

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADX920/1/2/3 causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 3 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to µV.

$$\text{Temperature (°C)} = \left[\frac{\text{Temperature Reading (µV)} - 143200\mu V}{481\mu V/°C}\right] + 25°C \quad (3)$$

10.3.8 SUPPLY MEASUREMENTS (MVDDP, MVDDN)

Setting CHnSET(3:0) = 0011 sets the channel inputs to different supply voltages of the device. For channel 1, (MVDDP – MVDDN) is (0.5 (AVDD + AVSS)), for channel 2, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to 1.

10.3.9 LEAD-OFF EXCITATION SIGNALS (LOFFP, LOFFN)

The lead-off excitation signals are fed into the multiplexer before the switches. The comparators that detect the lead-off condition are also connected to the multiplexer block before the switches. For a detailed description of the lead-off block, refer to the LEAD-OFF DETECTION section.

10.3.10 AUXILIARY SINGLE-ENDED INPUT

The RLDIN/RLDREF pin is primarily used for routing the right leg drive signal to any of the electrodes in case the right leg drive electrode falls off. However, the RLDIN/RLDREF pin can be used as a multiple single-ended input channel. The signal at the RLDIN/RLDREF pin can be measured with respect to the midsupply ((AVDD + AVSS) / 2). This measurement is done by configuring the channel multiplexer setting MUXn(3:0) to 0010 in the CH1SET and CH2SET registers.

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10.3.11 ANALOG INPUT

The ADX920/1/2/3 analog inputs are fully differential. Assuming PGA = 1, the differential input (INP – INN) can span between $-V_{REF}$ to $+V_{REF}$. Note that the absolute range for INP and INN must be between AVSS – 0.3V and AVDD + 0.3V. Refer to Table 27 for an explanation of the correlation between the analog input and the digital codes. There are two general methods of driving the ADX920/1/2/3 analog input: single-ended or differential, as shown in Figure 22 and Figure 23. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is (common-mode + 1/2 V_{REF}) and (common-mode – 1/2 V_{REF}). When the input is differential, the common-mode is given by (INP + INN) / 2. Both INP and INN inputs swing from (common-mode + 1/2 V_{REF} to common-mode – 1/2 V_{REF}). For optimal performance, it is recommended that the ADX920/1/2/3 be used in a differential configuration.

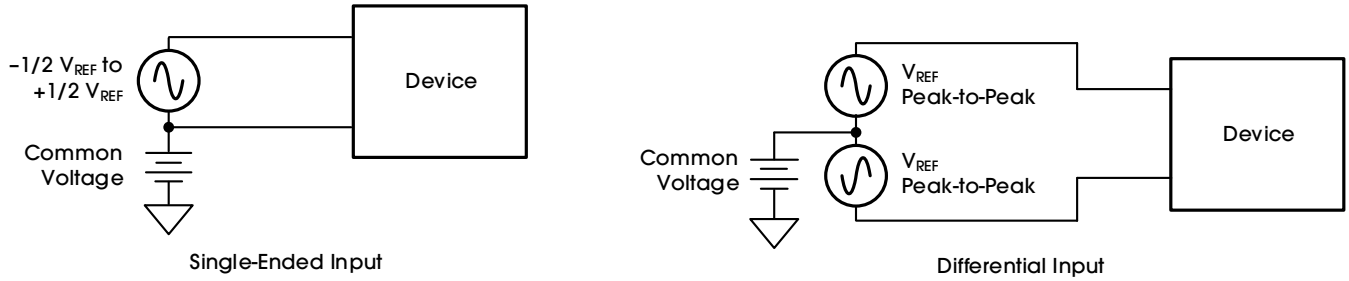
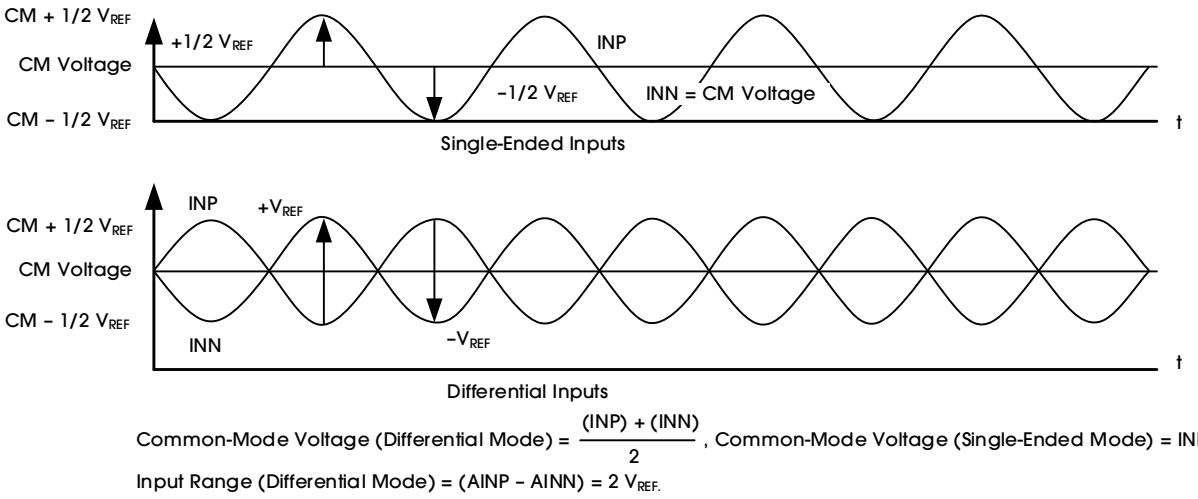


Figure 22. Methods of Driving the ADX920/1/2/3: Single-Ended or Differential



Common-Mode Voltage (Differential Mode) = $\frac{(INP) + (INN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = INN.

Input Range (Differential Mode) = (AINP – AINN) = 2 V_{REF}.

Figure 23. Using the ADX920/1/2/3 in Single-Ended and Differential Input Modes

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10.3.12 PGA SETTINGS AND INPUT RANGE

The PGA is a differential input or differential output amplifier. It has seven gain settings (1, 2, 3, 4, 6, 8, and 12) that can be set by writing to the CHnSET register (see the CH1SET and CH2SET Registers in the REGISTER MAPS section for details). The ADX920/1/2/3 devices have CMOS inputs and hence have negligible current noise.

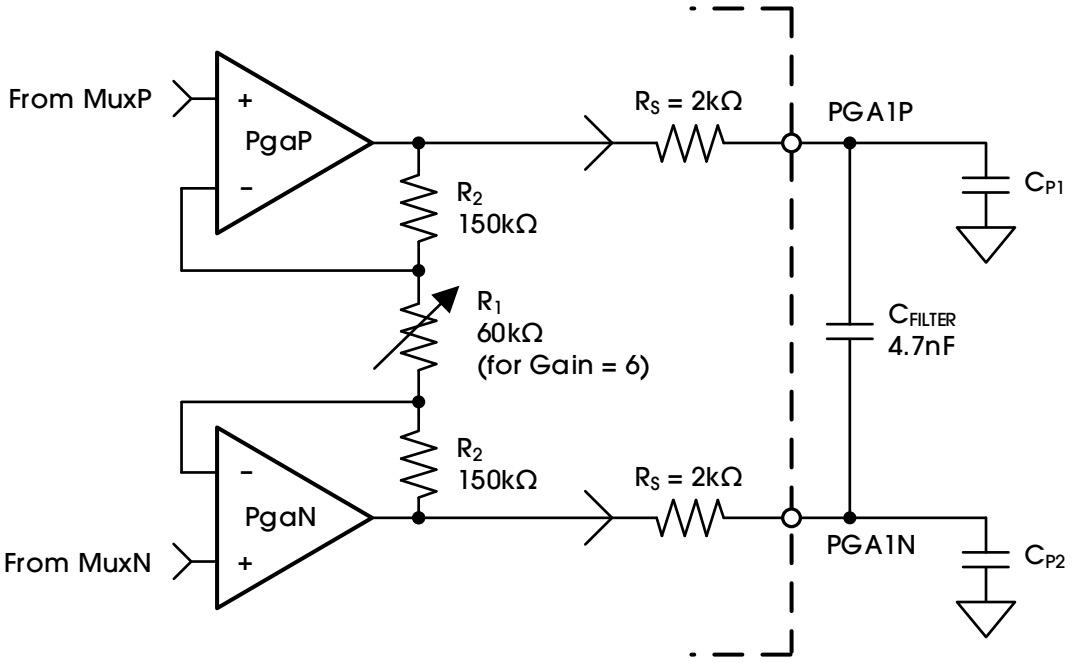

Figure 24. PGA Implementation

The PGA resistor string that implements the gain has 360kΩ of resistance for a gain of 6. This resistance provides a current path across the outputs of the PGA in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input. The PGA output is filtered by an RC filter before it goes to the ADC. The filter is formed by an internal resistor R_S = 2kΩ and an external capacitor C_{FILTER} (4.7nF, typical). This filter acts as an anti-aliasing filter with the –3dB bandwidth of 8.4kHz. The internal R_S resistor is accurate to 15%, so actual bandwidth will vary. This RC filter also suppresses the glitch at the PGA output caused by ADC sampling. The minimum value of C_{FILTER} that can be used is 4nF. A larger value C_{FILTER} capacitor can be used for increased attenuation at higher frequencies for anti-aliasing purposes. If channel 1 of the ADX922/3 is used for respiration measurement, then a 4.7nF external capacitor is recommended. The tradeoff is that a larger capacitor value gives degraded THD performance. See Figure 25 for a diagram explaining the THD versus C_{FILTER} value for a 10Hz input signal. Capacitor 1 and capacitor 2 can be 220pF ± 5% for typical application.

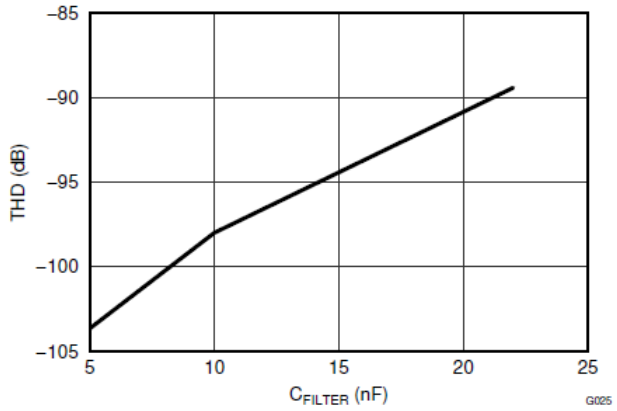

Figure 25. THD vs. C_{FILTER} Value

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Special care must be taken in PCB layout to minimize the parasitic capacitance C_{P1} / C_{P2}. The absolute value of these capacitances must be less than 20pF. Ideally, C_{FILTER} should be placed right at the pins to minimize these capacitors. Mismatch between these capacitors will lead to CMRR degradation. Assuming everything else is perfectly matched, the 60Hz CMRR as a function of this mismatch is given by Equation 4.

$$CMRR = 20\log \frac{Gain}{2\pi \times 2e3 \times \Delta C_P \times 60} \quad (4)$$

Where:

- $\Delta C_P = C_{P1} - C_{P2}$.

For example, a mismatch of 20pF with a gain of 6 limits the CMRR to 112dB. If ΔCP is small, then the CMRR is limited by the PGA itself and is as specified in the ELECTRICAL CHARACTERISTICS table. The PGA are chopped internally at either 8, 32, or 64kSPS, as determined by the CHOP bits (see the RLD_SENS register, bits(7:6)). The digital decimation filter filters out the chopping ripple in the normal path, so the chopping ripple is not a concern. If PGA output is used for hardware PACE detection, the chopping ripple must be filtered. First-order filtering is provided by the RC filter at the PGA output. Additional filtering may be needed to suppress the chopping ripple. If the PGA output is routed to other circuitry, a 20kΩ series resistance must be added in the path near the CFILTER capacitor. The routing should be matched to maintain the CMRR performance.

10.3.12.1 INPUT COMMON-MODE RANGE

The usable input common-mode range of the front end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. Equation 5 describes this range.

$$AVDD - 0.2V - \left(\frac{Gain \times V_{MAX\_DIFF}}{2}\right) > CM > AVSS + 0.2V + \left(\frac{Gain \times V_{MAX\_DIFF}}{2}\right) \quad (5)$$

Where:

- V_{MAX_DIFF} = maximum differential signal at the input of the PGA.

CM = common-mode range.

For example:

If VDD = 3V, gain = 6, and VMAX_DIFF = 350mV, then 1.25V < CM < 1.75V.

10.3.12.2 INPUT DIFFERENTIAL DYNAMIC RANGE

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. Equation 6 shows this range.

$$Max\ (INP - INN) < \frac{V_{REF}}{Gain}, \text{Full-Scale Range} = \frac{\pm V_{REF}}{Gain} = \frac{2V_{REF}}{Gain} \quad (6)$$

The 3V supply, with a reference of 2.4V and a gain of 6 for ECGs, is optimized for power with a differential input signal of approximately 300mV. For higher dynamic range, a 5V supply with a reference of 4V (set by the VREF_4V bit of the CONFIG2 register) can be used to increase the differential dynamic range.

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10.3.12.3 ADC ΔΣ MODULATOR

Each channel of the ADX920/1/2/3 has a 24-bit ΔΣ ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of $f_{MOD} = f_{CLK} / 4$ or $f_{CLK} / 16$, as determined by the CLK_DIV bit. In both cases, the sampling clock has a typical value of 128kHz. As in the case of any ΔΣ modulator, the ADX920/1/2/3 noise is shaped until $f_{MOD} / 2$, as shown in Figure 26. The on-chip digital decimation filters explained in the DIGITAL DECIMATION FILTER section can be used to filter out the noise at higher frequencies. These on-chip decimation filters also provide antialias filtering. This feature of the ΔΣ converters drastically reduces the complexity of analog antialiasing filters that are typically needed with nyquist ADCs.

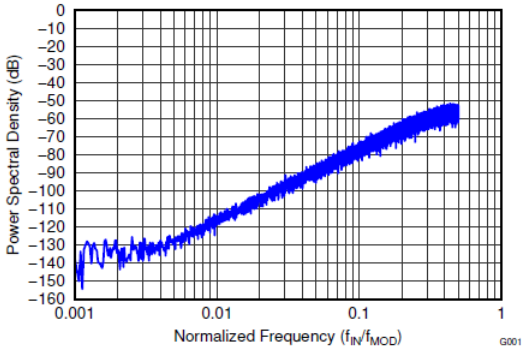

Figure 26. Power Spectral Density (PSD) of a ΔΣ Modulator (4-Bit Quantizer)

10.3.13 DIGITAL DECIMATION FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in ECG applications for implementing software pace detection and AC lead-off detection.

The digital filter on each channel consists of a third-order sinc filter. The decimation ratio on the sinc filters can be adjusted by the DR bits in the CONFIG1 register (see the REGISTER MAPS section for details). This setting is a global setting that affects all channels and, therefore, in a device all channels operate at the same data rate.

10.3.14 SINC FILTER STAGE (SINX / X)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter.

Equation 7 shows the scaled Z-domain transfer function of the sinc filter.

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3 \tag{7}$$

The frequency-domain transfer function of the sinc filter is shown in Equation 8.

$$|H(f)| = \left| \frac{\sin\left[\frac{N\pi f}{f_{MOD}}\right]}{N \times \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^3 \tag{8}$$

Where:

- N = decimation ratio

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The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 27 shows the sinc filter frequency response and Figure 28 shows the sinc filter roll-off. With a step change at input, the filter takes 3 t_{DR} to settle. After a START signal rising edge, the filter takes t_{SETTLE} time to give the first data output. The filter settling times at various data rates are discussed in the START section. Figure 29 and Figure 30 show the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 31 shows the transfer function extended until 4 f_{MOD}. It can be seen that the ADX920/1/2/3 passband repeats itself at every f_{MOD}. The input R-C anti-aliasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

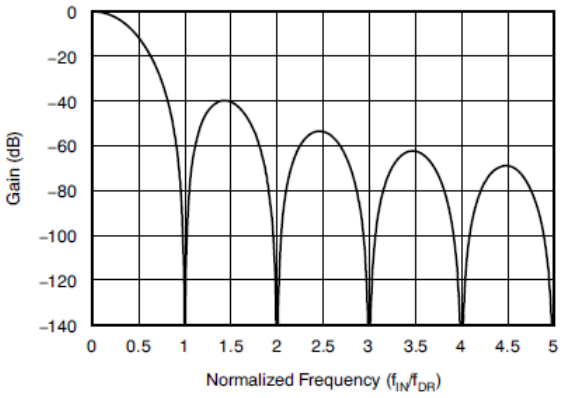

Figure 27. Sinc Filter Frequency Response

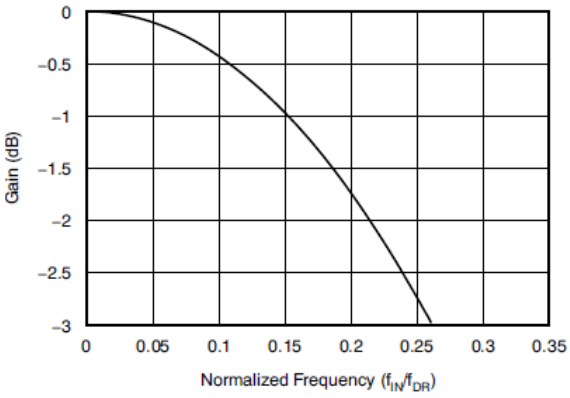

Figure 28. Sinc Filter Roll-Off

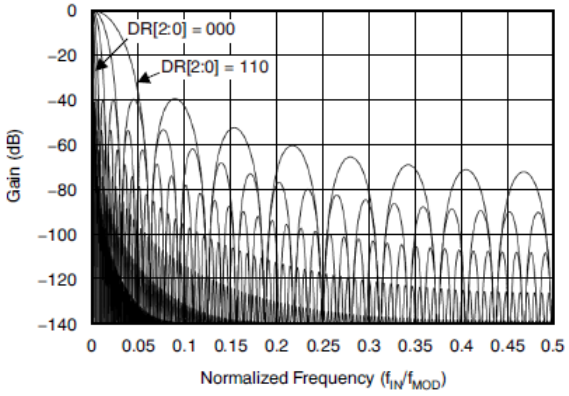

Figure 29. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 2

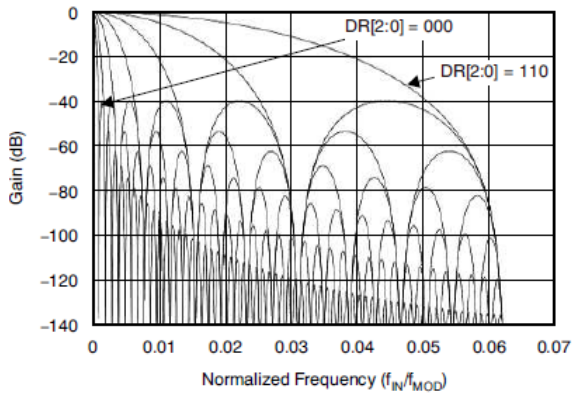

Figure 30. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 16

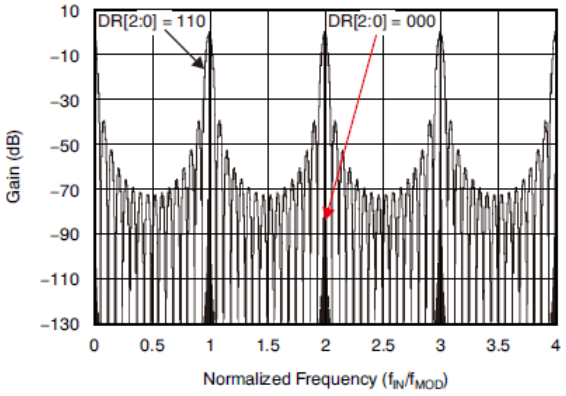

Figure 31. Transfer Function of On-Chip Decimation Filters Until 4 f_{MOD} for DR(2:0) = 000 and DR(2:0) = 110

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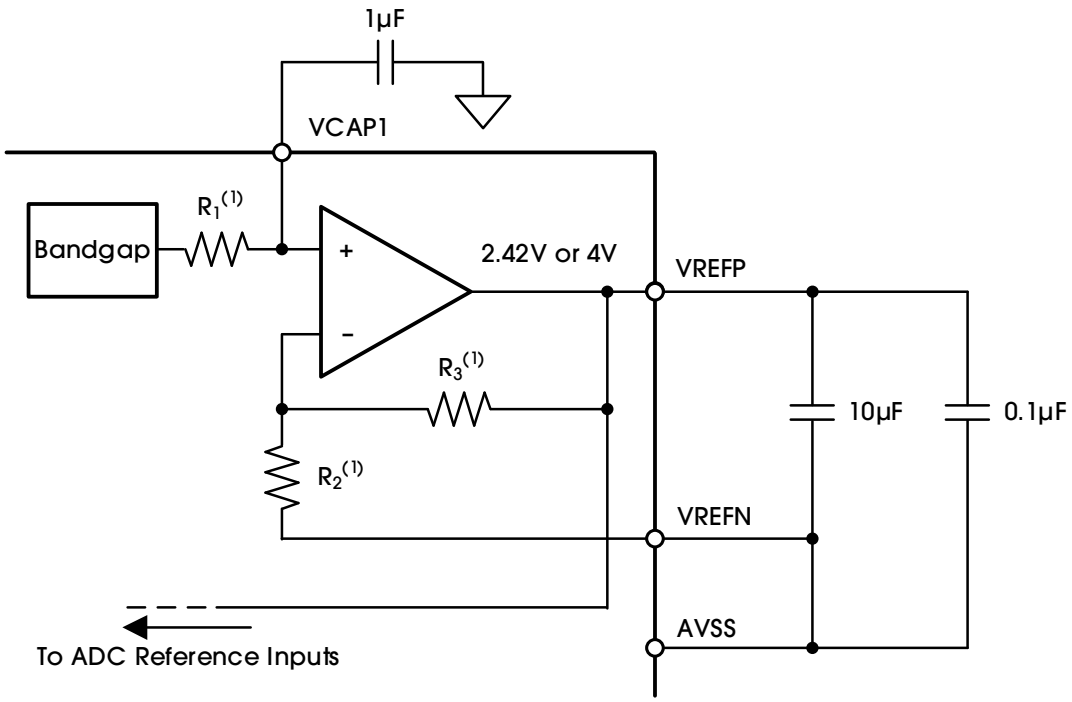
10.3.15 REFERENCE

Figure 32 shows a simplified block diagram of the ADX920/1/2/3 internal reference. The reference voltage is generated with respect to AVSS. The VREFN pin must always be connected to AVSS.



(1) For V_{REF} = 2.42V: R_1 = 100kΩ, R_2 = 200kΩ, and R_3 = 200kΩ. For V_{REF} = 4V: R_1 = 84kΩ, R_2 = 120kΩ, and R_3 = 280kΩ.

Figure 32. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end ECG systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10Hz so that the reference noise does not dominate the system noise. When using a 3V analog supply, the internal reference must be set to 2.4V. In case of a 5V analog supply, the internal reference can be set to 4V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be applied externally. Figure 33 shows a typical external reference drive circuitry. Power-down is controlled by the PDB_REFBUF bit in the CONFIG2 register. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

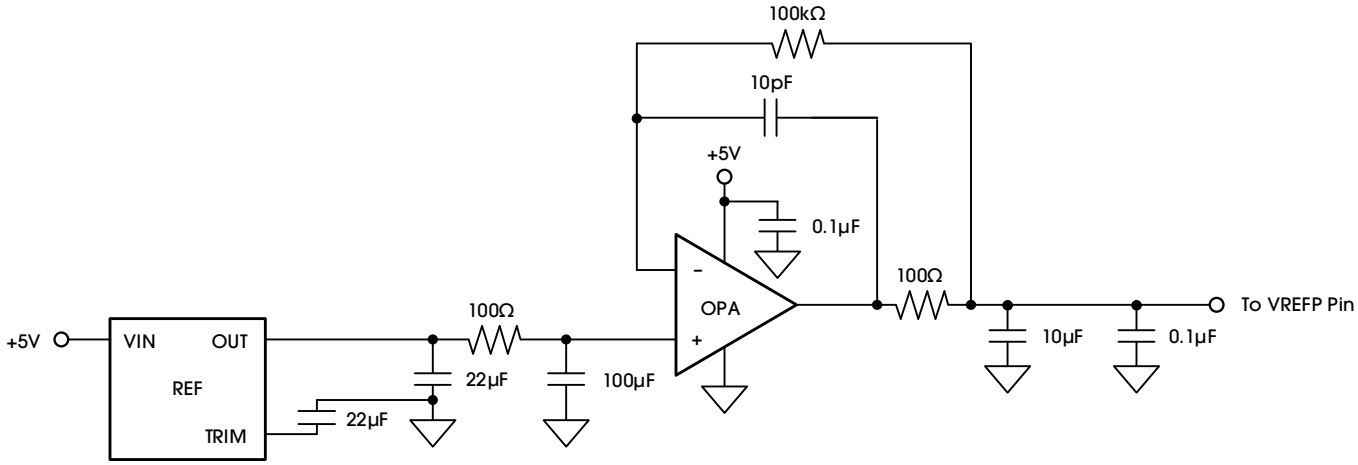


Figure 33. External Reference Driver

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10.3.16 CLOCK

The ADX920/1/2/3 devices provide two different methods for device clocking: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Over the specified temperature range the accuracy varies, see the ELECTRICAL CHARACTERISTICS. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG2 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 22. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. It is recommended that during power-down the external clock be shut down to save power.

Table 22. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG2.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

The ADX920/1/2/3 devices have the option to choose between two different external clock frequencies (512kHz or 2.048MHz). This frequency is selected by setting the CLK_DIV bit (bit 6) in the LOFF_STAT register. The modulator must be clocked at 128kHz, regardless of the external clock frequency. Figure 34 shows the relationship between the external clock (f_{CLK}) and the modulator clock (f_{MOD}). The default mode of operation is f_{CLK} = 512kHz. The higher frequency option has been provided to allow the SPI to run at a higher speed. SCLK can be only twice the speed of f_{CLK} during a register read or write, see section on sending multi-byte commands. Having the 2.048MHz option allows for register read and writes to be performed at SCLK speeds up to 4.096MHz.

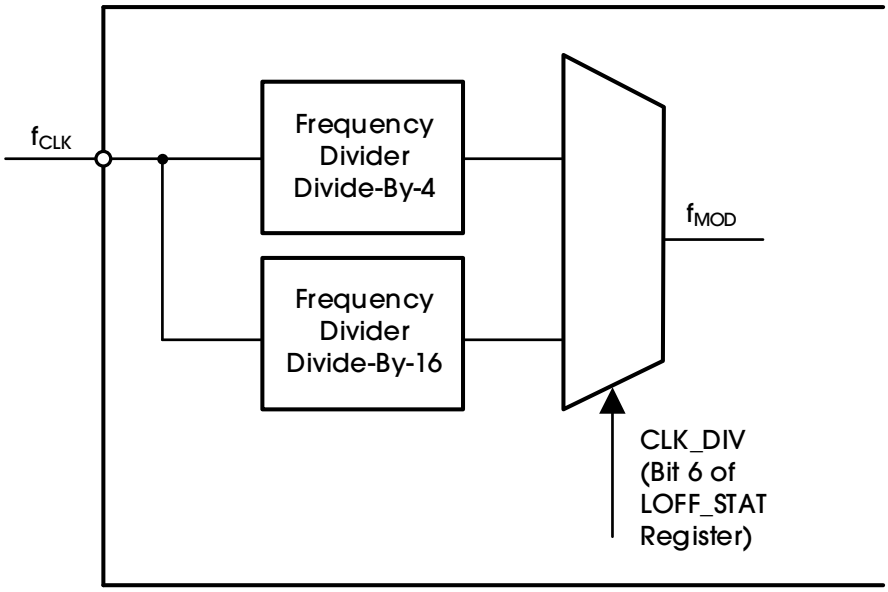

Figure 34. Relationship Between External Clock (f_{CLK}) and Modulator Clock (f_{MOD})

The ADX920/1/2/3 can set internal oscillator clock to detect external clock when the CLKSEL pin is 0. If the external clock missing extends 255 internal oscillator cycles, the device clock source will be switched to internal oscillator clock and the CLK_MISS field of MOD_STAT1 will be set. After CLK_MISS is set a chip level, reset is needed.

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10.3.17 POWER MODE

The device has four working modes to balance the performance and power for dedicated application usage. Table 23 shows the configuration for different modes. High Speed has better performance and the higher power consumption, while High Resolution has the better power consumption compared with the High Speed mode on the same data rate setting. Follow Table 23 to configure the power mode.

Table 23. WMODE Setting

WMODE(1:0)	CLOCK FREQUENCY	LOFF_STAT(6:5)	RESP2(6)	LOFF_SEN(6)	DR(2:0) and ODR
High Speed	1.024MHz /2.048MHz	2'b00 / 2'b10'	0: f_{MOD} = 256kHz	0	DR = 0, ODR = 250SPS
High Resolution	512kHz / 2.048MHz	2'b00 /2'b01	0: f_{MOD} = 128kHz	0	DR = 0, ODR = 125SPS

Table 24 and Table 25 show the noise performance with gain = 6 for High Speed mode.

Table 24. Channel 1 Noise Performance with Gain = 6

SETTING	MODCLK = 0 (256kHz)			
	LOFF_SEN(6) = 0		LOFF_SEN(6) = 1	
	250SPS	500SPS	250SPS	500SPS
NOISE	3.7μV_{PP}	4.9μV_{PP}	3.9μV_{PP}	5.3μV_{PP}

Table 25. Channel 2 Noise Performance with Gain = 6

SETTING	MODCLK = 0 (256kHz)			
	LOFF_SEN(6) = 0		LOFF_SEN(6) = 1	
	250SPS	500SPS	250SPS	500SPS
NOISE	14.9μV_{PP}	17.2μV_{PP}	16.3μV_{PP}	18.1μV_{PP}

With different work mode, the data rate can be configured to meet application requirements. The f_{MOD} is decided by WMODE, clock frequency and clock divider.

Table 26. Data Rate Configuration

BIT	OVERSAMPLING RATIO	f_{MOD} = 256kHz	f_{MOD} = 128kHz
000	f_{MOD} / 1024	250SPS	125SPS
001	f_{MOD} / 512	500SPS	250SPS
010	f_{MOD} / 256	1kSPS (default)	500SPS (default)
011	f_{MOD} / 128	2kSPS	1kSPS
100	f_{MOD} / 64	4kSPS	2kSPS
101	f_{MOD} / 32	8kSPS	4kSPS
110	f_{MOD} / 16	16kSPS	8kSPS
111	Do not use	Do not use	Do not use

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10.3.18 DATA FORMAT

The ADX920/1/2/3 devices output 24 bits of data per channel in binary two's complement format, MSB first. The LSB has a weight of V_{REF} / (2^{23} – 1). A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 27 summarizes ideal output codes for different input signals. All 24 bits toggle when the analog input is at positive or negative full-scale.

Table 27. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ V_{REF}	7FFFFFh
+V_{REF} / (2^{23} – 1)	000001h
0	000000h
–V_{REF} / (2^{23} – 1)	FFFFFFh
≤ –V_{REF} (2^{23} / 2^{23} – 1)	800000h

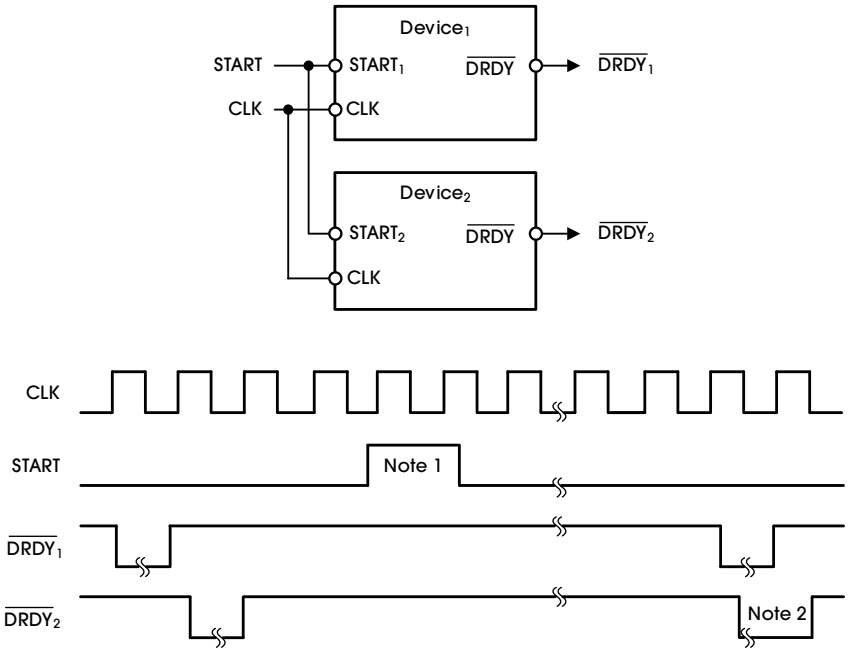
Note: Excludes effects of noise, linearity, offset, and gain error.

10.3.19 MULTIPLE DEVICE CONFIGURATION

The ADX920/1/2/3 devices are designed to provide configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{CS}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface n devices is 3 + n.

The right leg drive amplifiers can be daisy-chained as explained in the RLD CONFIGURATION WITH MULTIPLE DEVICES section. To use the internal oscillator in a daisy-chain configuration, one of the devices must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to 1. This master device clock is used as the external clock source for the other devices.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{DRDY}$ signal is fixed for a fixed data rate (see the START section for more details on the settling times). Figure 35 shows the behavior of two devices when synchronized with the START signal.



(1) Start pulse must be at least one t_{MOD} cycle wide.
(2) Settling time number uncertainty is one t_{MOD} cycle.

Figure 35. Synchronizing Multiple Converters

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10.3.20 STANDARD MODE

Figure 36 shows a configuration with two devices cascaded together. One of the devices is an ADX923 and the other is an ADX922. Together, they create a system with four channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{CS}$ being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus.

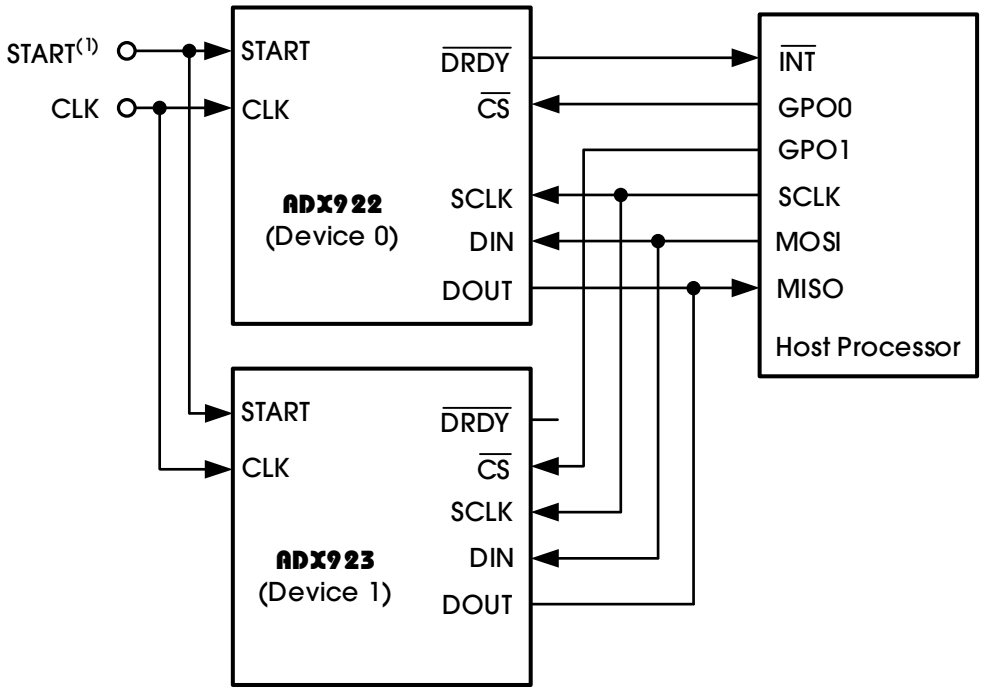

Figure 36. Multiple Device Configurations

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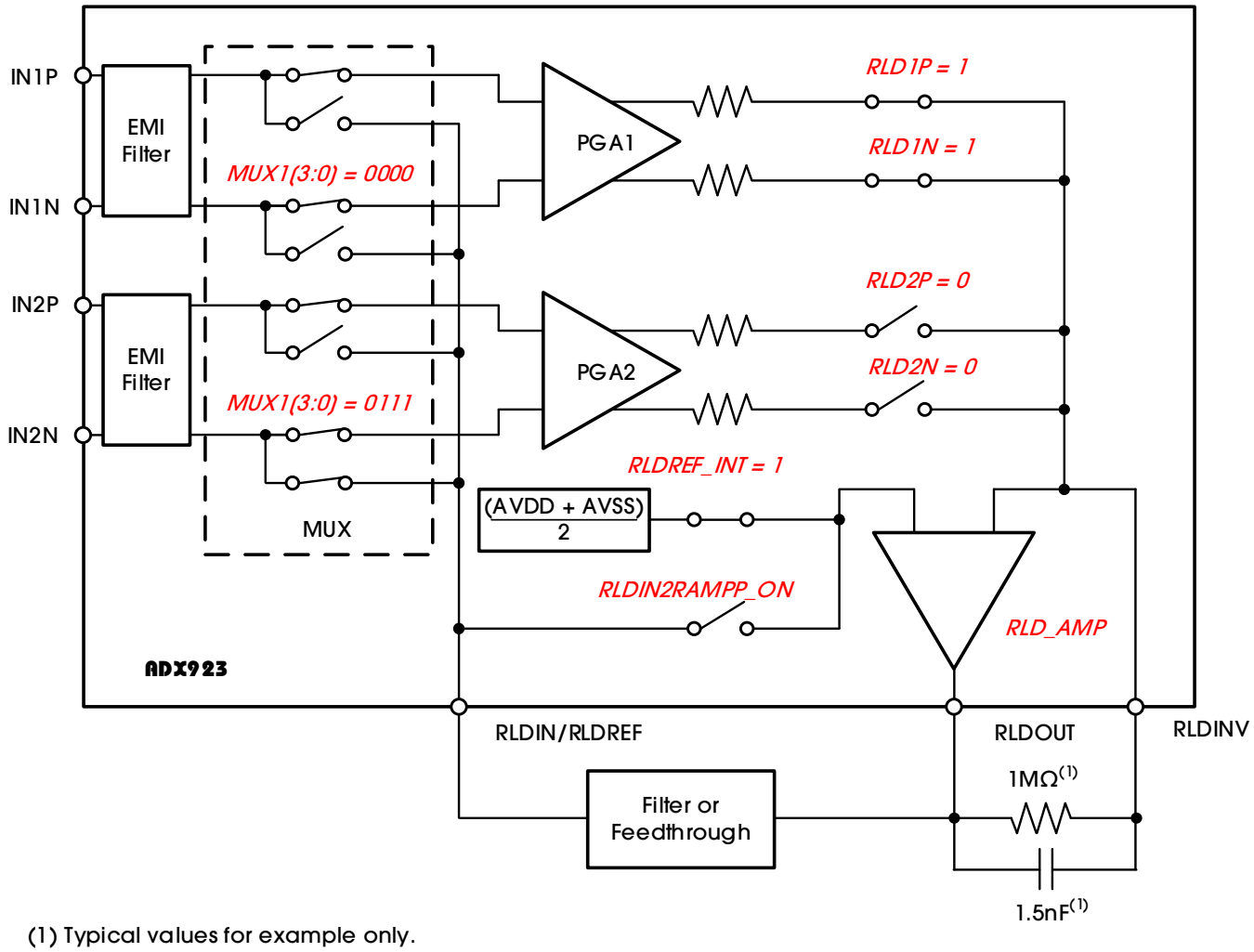
10.3.21 ECG-SPECIFIC FUNCTIONS

10.3.22 INPUT MULTIPLEXER (REROUTING THE RIGHT LEG DRIVE SIGNAL)

The input multiplexer has ECG-specific functions for the right leg drive signal. The RLD signal is available at the RLDOUT pin once the appropriate channels are selected for RLD derivation, feedback elements are installed external to the chip, and the loop is closed. This signal can be fed after filtering or fed directly into the RLDIN pin, as shown in Figure 37. This RLDIN signal can be multiplexed into any one of the input electrodes by setting the MUX bits of the appropriate channel set registers to 0110 for P -side or 0111 for N -side. Figure 37 shows the RLD signal generated from channel 1 and routed to the N-side of channel 2. This feature can be used to dynamically change the electrode that is used as the reference signal to drive the patient body. Note that the corresponding channel cannot be used and can be powered down.



(1) Typical values for example only.

Figure 37. Example RLDOUT Signal Configured to be Routed to IN2N

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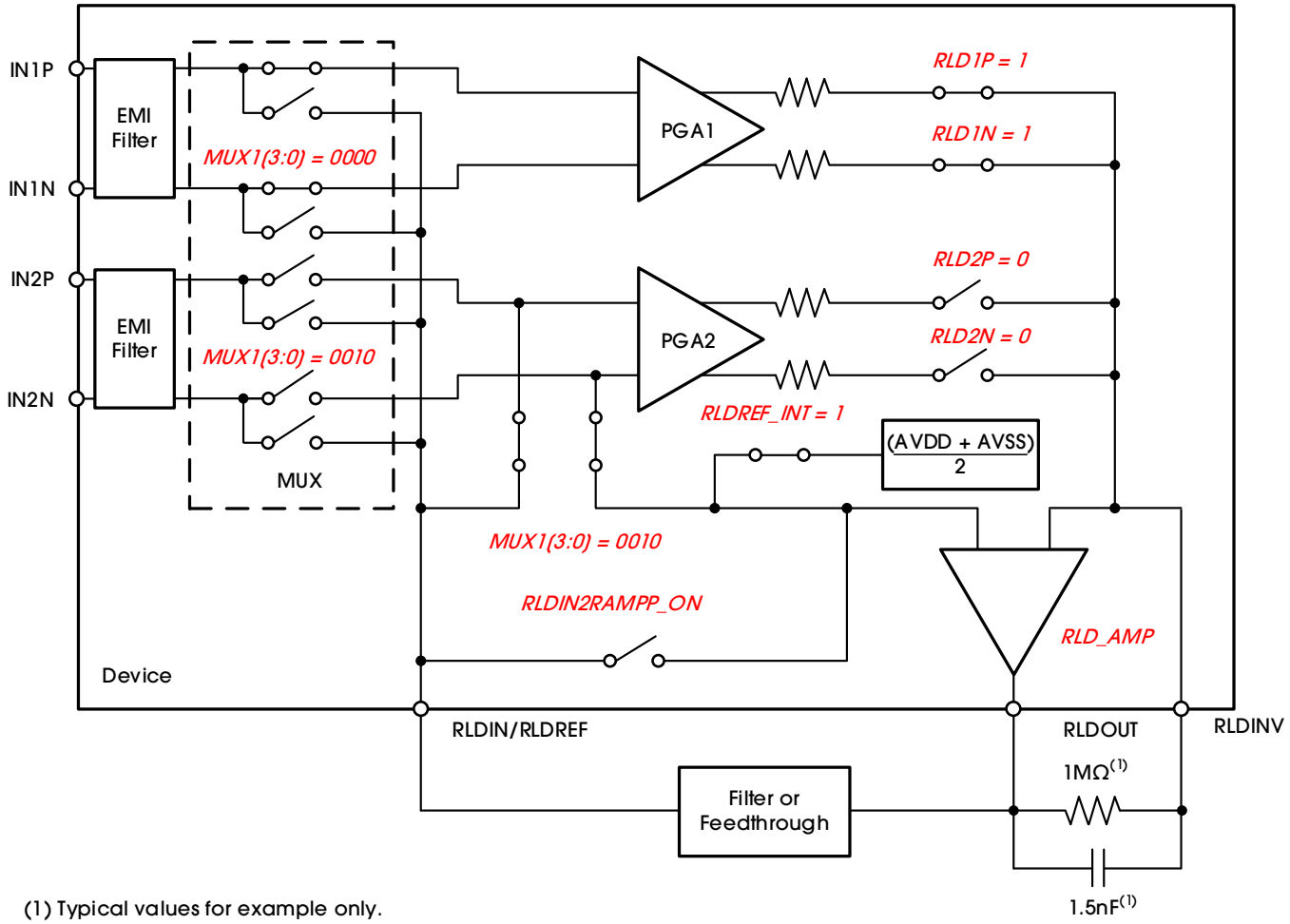
10.3.22.1.1 INPUT MULTIPLEXER (MEASURING THE RIGHT LEG DRIVE SIGNAL)

The RLDOUT signal can also be routed to a channel (that is not used for the calculation of RLD) for measurement. Figure 38 shows the register settings to route the RLDIN signal to channel 2. The measurement is done with respect to the voltage (AVDD + AVSS) / 2. This feature is useful for debugging purposes during product development.



(1) Typical values for example only.

Figure 38. RLDOUT Signal Configured to be Read Back by Channel 2

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10.3.22.2 ERM MULTIPLEXER (ELECTRODE ROTATION MODE TO REDIRECT RLD SIGNAL)

The ADX923 input multiplexer has ECG-specific functions for the right leg drive signal with ERM mode. In ERM mode, IN2P will be used as fixed RA node, IN2N will be used as fixed LA node, PGA2N will be used as fixed LL node, and RLD will be redirected to the ERM flex routing switch. The RLD rotation switch is controlled by the ERM_CFG register (RLD2RA, RLD2LA, and RLD2LL fields), and the PGA2N pin is disconnected by CONFIG3. See Figure 39 for the rerouting diagram.

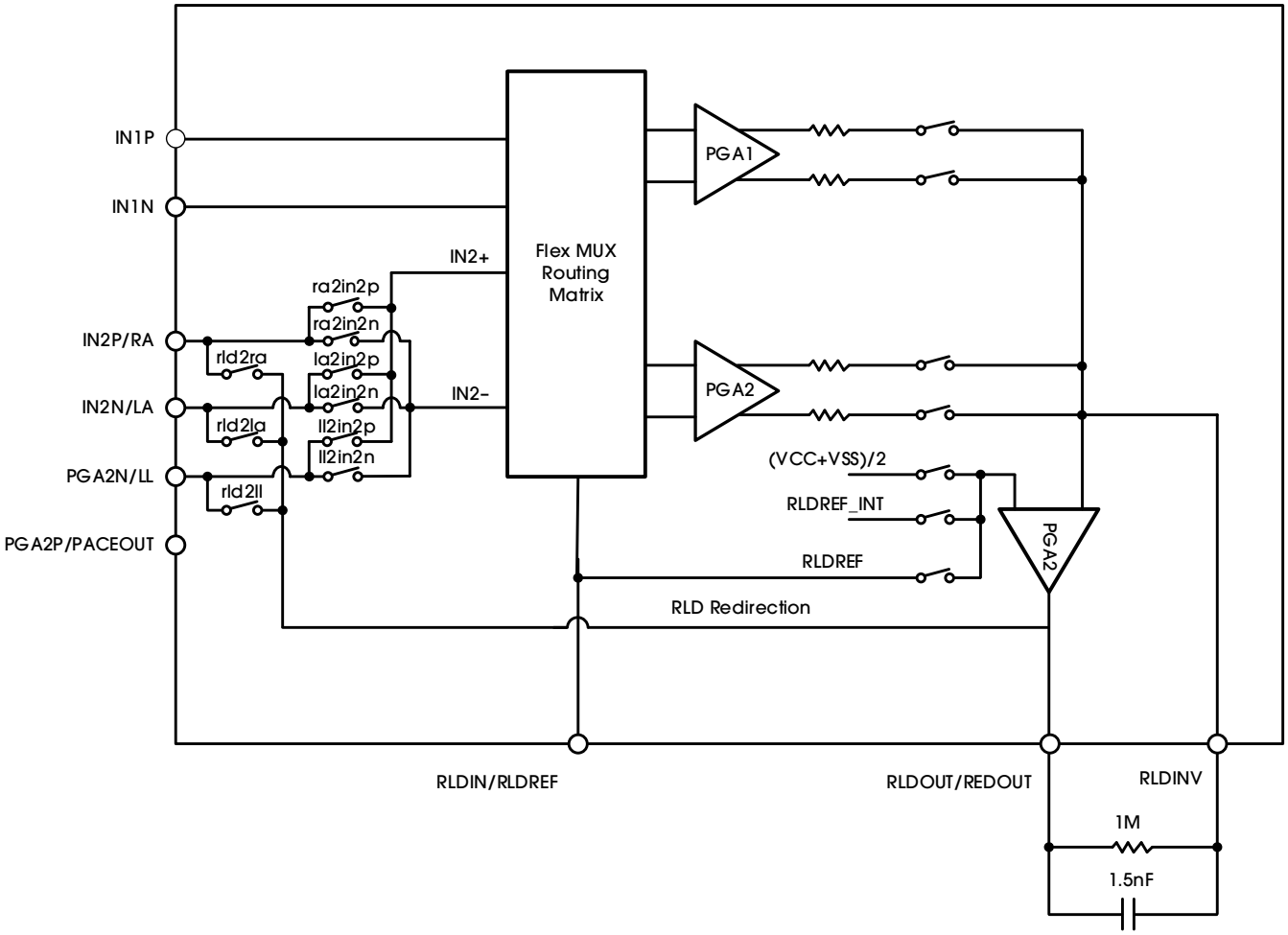

Figure 39. Re-routing Diagram

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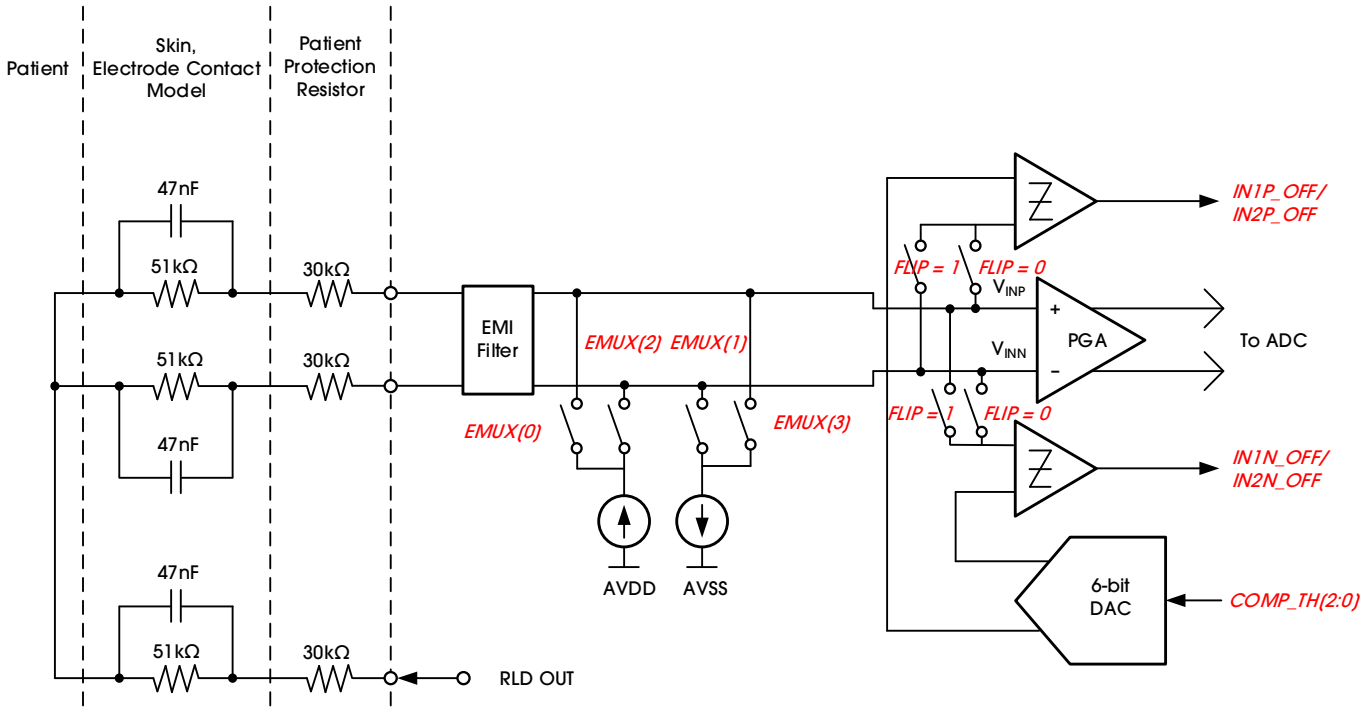
10.3.22.3 LEAD-OFF DETECTION

Patient electrode impedances are known to decay over time. It is necessary to continuously monitor these electrode connections to verify a suitable connection is present. The ADX920/1/2/3 lead-off detection functional blocks provide significant flexibility to the user to choose from various lead-off detection strategies. Though called lead-off detection, this is in fact an electrode-off detection.

The basic principle is to inject an excitation signal and measure the response to find out if the electrode is off. As shown in the lead-off detection functional block diagram in Figure 40, this circuit provides two different methods of determining the state of the patient electrode. The methods differ in the frequency content of the excitation signal. Lead-off can be selectively done on a per channel basis using the LOFF_SENS register. Also, the internal excitation circuitry can be disabled and just the sensing circuitry can be enabled.



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification in the latest revision of IEC 60601).

Figure 40. Lead-Off Detection

The LOD block can work in one of the three following modes: 1) DC lead-off detect, 2) software AC lead-off detect, or 3) digital AC lead-off detect. All three LOD modes use a common DAC that provides a programmable reference current.

Both hardware DC lead-off and digital AC lead-off share the same debounce filter to remove the 50Hz/60Hz power frequency interference by enabling debounce(1:0) of LON_CFG register. The debounce time is the setting time for the first valid data.

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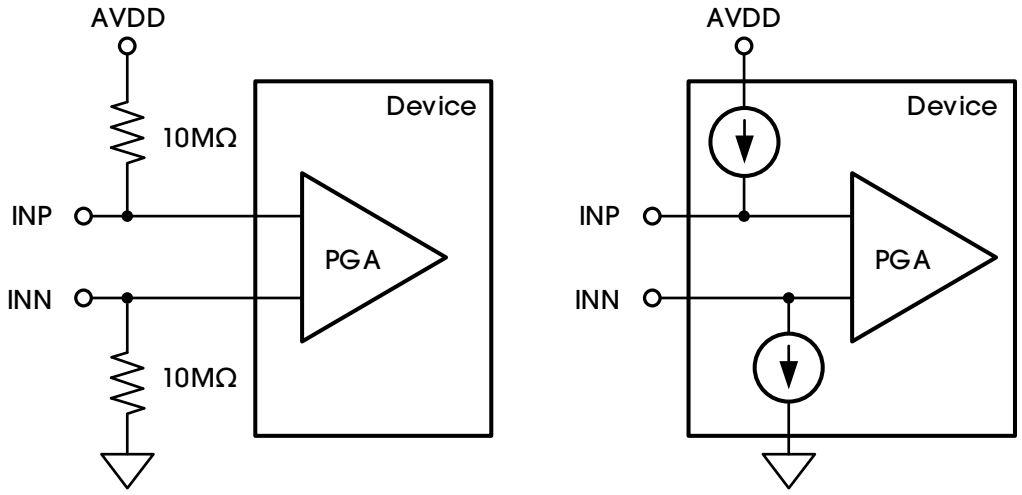
10.3.22.3.1 DC LEAD-OFF

In this method, the lead-off excitation is with a DC signal. The DC excitation signal can be chosen from either an external pull-up or pull-down resistor or a current source or sink, as shown in Figure 41. One side of the channel is pulled to supply and the other side is pulled to ground. The internal current source and current sink can be swapped by setting the FLIP1 and FLIP2 bits in the LOFF_SENS register. In case of current source or sink, the magnitude of the current can be set by using the ILEAD_OFF(1:0) bits in the LOFF register. The current source or sink gives larger input impedance compared to the 10MΩ pull-up or pull-down resistor.



a) External Pull-Up/Pull-Down Resistors b) Input Current Source

Figure 41. DC Lead-Off Excitation Options

Sensing of the response can be done either by looking at the digital output code from the device or by monitoring the input voltages with an on-chip comparator. If either of the electrodes is off, the pull-up resistors and the pull-down resistors saturate the channel. By looking at the output code, it can be determined that either the P-side or the N-side is off. To pinpoint which one is off, the comparators must be used. The input voltage is also monitored using a comparator and a 6-bit digital-to-analog converter (DAC) whose levels are set by the COMP_TH(2:0) bits in the LOFF register. The output of the comparators are stored in the LOFF_STAT register. These two registers are available as a part of the output data stream. (See the DATA OUTPUT (DOUT) section.) If DC lead-off is not used, the lead-off comparators can be powered down by setting the PDB_LOFF_COMP bit in the CONFIG2 register.

LOFF_ISTEP can be used to adjust the current value and comparator voltage for lead-off detection. If CUR_LEVEL of LOFF_ISTEP is 0, the amplitude of the excitation current used for lead-off detection can be programmed in the ISTEP field, where codes 0 to 63 result in currents ranging from 0nA to 138.6nA in steps of 2nA. An example procedure to turn on DC lead-off is given in the LEAD-OFF section.

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10.3.22.3.2 AC LEAD-OFF (ADX922/3 ONLY)

10.3.22.3.2.1 INTEGRATED DIGITAL AC LEAD-OFF DETECTION

For integrated digital AC lead-off function, the Wave Generate block generates the Fout wave to inject excitation, and the feedback signal will be processed by LPF. The Mixer is used to recover the inject excitation. The LPF is used to remove the noise, and then get the DC signal absolute value to comparator. When the DC value exceeds the comparator value, it will go through a 117ms debounce filter. The debounce filter outputs the final AC lead-off status. The wave generator generates a Fout excitation. For typical usage, the 4K or 500Hz Fout excitation is a recommended option.

$$Fout = 64kHz \times (ACDIV\_FRQ+ 1) / (K \times 64)$$

Where:

- K = 1 if ACDIV_FACTOR = 0.
- K = 8 if ACDIV_FACTOR = 1.

Figure 42 shows the integrated digital AC lead-off detection block diagram.

The SPI interface can be used to output LPF data by enabling the AC_DATA_OUT_EN field of ERM_CFG register. RDATA, RDATAC, and RFIFO are able to read the LPF data in a fixed 72-bit format.

```
{24-bit status data + 24-bit channel 1 sine/cosine LPF data + 24-bit channel 2
                        sine/cosine LPF data}
```

For more information about the format, see the DATA RETRIEVAL section. Sine and Cosine can be set by the AC_OUT_DATA_SEL bit in the ERM_CFG register.

The AC_OUT_DATA_SEL field of ERM_CFG is used to select LPF sine data or cosine data. Once AC_DATA_OUT_EN is enabled, the normal ADC output will be blocked, and the output LPF data can be used to set the threshold value. The data rate of the LPF output data is 4K or 500Hz when AC_DATA_FEQ is zero and the LPF output data is 16K or 2K when AC_DATA_FEQ is one, both of which depending on the ACDIV_FACTOR configuration of comparator. DAC amplitude can be controlled by AC_EXCT_THD(1:0). If gain > 1 is used in AC lead-off, AC_AMP_SCALE(2:0) can adjust the amplitude in the ABS module, and comparator threshold can be set by the AC LEAD-OFF COMPARATOR THRESHOLD register. See AC_CMP_THD(2:0) for more information.

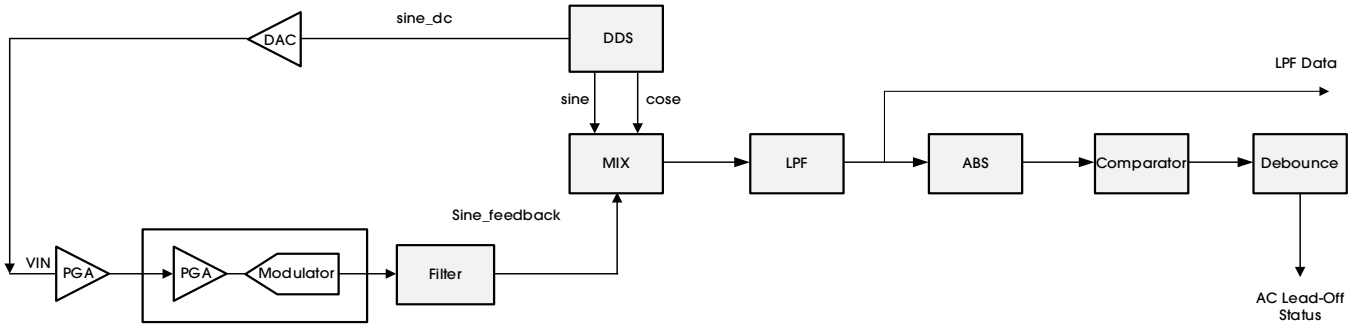

Figure 42. Integrated Digital AC Lead-Off Detection

10.3.22.3.2.2 AC DETECTION DURING NORMAL OPERATION

In this method, an out-of-band AC signal is used for excitation. The AC signal is generated by wave generator. The excitation frequency is a function of Fout. This out-of-band excitation signal is passed through the channel and measured at the output.

Sensing of the AC signal is done by passing the signal through the channel to digitize it and measure at the output. The AC excitation signals are introduced at a frequency that is above the band of interest, generating an out-of-band differential signal that can be filtered out separately and processed. By measuring the magnitude of the excitation signal at the output spectrum, the lead-off status can be calculated. Therefore, the AC lead-off detection can be accomplished simultaneously with the ECG signal acquisition.

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10.3.22.3.3 RLD LEAD-OFF

The ADX920/1/2/3 devices provide two modes for determining whether the RLD is correctly connected:

- RLD lead-off detection during normal operation
- RLD lead-off detection during power-up

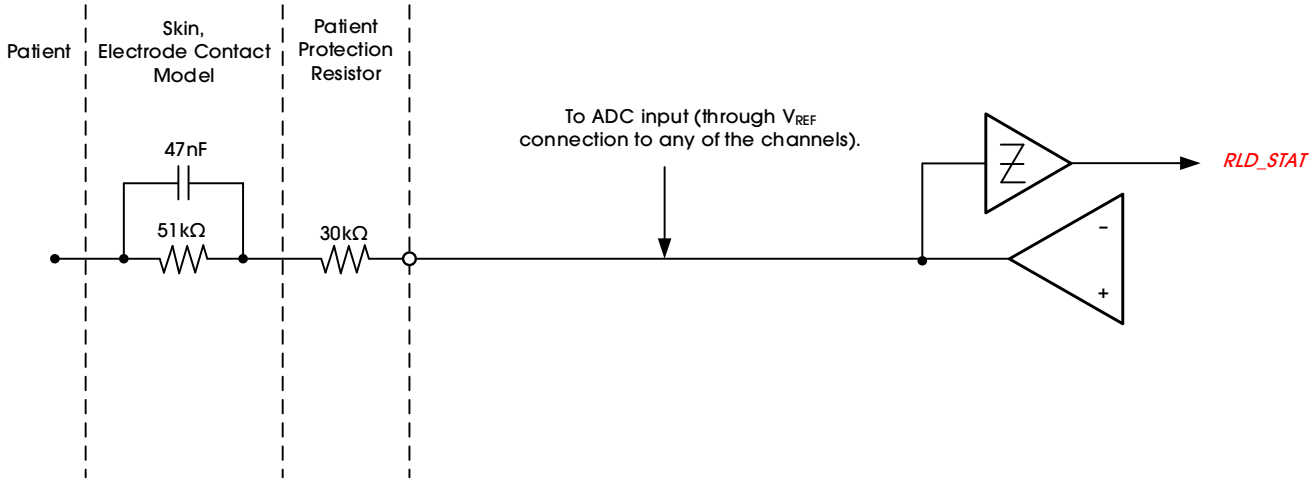
The following sections provide details of the two modes of operation.

10.3.22.3.4 RLD LEAD-OFF DETECTION DURING NORMAL OPERATION

During normal operation, the ADX920/1/2/3 RLD lead-off at power-up function cannot be used because it is necessary to power off the RLD amplifier.

10.3.22.3.5 RLD LEAD-OFF DETECTION AT POWER-UP

This feature is included in the ADX920/1/2/3 for use in determining whether the right leg electrode is suitably connected. At power-up, the ADX920/1/2/3 devices provide a procedure to determine the RLD electrode connection status using a current sink, as shown in Figure 43. The reference level of the comparator is set to determine the acceptable RLD impedance threshold.



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification in the latest revision of IEC 60601).

Figure 43. RLD Lead-Off Detection at Power-Up

When the RLD amplifier is powered on, the current source has no function. Only the comparator can be used to sense the voltage at the output of the RLD amplifier. The comparator thresholds are set by the same LOFF(7:5) bits used to set the thresholds for other negative inputs. It is optional to use LOFF_RLD to set the threshold of positive and negative rails via the RLD_DEC_EN and the RCOMP_TH(2:0) bits to control the voltage value.

RLD_LOFF_P and RLD_LOFF_N in the MOD_STAT2 register show the status of RLD lead-off.

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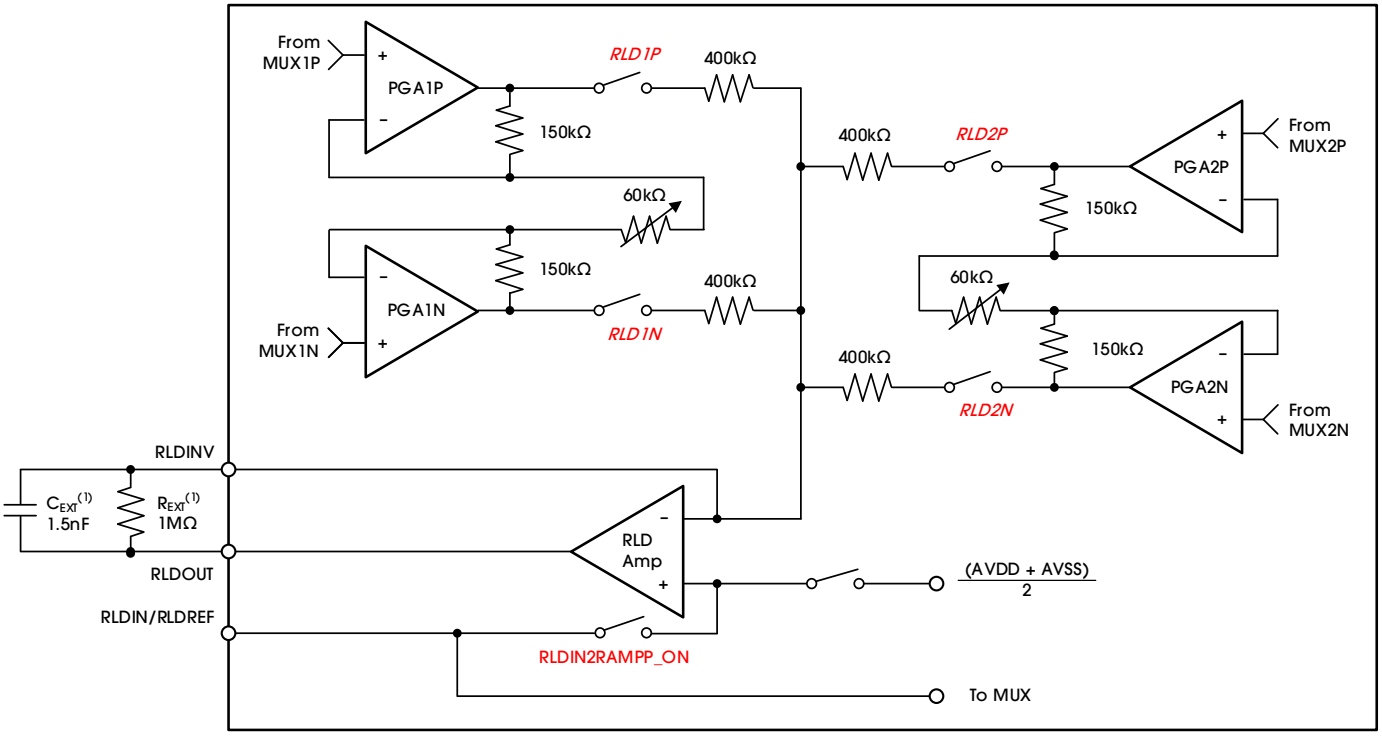
10.3.22.3.6 RIGHT LEG DRIVE (RLD DC BIAS CIRCUIT)

The right leg drive (RLD) circuitry is used as a means to counter the common-mode interference in an ECG system as a result of power lines and other sources, including fluorescent lights. The RLD circuit senses the common-mode of a selected set of electrodes and creates a negative feedback loop by driving the body with an inverted common-mode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual user system based on the various poles in the loop. The ADX920/1/2/3 devices integrate the MUXes to select the channel and an operational amplifier. All the amplifier terminals are available at the pins, allowing the user to choose the components for the feedback loop. The circuit shown in Figure 44 shows the overall functional connectivity for the RLD bias circuit.

The reference voltage for the right leg drive can be chosen to be internally generated (AVDD + AVSS) / 2 or it can be provided externally with a resistive divider. The selection of an internal versus external reference voltage for the RLD loop is defined by writing the appropriate value to the RLDREF_INT bit in the RESP2 register.



(1) Typical values.

Figure 44. RLD Channel Selection

If the RLD function is not used, the amplifier can be powered down using the PDB_RLD bit. This bit is also used in daisy-chain mode to power down all but one of the RLD amplifiers.

The functionality of the RLDIN pin is explained in the INPUT MULTIPLEXER section.

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10.3.22.3.6.1 RLD CONFIGURATION WITH MULTIPLE DEVICES

Figure 45 shows multiple devices connected to an RLD.

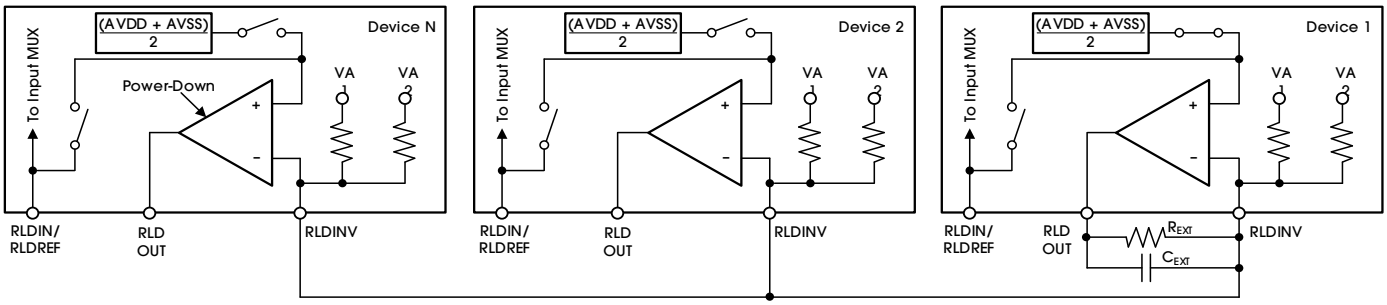

Figure 45. RLD Connection for Multiple Devices

10.3.22.4 PACE DETECT

Integrated analog pace and external pace hardware can be used to do pace detection.

10.3.22.4.1 INTEGRATED ANALOG PACE

The ADX923 features an additional analog pace channel to process pulses from a pacemaker. The analog pace channel is suitable for low-power applications where the device can be configured for low data rates in ECG mode only, while an analog channel detects PACE pulses. This channel consists of a traditional three opamp instrumentation amplifier and is designed to amplify an ECG signal in a typical bandwidth, as specified in the ELECTRICAL CHARACTERISTICS table, allowing for external circuitry to detect the PACE pulses. The analog pace implementation inside the ADX921/2/3 is depicted in Figure 46. The analog pace channel is not limited to PACE detection, it is a full-analog channel that could be used to pre-amplify signals, for instance, from a respiration sensor.

The output voltage of the analog pace channel can be calculated with Equation 10:

$$Vpaceout = PACE\_GAIN \times (Vinp - Vinm) + RLDREF \quad (10)$$

Where:

- Vinp and Vinm are the positive and negative inputs of the analog pace channel. The Vinp and Vinm sources are decided by the PACE_CFG1 register . Both of them have a common switch to control the connection using the PACE_CFG1 register.

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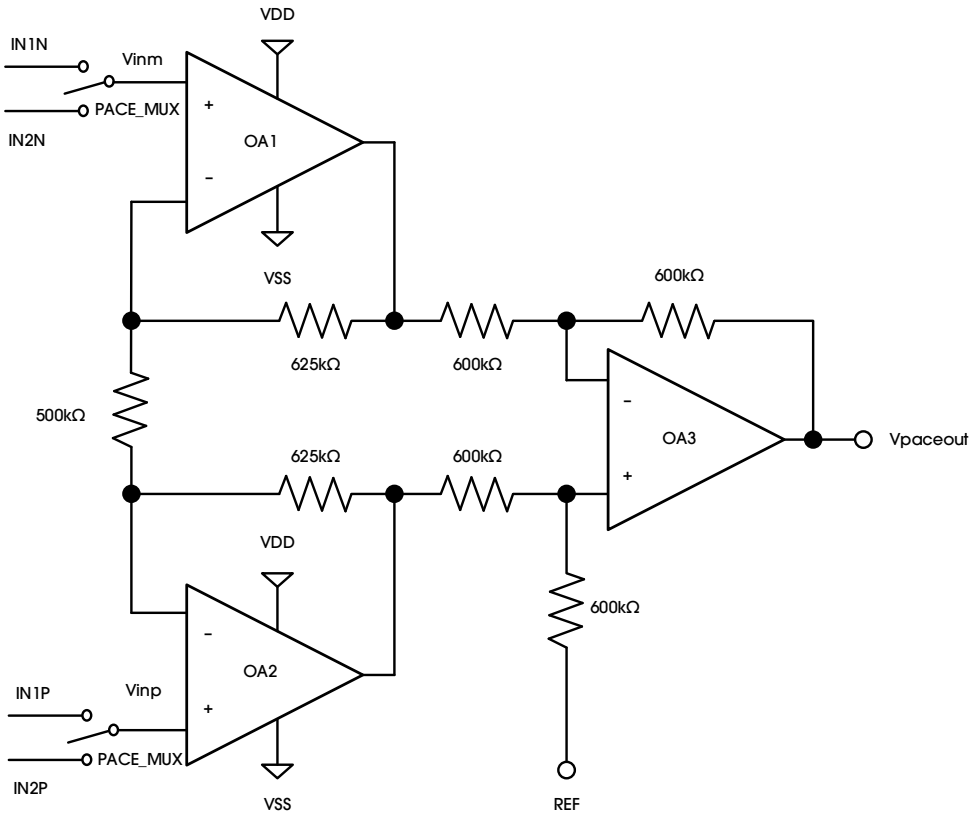

Figure 46. Analog Pace Channel Instrumentation Amplifier

The output of the analog pace channel can be multiplexed to PGA2P as the PACEOUT pin using the PACEOUT_ON field of the PACE_CFG1 register. PACEOUT refers to REF which is internally connected to a buffer output. The buffer input is connected to RLDREF. RLDREF can be driven from extra amplifier, or RLDREF can be set to (AVDD+AVSS) / 2 by configuring RLDREF_INT and RLDIN2RAMPP_ON. The all-pace channel is controlled by the PACE_EN field of the PACE_CFG register. If the pace function is not used in customer application, the pace circuit can be disabled to save power by configuring the PACE_EN field of the PACE_CFG1 register to 0.

The analog pace channel is designed to drive a high-pass filter and can directly drive a capacitive load of 100pF. For analog pace detection, it is recommended to have a band-pass filter at the output of the analog pace channel, amplify the resulting signal with a relatively high bandwidth amplifier, and compare the amplified pulses with a relatively high-speed window comparator. The bandwidth of the band-pass filter, gain of the amplification, and the thresholds of the window comparator should be tuned so the comparators trigger on pacemaker pulses, but not to other signals present in the ECG environment.

10.3.22.4.2 External Pace Detection

The ADX920/1/2/3 devices provide flexibility for PACE detection by using an external hardware. The external hardware approach is made possible by bringing out the output of the PGA at pins: PGA1P, PGA1N.

External hardware circuitry can be used to detect the presence of the pulse. The output of the PACE detection logic can then be fed into the device through one of the GPIO pins. The GPIO data are transmitted through the SPI port and loaded 2 t_{CLK}s before $\overline{DRDY}$ goes low.

When in pace detection mode, the chopping ripple can interfere with pace detect in hardware. It is therefore preferred to chop the PGA at a higher frequency (32kHz or 64kHz). The RC filter at the PGA output, suppresses this ripple to a reasonable level. Additionally, suppression can be obtained with an additional RC stage. The trade-off with chopping the PGA at a higher frequency is an increase in the input bias current.

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10.3.22.5 RESPIRATION

The ADX922/3 provide two options for respiration: internal respiration with external clock and internal respiration with internal clock, as shown in Table 28.

Table 28. Respiration Control

RESP_CTRL	DESCRIPTION
0	Internal respiration with internal clock
1	Internal respiration with external clock

10.3.22.5.1 INTERNAL RESPIRATION CIRCUITRY WITH INTERNAL CLOCK (ADX922/3)

This mode is set by RESP_CTRL = 0. Figure 47 shows a block diagram of the internal respiration circuitry. The internal modulation and demodulator circuitry can be selectively used. The modulation block is controlled by the RESP_MOD_EN bit and the demodulation block is controlled by the RESP_DEMOD_EN bit. The modulation signal is a square wave of the magnitude VREFP – AVSS. When the internal modulation circuitry is used, the output of the modulation circuitry is available at the RESP_MODP and RESP_MODM pins of the device. This availability allows custom filtering to be added to the square wave modulation signal. In this mode, GPIO1 and GPIO2 can be used for other purposes. The modulation frequency of the respiration circuit is set by the RESP_FREQ bits.

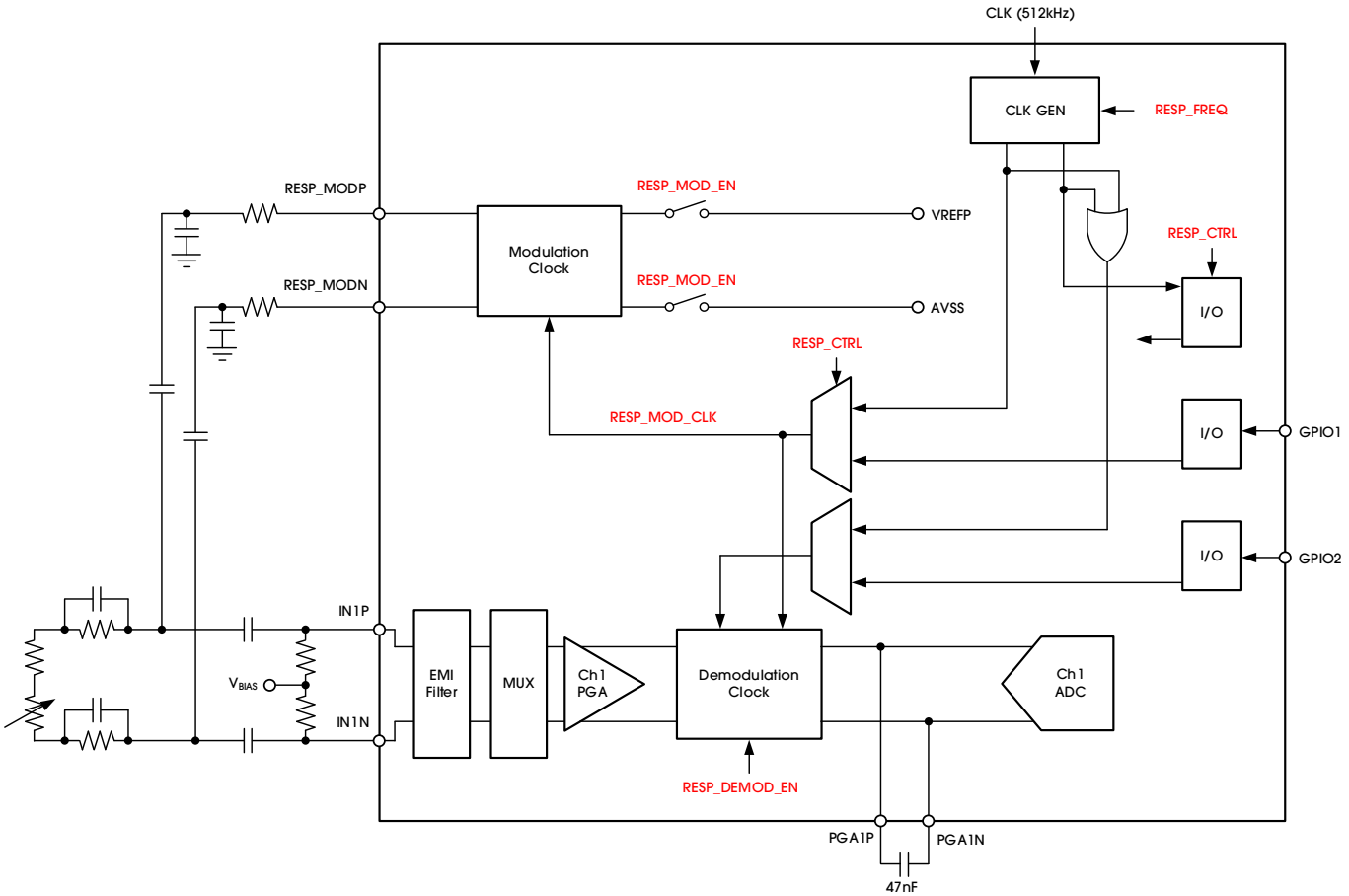

Figure 47. Internal Respiration Timing Diagram

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10.3.22.5.2 INTERNAL RESPIRATION CIRCUITRY WITH EXTERNAL CLOCK (ADX922/3)

This mode is set by RESP_CTRL = 1. In this mode, GPIO1 and GPIO2 are automatically configured as inputs. GPIO1 and GPIO2 cannot be used for other purposes. The signals must be provided as described in Figure 48. An external, synchronous master clock (CLK) is required for this mode in order to operate.

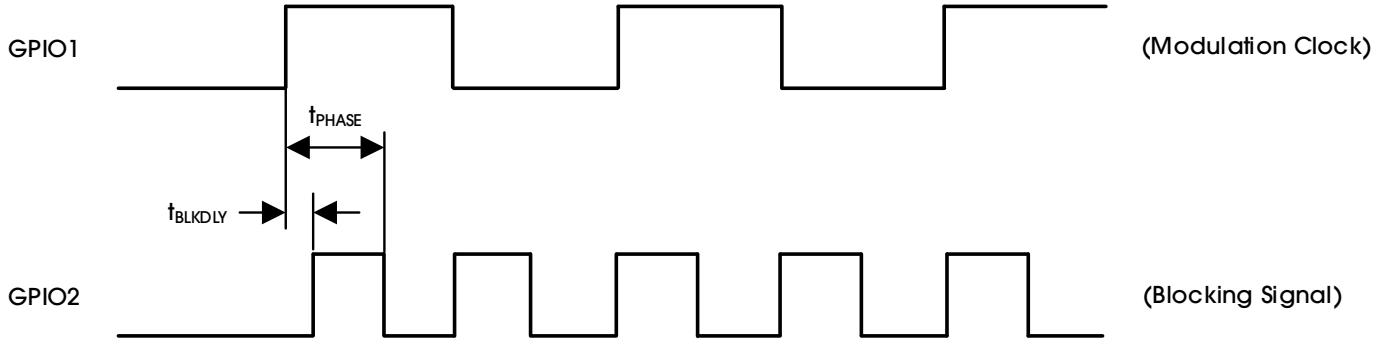

Figure 48. Internal Respiration (RESP_CTRL = 1) Timing Diagram

Table 29. Timing Characteristics for Figure 48

PARAMETER	SYMBOL	1.65V ≤ DVDD ≤ 3.6V			UNITS
		MIN	TYP	MAX	
Respiration Phase Delay	t_{PHASE}	0		168.75	Degrees
Modulation Clock Rising Edge to XOR Signal	t_{BLKDLY}		0	5	ns

Note: Specifications apply from –40°C to 85°C.

10.3.23 FIFO

The ADX920/1/2/3 devices have 12 depth sample FIFO inside. The width of every sample is 56 bits. The software uses the FIFO_CFG2 depth field to set the FIFO content numbers for triggering MCU to read FIFO data, and GPIO_SEL(1:0) are used to select the output GPIO status. Figure 49 shows the FIFO sample frame format for FRAME_CFG(2:0) of the FIFO_CFG1 register.

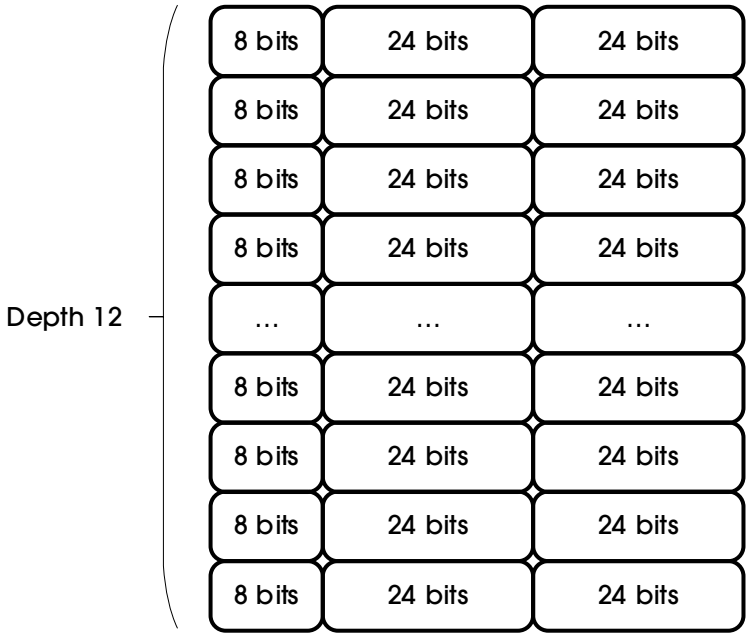

Figure 49. FIFO Frame Format

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There are three formats for FIFO usage application. In those occasions, the FIFO data will not enable the CRC.

- If the application only activates one ADC channel to sample the ECG data, it is better to configure FRAME_CFG = 000. The frame format is as below: Two continuous ADC data (first ECG content and second ECG content) make one FIFO sample item. The active channel is decided by the PD fields of CH1SET and CH2SET.

  `{3-bit LEAD_OFF (1st), 3-bit LEAD_OFF (2nd), 1-bit PACE (1st) or 1-bit GPIO (1st), 1-bit PACE (2nd) or 1-bit GPIO (2nd), 24-bit ECG data (1st), 24-bit ECG data (2nd)}`

  Note that the 3-bit LEAD_OFF is the active channel to sample ECG data electrode lead-off status based on the register configuration.

- If the application activates two ADC channels, one for sampling the ECG data, and the other for respiration or ECG, it is better to configure FRAME_CFG = 001. The active channel is decided by the PD fields of CH1SET and CH2SET. The frame format is as below:

  `{5-bit LEAD_OFF, 1b0, 2-bit GPIO or 2-bit PACE data, 24-bit CH1 ECG or respiration data,24-bit CH2 ECG data}`

  Note that the 3-bit LEAD_OFF is the active channel to sample ECG data electrode lead-off status based on the register configuration.

Note 1: The 5-bit LEAD_OFF is the active channel to sample ECG data electrode lead-off status based on the register configuration.

Note 2: Regarding the 16-it ADC product, refer to the DATA RETRIEVAL section for data format definition. The FIFO 24-bit ECG data format is: `{16-bit ECG data + 8'b0}`.

10.3.23.1 FIFO USAGE SEQUENCE

The software needs to stop the RDATAC mode before enabling FIFO. The RFIFO command will be dropped if CRC check fails and there is no data output. If FIFO is disabled, the system will always read wrong FIFO entry data, but it will not disturb the FIFO data. FIFO will output a $\overline{\text{DRDY}}$ or a GPIO interrupt to external MCU, and then wait the external MCU to send the RFIFO command to read FIFO data. The external MCU is able to read more data items than threshold value based on the DLVL(4:0) fields of FIFO_STAT register status, however, the RFIFO number cannot exceed the maximum FIFO depth.

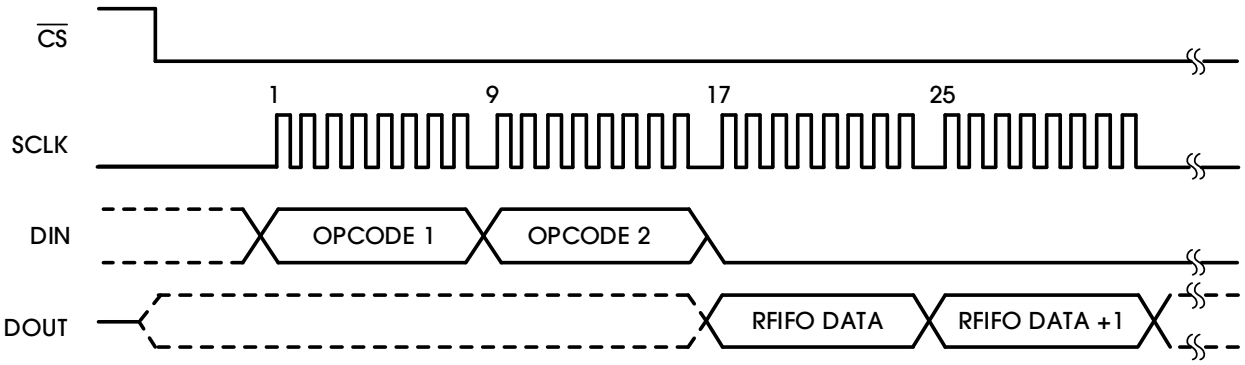

Figure 50. RFIFO Sequence

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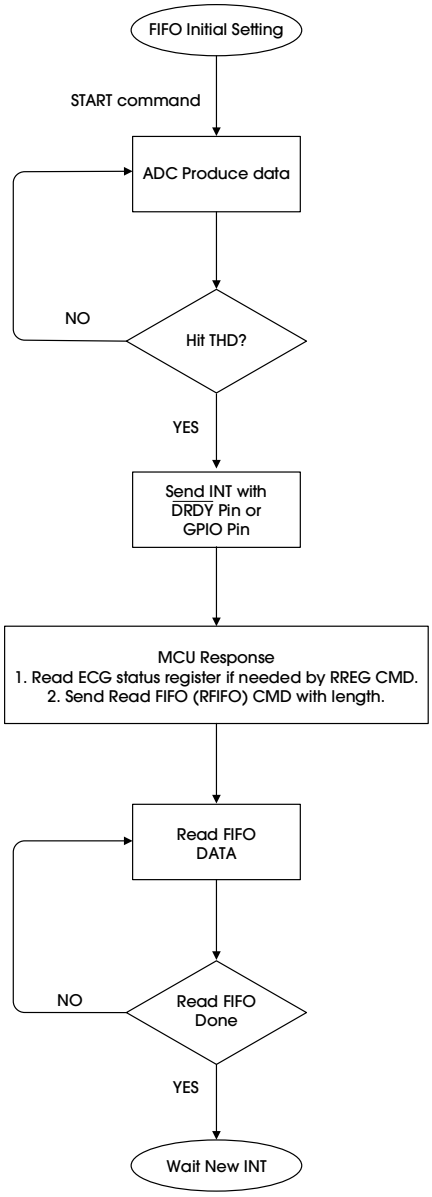

Figure 51. FIFO Read Usage Sequence

10.3.24 SHORT PROTECTION

The device is enabled to detect the output pin short ground or short power status when IO_3MA field of CONIFG5 is configured to IO High Drive mode, and it will reduce the current to 500μA automatically when short condition is met. The DOUT, $\overline{\text{DRDY}}$, GPIO1, GPIO2, and CLK pin has this capability when they are configured as output. The first short status will be captured into MOD_STAT1 register with the SHORT_GND and SHORT_PWD fields. The software needs to clear the fields before capturing the new short status. When any of the output pin is shorted to ground, the SHORT_GND will be set. When any of the output pin is shorted to power, SHORT_PWD will be set.

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10.3.25 I/O TIMING CAPABILITY

For digital I/O output function, the IO_3MA and IO_SRM fields of the CONFIG5 register is used to control the I/O power consumption, maximum frequency, and anti-EMI interference capability except the DOUT pin. The DOUT pin has a dedicated DOUT_DO3MA controller bit in the EPMIX_CFG register, All I/O share one IO_SRM configuration value. Follow the settings listed in Table 30 to configurate a reasonable value based on application requirement.

Table 30. Recommended I/O Configuration

I/O Frequency Max. Out	IO_SRM Value	IO_3MA	DOUT_DO3MA	Anti-EMI	Power
3MHz	0	0	1	Best	Lower
4MHz	0	1	0	Middle	Low
10MHz	1	0	1	Middle	High
20MHz	1	1	0	Wort	Higher

10.3.26 INTERRUPT

The device has five interrupt sources and the interrupt is output to GPIO by configuring the INTGPIO field of COFNG5 and enabling the GPIO register output function. The five interrupts are LOFF interrupt INT1, ADC data out of range interrupt INT2, FIFO interrupt INT3, CLK missing interrupt INT4, and invalid SPI CMD interrupt INT5. All Interrupts will drive GPIO to high when the interrupt is triggered.

- For INT1, the minimum interrupt pulse is different. It is about 15.6ms when the DEBOUCE field of LON_CFG is configured to 2'b10, and it is about 7.8ms when the DEBOUCE field is configured to 2'b01. Before using INT1, enable the LOFF_ISTEP.LOFF_INT_EN field.
- For INT2, the minimum interrupt pulse is one FDR cycle. Before using INT2, enable the CONFIG4.DR_INT_EN field.
- For INT3, the minimum interrupt pulse is about 4μs. Before using INT3, enable the FIFO_CFG1.FIFO_INT_EN field.
- For INT4, the CLK missing is a long pulse until the software clears it or there is a system reset. Before using INT4, enable the CONFIG4.CLK_MISS_INT_EN field.
- For INT5, the first invalid command is reported, and the interrupt is a long pulse until the software clears the invalid command status. Before using INT5, enable the CONFIG5.INV_CMD_INT_EN field.

10.3.27 SETTING THE DEVICE FOR BASIC DATA CAPTURE

This section outlines the procedure to configure the device in a basic state and capture data. The procedure is intended to put the device in a datasheet condition to check if the device is working properly in the users system. It is recommended that this procedure be followed initially to get familiar with the device settings. Once this procedure has been verified, the device can be configured as needed. For details on the timings for commands, refer to the appropriate sections in the datasheet. Furthermore, some sample programming codes are added for the ECG-specific functions. Figure 52 details a flowchart of the configuration procedure.

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10.3.27.1 LEAD-OFF

Sample code to set DC lead-off with current source or sink resistors on all channels:

```
WREG LOFF 10h // Comparator threshold at 95% and 5%, current source or sink resistor // DC lead-off
WREG CONFIG2 E0h // Turn on DC lead-off comparators
WREG LOFF_SENS 0Fh // Turn on both P- and N-side of all channels for lead-off sensing
```

Observe the status bits of the output data stream to monitor lead-off status.

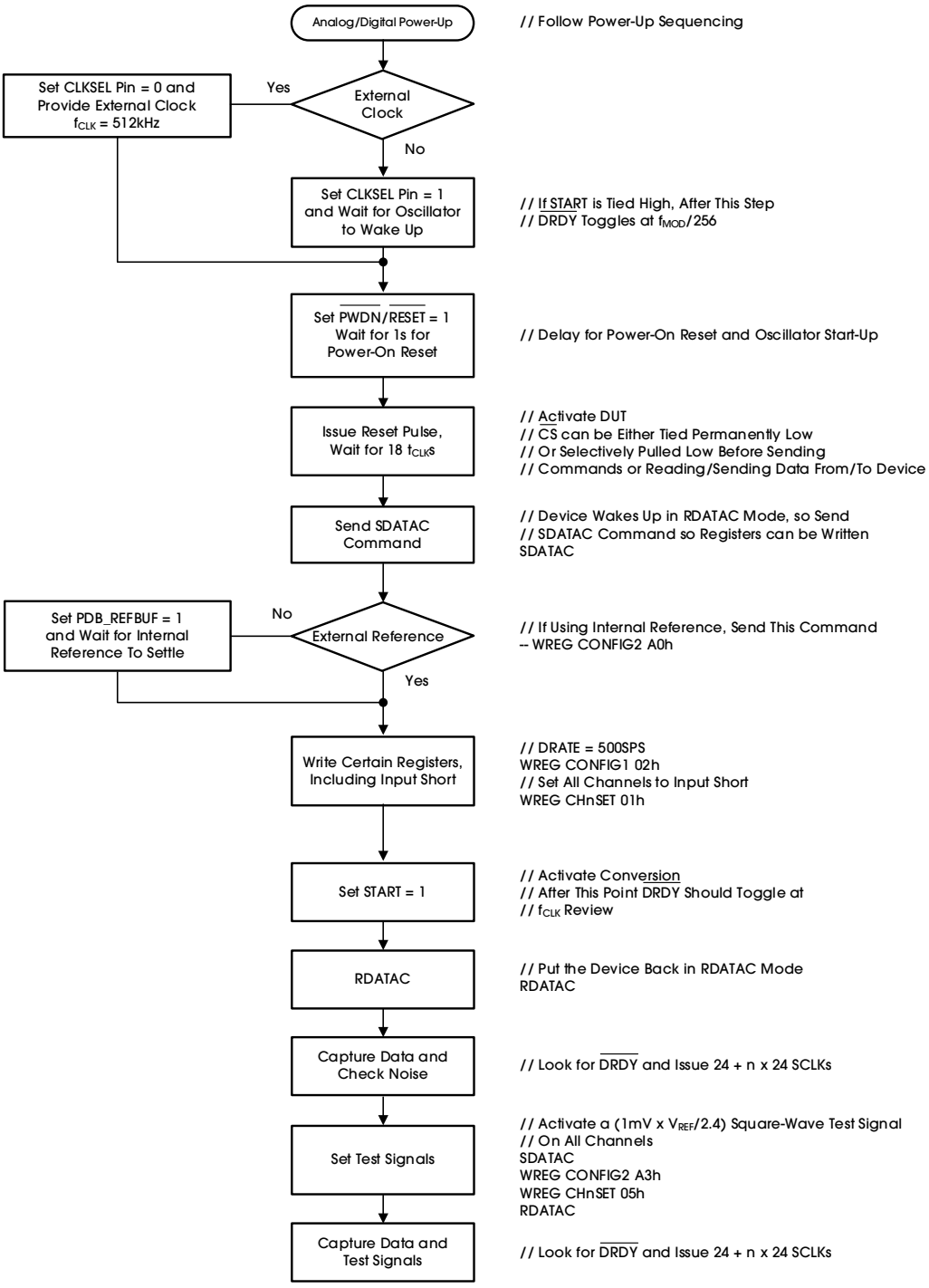

Figure 52. Initial Flow at Power-Up

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10.3.28 DEVICE FUNCTIONAL MODES

The ADX920/1/2/3 can be used in different functional modes, as a single device in a system, or as multiple devices in a system. The ADX920/1/2/3 devices are designed to provide configuration flexibility when multiple devices are used in a system, as explained in the MULTIPLE DEVICE CONFIGURATION section.

In terms of data conversion, the device can operate in continuous mode as explained in the CONTINUOUS MODE section, or in the Single-Shot mode as explained in the SINGLE-SHOT MODE section.

10.3.29 FUNCTION SAFETY MANUAL

Table 31 provides an overview of safety mechanism. The functional safety feature is useful for auto-application, please take care the safety mechanism and user registers content to use this features.

Table 31. Safety Mechanism Overview

SM	DIAGNOSTIC NAME	DESCRIPTION/SAFETY STATE	STATUS FLAG
1	Device Error	Device initial setting error	EF_UERR
2	CLK Miss or Invalid	External clock is missing or invalid.	CLK_MISS
3	PGA1 Out of Range	PGA1 P side or N side out of range	PGA1P_OOR PGA1N_OOR
4	PGA2 Out of Range	PGA2 P side or N side out of range	PGA2P_OOR PGA2N_OOR
5	RLD Lead Off	RLD lead-off for P side or N side	RLD_LOFF_P RLD_LOFF_N
6	Channel 1 Lead Off	Channel 1 P or N side lead-off	IN1N_OFF IN1P_OFF
7	Channel 2 Lead Off	Channel 2 P or N side lead-off	IN2N_OFF IN2P_OFF
8	Output Pin Short	Output pin is shorted to power or ground.	SHOT_PWR SHOT_GND
9	Invalid Command	Invalid command is detected.	INVALID_CMD_ERR
10	CRC Error	Command CRC or data CRC error	DAT_CRC_ERR CMD_CRC_ERR
11	FRAME Miss	Frame is missing or overlapped by new data.	FRAME_MISS
12	FIFO Error	FIFO read pointer is not equal to write pointer when FIFO is disabled.	FIFO_ERR

10.3.30 OFFSET CALIBRATION

The ADX920/1/2/3 devices provide offset calibration to reduce the offset error. After reset or power-on, perform an offset calibration to cancel most offset. The offset calibration can also offset temperature drift. It is recommended to perform an offset calibration when environment temperature changes significantly.

To perform an offset calibration, send an OFFSETCAL command. After the command is completed, offset adjustment value is written into the OFC_CH00 to OFC_CH22 registers. The conversion data is automatically compensated before it is read out. No more calculation is needed for offset calibration.

See Table 9 for the performance of offset after calibration. OFC_CH*xx* can be read and written. It is also supported to write a specific value in the OFC_CH*xx* register.

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10.4 PROGRAMMING

10.4.1 SPI INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls the ADX920/1/2/3 operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

10.4.1.1 CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ selects the ADX920/1/2/3 for SPI communication. $\overline{CS}$ must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

10.4.1.2 SERIAL CLOCK (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. SCLK is used to shift commands in and shift data out from the device. The serial clock features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADX920/1/2/3. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum SCLK limit is specified in the Table 10. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed needed for the SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the MULTIPLE DEVICE CONFIGURATION section.) The minimum speed can be calculated with Equation 9.

$$t_{SCLK} < \frac{t_{DR} - 4\,t_{CLK}}{72\ (2 \times 24\ \text{bits} + \text{STATUS})} \tag{9}$$

For example, if the ADX922/3 are used in a 500SPS mode (2 channels, 24-bit resolution), the minimum SCLK speed is approximately 36kHz.

Data retrieval can be done either by putting the device in RDATAC mode or by issuing a RDATA command for data on demand. The above SCLK rate limitation applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. Equation 9 assumes that no other commands are issued in between data captures. SCLK can only be twice the speed of f_{CLK} during register reads and writes. For faster SPI interface, use f_{CLK} = 2.048MHz and set the CLK_DIV register bit (in the LOFF_STAT register) to 1.

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10.4.1.3 DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADX920/1/2/3 (opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

10.4.1.4 DATA OUTPUT (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADX920/1/2/3. The START pin must transition from low to high before the data output pin can generate any data. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high.

Figure 53 shows the data output protocol for the ADX922/3.

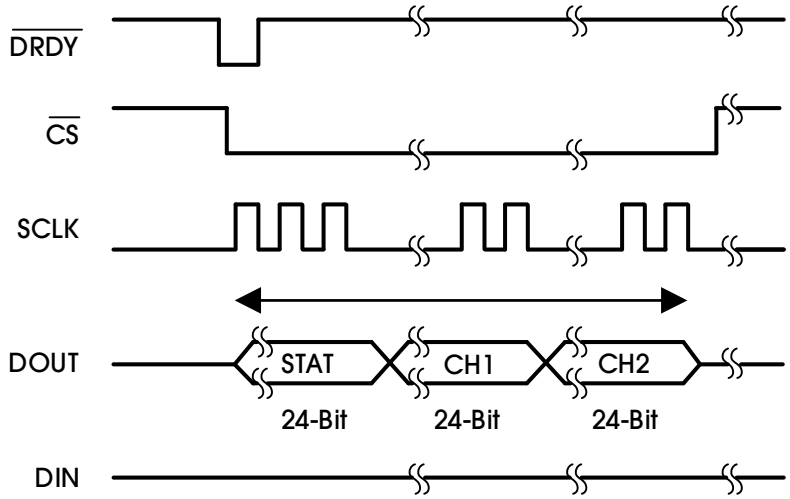

Figure 53. SPI Bus Data Output for the ADX922/3 (Two Channels)

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10.4.1.5 DATA RETRIEVAL

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the RDATAC: READ DATA CONTINUOUS section) can be used to set the device in a mode to read the data continuously without sending opcodes. The read data command (see the RDATA: READ DATA section) can be used to read just one data output from the device (see the SPI COMMAND DEFINITIONS section for more details). The conversion data are read by shifting data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{\text{DRDY}}$ returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADX922/3, the number of data outputs is (24 status bits + 24 bits × 2 channels) = 72 bits. The format of the 24 status bits is:

(1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 0s + 8 0s + 24 bits × 2 channels) when CONFG1. DOUT_CRC_EN is disabled, or

(1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 0s + 8 -bit CRC STATUS WORD + 24 bits × 2 channels) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 0s + 24 bits × 2 channels) data field.

The data format for each channel data is two's complement, MSB first. When channels are powered down using user register settings, the corresponding channel output is set to 0. However , the sequence of channel outputs remains the same. Table 32 lists the data formats.

Table 32. Data Format

PRODUCT	DATA FORMAT
24-bit ADC, 1-channel	The data format is 48 bits with the same 24 bits status and CRC rule for 2-channel product. (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 8 '0's + 24 bits) when CONFG1.DOUT_CRC_EN is disabled, or (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD + 24 bits) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 24 bits) data field,
16-bit ADC, 2-channel	The data format is 48 bits without CRC and data format is 56 bits with CRC. (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits × 2 channels) when CONFG1.DOUT_CRC_EN is disabled, or (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD +16 bits × 2 channels) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits × 2 channels) data field,
16-bit ADC, 1-channel	The data format is 32 bits without CRC and data format is 40 bits with CRC. (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits) when CONFG1.DOUT_CRC_EN is disabled, or (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD +16 bits) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + LOFF_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits) data field,
Any product with FIFO	The data format is 56 bits without CRC, and data format is 72 bits with CRC. (FIFO_ITEMB0 + FIFO_ITEMB1 + FIFO_ITEMB2 + FIFO_ITEMB3 + FIFO_ITEMB4 + FIFO_ITEMB5 + FIFO_ITEMB6) when CONFG1.DOUT_CRC_EN is disabled, or (FIFO_ITEMB0 + 8'b0 + 8-bit CRC STATUS WORD + FIFO_ITEMB1 + FIFO_ITEMB2 + FIFO_ITEMB3 + FIFO_ITEMB4 + FIFO_ITEMB5 + FIFO_ITEMB6) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (FIFO_ITEMB0 + 8'b0 + FIFO_ITEMB1 + FIFO_ITEMB2 + FIFO_ITEMB3 + FIFO_ITEMB4 + FIFO_ITEMB5 + FIFO_ITEMB6) data field,

The ADX920/1/2/3 devices also provide a multiple readback feature. Data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte. In RDATAC mode, hardware is able to check FRAME overwrite for SPI slow read reason or SPI interface hang by setting CONFIG5.FRAM_CHK_EN to 1. When the FRAME overwrite detection feature is enabled, the data cannot be read out multiple times by simply giving more SCLKs. In RFIFO mode, when FIFO_CFG1(0) is enabled, the RDATA and RDATAC commands are not allowed to be sent.

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10.4.1.6 DATA READY ($\overline{DRDY}$)

$\overline{DRDY}$ is an output. When it transitions low, new conversion data are ready. The $\overline{CS}$ signal has no effect on the data ready signal. The behavior of $\overline{DRDY}$ is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the RDATAC: READ DATA CONTINUOUS and RDATA: READ DATAs sections for further details).

When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode.

Figure 54 shows the relationship between $\overline{DRDY}$, DOUT, and SCLK during data retrieval (in case of an ADX920/1/2/3 with a selected data rate that gives 24-bit resolution). DOUT is latched out at the SCLK rising edge. $\overline{DRDY}$ is a fixed 4-6 µs low level when ADC data is ready for being read.

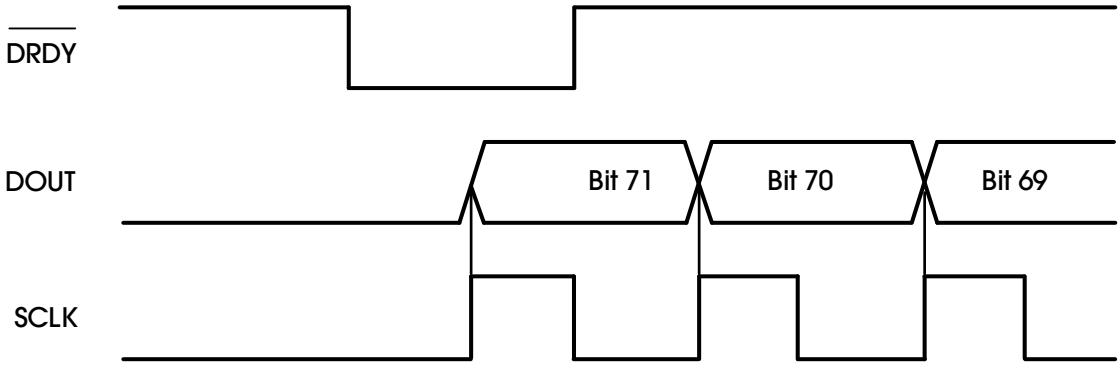

Figure 54. $\overline{DRDY}$ with Data Retrieval ($\overline{CS}$ = 0)

10.4.1.7 GPIO

The ADX920/1/2/3 devices have a total of two general-purpose digital input/output (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or as outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float) and valid GPIO data can be read after 4 t_{CLK} with CLKDIV = 0 or 16 t_{CLK} with CLKDIV = 1 once input pins are driven. The GPIO pins are set as inputs after power-on or after a reset. Figure 55 shows the GPIO port structure. The pins should be shorted to DGND with a series resistor if not used.

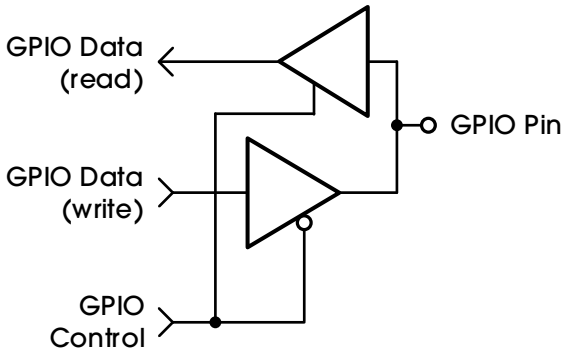

Figure 55. GPIO Port Pin

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10.4.1.8 POWER-DOWN AND RESET (PWDN/RESET)

The PWDN/RESET pins are shared. If PWDN/RESET is held low for longer than 2^9 f_{MOD} clock cycles, the device is powered down. The implementation is such that the device is always reset when PWDN/RESET makes a transition from high to low. If the device is powered down, it is reset first and then if 2^{10} clock elapses it is powered down. Hence, all registers must be rewritten after power-up.

There are two methods to reset the ADX920/1/2/3: pull the PWDN/RESET pin low, or send the RESET opcode command. When using the PWDN/RESET pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the PWDN/RESET pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset, it takes 18 t_{CLK} cycles to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever the CONFIG1, RESP1, RESP2, and ERM_CFG(2:0) are set to a new value with a WREG command.

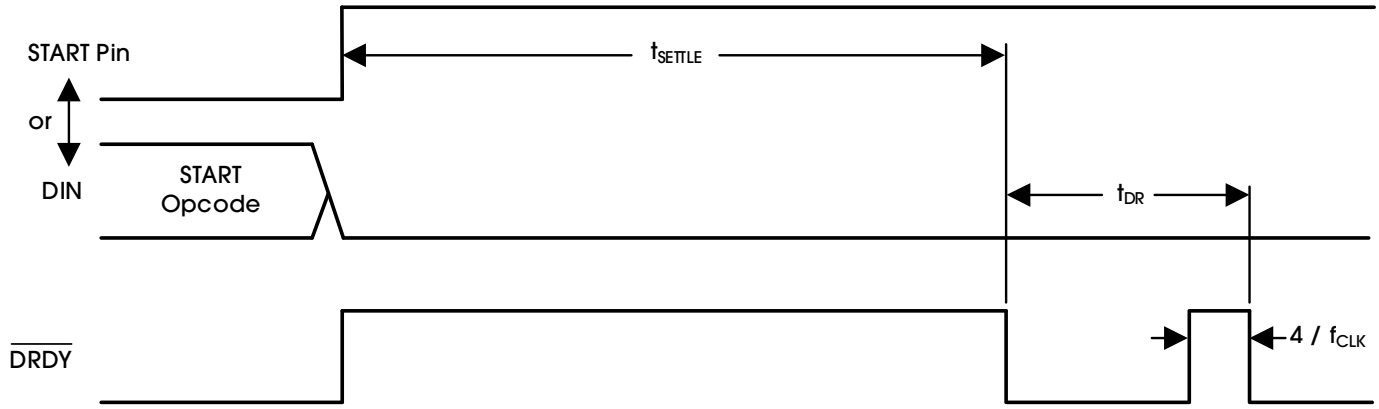
10.4.1.9 START

The START pin must be set high or the START command sent to begin conversions. When START is low or if the START command has not been sent, the device does not issue a DRDY signal (conversions are halted).

When using the START opcode to control conversion, hold the START pin low. The ADX920/1/2/3 devices feature two modes to control conversion: continuous mode and single-shot mode. The mode is selected by SINGLE_SHOT (bit 7 of the CONFIG1 register). In multiple device configurations, the START pin is used to synchronize devices (see the MULTIPLE DEVICE CONFIGURATION section for more details).

10.4.1.10 SETTLING TIME

The settling time (t_{SETTLE}) is the time it takes for the converter to output fully settled data when the START signal is pulled high. Once START is pulled high, DRDY is also pulled high. The next DRDY falling edge indicates that data are ready. Figure 56 shows the timing diagram and Table 33 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR(2:0) bits in the CONFIG1 register). Refer to Table 33 for the settling time as a function of t_{MOD}. Note that when START is held high and there is a step change in the input signal, it takes 3 t_{DR} for the filter to settle to the new value. Settled data are available on the fourth DRDY pulse. Settling time number uncertainty is one t_{MOD} cycle. Therefore, it is recommended to add one t_{MOD} cycle delay before issuing SCLK to retrieve data.



(1) Settling time uncertainty is one t_{MOD} cycle.

Figure 56. Settling Time

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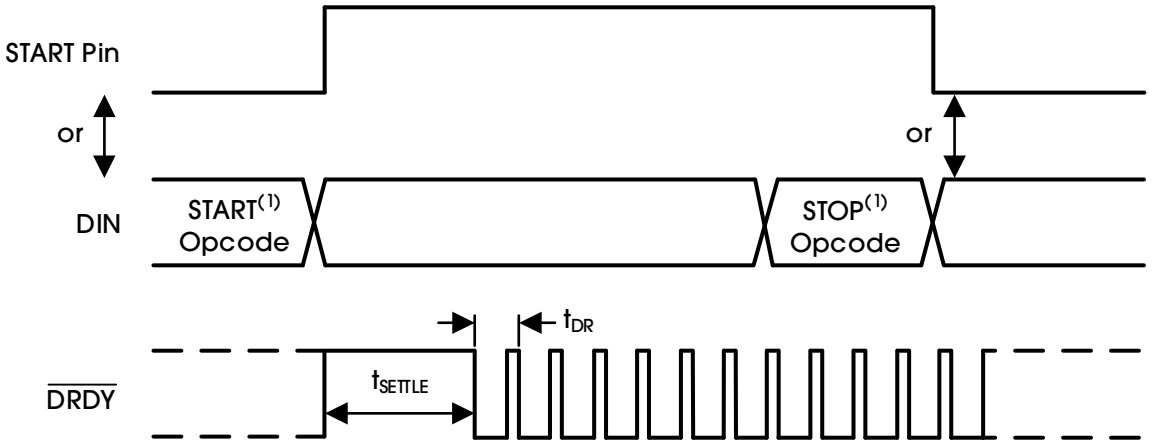
Table 33. Settling Time for Different Data Rates

DR(2:0)	SETTLING TIME(1)	UNITS(2)
000	4100	t_{MOD}
001	2052	t_{MOD}
010	1028	t_{MOD}
011	516	t_{MOD}
100	260	t_{MOD}
101	132	t_{MOD}
110	68	t_{MOD}
111	—	—

Note 1: Settling time uncertainty is one t_{MOD} cycle.
Note 2: t_{MOD} = 4 t_{CLK} for CLK_DIV = 0 and t_{MOD} = 16 t_{CLK} for CLK_DIV = 1.

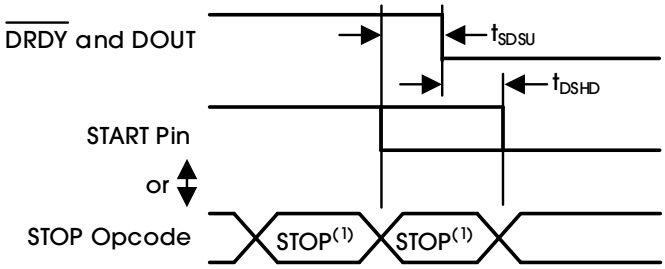
10.4.1.11 CONTINUOUS MODE

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 57, the $\overline{DRDY}$ output goes high when conversions start and trigger a 4μs negative pulse when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 57 and Table 34 show the required $\overline{DRDY}$ timing to the START pin and the START and STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high. Note that when switching from pulse mode to continuous mode, the START signal is pulsed or a STOP command must be issued, followed by a START command. This conversion mode is ideal for applications that require a fixed continuous stream of conversions results.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 57. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 58. START to $\overline{DRDY}$ Timing

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Table 34. Timing Characteristics for Figure 57

PARAMETER	SYMBOL	MIN	UNITS
START Pin Low or STOP Opcode to $\overline{DRDY}$ Setup Time to Halt Further Conversions	t_{SDSU}	8	t_{MOD}
START Pin Low or STOP Opcode to Complete Current Conversion	t_{DSHD}	8	t_{MOD}

Note: START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

10.4.1.12 SINGLE-SHOT MODE

The single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG1 register to 1. In single -shot mode, the ADX920/1/2/3 devices perform a single conversion when the START pin is taken high or when the START opcode command is sent. As seen in Figure 59, when a conversion is complete, $\overline{DRDY}$ goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, $\overline{DRDY}$ remains low. To begin a new conversion, take the START pin low and then back high, or transmit the START opcode again. When switching from continuous mode to pulse mode, make sure the START signal is pulsed or issue a STOP command followed by a START command.

This conversion mode is provided for applications that require non-standard or non-continuous data rates. Issuing a START command or toggling the START pin high resets the digital filter, effectively dropping the data rate by a factor of four. Note that this mode leaves the system more susceptible to aliasing effects, requiring more complex analog anti-aliasing filters at the inputs. Loading on the host processor increases because it must toggle the START pin or send a START command to initiate a new conversion cycle.

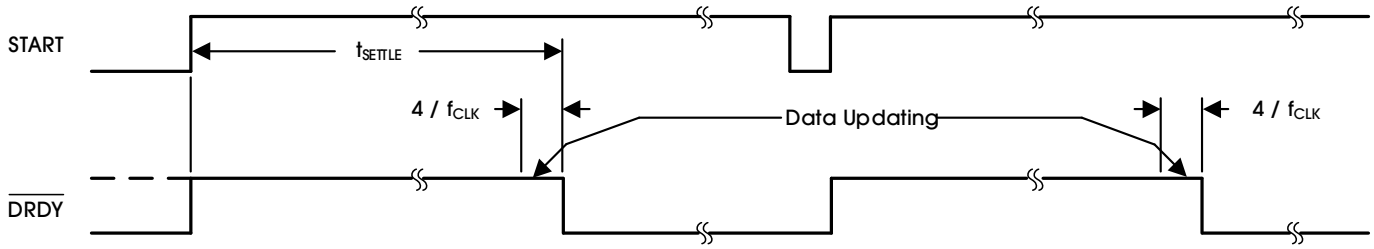

Figure 59. $\overline{DRDY}$ with No Data Retrieval in Single-Shot Mode

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10.4.2 SPI COMMAND DEFINITIONS

The ADX920/1/2/3 devices provide flexible configuration control. The opcode commands summarized in Table 35 control and configure the ADX920/1/2/3 operation. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the ADX920/1/2/3 on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 35. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
SYSTEM COMMANDS			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	0x0E (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
STANDBY	Enter standby mode	0000 0100 (04h)	0x1C (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
RESET	Reset the device	0000 0110 (06h)	0x12/0x13 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
START	Start or restart (synchronize) conversions	0000 1000 (08h)	0x38 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
STOP	Stop conversion	0000 1010 (0Ah)	0x36 (CRC byte when CONFIG3.DIN_CRC_EN) is enabled.
LOCK	Lock SPI interface	0001 0101 (15h)	0x6b (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
UNLOCK	Unlock SPI interface	0001 0110 (16h)	0x62 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	0x46 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
DATA READ COMMANDS			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	0x70 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	0x77 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
RDATA	Read data by command, supports multiple read back.	0001 0010 (12h)	0x7e (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
REGISTER READ COMMANDS			
RREG	Read n nnnn registers starting at address r rrrr	001r rrrr (2xh)(2)(4)	000n nnnn(2)
RFIFO	Read FIFO data command with read number	011 0000(60h)	000n nnnn(2)
WREG	Write n nnnn registers starting at address r rrrr	010r rrrr (4xh)(3)(4)	000n nnnn(2)

Note 1: When in RDATAC mode, the RREG command is ignored.
Note 2: n nnnn = number of registers to be read or written – 1. For example, to read or write three registers, set n nnnn = 0 (0010). r rrrr = starting register address for read and write opcodes.
Note 3: When CONFIG3.DIN_CRC_EN is enabled, the Command in the following sections includes both COMMAND byte and CRC status byte.
Note 4: Registers with address >1Fh can only be accessed through burst mode. They cannot be read or written directly.

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10.4.2.1 WAKEUP: EXIT STANDBY MODE

This opcode exits the low-power standby mode, see the STANDBY: ENTER STANDBY MODE section. Time is required when exiting standby mode (see the ELECTRICAL CHARACTERISTICS for details). There are no restrictions on the SCLK rate for this command and it can be issued any time. Any following command must be sent after 4 t_{CLK} cycles.

10.4.2.2 STANDBY: ENTER STANDBY MODE

This opcode command enters the low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the ELECTRICAL CHARACTERISTICS table. There are no restrictions on the SCLK rate for this command and it can be issued any time. Do not send any other command other than the wakeup command after the device enters the standby mode.

10.4.2.3 RESET: RESET REGISTERS TO DEFAULT VALUES

This command resets the digital filter cycle and returns all register settings to the default values. See the POWER-DOWN AND RESET (PWDN/RESET) section for more details. There are no restrictions on the SCLK rate for this command and it can be issued any time. It takes 9 f_{MOD} cycles to execute the RESET command. Avoid sending any commands during this time.

10.4.2.4 START: START CONVERSIONS

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress, this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command, then have a gap of 4 t_{CLK} cycles between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the START section for more details.) There are no restrictions on the SCLK rate for this command and it can be issued any time.

10.4.2.5 STOP: STOP CONVERSIONS

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no restrictions on the SCLK rate for this command and it can be issued any time.

10.4.2.6 OFFSETCAL: CHANNEL OFFSET CALIBRATION

This command is used to cancel the channel offset. The CALIB_ON bit in the RESP2 register must be set to 1 before issuing this command. OFFSETCAL must be executed every time there is a change in the PGA gain settings.

10.4.2.7 LOCK: LOCK SPI INTERFACE

This command is used to lock the SPI interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the RREG, RDATA, and UNLOCK commands and continues to output conversion data even when locked. The LOCK status will be cleared when there is an internal reset event or SPI reset, for example, reset by pulling the $\overline{CS}$ pin low to high. For the WREG command operation under the LOCK status, if the WREG number and data contain the RREG, RDATA, and UNLOCK decoding, it may disturb the LOCK command function, and the device status and command status registers can be read to check the exception status.

10.4.2.8 UNLOCK: UNLOCK SPI INTERFACE

This command is used to unlock the SPI interface if previously locked by the LOCK command.

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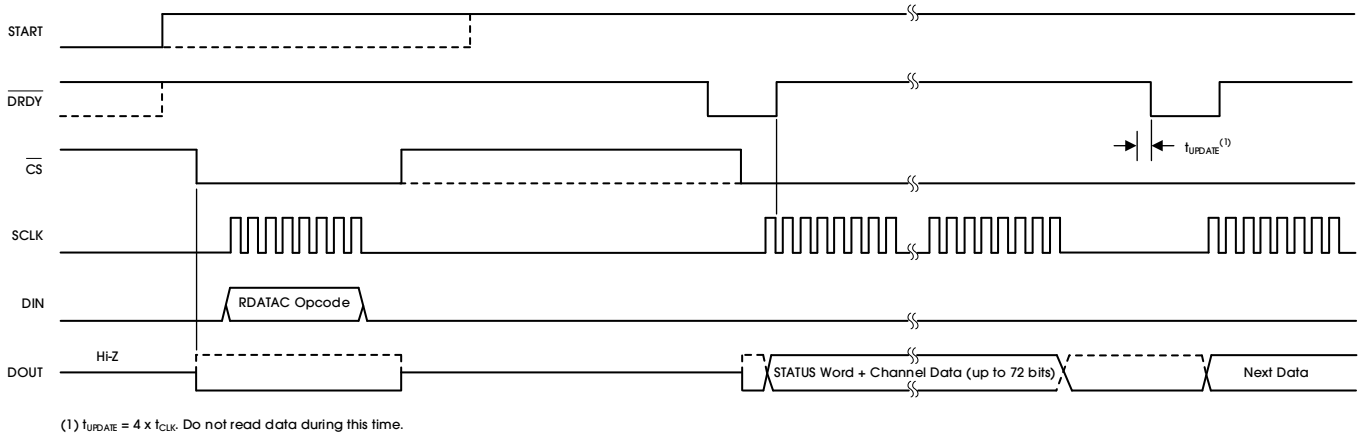
10.4.2.9 RDATAC: READ DATA CONTINUOUS

This opcode enables the output of conversion data on each $\overline{DRDY}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the device default mode, the device defaults to this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, a SDATAC command must be issued before any other commands (except LOCK and UNLOCK commands) can be sent to the device. There is no restriction on the SCLK rate for this command. However, the subsequent data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles. RDATAC timing is shown in Figure 60. As Figure 60 shows, there is a keep-out zone of 4 t_{CLK} cycles around the $\overline{DRDY}$ pulse where this command cannot be issued in. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 60 shows the recommended way to use the RDATAC command. RDATAC is ideally-suited for applications such as data loggers or recorders where registers are set once and do not need to be re-configured. $\overline{DRDY}$ is fixed 4-6 μs low level when ADC data is ready for being read.



(1) t_{UPDATE} = 4 x t_{CLK}. Do not read data during this time.

Figure 60. RDATAC Usage

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10.4.2.10 SDATAC: STOP READ DATA CONTINUOUS

This opcode cancels the Read Data Continuous mode. There is no restriction on the SCLK rate for this command, but the following command must wait for 4 t_{CLK} cycles.

10.4.2.11 RDATA: READ DATA

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There is no restriction on the SCLK rate for this command, and no wait time is needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption. Figure 61 shows the recommended way to use the RDATA command. RDATA is best suited for ECG- and EEG-type systems where register setting must be read or changed often between conversion cycles. $\overline{DRDY}$ is fixed 4-6μs low level when ADC data is ready for being read.

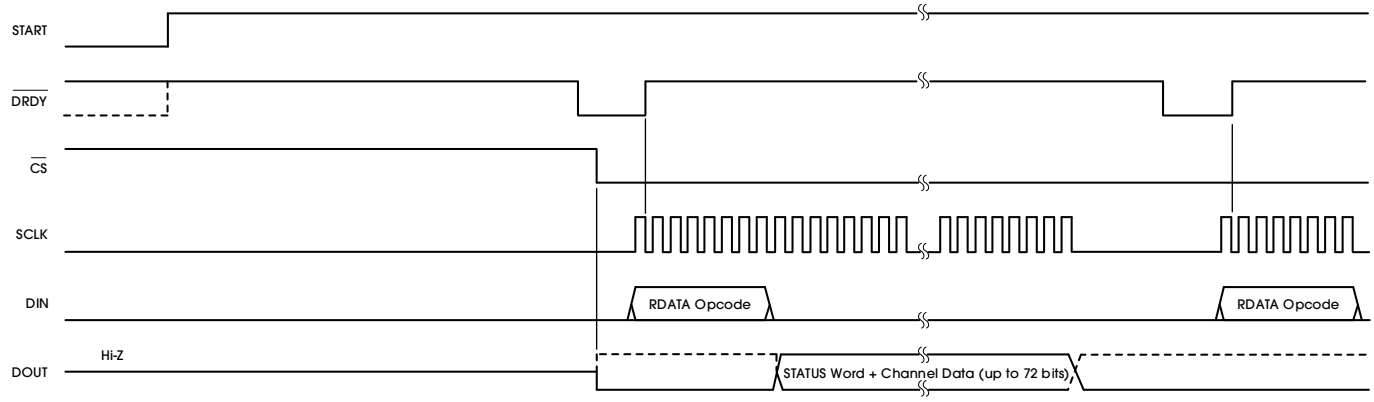

Figure 61. RDATA Usage

10.4.2.12 SENDING MULTI-BYTE COMMANDS

The ADX920/1/2/3 serial interfaces decode commands in bytes and require 4 t_{CLK} cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assume CLK is 512kHz, then $t_{SDECODE}$ (4 t_{CLK}) is 7.8125μs. When SCLK is 16MHz, one byte can be transferred in 500ns. This byte-transfer time does not meet the $t_{SDECODE}$ specification, therefore, a delay must be inserted so the end of the second byte arrives 7.3125μs later. If SCLK is 1MHz, one byte is transferred in 8μs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to move from single-byte transfer per cycle to multiple bytes.

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10.4.2.13 RREG: READ FROM REGISTER

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.

1. First opcode byte: 001r rrrr, where r rrrr is the starting register address.
2. Second opcode byte: 000n nnnn, where n nnnn is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 62. When the device is in read data continuous mode, it is necessary to issue a SDATAC command before the RREG command can be issued. The RREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the SERIAL CLOCK (SCLK) section for more details. Note that $\overline{CS}$ must be low for the entire command.

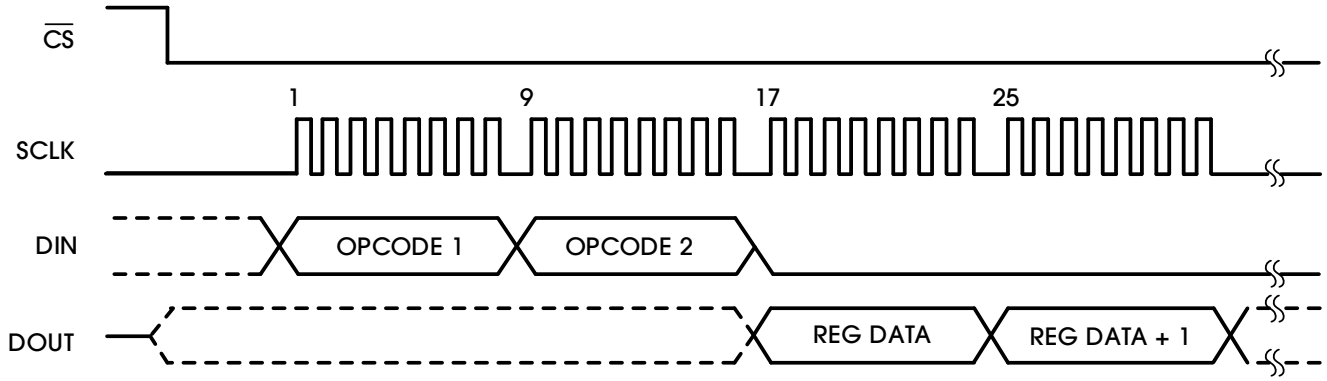

Figure 62. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

10.4.2.14 RFIFO: READ FIFO DATA

This opcode reads internal FIFO data. The FIFO Read command is a two-byte opcode followed by the output of the FIFO data. The first byte contains the command opcode. The second byte of the opcode specifies the number of FIFO items to read –1.

1. First opcode byte: 0110 0000.
2. Second opcode byte: 000n nnnn, where n nnnn is the number of FIFO items to read –1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first FIFO item data, as shown in Figure 63. When the device is in read data continuous mode, it is necessary to issue a SDATAC command before the RFIFO command can be issued. The RFIFO command can be issued when FIFO threshold is hit and the FIFO will set $\overline{DRDY}$ and interrupt to external MCU if the FIFO interrupt is enabled. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the SERIAL CLOCK (SCLK) section for more details. Note that $\overline{CS}$ must be low for the entire command.

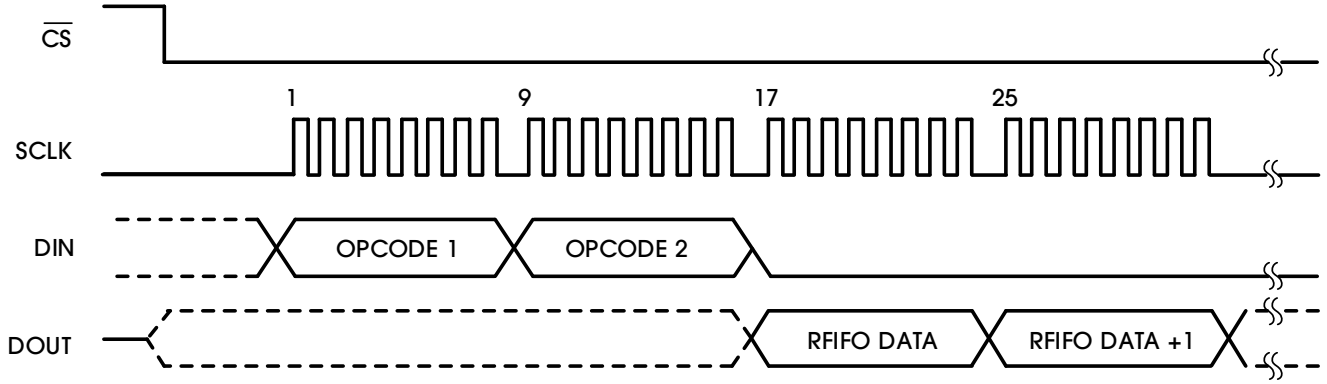

Figure 63. RFIFO Command Example: Read Two Registers Starting from FIFO

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10.4.2.15 WREG: WRITE TO REGISTER

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address.

The second byte of the opcode specifies the number of registers to write – 1.

1. First opcode byte: 010r rrrr, where r rrrr is the starting register address.
2. Second opcode byte: 000n nnnn, where n nnnn is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 64. The WREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the SERIAL CLOCK (SCLK) section for more details. Note that $\overline{CS}$ must be low for the entire command.

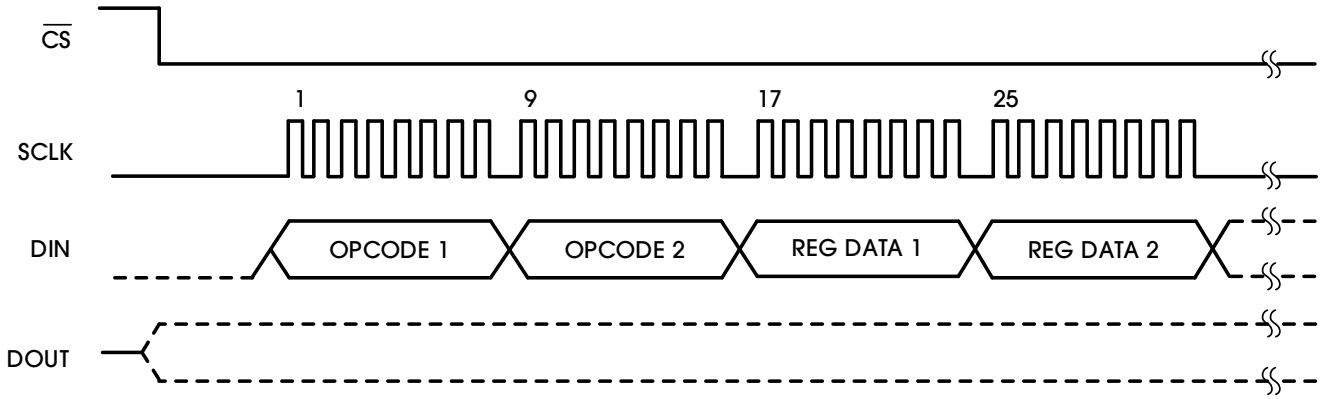

Figure 64. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

10.4.3 SPI CRC FEATURE

For all SPI commands, the 8-bit CRC status word follows the end of the whole command when CONFIG3.DIN_CRC_EN is enabled. The device will also check the CRC status word. Execution will not be performed for the WAKEUP, STANDBY, RESET, START, STOP, OFFSETCAL, LOCK, UNLOCK, RDATAC, SDATAC, RDATA, and RREG commands if the CRC status word is mismatched, and the MOD_STAT.CMD_CRC_ERR will be set. In other words, a CRC error occurs if the CRC words do not match. When the input CRC check fails, the device will not execute any commands, except for the WREG and RFIFO commands.

1. A WREG command always executes even when the CRC check fails. It will set MOD_STAT.DAT_CRC_ERR.
2. An RFIFO command executes one FIFO entry reading even when the CRC check fails. Only the first FIFO entry will be read, and the reading will repeat if RFIFO length is set in the command to inform user that CRC check of RFIFO fails. It will set MOD_STAT.DAT_CRC_ERR.

For burst register reading operation with RREG, the device will output a CRC status word at last when CONFIG3.DOUT_CRC_EN is enabled. The CRC status word will not be included in the count number in RREG.

For burst register writing operation with WREG, the host must provide a CRC status word at last when CONFIG3.DIN_CRC_EN is enabled. The CRC status word will not be included in the count number in WREG. To enable and disable CRC with CONFIG3.DIN_CRC_EN, the CRC check follows rules below:

1. If CRC is disabled, to enable the SPI CRC check, write CONFIG3.DIN_CRC_EN to one, and this whole write command does NOT have the CRC check.
2. If CRC is enabled, to disable the SPI CRC check, write CONFIG3.DIN_CRC_EN to zero, and this whole write command has the CRC check.

In CRC8 mode, it uses the CRC-8-CCITT formula as below:

$$P(x) = x^8 + x^2 + x + 1$$

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11. REGISTER MAPS

Table 36 describes the various ADX920/1/2/3 registers.

Table 36. Register Assignments

ADDRESS	REGISTER	RESET VALUE (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS (READ-ONLY REGISTERS)										
00h	ID	XX	REV_ID2	REV_ID1	REV_ID0	1	0	0	REV_ID1	REV_ID0
GLOBAL SETTINGS ACROSS CHANNELS (READ AND WRITE REGISTERS)										
01h	CONFIG1	02	SINGLE_SHOT	0	0	0	0	DR2	DR1	DR0
02h	CONFIG2	80	1	PDB_LOFF_COMP	PDB_REFBUF	VREF_4V	CLK_EN	0	INT_TEST	TEST_FREQ
03h	LOFF	10	COMP_TH2	COMP_TH1	COMP_TH0	1	ILEAD_OFF1	ILEAD_OFF0	0	FLEAD_OFF
CHANNEL-SPECIFIC SETTINGS (READ AND WRITE REGISTERS)										
04h	CH1SET	00	PD1	GAIN1_2	GAIN1_1	GAIN1_0	MUX1_3	MUX1_2	MUX1_1	MUX1_0
05h	CH2SET	00	PD2	GAIN2_2	GAIN2_1	GAIN2_0	MUX2_3	MUX2_2	MUX2_1	MUX2_0
06h	RLD_SENS	00	CHOP1	CHOP0	PDB_RLD	RLD_LOFF_SENS	RLD2N	RLD2P	RLD1N	RLD1P
07h	LOFF_SENS	00	0	CP_FREQ	FLIP2	FLIP1	EMUX_LOFF3	EMUX_LOFF2	EMUX_LOFF1	EMUX_LOFF0
08h	LOFF_STAT	00	0	CLK_DIV1	CLK_DIV0	RLD_STAT	IN2N_OFF	IN2P_OFF	IN1N_OFF	IN1P_OFF
GPIO AND OTHER REGISTERS (READ AND WRITE REGISTERS)										
09h	RESP1	00	RESP_DEMOD_EN1	RESP_MOD_EN	RESP_PH3	RESP_PH2	RESP_PH1	RESP_PH0	1	RESP_CTRL
0Ah	RESP2	02	CALIB_ON	0	0	0	0	RESP_FREQ	RLDREF_INT	1
0Bh	GPIO	0C	AC_AMP_SCALE2	AC_AMP_SCALE1	AC_AMP_SCALE0	0	GPIOC2	GPIOC1	GPIOD2	GPIOD1
ENHANCE PERFORMANCE SETTING REGISTERS (READ AND WRITE REGISTERS)										
0Ch	CONFIG3	00	AC_MODE	P5VREF_ON	0	0	DIN_CRC_EN	DOUT_CRC_EN	SPI_TIMEOUT1	SPI_TIMEOUT0
0Dh	CONFIG4	00	DR_INT_EN	ADC_DAT_THD1	ADC_DAT_THD0	0	CLK_MISS_INT_EN	0	RLDIN2RAMPP_ON	RAMPOUT2RAMPN_ON
0Eh	CONIFG5	71	OSC_2M_EN	INT2GPIO2	INT2GPIO1	INT2GPIO0	INV_CMD_INT_EN	FRAME_CHK_EN	IO_3MA	IO_SRM
0Fh	LOFF_ISTEP	00	LOFF_INT_EN	CUR_LEVEL	ISTEP5	ISTEP4	ISTEP_3	ISTEP2	ISTEP1	ISTEP0
10h	LOFF_RLD	00	EMUX_LOFF3	EMUX_LOFF2	EMUX_LOFF1	EMUX_LOFF0	RCOMP_TH2	RCOMP_TH1	RCOMP_TH0	RLD_DEC_EN
11h	LOFF_AC1	00	SQUARE_WAVE	ACDIV_FACTOR	ACDIV_FRQ5	ACDIV_FRQ4	ACDIV_FRQ3	ACDIV_FRQ2	ACDIV_FRQ1	ACDIV_FRQ0
12h	LON_CFG	00	HPF_EN	PF1	PF0	DEBOUNCE1	DEBOUNCE0	OFC_EN	AC_EXCT_THD1	AC_EXCT_THD0
13h	ERM_CFG	40	WMODE1	WMODE0	AC_DATA_OUT_EN	AC_DATA_OUT_SEL	AC_DATA_FEQ	ERM_MUX2	ERM_MUX1	ERM_MUX0
14h	EPMIX_CFG	10	PACE_CHOP_EN	PACE_COMP_EN	SHORT_PROTECT	FSEL1	FSEL0	DOUT_DO3MA	AC_CMP_CFG1	AC_CMP_CFG0
15h	PACE_CFG1	02	PACE_MUX2	PACE_MUX1	PACE_MUX0	PACE_GAIN2	PACE_GAIN1	PACE_GAIN0	PACEOUT_ON	PACE_EN
16h	FIFO_CFG1	00	FIFO_INT_EN	0	0	FIFO_RST	FRAME_CFG2	FRAME_CFG1	FRAME_CFG0	FIFO_EN

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ADDRESS	REGISTER	RESET VALUE (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
17h	FIFO_CFG2	00	STATUS_SEL2	STATUS_SEL1	STATUS_SEL0	DEPTH4	DEPTH3	DEPTH2	DEPTH1	DEPTH0
DEVICE STATUS AND PROPERTY (READ-ONLY REGISTERS)										
18h	FIFO_STAT	40	FIFO_RDY	FIFO_EMPTY	FIFO_FULL	FIFO_ERR	DLVL3	DLVL2	DLVL 1	DLVL0
DEVICE STATUS AND PROPERTY (READ AND WRITE REGISTERS)										
19h	MOD_STAT 1	00	INVALID_CMD_ERR	SHORT_GND	CLK_MISS	FRAME_MISS	DAT_CRC_ERR	CMD_CRC_ERR	OORNG	SHORT_PWR
1Ah	MOD_STAT 2	00	RLD_LOFF_P	RLD_LOFF_N	RSV	RSV	PGA2N_OOR	PGA2P_OOR	PGA1N_OOR	PGA1P_OOR
1Bh	OP_STAT_CMD	00	EFU_UERR	EFU_CERR	RDATAC_DONE	RD_FIFO_DONE	CAL_DONE	RDATA_DONE	REG_WR_DONE	REG_RD_DONE
DEVICE STATUS AND PROPERTY (READ-ONLY REGISTERS)										
1Ch	OP_STAT_SYS	92	SPI_UNLOCK	SPI_LOCK	SDC_MODE	RDC_MODE	STOP	START	WAKEUP	STARNDBY
1Dh	FI	XX	MF_ID3	MF_ID2	MF_ID1	MF_ID0	FS_ID3	FS_ID2	FS_ID1	FS_ID0
1Eh	ID_PR	70	PAR_ID3	PAR_ID2	PAR_ID1	PAR_ID0	REV_ID3	REV_ID2	REV_ID1	REV_ID0
EXTENDED FEATURE CONFIGURATION										
1Fh	AC_CMP_THD0	00	CMP_THD7	CMP_THD6	CMP_THD5	CMP_THD4	CMP_THD3	CMP_THD2	CMP_THD1	CMP_THD0
20h(1)	AC_CMP_THD1	00	CMP_THD15	CMP_THD14	CMP_THD13	CMP_THD12	CMP_THD11	CMP_THD10	CMP_THD9	CMP_THD8
21h(1)	AC_CMP_THD2	00	CMP_THD23	CMP_THD22	CMP_THD21	CMP_THD20	CMP_THD19	CMP_THD18	CMP_THD17	CMP_THD16
22h(1)	OFC_CH10	00	OFC_B7	OFC_B6	OFC_B5	OFC_B4	OFC_B3	OFC_B2	OFC_B1	OFC_B0
23h(1)	OFC_CH11	00	OFC_B15	OFC_B14	OFC_B13	OFC_B12	OFC_B11	OFC_B10	OFC_B9	OFC_B8
24h(1)	OFC_CH12	00	OFC_B23	OFC_B22	OFC_B21	OFC_B20	OFC_B19	OFC_B18	OFC_B17	OFC_B16
25h(1)	OFC_CH20	00	OFC_B7	OFC_B6	OFC_B5	OFC_B4	OFC_B3	OFC_B2	OFC_B1	OFC_B0
26h(1)	OFC_CH21	00	OFC_B15	OFC_B14	OFC_B13	OFC_B12	OFC_B11	OFC_B10	OFC_B9	OFC_B8
27h(1)	OFC_CH22	00	OFC_B23	OFC_B22	OFC_B21	OFC_B20	OFC_B19	OFC_B18	OFC_B17	OFC_B16
28h(1)	Reserved	04	0	0	0	0	0	1	0	0

Note: Registers with address > 1Fh can only be accessed through burst mode. They cannot be read or written directly.

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11.1 REGISTER DESCRIPTIONS

11.1.1 ID: ID CONTROL REGISTER (READ-ONLY) (ADDRESS = 00H)

Return to the SUMMARY TABLE. This register is programmed during device manufacturing to indicate device characteristics.

Table 37. ID Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	REV_ID(2:0)	Identification 000 = Reserved 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = ADX920/1/2/3
4	1	Reads High
3:2	0	Reads Low
1	1	Reads High
0	REV_ID	Feature set identification 1 = 2-channel product 0 = 1-channel product

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11.1.2 CONFIG1: CONFIGURATION REGISTER 1 (ADDRESS = 01H)

Return to the SUMMARY TABLE. This register configures each ADC channel sample rate.

Table 38. CONFIG1 Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>SINGLE_SHOT</td><td>Single-shot conversion
This bit sets the conversion mode.
0 = Continuous conversion mode (default)
1 = Single-shot mode</td></tr>
<tr><td>6:3</td><td>0</td><td>Must be set to ‘0’.</td></tr>
<tr><td>2:0</td><td>DR(2:0)</td><td>These bits determine the oversampling ratio of both channel 1 and channel 2.
<table>
<tr><th>BIT</th><th>OVERSAMPLING RATIO</th><th>f_{MOD} = 256kHz</th><th>f_{MOD} = 128kHz</th></tr>
<tr><td>000</td><td>f_{MOD} / 1024</td><td>250SPS</td><td>125SPS</td></tr>
<tr><td>001</td><td>f_{MOD} / 512</td><td>500SPS</td><td>250SPS</td></tr>
<tr><td>010</td><td>f_{MOD} / 256</td><td>1kSPS (default)</td><td>500SPS (default)</td></tr>
<tr><td>011</td><td>f_{MOD} / 128</td><td>2kSPS</td><td>1kSPS</td></tr>
<tr><td>100</td><td>f_{MOD} / 64</td><td>4kSPS</td><td>2kSPS</td></tr>
<tr><td>101</td><td>f_{MOD} / 32</td><td>8kSPS</td><td>4kSPS</td></tr>
<tr><td>110</td><td>f_{MOD} / 16</td><td>16kSPS</td><td>8kSPS</td></tr>
<tr><td>111</td><td>Do not use</td><td>Do not use</td><td>Do not use</td></tr>
</table></td></tr>
</table>

Note: f_{CLK} = 512kHz and CLK_DIV = 0 or f_{CLK} = 2.048MHz and CLK_DIV = 1.

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11.1.3 CONFIG2: CONFIGURATION REGISTER 2 (ADDRESS = 02H)

Return to the SUMMARY TABLE. This register configures the test signal, clock, reference, and LOFF buffer.

Table 39. CONFIG2 Field Descriptions

BIT	FIELD	DESCRIPTION
7	1	Must be set to '1'.
6	PDB_LOFF_COMP	Lead-off comparator power-down This bit powers down the lead-off comparators. 0 = Lead-off comparators disable (default) 1 = Lead-off comparators enable
5	PDB_REFBUF	Reference buffer power-down This bit powers down the internal reference buffer so that the external reference can be used. 0 = Reference buffer is powered down (default). 1 = Reference buffer is enabled.
4	VREF_4V	Enables 4V reference This bit chooses either the 2.4V or 4V reference. 0 = 2.4V reference (default) 1 = 4V reference
3	CLK_EN	CLK connection This bit determines whether the internal oscillator signal is connected to the CLK pin when an internal oscillator is used. 0 = Oscillator clock output disable (default) 1 = Oscillator clock output enable
2	0	Must be set to '0'.
1	INT_TEST	Test signal selection This bit determines whether the test signal is turned on. 0 = Off (default) 1 = On, amplitude = ±(VREFP – VREFN) / 2400
0	TEST_FREQ	Test signal frequency This bit determines the test signal frequency. 0 = At DC (default) 1 = Square wave at 1Hz

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11.1.4 LOFF: LEAD-OFF CONTROL REGISTER (ADDRESS = 03H)

Return to the SUMMARY TABLE. This register configures the lead-off detection operation.

Table 40. LOFF Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	COMP_TH(2:0)	Lead-off comparator threshold These bits determine the lead-off comparator threshold. See the LEAD-OFF DETECTION section for a detailed description. Comparator positive side 000 = 95% (default) 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator negative side 000 = 5% (default) 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
4	1	Must be set to '1'.
3:2	ILEAD_OFF(1:0)	Lead-off current magnitude These bits determine the magnitude of current for the current lead-off mode when CUR_LEVEL is zero; otherwise the current magnitude is decided by the ISTEP field. 00 = 6nA (default) 01 = 22nA 10 = Reserved 11 = Reserved
1	0	Must be set to '0'.
0	FLEAD_OFF	Lead-off frequency This bit selects AC or DC lead-off. 0 = DC lead-off detect (default) 1 = AC lead-off detect at f_{DR} / 4 (500Hz for a 2kHz output rate)

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11.1.5 CH1SET: CHANNEL 1 SETTINGS (ADDRESS = 04H)

Return to the SUMMARY TABLE. This register configures the power mode, PGA gain, and multiplexer settings channels. See the INPUT MULTIPLEXER section for details.

Table 41. CH1SET Field Descriptions

BIT	FIELD	DESCRIPTION
7	PD1	Channel 1 power-down 0 = Normal operation (default) 1 = Channel 1 power-down(1)
6:4	GAIN1(2:0)	Channel 1 PGA gain setting These bits determine the PGA gain setting for channel 1. 000 = 6 (default) 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12
3:0	MUX1(3:0)	Channel 1 input selection These bits determine the channel 1 input selection. 0000 = Normal electrode input (default) 0001 = Input shorted (for offset measurements) 0010 = RLD_MEASURE 0011 = MVDD(2) for supply measurement 0100 = Temperature sensor 0101 = Test signal 0110 = RLD_DRP (positive input is connected to RLDIN.) 0111 = RLD_DRM (negative input is connected to RLDIN.) 1000 = RLD_DRPM (both positive and negative inputs are connected to RLDIN.) 1001 = Route IN3P and IN3N to channel 1 inputs 1010 = Reserved 1011 = RLD_OUT

Note 1: When powering down channel 1, make sure the input multiplexer is set to input short configuration. Bits(3:0) = 001.

Note 2: For channel 1, (MVDDP – MVDDN) is (0.5(AVDD + AVSS)).
For channel 2, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to 1.

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11.1.6 CH2SET: CHANNEL 2 SETTINGS (ADDRESS = 05H)

Return to the SUMMARY TABLE. This register configures the power mode, PGA gain, and multiplexer settings channels. See the INPUT MULTIPLEXER section for details.

Table 42. CH2SET Field Descriptions

BIT	FIELD	DESCRIPTION
7	PD2	Channel 2 power-down 0 = Normal operation (default) 1 = Channel 2 power-down(1)
6:4	GAIN2(2:0)	Channel 2 PGA gain setting These bits determine the PGA gain setting for channel 2. 000 = 6 (default) 011 = 3 100 = 4 101 = 8 110 = 12 Others: Reserved
3:0	MUX2(3:0)	Channel 2 Input Selection These Bits Determine The Channel 2 Input Selection. 0000 = Normal Electrode Input (Default) 0001 = Input Shorted (For Offset Measurements) 0010 = RLD_MEASURE 0011 = VDD / 2 For Supply Measurement 0100 = Temperature Sensor 0101 = Test Signal 0110 = RLD_DRP (Positive Input Is Connected To RLDIN.) 0111 = RLD_DRM (Negative Input Is Connected To RLDIN.) 1000 = RLD_DRPM (Both Positive And Negative Inputs Are Connected To RLDIN.) 1001 = Route IN3P And IN3N To Channel 2 Inputs 1010 = Reserved 1011 = RLD_OUT 1111 = ERM Enable Others: Reserved

Note: When powering down channel 2 and for the ADX921, make sure the input multiplexer is set to input short configuration. Bits(3:0) = 001.

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11.1.7 RLD_SENS: RIGHT LEG DRIVE SENSE SELECTION (ADDRESS = 06H)

Return to the SUMMARY TABLE. This register controls the selection of the positive and negative signals from each channel for right leg drive derivation. See the RIGHT LEG DRIVE (RLD DC BIAS CIRCUIT) section for details.

Table 43. RLD_SENS Field Descriptions

BIT	FIELD	DESCRIPTION
7:6	CHOP(1:0)	Chop frequency (NOT USED)
5	PDB_RLD	RLD buffer power This bit determines the RLD buffer power state. 0 = RLD buffer is powered down (default). 1 = RLD buffer is enabled.
4	RLD_LOFF_SENS	RLD lead-off sense function This bit enables the RLD lead-off sense function. 0 = RLD lead-off sense is disabled (default). 1 = RLD lead-off sense is enabled.
3	RLD2N	Channel 2 RLD negative inputs This bit controls the selection of negative inputs from channel 2 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN2N
2	RLD2P	Channel 2 RLD positive inputs This bit controls the selection of positive inputs from channel 2 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN2P
1	RLD1N	Channel 1 RLD negative inputs This bit controls the selection of negative inputs from channel 1 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN1N
0	RLD1P	Channel 1 RLD positive inputs This bit controls the selection of positive inputs from channel 1 for right leg drive derivation. 0 = Not connected (default) 1 = RLD connected to IN1P

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11.1.8 LOFF_SENS: LEAD-OFF SENSE SELECTION (ADDRESS = 07H)

Return to the SUMMARY TABLE. This register selects the positive and negative side from each channel for lead-off detection. See the LEAD-OFF DETECTION section for details. Note that the LOFF_STAT register bits should be ignored if the corresponding LOFF_SENS bits are set to 1.

Table 44. LOFF_SENS Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>0</td><td>Must be set to '0'.</td></tr>
<tr><td>6</td><td>CP_FREQ</td><td>Charge Pump Frequency Selection
This bit sets the charge pump frequency with difference WMODE setting. See the POWER MODE section.
<table>
<tr><th>BIT</th><th>HI-SPEED</th><th>HI-RESOLUTION</th></tr>
<tr><td>0</td><td>512kHz</td><td>256kHz</td></tr>
<tr><td>1</td><td>256kHz</td><td>128kHz</td></tr>
</table></td></tr>
<tr><td>5</td><td>FLIP2</td><td>CH2 Comparator Polarity Selection
This bit controls the direction of the comparator used for lead-off derivation of channel 2.
0 = ECGP connects to the positive side of comparator, and ECGN connects to the negative side of comparator (default).
1 = ECGN connects to the positive side of comparator, and ECGP connects to the negative side of comparator.</td></tr>
<tr><td>4</td><td>FLIP1</td><td>CH1 Comparator Polarity Selection
This bit controls the direction of the comparator used for lead-off derivation of channel 1.
0 = ECGP connects to the positive side of comparator, and ECGN connects to the negative side of comparator (default).
1 = ECGN connects to the positive side of comparator, and ECGP connects to the negative side of comparator.</td></tr>
<tr><td>3:0</td><td>EMUX_LOFF(3:0)</td><td>Channel 1 lead-off configuration setting
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0: The positive side of the ECG channel is disconnected to AVDD (default).
1: The positive side of the ECG channel is connected to AVDD.</td></tr>
<tr><td>1</td><td>0: The negative side of the ECG channel is disconnected to AVSS (default).
1: The negative side of the ECG channel is connected to AVSS.</td></tr>
<tr><td>2</td><td>0: The negative side of the ECG channel is disconnected to AVDD (default).
1: The negative side of the ECG channel is connected to AVDD.</td></tr>
<tr><td>3</td><td>0: The positive side of the ECG channel is disconnected to AVSS (default).
1: The positive side of the ECG channel is connected to AVSS.</td></tr>
</table></td></tr>
</table>

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11.1.9 LOFF_STAT: LEAD-OFF STATUS (ADDRESS = 08H)

Return to the SUMMARY TABLE. This register stores the status of whether the positive or negative electrode on each channel is on or off. See the LEAD-OFF DETECTION section for details. Ignore the LOFF_STAT values if the corresponding LOFF_SENS bits are not set to 1.

0 is lead -on (default) and 1 is lead -off. When the LOFF_SENS bits(3:0) are 0 , the LOFF_STAT bits should be ignored.

Table 45. LOFF_STAT Field Descriptions

BIT	FIELD	DESCRIPTION
7	0	Must be set to '0'.
6:5	CLK_DIV(1:0)	Clock divider selection This bit sets the modular divider ratio between f_{CLK} and f_{MOD}. 00 = f_{MOD} = f_{CLK} / 4 01 = f_{MOD} = f_{CLK} / 8 10 = f_{MOD} = f_{CLK} / 16 11 = Reserved
4	RLD_STAT	RLD lead-off status This bit determines the status of RLD. 0 = RLD is connected (default). 1 = RLD is not connected.
3	IN2N_OFF	Channel 2 negative electrode status This bit determines if the channel 2 negative electrode is connected. 0 = Connected (default) 1 = Not connected
2	IN2P_OFF	Channel 2 positive electrode status This bit determines if the channel 2 positive electrode is connected. 0 = Connected (default) 1 = Not connected
1	IN1N_OFF	Channel 1 negative electrode status This bit determines if the channel 1 negative electrode is connected. 0 = Connected (default) 1 = Not connected
0	IN1P_OFF	Channel 1 positive electrode status This bit determines if the channel 1 positive electrode is connected. 0 = Connected (default) 1 = Not connected

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11.1.10 RESP1: RESPIRATION CONTROL REGISTER 1 (ADDRESS = 09H)

Return to the SUMMARY TABLE. This register controls the respiration functionality. This register applies to the ADX923 version only. For the ADX921/2 devices, 02h must be written to the RESP1 register.

Table 46. RESP1 Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>RESP_DEMOD_EN1</td><td>Enables respiration demodulation circuitry
This bit enables and disables the demodulation circuitry on channel 1.
0 = RESP demodulation circuitry disable (default)
1 = RESP demodulation circuitry enable</td></tr>
<tr><td>6</td><td>RESP_MOD_EN</td><td>Enables respiration modulation circuitry
This bit enables and disables the modulation circuitry on channel 1.
0 = RESP modulation circuitry disable (default)
1 = RESP modulation circuitry enable</td></tr>
<tr><td>5:2</td><td>RESP_PH(3:0)</td><td>Respiration phase(1)
These bits control the phase of the respiration demodulation control signal.
<table>
<tr><th>RESP_PH(3:0)</th><th>RESP_ FREQ= 32kHz</th><th>RESP_FREQ= 64kHz</th></tr>
<tr><td>0000</td><td>0° (default)</td><td>0° (default)</td></tr>
<tr><td>0001</td><td>11.25°</td><td>22.5°</td></tr>
<tr><td>0010</td><td>22.5°</td><td>45°</td></tr>
<tr><td>0011</td><td>33.75°</td><td>67.5°</td></tr>
<tr><td>0100</td><td>45°</td><td>90°</td></tr>
<tr><td>0101</td><td>56.25°</td><td>112.5°</td></tr>
<tr><td>0110</td><td>67.5°</td><td>135°</td></tr>
<tr><td>0111</td><td>78.75°</td><td>157.5°</td></tr>
<tr><td>1000</td><td>90°</td><td>Not available</td></tr>
<tr><td>1001</td><td>101.25°</td><td>Not available</td></tr>
<tr><td>1010</td><td>112.5°</td><td>Not available</td></tr>
<tr><td>1011</td><td>123.75°</td><td>Not available</td></tr>
<tr><td>1100</td><td>135°</td><td>Not available</td></tr>
<tr><td>1101</td><td>146.25°</td><td>Not available</td></tr>
<tr><td>1110</td><td>157.5°</td><td>Not available</td></tr>
<tr><td>1111</td><td>168.75°</td><td>Not available</td></tr>
</table></td></tr>
<tr><td>1</td><td>1</td><td>Must be set to '1'.</td></tr>
<tr><td>0</td><td>RESP_CTRL</td><td>Respiration control
This bit sets the mode of the respiration circuitry.
0 = Internal respiration with internal clock
1 = Internal respiration with external clock</td></tr>
</table>

Note: The RESP_PH3 bit is ignored when RESP_FREQ = 64kHz.

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11.1.11 RESP2: RESPIRATION CONTROL FREQUENCY (ADX922/3 ONLY) (ADDRESS = 0AH)

Return to the SUMMARY TABLE. This register controls the respiration and calibration functionality.

Table 47. RESP2 Field Descriptions

BIT	FIELD	DESCRIPTION
7	CALIB_ON	Calibration on This bit is used to enable offset calibration. 0 = Off (default) 1 = On
6	0	Must be set to '0'.
5:3	0	Must be set to '0'.
2	RESP_FREQ	Respiration control frequency (ADX923 only) This bit controls the respiration control frequency when RESP_CTRL = 0. This bit must be written with '1' for the ADX920/1/2. When system clock = 512kHz, in the HR mode. 0 = 32kHz (default) 1 = 64kHz
1	RLDREF_INT	RLDREF signal This bit determines the RLDREF signal source. 0 = RLDREF signal fed externally 1 = RLDREF signal (AVDD + AVSS) / 2 generated internally (default)
0	1	Must be set to '1'.

11.1.12 GPIO: GENERAL-PURPOSE I/O REGISTER (ADDRESS = 0BH)

Return to the SUMMARY TABLE. This register controls the GPIO pins.

Table 48. GPIO Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	AC_AMP_SCALE(2:0)	AC lead-off amplitude configuration 000 = Original amplitude 001 = Amplitude / 2 010 = Amplitude / 4 011 = Amplitude / 8 100 = Amplitude / 16 Others = Reserved
4	0	Must be set to '0'.
3:2	GPIOC(2:1)	GPIO 1 and 2 control These bits determine if the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input (default)
1:0	GPIOD(2:1)	GPIO 1 and 2 data These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, no matter that they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. GPIO is not available in certain respiration modes.

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11.1.13 CONFIG3: FUNCTION CONFIGURATION REGISTER 3 (ADDRESS = 0CH)

Return to the SUMMARY TABLE. This register controls the feature configuration.

Table 49. CONFIG3 Field Descriptions

BIT	FIELD	DESCRIPTION
7	AC_MODE	Software AC lead-off and Digital AC lead-off mode selection 0: Software AC mode (default) 1: Hardware Digital AC mode
6	P5VREF_ON	V_{REF} / 2 switch 0 = 1/2 V_{REF} switch is turned off (default). 1 = 1/2 V_{REF} switch is turned on.
5	0	Must be set to '0'.
4	0	Must be set to '0'.
3	DIN_CRC_EN	Communication input data CRC check enable 0 = Input data CRC disable (default) 1 = Input data CRC enable
2	DOUT_CRC_EN	Communication output data CRC check enable 0 = Output data CRC disable (default) 1 = Output data CRC enable
1:0	SPI_TIMEOUT(1:0)	SPI interface reset function control to detect idle clock number 00 = Disable (default) 01 = SPI interface will be reset after 255 divider clock cycles with LOFF_STAT(6).CLK_DIV configuration. 10 = SPI interface will be reset after 1023 divider clock cycles with LOFF_STAT(6).CLK_DIV configuration. 11 = SPI interface will be reset after 4095 divider clock cycles with LOFF_STAT(6).CLK_DIV configuration.

11.1.14 CONFIG4: FUNCTION CONFIGURATION REGISTER 4 (ADDRESS = 0DH)

Return to the SUMMARY TABLE. This register controls the feature configuration.

Table 50. CONFIG4 Field Descriptions

BIT	FIELD	DESCRIPTION
7	DR_INT_EN	ADC data out of range interrupt enable 0 = ADC data out of range interrupt disable (default) 1 = ADC data out of range interrupt enable
6:5	ADC_DAT_THD(1:0)	ADC data threshold to set out of range flag 00 = ADC data range exceeds 24-bit data range (default). Others = Reserved
4	0	Must be set to '0'.
3	CLK_MISS_INT_EN	External clock miss interrupt enable 0 = Clock Miss Interrupt disable 1 = Clock Miss Interrupt enable
2	0	Must be set to '0'.
1	RLDIN2RAMPP_ON	RLDIN input to RLD AMP input positive switch 0 = Switch is disconnected (default). 1 = Switch is connected.
0	RAMPOUT2RAMPN_ON	RLD AMP output to RLD AMP input negative switch 0 = Switch is disconnected (default). 1 = Switch is connected.

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11.1.15 CONFIG5: FUNCTION CONFIGURATION REGISTER 5 (ADDRESS = 0EH)

Return to the SUMMARY TABLE. This register controls the feature configuration.

Table 51. CONFIG5 Field Descriptions

BIT	FIELD	DESCRIPTION
7	OSC_2M_EN	2M OSC enable control External clock is selected when the CLKSEL pin is 0. It is used to monitor external CLK missing or invalid issue. 0 = Disable OSC (default). 1 = Enable OSC to check External Clock idle status.
6:4	INTGPIO(2:0)	Interrupt output to GPIO, including LOFF interrupt INT1, ADC data out of range interrupt INT2, FIFO interrupt INT3, CLK missing interrupt INT4, and invalid SPI command interrupt INT5. 000 = INT1, INT2, INT3, INT4, INT5 output to external with GPIO1. 001 = INT1, INT2, INT3, INT4, INT5 output to external with GPIO2. 010 = INT1, INT2, INT3, INT5 output to external with GPIO1, INT4 output to external with GPIO2. 011 = INT1, INT2, INT4, INT5 output to external with GPIO1, INT3 output to external with GPIO2. 100 = INT1, INT3, INT4, INT5 output to external with GPIO1, INT2 output to external with GPIO2. 101 = INT2, INT3, INT4, INT5 output to external with GPIO1, INT1 output to external with GPIO2. 110 = INT1, INT2, INT3, INT4 output to external with GPIO1, INT5 output to external with GPIO2. 111 = NO interrupt output to GPIO pin. (default) Others = Reserved
3	INV_CMD_INT_EN	Invalid SPI command interrupt enable It generates an interrupt for the invalid command if the command is detected. 0 = Invalid SPI command Interrupt disable 1 = Invalid SPI command Interrupt enable
2	FRAME_CHK_EN	FRAME Overwrite Check enable (it does not check FIFO overwrite) 0 = Disable FRAME miss check for SPI slow read (default) 1 = Enable FRAME miss check for SPI slow read
1	IO_3MA	IO strong (3mA) mode enable 0 = Strong mode disable (default) 1 = Strong mode enable
0	IO_SRM	IO slew read mode enable 1 = IO slew read mode enable (default) 0 = IO slew read mode disable

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11.1.16 LOFF_ISTEP: LEAD-OFF CURRENT STEP CONFIGURATION REGISTER (ADDRESS = 0FH)

Return to the SUMMARY TABLE. This register controls the IDAC current step.

Table 52. LOFF_ISTEP Field Descriptions

BIT	FIELD	DESCRIPTION
7	LOFF_INT_EN	Lead-off interrupt enable 0 = Lead-off interrupt disable (default) 1 = Lead-off interrupt enable, and the interrupt is output to the GPIO1 or GPIO2 pin.
6	CUR_LEVEL	Lead-off current level selection it this bit is zero, the IDAC current setting comes from the ILEAD_OFF(1:0) value. 0 = Disable ISTEP value configuration (default) 1 = Enable ISTEP value configuration
5:0	ISTEP(5:0)	Lead-off current magnitude These bits determine the magnitude of current for the current lead-off mode when CUR_LEVEL is one; otherwise the current magnitude is decided by the ILEAD_OFF(1:0) field. 000000 = 0nA and step = 2.2nA (default) 000001 = 2.2nA ..... 111111 = 138.6nA

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11.1.17 LOFF_RLD: LEAD-OFF STEP CONFIGURATION REGISTER (ADDRESS = 10H)

Return to the SUMMARY TABLE. This register controls the RLD threshold step.

Table 53. LOFF_RLD Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>DESCRIPTION</th></tr>
<tr><td>7:4</td><td>EMUX_LOFF(3:0)</td><td>Channel 2 lead-off configuration setting
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0: The positive side of the ECG channel is disconnected to AVDD (default).
1: The positive side of the ECG channel is connected to AVDD.</td></tr>
<tr><td>1</td><td>0: The negative side of the ECG channel is disconnected to AVSS (default).
1: The negative side of the ECG channel is connected to AVSS.</td></tr>
<tr><td>2</td><td>0: The negative side of the ECG channel is disconnected to AVDD (default).
1: The negative side of the ECG channel is connected to AVDD.</td></tr>
<tr><td>3</td><td>0: The positive side of the ECG channel is disconnected to AVSS (default).
1: The positive side of the ECG channel is connected to AVSS.</td></tr>
</table></td></tr>
<tr><td>3:1</td><td>RCOMP_TH(2:0)</td><td>RLD lead-off comparator threshold
These bits determine the lead-off comparator threshold. See the LEAD-OFF DETECTION section for a detailed description.
Comparator positive side
000 = 95% (default)
001 = 92.5%
010 = 90%
011 = 87.5%
100 = 85%
101 = 80%
110 = 75%
111 = 70%
Comparator negative side
000 = 5% (default)
001 = 7.5%
010 = 10%
011 = 12.5%
100 = 15%
101 = 20%
110 = 25%
111 = 30%</td></tr>
<tr><td>0</td><td>RLD_DEC_EN</td><td>RLD dedicated threshold comparator enable
0 = RLD shares the threshold comparator with the RA, LA, and LL pins (default).
1 = RLD uses standalone comparator and needs configure RCOMP_TH(2:0) for threshold setting.</td></tr>
</table>

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11.1.18 LOFF_AC1: AC LEAD-OFF CONFIGURATION REGISTER (ADDRESS = 11H)

Return to the SUMMARY TABLE. This register controls the AC lead-off detection.

Table 54. LOFF_AC1 Field Descriptions

BIT	FIELD	DESCRIPTION
7	SQUARE_WAVE	Square or sine wave 0: Sine wave (default) 1: Square wave
6	ACDIV_FACTOR	AC lead-off test frequency division factor 0: Clock divider factor K = 1 (default) 1: Clock divider factor K = 8
5:0	ACDIV_FRQ(5:0)	System clock = 512kHz, HR mode. If ACDIV_FACTOR = 0, step = 1000Hz. ACDIV_FREQ odd configuration number is suggested. 000000 = 1000Hz … 000111 = 8000Hz Others = Reserved If ACDIV_FACTOR = 1, step = 125Hz. ACDIV_FREQ odd configuration number is suggested. 000000 = 125Hz … 000111 = 1000Hz Others = Reserved

11.1.19 LON_CFG: LEAD-ON NEIGHBORING CONFIGURATION REGISTER (ADDRESS = 12H)

Return to the SUMMARY TABLE. This register controls the lead-on detection.

Table 55. LON_CFG Field Descriptions

BIT	FIELD	DESCRIPTION
7	HPF_EN	ECG channel digital high-pass filter enable 0 = HPF disable (default) 1 = HFP enable
6:5	PF(1:0)	ECG channel digital high-pass filter cutoff frequency (only support 125 ODR and 250 ODR) 00 = 0.5Hz (default) 01 = 0.67Hz 10 = 7.0Hz 11 = Reserved
4:3	DEBOUNCE(1:0)	ECG DC lead-off output debounce time 00 = Debounce disable (default) 01 = Debounce time 117ms 10 = Debounce time 335ms 11 = Reserved
2	OFC_EN	Function offset calibration enable 0 = User calibration disable 1 = User calibration enable
1:0	AC_EXCT_THD(1:0)	AC excitation amplitude selection 00 = The maximum AC excitation amplitude is 160nA. 01 = The maximum AC excitation amplitude is 80nA. 10 = The maximum AC excitation amplitude is 40nA. 11 = The maximum AC excitation amplitude is 20nA.

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11.1.20 ERM_CFG: ELECTRODE ROTATION MODE REGISTER (ADDRESS = 13H)

Return to the SUMMARY TABLE. This register controls electrode rotation mode.

Table 56. ERM_CFG Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>DESCRIPTION</th></tr>
<tr><td>7:6</td><td>WMODE(1:0)</td><td>Device power mode selection
00 = High-Speed mode
01 = High-Resolution mode
10 = Reserved
11 = Reserved</td></tr>
<tr><td>5</td><td>AC_DATA_OUT_EN</td><td>AC lead-off data output enable
0 = AC lead-off data output disable
1 = AC lead-off data output enable in RDATAC mode</td></tr>
<tr><td>4</td><td>AC_OUT_DATA_SEL</td><td>AC lead-off data output channel selection
0 = Output AC lead-off LPF sine data of channel 1 and channel 2
1 = Output AC lead-off LPF cosine data of channel 1 and channel 2</td></tr>
<tr><td>3</td><td>AC_DATA_FEQ</td><td>AC lead-off data output frequency selection
0 = Output data rate is 4K if ACDIV_FACTOR = 0, and data rate is 500Hz if ACDIV_FACTOR = 1. (default)
1 = Output data rate is 16K if ACDIV_FACTOR = 0, and data rate is 2K if ACDIV_FACTOR = 1.</td></tr>
<tr><td>2:0</td><td>ERM_MUX(2:0)</td><td>EMR MUX selection
There are 7 valid options for ERM configuration. When any ERM switch is 1, the channel 2 MUX must be set to 4’b1111.
<table>
<tr><th></th><th>001</th><th>010</th><th>011</th><th>100</th><th>101</th><th>110</th><th>OTHERS</th></tr>
<tr><td>RLD2RA</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RLD2LA</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RLD2LL</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>LL2IN2P</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>LA2IN2P</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RA2IN2P</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>LL2IN2N</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>LA2IN2N</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>RA2IN2N</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
</table>

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11.1.21 EPMIX_CONFIG: ERMA AND PACE CONFIGURATION REGISTER (ADDRESS = 14H)

Return to the SUMMARY TABLE. This register controls the pace configuration.

Table 57. EPMIX_CONFIG Field Descriptions

BIT	FIELD	DESCRIPTION
7	PACE_CHOP_EN	PACE_CHOP_EN enable selection 0 = PACE PGA chopper disable (default) 1 = PACE PGA chopper enable
6	PACE_COMP_EN	PACE_PGA comparator enable control 0 = PGA comparator enable (default) 1 = PGA comparator disable
5	SHORT_PROTECT	SHORT_PROTECT enable control 0 = Short protect disable (default) 1 = Short protect enable
4:3	FSEL(1:0)	FSEL to select internal OSC clock frequency 00 = Reserved 01 = 1024kHz 10 = 512kHz (default) 11 = 256kHz
2	DOUT_DO3MA	DOUT pin current strength control 0 = DOUT pin has strong driving strength. 1 = DOUT pin has low driving strength to save power.
1:0	AC_CMP_CFG(1:0)	AC comparator threshold configuration 00 = Channel 1 and channel 2 share the 24-bit comparator threshold for AC lead-off result comparison. 01 = Channel 1 uses the low 12 bits of comparator threshold, and channel 2 uses the high 12 bits of comparator threshold to compare with the high 12-bit AC lead-off result. 10 = Channel 1 uses the low 12 bits of comparator threshold, and channel 2 uses the high 12 bits of comparator threshold to compare with the low 12-bit AC lead-off result. 11 = Reserved.

11.1.22 PACE_CFG1: PACE CONFIGURATION REGISTER (ADDRESS = 15H)

Return to the SUMMARY TABLE. This register controls the pace configuration.

Table 58. PACE_CFG1 Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	PACE_MUX(2:0)	PACE Vinp and Vinm source selection 000 = PACE terminal is connected to IN1P and IN1N (default). 001 = PACE terminal is connected to IN2P and IN2N. Others = Reserved
4:2	PACE_GAIN(2:0)	PACE PGA gain setting 000 = 4 (default) 001 = 2/3 010 = 4/3 011 = 2 100 = 8/3 101 = 16/3 110 = 8
1	PACEOUT_ON	PACEOUT_ON: Pace output to the PGA2P pin control 1 = Output enable (default) 0 = Output disable.
0	PACE_EN	PACE function module enable 0 = The PACE function module is disabled to save power (default). 1 = The PACE function module is enabled for pace detection.

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11.1.23 FIFO_CFG1: FIFO CONFIGURATION REGISTER 1 (ADDRESS = 16H)

Return to the SUMMARY TABLE. This register controls the FIFO configuration.

Table 59. FIFO_CFG1 Field Descriptions

BIT	FIELD	DESCRIPTION
7	FIFO_INT_EN	FIFO interrupt enable when FIFO data hit threshold. 0: FIFO interrupt disable (default) 1: FIFO interrupt enable
6:5	0	Must be set to '0'.
4	FIFO_RST	FIFO reset control 0 = FIFO software reset disable (default). 1 = FIFO software reset enable. Software must write 0 to clear the FIFO_RST bit.
3:1	FRAME_CFG(2:0)	FRAME configuration 5-bit LEAD_OFF (rld_stat, in2n_off, in2p_off, in1n_off, in1p_off) 3-bit LEAD_OFF (rld_stat, in2n_off, in2p_off) when channel 2 is active. 3-bit LEAD_OFF (rld_stat, in1n_off, in1p_off) when channel 1 is active.
0	FIFO_EN	FIFO enable control 0 = FIFO is disabled (default). 1 = FIFO is enabled.

BIT	DESCRIPTION
000	Only one active channel for ECG data The frame format is as below (default): 3-bit LEAD_OFF (1st), 3-bit LEAD_OFF (2nd), 1-bit PACE (1st) or 1-bit GPIO (1st), 1-bit PACE (2nd) or 1-bit GPIO (2nd), 24-bit ECG data (1st), 24-bit ECG data (2nd)
001	Two active channels for ECG or respiration. The frame format is as below: {5-bit LEAD_OFF, 1'b0, 2-bit GPIO or 2-bit PACE data, 24-bit CH1 ECG/respiration data, 24-bit CH2 ECG data}
Others	Reserved

11.1.24 FIFO_CFG2: FIFO CONFIGURATION REGISTER 2 (ADDRESS = 17H)

Return to the SUMMARY TABLE. This register controls the FIFO configuration.

Table 60. FIFO_CFG2 Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	STATUS_SEL(2:0)	FIFO read pointer overwrite pointer FAULT 000 = No GPIO and PACE flag into FIFO frame (default) 001 = Put GPIO1 data into FIFO frame 010 = Put GPIO2 data into FIFO frame 011 = Put GPIO1 and GPIO2 data into FIFO frame Others = Reserved
4:0	DEPTH(4:0)	FIFO data to trigger MCU read data 00000 = 1-item data to trigger MCU read data (default) 00001 = 2-item data to trigger MCU read data 00010 = 3-item data to trigger MCU read data … 01011 = 12-item data to trigger MCU read data Others = Reserved

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11.1.25 FIFO_STAT: FIFO STATUS REGISTER (ADDRESS = 18H)

Return to the SUMMARY TABLE. This register controls the FIFO status.

Table 61. FIFO_STAT Field Descriptions

BIT	FIELD	DESCRIPTION
7	FIFO_RDY	FIFO data is ready for MCU read. 0 = FIFO data does not meet threshold (default). 1 = FIFO data is ready for MCU read.
6	FIFO_EMPTY	FIFO status 0 = FIFO is not empty. 1 = FIFO is empty (default).
5	FIFO_FULL	FIFO status 0 = FIFO is not full (default). 1 = FIFO is full.
4	FIFO_ERROR	FIFO error occurs. Write the FIFO_RST field of FIFO_CFG1 to clear FIFO error. 0 = No FIFO error. 1 = If FIFO is disabled and FIFO read pointer is not equal to write pointer, the FIFO error occurs. FIFO will be disabled when the read/write is triggered unexpectedly, or when FIFO is not empty.
3:0	DLVL(3:0)	FIFO data watermark level for MCU read data 0000 = No-item data in FIFO for MCU read (default) 0001 = 1-item data in FIFO for MCU read data 0010 = 2-item data in FIFO for MCU read data … 1011 = 12-item data in FIFO for MCU read data Others = Reserved

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11.1.26 MOD_STAT1: INTERNAL MODULE STATUS REGISTER 1 (ADDRESS = 19H)

Return to the SUMMARY TABLE. This register stores the status of device submodule.

Table 62. MOD_STAT1 Field Descriptions

BIT	FIELD	DESCRIPTION
7	INVALID_CMD_ERR	Invalid SPI command is detected. Only the first invalid command will set this bit, Ignore this bit when DIN_CRC_EN is set. 0 = There is no invalid SPI command error. 1 = There is an invalid SPI command error.
6	SHORT_GND	Digital pin shorted to ground. Software needs to write zero to clear last status before using it again. 0 = No pin shorted to ground (default) 1 = Digital pin shorted to ground
5	CLK_MISS	Input clock missing or invalid issue occurs. This bit will always be set until device reset is triggered. This is a critical fault for application. 0 = No clock missing occurs (default). 1 = Clock missing occurs.
4	FRAME_MISS	Frame buffer overwrite occurs. 0 = No frame buffer overwrite (default). 1 = Frame buffer is overwritten and missing occurs.
3	DAT_CRC_ERR	SPI write command and data CRC error occurs. 0 = SPI write data has no CRC error (default). 1 = SPI write data has CRC error.
2	CMD_CRC_ERR	SPI command CRC error occurs, except WREG command 0 = Input command has no CRC error (default). 1 = Input command has CRC error.
1	OORNG	ADC value out-of-range occurs. The ADC result out of range flag (default) 0 = ADC value not out of range 1 = ADC value out of range
0	SHORT_PWR	Digital pin shorted to power. Software needs to write zero to clear last status before using it again. 0 = No pin shorted to power (default) 1 = Digital pin shorted to power

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11.1.27 MOD_STAT2: INTERNAL MODULE REGISTER 2 (ADDRESS = 1AH)

Return to the SUMMARY TABLE. This register stores the status of device submodule.

Table 63. MOD_STAT2 Field Descriptions

BIT	FIELD	DESCRIPTION
7	RLD_LOFF_P	RLD lead-off status Software needs to write zero to clear last status before using it again. 0 = No RLD positive lead-off occurs (default). 1 = RLD positive lead-off occurs.
6	RLD_LOFF_N	RLD lead-off status Software needs to write zero to clear last status before using it again. 0 = No RLD negative lead-off occurs (default). 1 = RLD negative lead-off occurs.
5	RSV	Reserved
4	RSV	Reserved
3	PGA2N_OOR	PGA2 negative out of range Software needs to write zero to clear last status before using it again. 0 = No PGA2 negative out of range (default). 1 = PGA2 negative out of range occurs.
2	PGA2P_OOR	PGA2 positive out of range Software needs to write zero to clear last status before using it again. 0 = No PGA2 positive out of range (default). 1 = PGA2 positive out of range occurs.
1	PGA1N_OOR	PGA1 negative out of range Software needs to write zero to clear last status before using it again. 0 = No PGA1 negative out of range (default). 1 = PGA1 negative out of range occurs.
0	PGA1P_OOR	PGA1 positive out of range Software needs to write zero to clear last status before using it again. 0 = No PGA1 positive out of range (default). 1 = PGA1 positive out of range occurs.

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11.1.28 OP_STAT_CMD: OPERATION STATUS COMMAND REGISTER (ADDRESS = 1BH)

Return to the SUMMARY TABLE. This register stores the status of user command.

Table 64. OP_STAT_CMD Field Descriptions

BIT	FIELD	DESCRIPTION
7	EFU_UERR	eFuse unacceptable error 0 = No unacceptable error 1 = Unacceptable error
6	EFU_CERR	eFuse Correct error 0 = No correctable error 1 = Correctable error
5	RDATAC_DONE	RDATA Continuously command The bit shows the RDATA command status if device executes the RDATAC command. 0 = NO RDATAC command is executed (default). 1 = RDATAC command is executed.
4	RD_FIFO_DONE	FIFO Read Command execution status when FIFO is enabled. The RFIFO command will be dropped if FIFO is enabled. 0 = Device has NOT executed the RFIFO command (default). 1 = Device has executed the RFIFO command.
3	CAL_DONE	Device Calibration done The bit shows the Channel Offset Calibration status if device executes the OFFSETCAL command. 0 = No device calibration (default) 1 = Device calibration done
2	RDATA_DONE	Read ADC data to shift register status. 0 = Device has NOT executed the RDATA command (default) 1 = Device has executed the RDATA command.
1	REG_WR_DONE	Device has executed a WREG command. 0 = Device has NOT executed the WREG command (default). 1 = Device has executed the WREG command
0	REG_RD_DONE	Device has executed a RREG command. 0 = Device has NOT executed the RREG command (default). 1 = Device has executed the RREG command.

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11.1.29 OP_STAT_SYS: SYSTEM OPERATION STATUS REGISTER (ADDRESS = 1CH)

Return to the SUMMARY TABLE. This register stores the status of user operation.

Table 65. OP_STAT_SYS Field Descriptions

BIT	FIELD	DESCRIPTION
7	SPI_UNLOCK	Device is locked for the LOCK command. The device SPI is in locked status if device executes the UNLOCK command, and the status is cleared to zero when device executes the LOCK command. 0 = SPI interface is locked. 1 = SPI interface is unlocked (default).
6	SPI_LOCK	Device is locked for the LOCK command. The device SPI is in locked status if device executes the LOCK command, and the status is cleared to zero when device executes the UNLOCK command. 0 = SPI interface is unlocked (default). 1 = SPI interface is locked.
5	SDC_MODE	Stop Read Data Continuously mode The device is in Stop Read Data Continuously mode if device executes the SDATAC command. The status is cleared to zero when device executes the RDATAC command. 0 = Device in Read Data Continuously mode (default). 1 = Device NOT in Read Data Continuously mode
4	RDC_MODE	Read Data Continuously mode (only indicates device mode) The device is in Read Data Continuously mode if device executes the RDATAC command. The status is cleared to zero when device executes the SDATAC command. 0 = Device NOT in Read Data Continuously mode 1 = Device in Read Data Continuously mode (default)
3	STOP	Stop Conversion status The device is in Stop Conversion state if device executes the STOP command. The status is cleared to ZERO when device executes the START command or sets the START pin. 0 = Device NOT in Stop Conversion status (default). 1 = Device in Stop Conversions status
2	START	Start Conversion status The device has executed the START command or a valid START event from the START pin. 0 = Device has NOT executed the START command or START Pin event (default). 1 = Device executed a START command or START Pin event.
1	WAKEUP	Device in WAKEUP mode The device is in WAKEUP mode if the device executes a wakeup command. The bit is cleared to zero if the device executes a STANDBY command. 0 = Device NOT in WAKEUP mode 1 = Device in WAKEUP mode (default)
0	STANDBY	Device in STANDBY mode The device is in STANDBY mode if the device executes a standby command. The bit is cleared to zero if the device executes a WAKEUP command. 0 = Device NOT in STANDBY mode (default) 1 = Device in STANDBY mode

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11.1.30 FI: FUCTION INDICATOR REGISTER (READ-ONLY) (ADDRESS = 1DH)

Return to the SUMMARY TABLE. This register stores the device manufacture information.

Table 66. FI Field Descriptions

BIT	FIELD	DESCRIPTION
7:6	RSV(1:0)	Reserved
5:0	FS_ID(5:0)	Feature set identification Bit 0 = 0: Has PACE Bit 1 = 0: Has RESP Bit 2 = 0: Has AC-LOFF Bit 3 = 0: Has FIFO Bit 4 = 0: Has DFS Bit 5 = 0: Has DHP

11.1.31 ID_PR: ID PART INFORMATION REGISTER (READ-ONLY) (ADDRESS = 1EH)

Return to the SUMMARY TABLE. This register indicates the device part information.

Table 67. ID_PR Field Descriptions

BIT	FIELD	DESCRIPTION
7:4	PAR_ID(3:0)	Identification 0x7: ADX920/1/2/3 Others: Reserved
3:0	RSV(3:0)	Reserved

11.1.32 AC_CMP_THD0: AC LEAD-OFF COMPARATOR THRESHOLD REGISTER 0 (ADDRESS = 1FH)

Return to the SUMMARY TABLE. This register controls the AC lead-off comparator threshold.

Table 68. AC_CMP_THD0 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	CMP_THD(7:0)	AC lead-off comparator threshold low byte

11.1.33 AC_CMP_THD1: AC LEAD-OFF COMPARATOR THRESHOLD REGISTER 1 (ADDRESS = 20H)

Return to the SUMMARY TABLE. This register controls the AC lead-off comparator threshold.

Table 69. AC_CMP_THD1 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	CMP_THD(15:8)	AC lead-off comparator threshold middle byte

11.1.34 AC_CMP_THD2: AC LEAD-OFF COMPARATOR THRESHOLD REGISTER 2 (ADDRESS = 21H)

Return to the SUMMARY TABLE. This register controls the AC lead-off comparator threshold.

Table 70. AC_CMP_THD2 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	CMP_THD(31:16)	AC lead-off comparator threshold high byte

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11.1.35 OFC_CH10: CHANNEL 1 OFFSET CALIBRATION REGISTER 0 (ADDRESS = 22H)

Return to the SUMMARY TABLE. This register controls the channel 1 offset calibration.

Table 71. OFC_CH10 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(7:0)	Offset calibration register byte 0 (channel 1)

11.1.36 OFC_CH11: CHANNEL 1 OFFSET CALIBRATION REGISTER 1 (ADDRESS = 23H)

Return to the SUMMARY TABLE. This register controls the channel 1 offset calibration.

Table 72. OFC_CH11 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(15:8)	Offset calibration register byte 1 (channel 1)

11.1.37 OFC_CH12: CHANNEL 1 OFFSET CALIBRATION REGISTER 2 (ADDRESS = 24H)

Return to the SUMMARY TABLE. This register controls the channel 1 offset calibration.

Table 73. OFC_CH12 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(23:16)	Offset calibration register byte 2 (channel 1)

11.1.38 OFC_CH20: CHANNEL 2 OFFSET CALIBRATION REGISTER 0 (ADDRESS = 25H)

Return to the SUMMARY TABLE. This register controls the channel 2 offset calibration.

Table 74. OFC_CH20 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(15:8)	Offset calibration register byte 0 (channel 2)

11.1.39 OFC_CH21: CHANNEL 2 OFFSET CALIBRATION REGISTER 1 (ADDRESS = 26H)

Return to the SUMMARY TABLE. This register controls the channel 2 offset calibration.

Table 75. OFC_CH21 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(7:0)	Offset calibration register byte 1 (channel 2)

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11.1.40 OFC_CH22: CHANNEL 2 OFFSET CALIBRATION REGISTER 2 (ADDRESS = 27H)

Return to the SUMMARY TABLE. This register controls the channel 2 offset calibration.

Table 76. OFC_CH22 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(23:16)	Offset calibration register byte 2 (channel 2)

11.1.41 RESERVED REGISTER (ADDRESS = 28H)

Return to the SUMMARY TABLE. This register stores the device configuration information.

Table 77. Reserved Field Descriptions

BIT	FIELD	DESCRIPTION
7	RESP_CLK_HALF	Reduce respiration clock speed to half 0 = Respiration clock can be 32k / 64k. 1 = Respiration clock can be 16k / 32k.
6:0	Reserved(7:0)	Must write 04h

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12. APPLICATION AND IMPLEMENTATION

NOTE

The information provided in this section is not part of the AnalogySemi component specification. Hence, AnalogySemi does not warrant its completeness or accuracy. Customers are responsible for determining suitability of components and system functionality for their applications. Validation and testing should be performed prior to design implementation.

12.1 APPLICATION INFORMATION

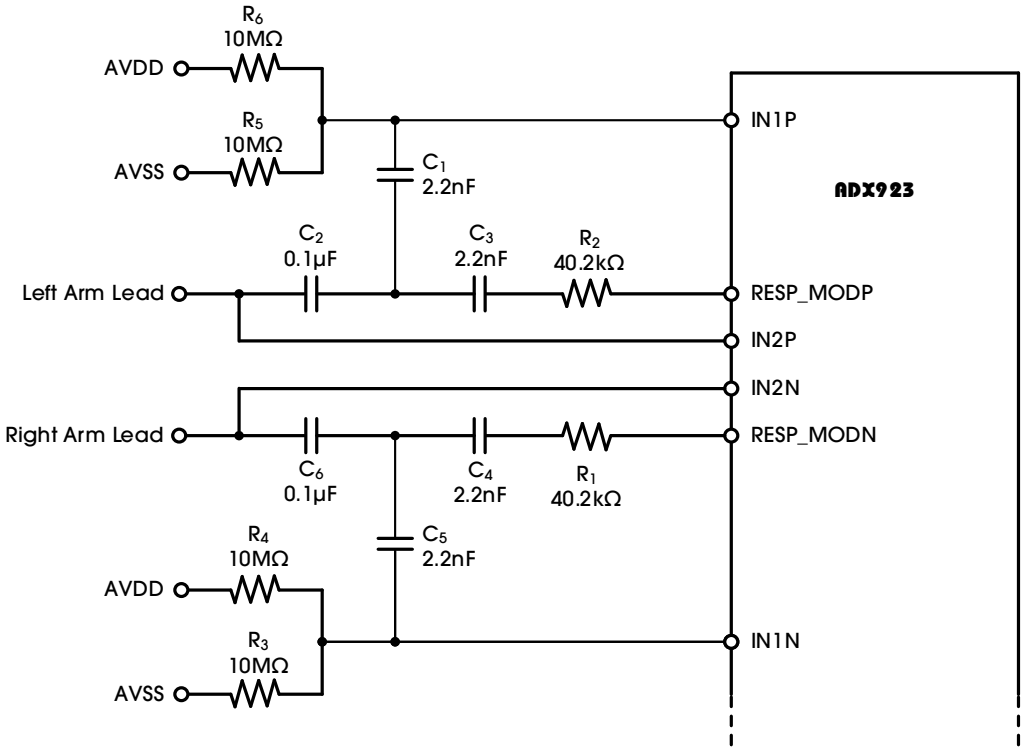
The ADX920/1/2/3 devices incorporate all features commonly required in a low-power medical electrocardiogram (ECG) application.

The ADX920/1/2/3 devices have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and lead-off detection. Additionally, any configuration of input channels can be selected for derivation of the right leg drive (RLD) output signal. Lead-off detection can be implemented internal to the device, using the device internal excitation current sink or source. The ADX923 version includes a fully integrated respiration impedance measurement function.

12.2 TYPICAL APPLICATION

A typical application for the ADX923 is the acquisition of ECG signals in combination with a respiration impedance measurement.

The ADX923 channel 1 with respiration enabled mode cannot be used to acquire ECG signals. If the right arm (RA) and left arm (LA) leads are intended to measure respiration and ECG signals, the two leads can be wired into channel 1 for respiration and channel 2 for ECG signals, as shown in Figure 65.



NOTE: Patient and input protection circuitry not shown.

Figure 65. Typical Respiration Circuitry

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12.2.1 DESIGN REQUIREMENTS

This design requires the measurement of respiration and ECG signals on the right arm (RA) and left arm (LA) with very low noise. Standard requirements are respiration impedance values ranging from 2kΩ to 15kΩ, modulation clock frequencies of 32kHz or 64kHz, and noise levels of less than 10μV.

12.2.2 RESPIRATION NOISE TEST CIRCUIT

Figure 66 shows a respiration noise test circuit.

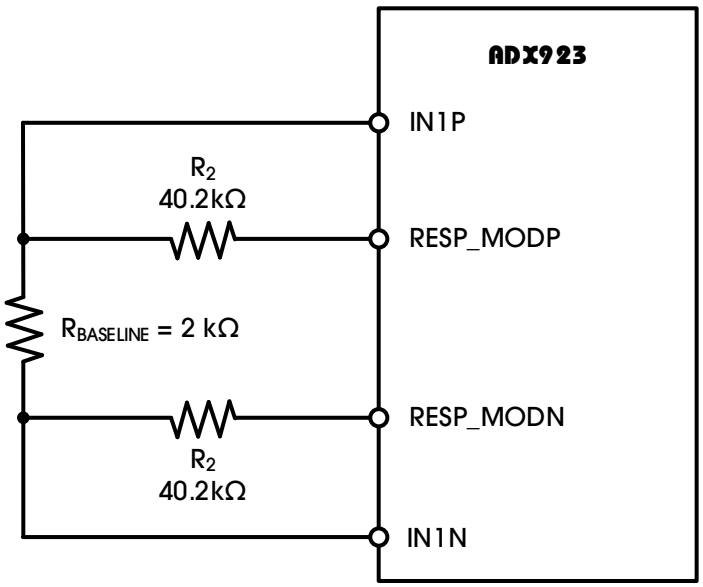

Figure 66. Respiration Noise Test Circuit

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13. POWER SUPPLY RECOMMENDATIONS

The nominal performance of the device is specified with an analog supply voltage AVDD of 3V and an internal reference voltage VREFP of 2.4V. The device also operates using power supplies at the AVDD pin from 2.7V to 5.5V with excellent performance.

13.1 POWER-SUPPLY SEQUENCING

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 67. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed, see the CONFIG1 register for details. The power-up sequence timing is shown in Table 78.

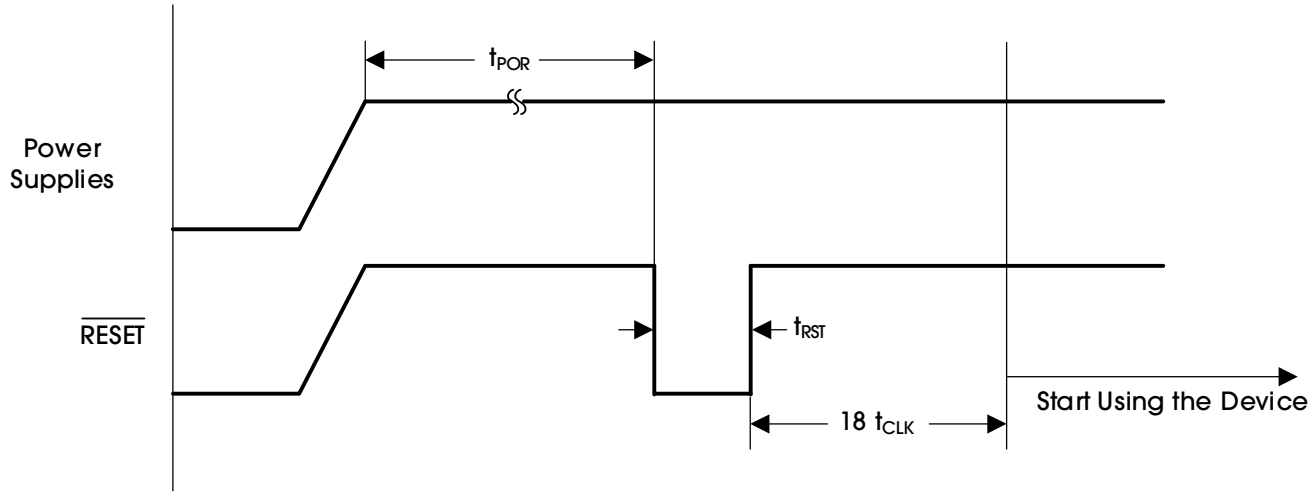

Figure 67. Power-Up Timing Diagram

Table 78. Power-Up Sequence Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Wait after Power-Up until Reset	t_{POR}	2^{12}			t_{MOD}
Reset Low Width	t_{RST}	1			t_{MOD}

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14. LAYOUT

14.1 LAYOUT GUIDELINES

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices.

Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.

Place the external components as close to the device as possible. Keep the traces as short as possible.

14.1.1 PCB LAYOUT

14.1.1.1 POWER SUPPLIES AND GROUNDING

The ADX920/1/2/3 devices have two supplies: AVDD and DVDD. AVDD should be as quiet as possible. AVDD provides the supply to the charge pump block and has transients at f_{CLK}. It is important to eliminate noise from AVDD that is non-synchronous with the ADX920/1/2/3 operation. Each ADX920/1/2/3 supply should be bypassed with 10μF and a 0.1μF solid ceramic capacitors. It is recommended that placement of the digital circuits (such as the DSP, microcontrollers, and FPGAs) in the system is done so that the return currents on those devices do not cross the ADX920/1/2/3 analog return path. The ADX920/1/2/3 can be powered from unipolar or bipolar supplies.

The capacitors used for decoupling can be of the surface-mount, low-cost, low-profile multi-layer ceramic type. In most cases, the VCAP1 capacitor can also be a multi-layer ceramic, but in systems where the board is subjected to high or low frequency vibration, it is recommended that a non-ferroelectric capacitor such as a tantalum or class 1 capacitor (for example, C0G or NPO) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, X8R, and such) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using internal reference, noise on the VCAP1 node results in performance degradation.

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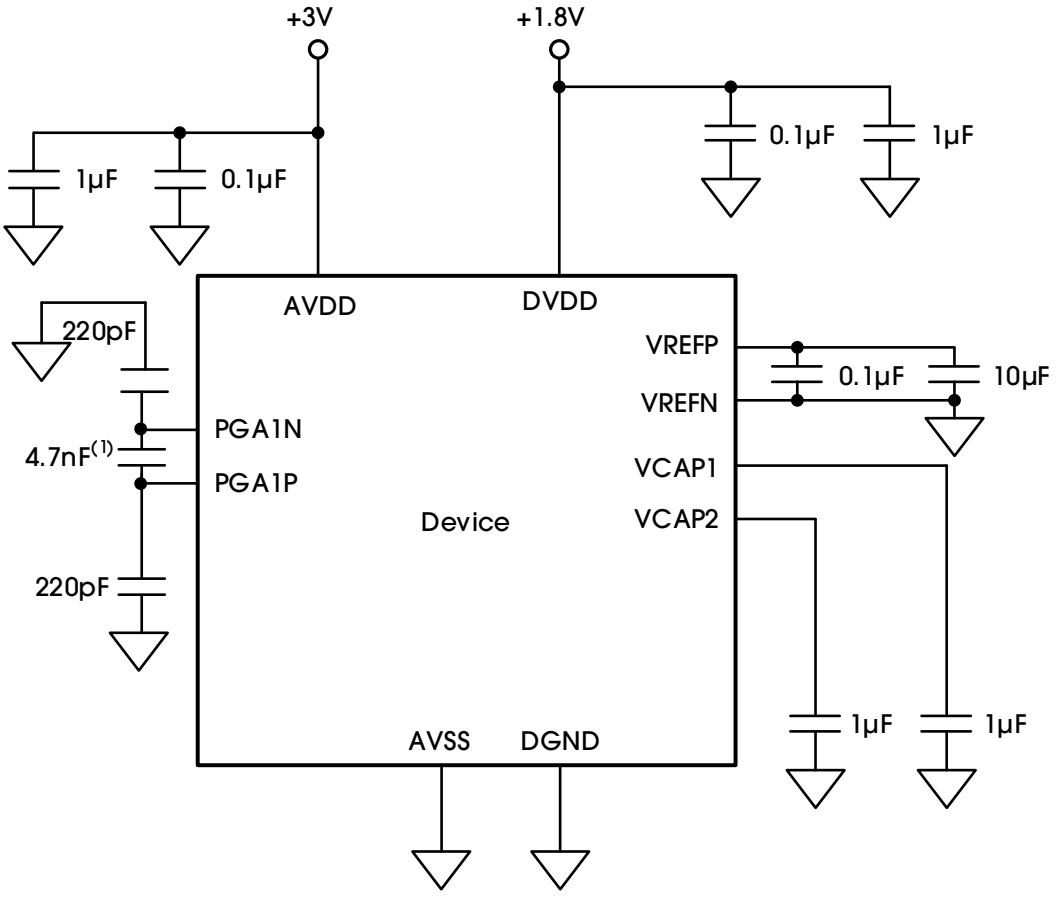
14.1.1.1.1 CONNECTING THE DEVICE TO UNIPOLAR (+3V OR +1.8V) SUPPLIES

Figure 68 shows the ADX920/1/2/3 connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to analog ground (AVSS) and the digital supply (DVDD) is referenced to digital ground (DGND).



(1) This capacitor must be 47nF when using the ADX923 and the channel 1 respiration function. Regarding the capacitors for supply, reference, VCAP1, and VCAP2, place them as close to the package as possible.

Figure 68. Single-Supply Operation

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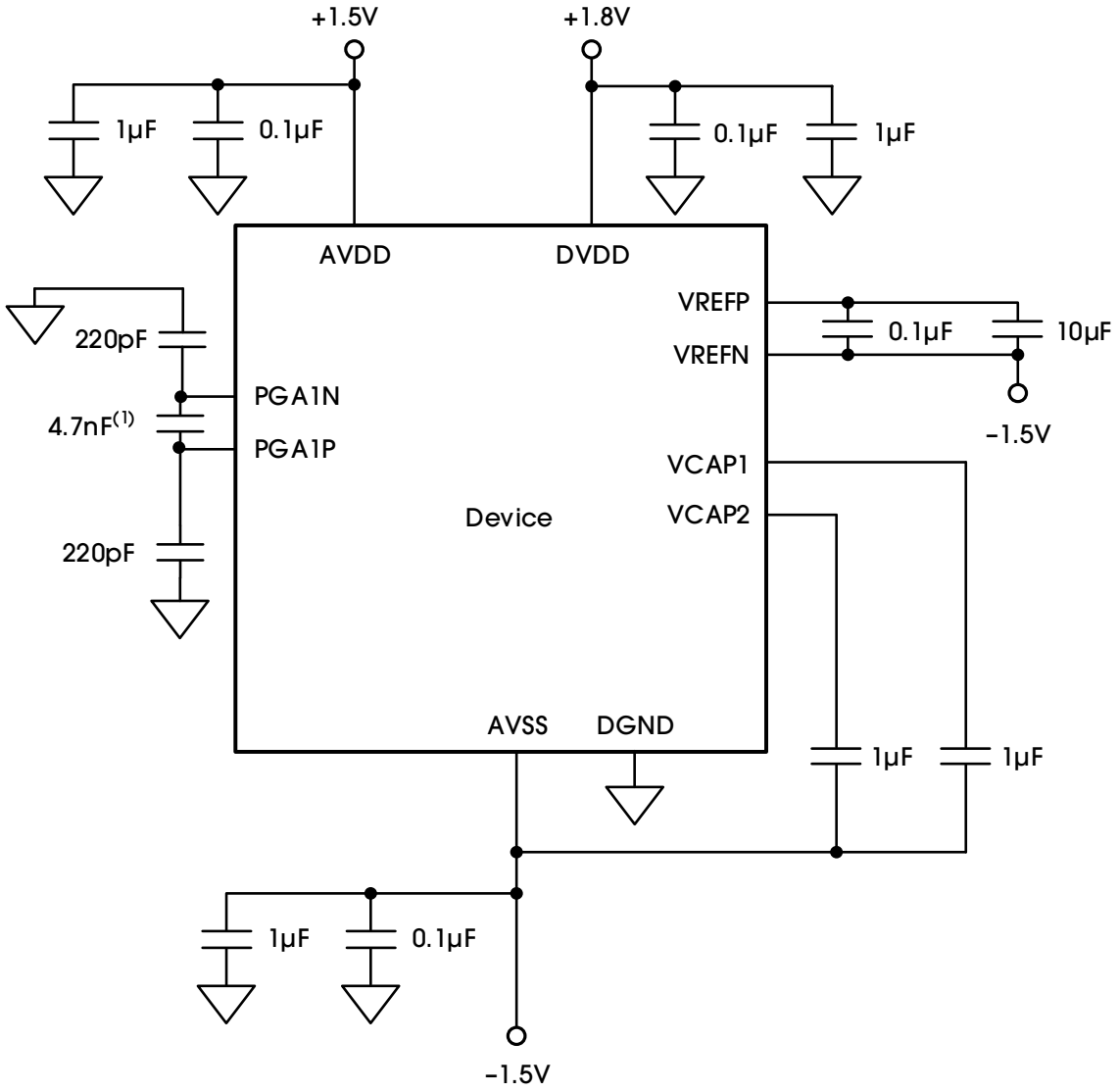
14.1.1.1.2 CONNECTING THE DEVICE TO BIPOLAR (±1.5V OR 1.8V) SUPPLIES

Figure 69 illustrates the ADX920/1/2/3 connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



(1) This capacitor must be 47nF when using the ADX923 and the channel 1 respiration function. Regarding the capacitors for supply, reference, VCAP1, and VCAP2, place them as close to the package as possible.

Figure 69. Bipolar Supply Operation

14.1.1.2 SHIELDING ANALOG SIGNAL PATHS

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the ADX920/1/2/3 input bias current if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

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14.2 LAYOUT EXAMPLE

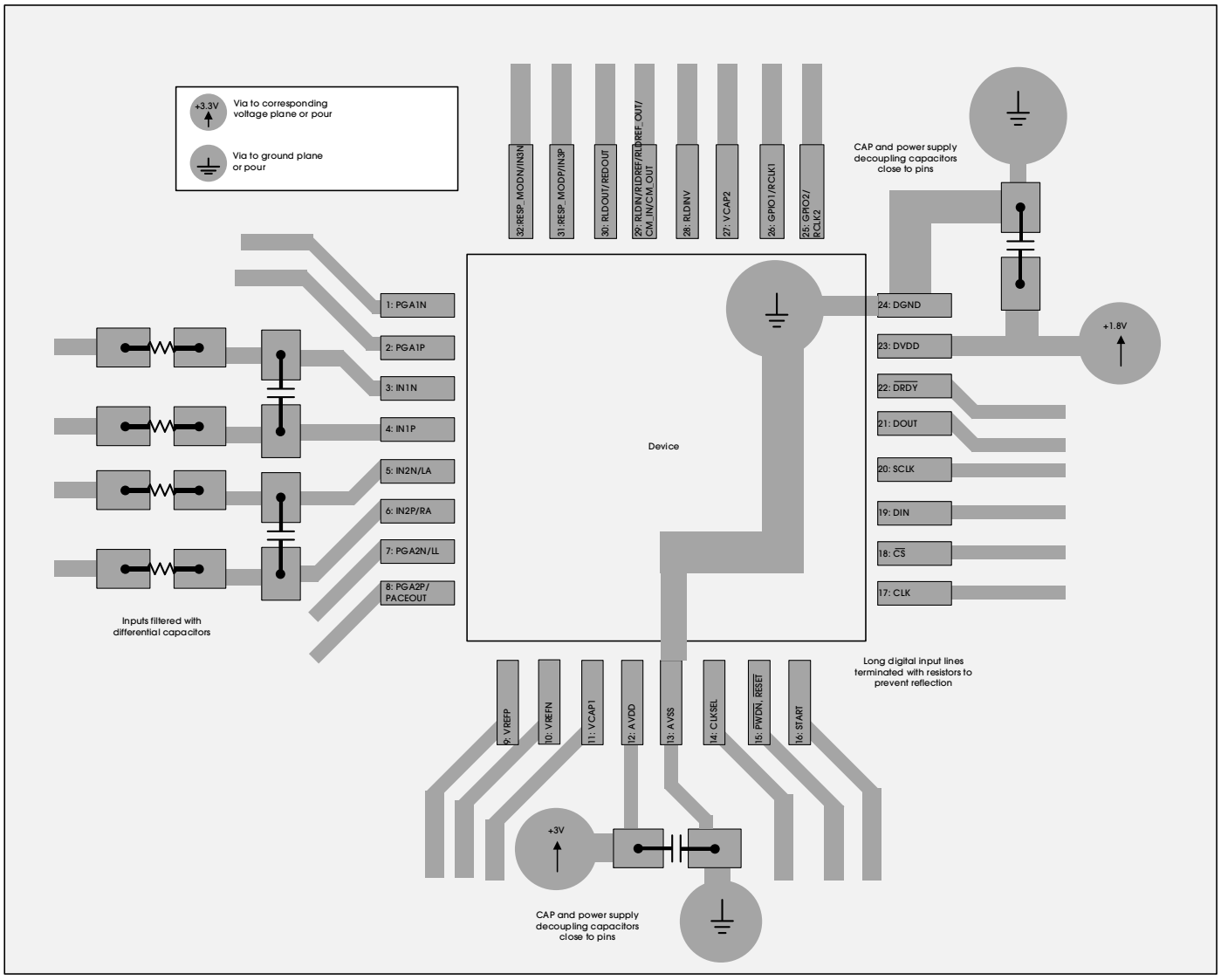

Figure 70. Example PCB Layout for Single-Supply Operation

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15. PACKAGE INFORMATION

The ADX920/1/2/3 is available in the QFN-32 packages. Figure 71 shows the package view.

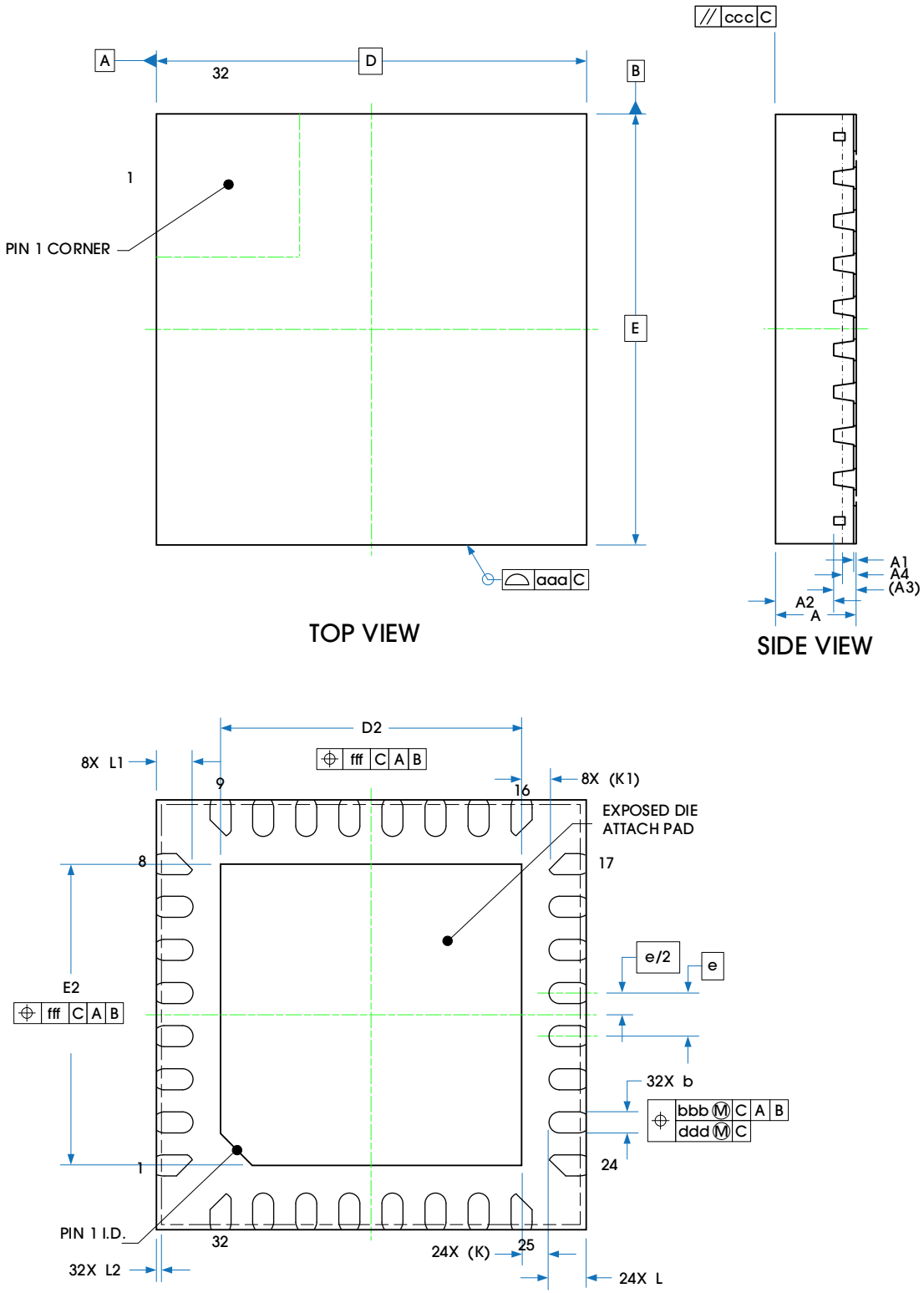

Figure 71. Package View

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Table 79 provides detailed information about the dimensions.

Table 79. Dimensions

PARAMETER		SYMBOL	DIMENSIONS IN MILLIMETERS		
			MIN	NOM	MAX
Total Thickness		A	0.7	0.75	0.8
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	—	0.55	—
L/F Thickness		A3		0.203 REF	
Side Wettable Depth		A4	0.075	—	0.18
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		4 BSC	
	Y	E		4 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
Lead Length		L	0.25	0.35	0.45
		L1	0.235	0.335	0.435
Side Wettable Width		L2	0.01	—	0.09
Lead Tip to Exposed Pad Edge		K		0.25 REF	
		K1		0.265 REF	
Package Edge Tolerance		aaa		0.1	
Mold Flatness		ccc		0.1	
Lead Offset		bbb		0.07	
		ddd		0.05	
Exposed Pad Offset		fff		0.1	

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16. TAPE AND REEL INFORMATION

Figure 72 illustrates the carrier tape.

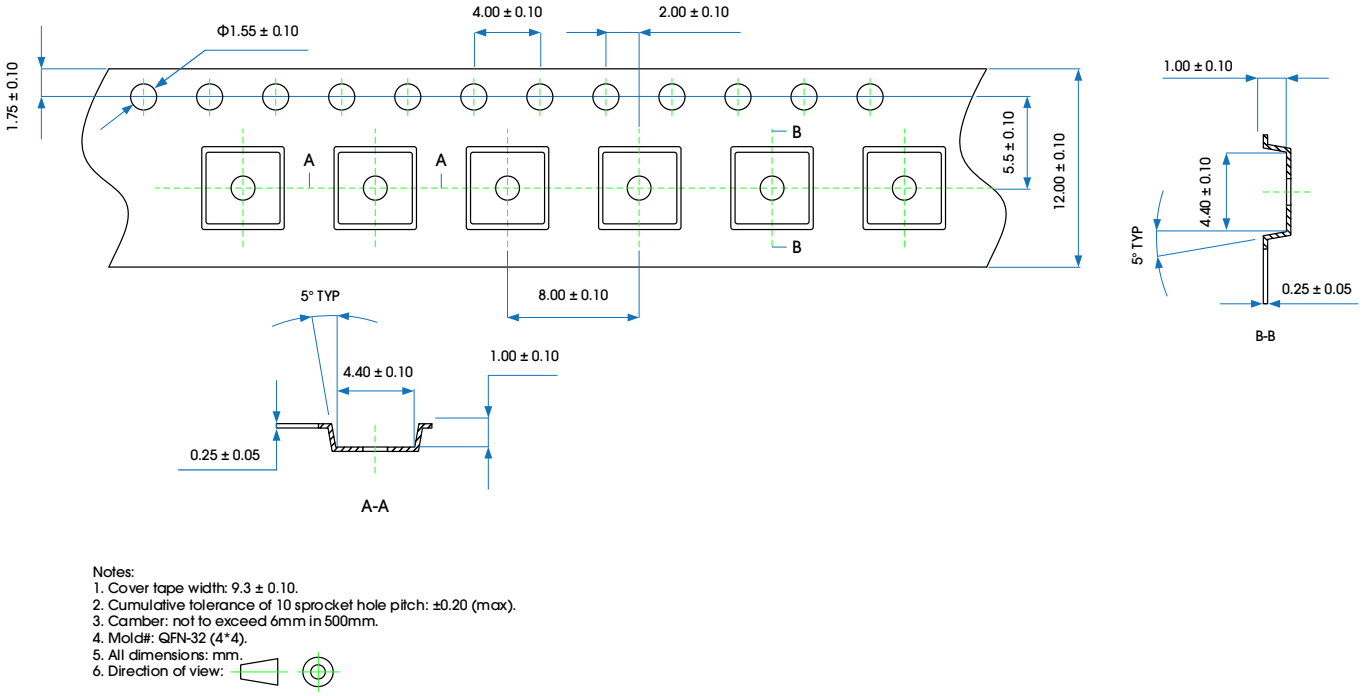

Figure 72. Carrier Tape Drawing

Table 80 provides information about tape and reel.

Table 80. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
QFN-32 4*4	7''	1500	1	20	30000	240*20*265	455*275*255

Figure 73 shows the product loading orientation—pin 1 is assigned at Q2.

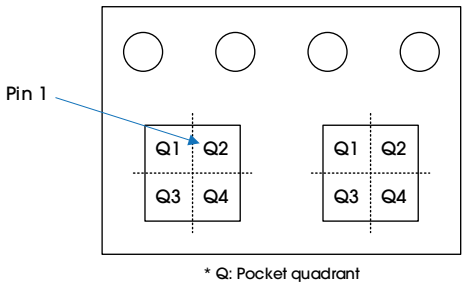

Figure 73. Product Loading Orientation

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REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	02 September 2022	Rev A release.

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