ANALOGYSEMI

1. FEATURES

- Senses bus voltages from 0V to 36V
- High-side or low-side sensing
- Reports current, voltage, and power
- High accuracy:
  - 0.1% gain error (max)
  - 2.5µV offset (max)
- Configurable averaging options
- 16 programmable addresses
- Operates from 2.7V to 5.5V power supply
- MSOP-10 package

2. APPLICATIONS

- Servers
- Telecom equipment
- Computing
- Power management
- Battery chargers
- Power supplies
- Test equipment

3. DESCRIPTION

The CSD202 senses the bi-directional current on a high common-mode bus and monitors the bus voltage with an I2C™- or SMBUS-compatible digital interface. The programmable calibration value, conversion times, averaging, and an internal multiplier make it easy to read out current, bus voltage, and power values directly from registers.

The CSD202 senses current on common-mode bus voltages that can vary from 0V to 36V, independent of the supply voltage. The device operates from a single 2.7V to 5.5V supply, drawing a typical of 340µA of supply current. The device is specified over the operating temperature range between –40°C and 125°C and features up to 16 programmable addresses on the I2C-compatible interface. See Table 1 for the order information.
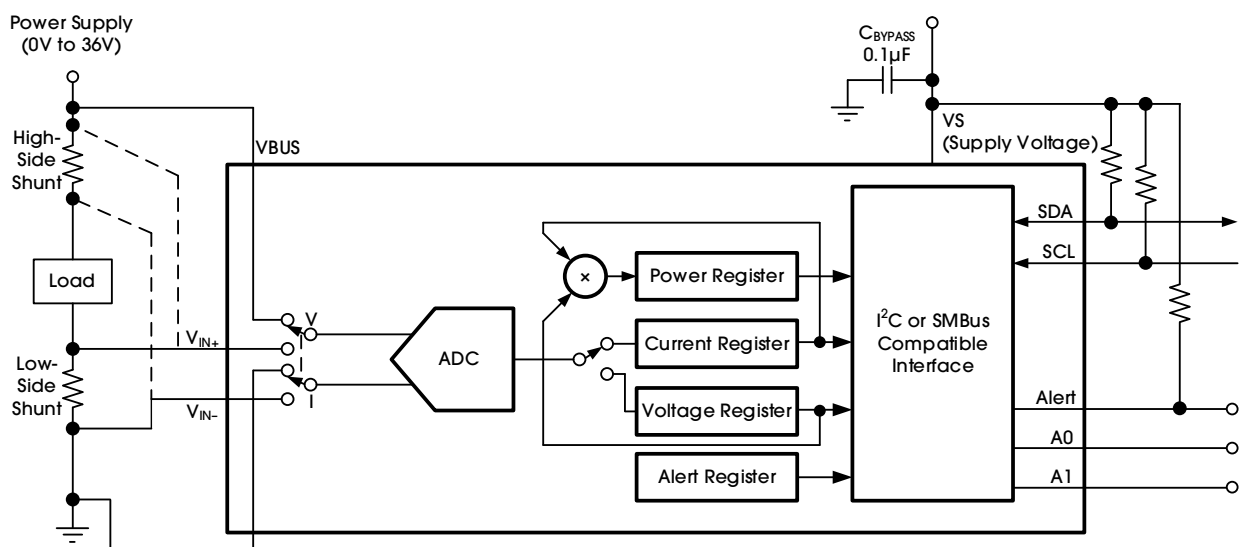

High-Side or Low-Side Sensing Application

Table 1 lists the order information.

Table 1. Order Information

| ORDER NUMBER[1]	PART NUMBER	BITS (#)	PACKAGE	MARKING	INTERFACE	V_{CM} (V)	TEMP SENSOR LP MODE ALERT	OP. TEMP (°C)	RATING	PKG. OPTION
CSD202CMSOP10	CSD202	16	MSOP-10	CSD202	I²C	0-36	No	–40-125	Industry	T/R-3000

Table 2. Family Selection Guide

ORDER NUMBER[1]	PART NUMBER	BITS (#)	PACKAGE	MARKING	INTERFACE	V_{CM} (V)	TEMP SENSOR LP MODE ALERT	OP. TEMP (°C)	RATING	PKG. OPTION
CSD201CMSOP10	CSD201	12	MSOP-10	CSD201	I²C	0-26	No	–40-125	Industry	T/R-3000
CSD203LDMSOP10	CSD203L	16	MSOP-10	CSD203L	I²C	0-36	Yes	–40-125	Industry	T/R-3000
CSD203MDMSOP10	CSD203M	20	MSOP-10	CSD203M	I²C	0-36	Yes	–40-125	Industry	T/R-3000
CSD203HDMSOP10	CSD203H	16	MSOP-10	CSD203H	I²C	0-65	Yes	–40-125	Industry	T/R-3000
CSD203PDMSOP10	CSD203P	20	MSOP-10	CSD203P	I²C	0-65	Yes	–40-125	Industry	T/R-3000
CSD204LDMSOP10	CSD204L	16	MSOP-10	CSD204L	I²C	–5-65	Yes	–40-125	Industry	T/R-3000
CSD204MDMSOP10	CSD204M	20	MSOP-10	CSD204M	I²C	–5-65	Yes	–40-125	Industry	T/R-3000
CSD205LDMSOP10	CSD205L	16	MSOP-10	CSD205L	SPI	0-36	Yes	–40-125	Industry	T/R-3000
CSD205MDMSOP10	CSD205M	20	MSOP-10	CSD205M	SPI	0-36	Yes	–40-125	Industry	T/R-3000
CSD205HDMSOP10	CSD205H	16	MSOP-10	CSD205H	SPI	0-65	Yes	–40-125	Industry	T/R-3000
CSD205PDMSOP10	CSD205P	20	MSOP-10	CSD205P	SPI	0-65	Yes	–40-125	Industry	T/R-3000
CSD206LDMSOP10	CSD206L	16	MSOP-10	CSD206L	SPI	–5-65	Yes	–40-125	Industry	T/R-3000
CSD206MDMSOP10	CSD206M	20	MSOP-10	CSD206M	SPI	–5-65	Yes	–40-125	Industry	T/R-3000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note:

Order Number

CSD20x(X)-Package Code

Device

V_{CM} & Accuracy

Package Code
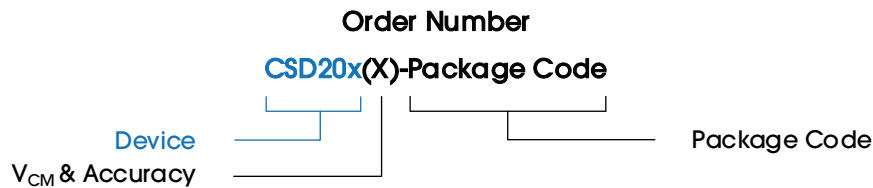
4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.
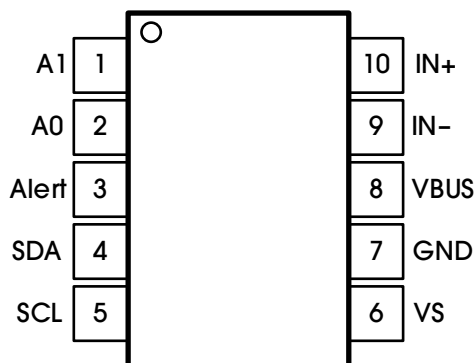
Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

PIN	POSITION	TYPE	DESCRIPTION
A1	1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 9 shows pin settings and corresponding addresses.
A0	2	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 9 shows pin settings and corresponding addresses.
Alert	3	Digital output	Multi-functional alert, open-drain output
SDA	4	Digital I/O	Serial bus data line, open-drain input/output
SCL	5	Digital input	Serial bus clock line, open-drain input
VS	6	Analog	Power supply, 2.7V to 5.5V
GND	7	Analog	Ground
VBUS	8	Analog input	Bus voltage input
IN–	9	Analog input	Connect to load side of shunt resistor
IN+	10	Analog input	Connect to supply side of shunt resistor

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the CSD202. Over operating free-air temperature range, unless otherwise noted.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Supply, V_{VS}			6	V
	Analog inputs, IN+, IN–	Differential $(V_{IN+} - V_{IN-})$[2]	–40	40	V
		Common-Mode $(V_{IN+} + V_{IN-})$ / 2	–0.3	40	
	V_{VBUS}		–0.3	40	V
	V_{SDA}		GND – 0.3	6	V
	V_{SCL}		GND – 0.3	V_{VS} + 0.3	V
Current	Input current into any pin, I_{IN}			5	mA
	Open-drain digital output current, I_{OUT}			10	mA
Temperature	Junction, T_J			150	°C
	Storage, T_{stg}		–65	150	°C

Note 1: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: IN+ and IN– may have a differential voltage of –40V to 40V; however, the voltage at these pins must not exceed the range of –0.3V to 40V.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the CSD202.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±2000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the CSD202. Over operating free-air temperature range, unless otherwise noted.

Table 6. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Common-Mode Input Voltage	V_{CM}		12		V
Operating Supply Voltage	V_{VS}	2.7	3.3	5.5	V
Operating Free-Air Temperature	T_A	−40		125	°C

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the CSD202.

Table 7. Thermal Information

PARAMETER	SYMBOL	MSOP-10	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	171.4	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	42.9	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	91.8	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	1.5	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	90.2	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	—	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of CSD202. T_A = 25°C, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} − V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
Shunt Voltage Input Range			−81.69		81.69	mV
Bus Voltage Input Range[1]			0		36	V
Common-Mode Rejection	CMRR	0V ≤ V_{IN+} ≤ 36V	140	160		dB
Shunt Offset Voltage, RTI[2]	VOS			±1	±2.5	µV
Shunt Offset Voltage, RTI[2] vs. Temperature		−40°C ≤ T_A ≤ 125°C		0.02	0.1	µV/°C
Shunt Offset Voltage, RTI[2] vs. Power Supply	PSRR	2.7 ≤ V_S ≤ 5.5V		1		µV/V
Bus Offset Voltage, RTI[2]	V_{OS}			±1.25	±1.5	mV
Bus Offset Voltage, RTI[2] vs. Temperature		−40°C ≤ T_A ≤ 125°C		10	40	µV/°C
Bus Offset Voltage, RTI[2] vs. Power Supply	PSRR			0.5		mV/V
Input Bias Current (I_{IN+}, I_{IN-} Pins)	I_B			0.2	5	µA
VBUS Input Impedance				750		kΩ
Input Leakage[3]		(IN+ pin) + (IN− pin), power-down mode		0.1	0.5	µA
DC ACCURACY						
ADC Native Resolution				16		Bits
1 LSB Step Size		Shunt voltage		2.5		µV
		Bus voltage		1.25		mV
Shunt Voltage Gain Error				0.01%	0.1%	
Shunt Voltage Gain Error vs. Temperature		−40°C ≤ T_A ≤ 125°C		3	20	ppm/°C
Bus Voltage Gain Error				0.01%	0.1%	
Bus Voltage Gain Error vs. Temperature		−40°C ≤ T_A ≤ 125°C		4.5	20	ppm/°C
Differential Nonlinearity				±0.1		LSB
ADC Conversion Time	t_{CT}	CT bit = 000		140	154	µs
		CT bit = 001		204	224	
		CT bit = 010		332	365	
		CT bit = 011		588	646	
		CT bit = 100		1.1	1.21	ms
		CT bit = 101		2.116	2.328	
		CT bit = 110		4.156	4.572	
		CT bit = 111		8.244	9.068	
SMBUS						
SMBus Timeout[4]				28	35	ms
DIGITAL INPUT/OUTPUT						
Input Capacitance				3		pF
Leakage Input Current		0V ≤ V_{SCL} ≤ V_{VS}, 0V ≤ V_{SDA} ≤ V_{VS}, 0V ≤ V_{Alert} ≤ V_{VS}, 0V ≤ V_{A0} ≤ V_{VS}, 0V ≤ V_{A1} ≤ V_{VS}		0.1	1	µA
High-Level Input Voltage	V_{IH}		0.7 × V_{VS}		6	V
Low-Level Input Voltage	V_{IL}		−0.5		0.3 × V_{VS}	V
Low-Level Output Voltage, SDA, Alert	V_{OL}	I_{OL} = 3mA	0		0.4	V
Hysteresis				500		mV
POWER SUPPLY						
Operating Supply Range			2.7		5.5	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I_Q			330	360	µA
Quiescent Current, Power-Down (Shutdown) Mode				0.1	0.5	µA
Power-On Reset Threshold	V_{POR}			2.1		V

Note 1: While the input range is 36V, the full-scale range of the ADC scaling is 40.96V. See the BASIC ADC FUNCTIONS section. Do not apply more than 36V.

Note 2: RTI = Referred-to-input.

Note 3: Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

Note 4: SMBus timeout in the CSD202 resets the interface any time SCL is low for more than 28ms.

6. TYPICAL CHARACTERISTICS

T_A = 25°C, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} − V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.
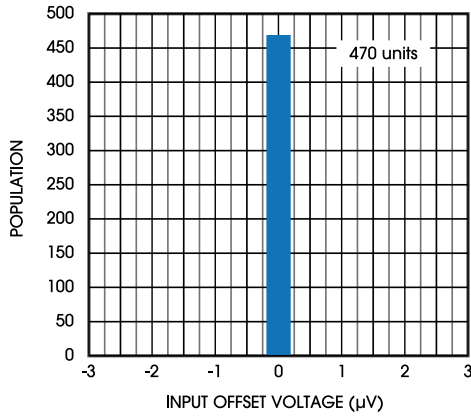
Figure 2. Shunt Input Offset Voltage Production Distribution
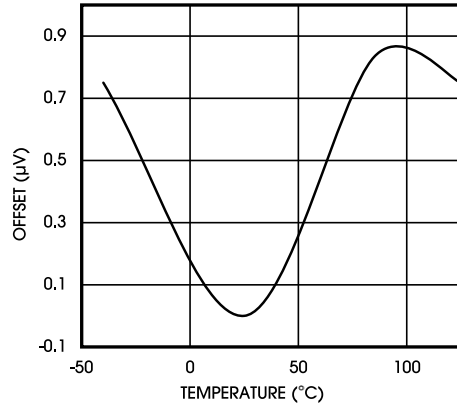
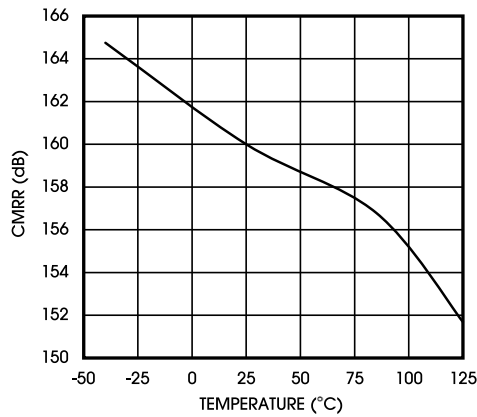Figure 3. Shunt Input Offset Voltage vs. Temperature

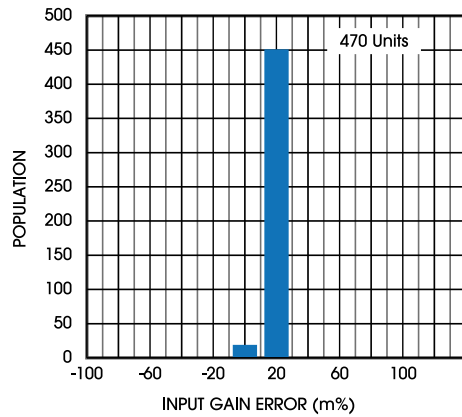Figure 4. Shunt Input Common-Mode Rejection Ratio vs. Temperature

Figure 5. Shunt Input Gain Error Production Distribution
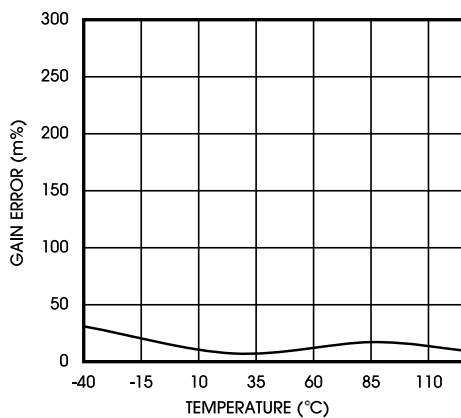
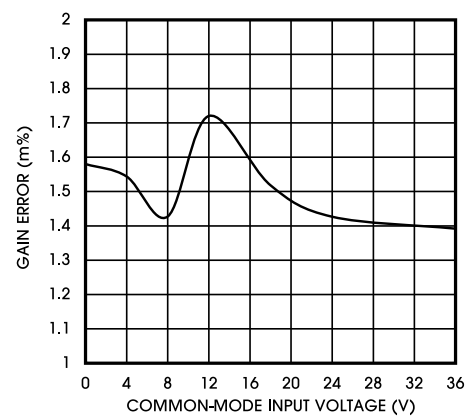Figure 6. Shunt Input Gain Error vs. Temperature

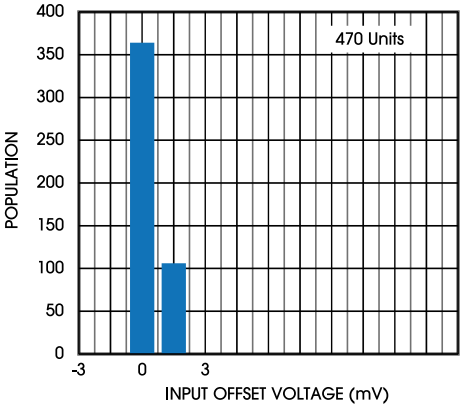Figure 7. Shunt Input Gain Error vs. Common-Mode Voltage

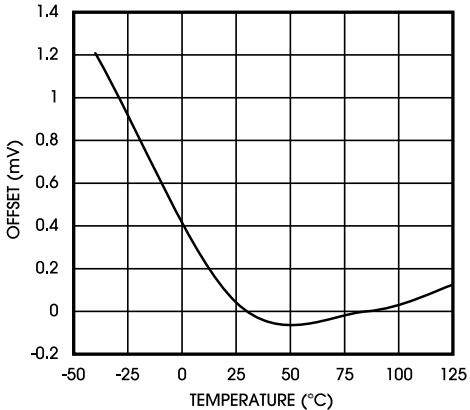Figure 8. Bus Input Offset Voltage Production Distribution

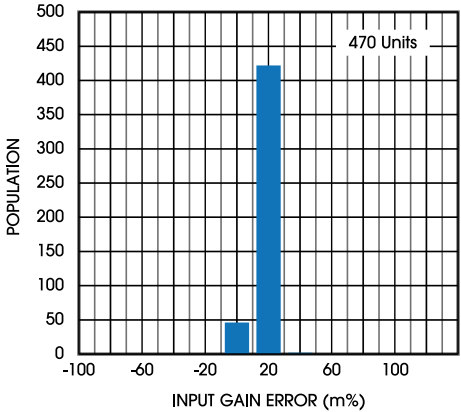Figure 9. Bus Input Offset Voltage vs. Temperature

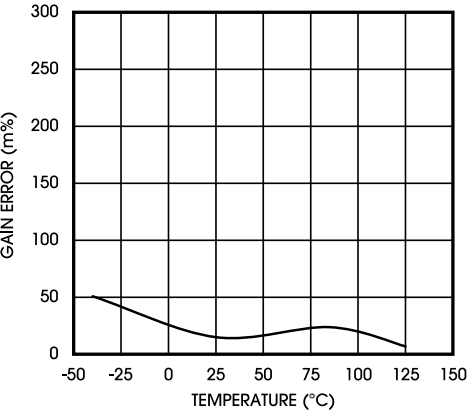Figure 10. Bus Input Gain Error Production Distribution

Figure 11. Bus Input Gain Error vs. Temperature
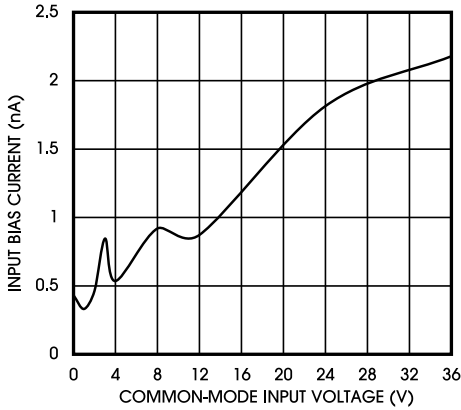
Figure 12. Input Bias Current vs. Common-Mode Voltage
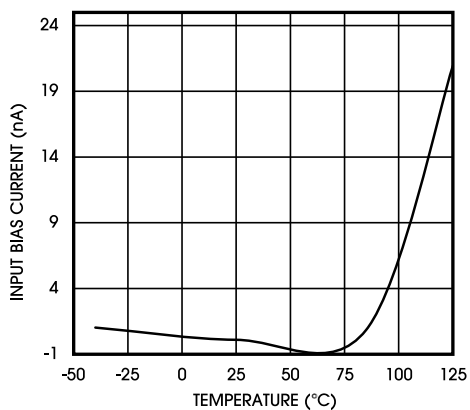
Figure 13. Input Bias Current vs. Temperature
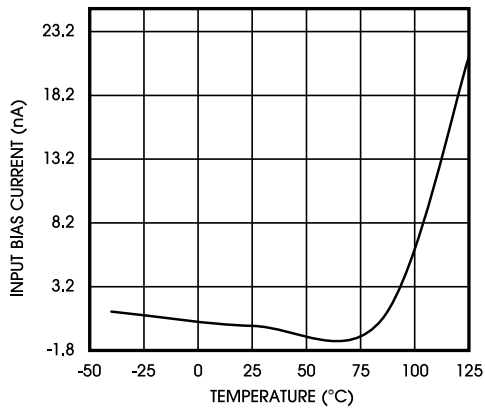
Figure 14. Input Bias Current vs. Temperature, Shutdown
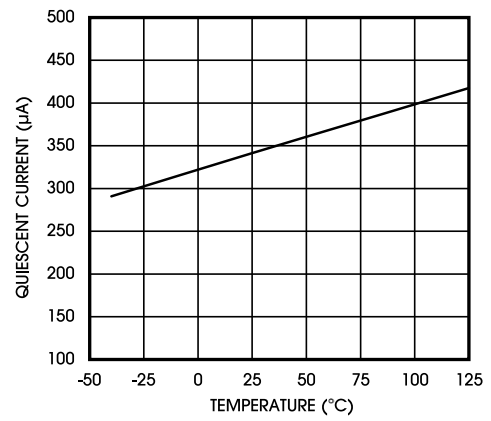
Figure 15. Active I_Q vs. Temperature
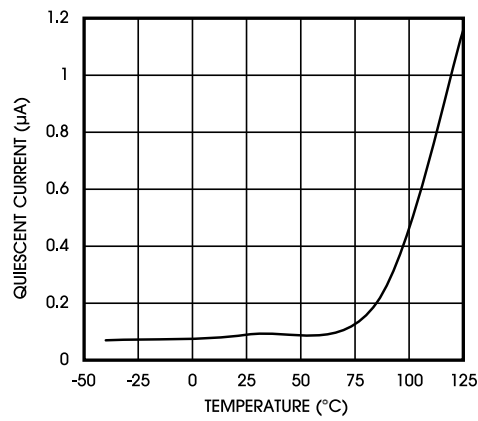
Figure 16. Shutdown I_Q vs. Temperature

7. DETAILED DESCRIPTION

7.1 OVERVIEW

The CSD202 is a digital current sense amplifier with an I²C- and SMBus-compatible interface. The programmable calibration value, conversion times, averaging, and an internal multiplier make it easy to read out current, bus voltage, and power values directly from registers, which is suitable for accurate decision-making system. Detailed register information appears at the end of this datasheet, beginning with Table 12.

7.2 FUNCTIONAL BLOCK DIAGRAM

(1) Read-only
(2) Read/write
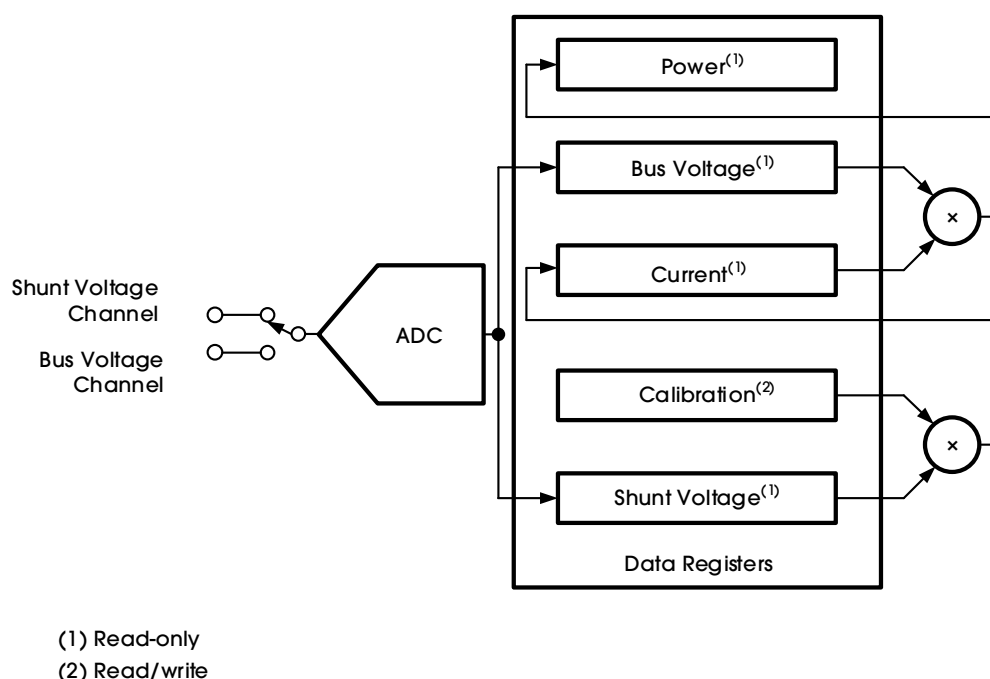
Figure 17. Functional Block Diagram

7.3 FEATURE DESCRIPTION

7.3.1 BASIC ADC FUNCTIONS

The CSD202 performs two measurements: the load current that flows through a shunt resistor at IN+ and IN-; the power supply voltage connected to the VBUS pin. The differential shunt voltage is measured with respect to the IN– pin while the bus voltage is measured with respect to ground.

The CSD202 is powered by a separate 2.7V to 5.5V supply while the bus voltage that is being monitored ranges from 0V to 36V. The full-scale register results is 40.96V with a fixed 1.25mV LSB. There is no sequence requirement for power supply and bus voltage as they are independent of each other. Bus voltage can be present with power supply ON or OFF, and vice versa.

NOTE
Do not apply more than 36V of actual voltage to the input pins.

The device takes two measurements, shunt voltage, and bus voltage. It then converts these measurements to current, based on the Calibration Register value, and then calculates power. Refer to the PROGRAMMING THE CALIBRATION REGISTER section for additional information on programming the Calibration Register.

The device has two operating modes, continuous and triggered. In continuous operating mode (MODE bits of the Configuration Register (00h) are set to '111'), it continuously converts a shunt voltage followed by bus voltage. Just after the shunt voltage reading, current value is calculated based on Equation 3. This current value is then used to calculate the power result with Equation 4. The measurement/calculation sequence repeats until the number of averages set in the Configuration Register (00h) is reached. After each sequence, append the currently measured and calculated set of values to the previously collected values. After all averaging is done, the final values of shunt voltage, bus voltage, current and power are updated in the corresponding registers and can then be read. These values remain in the data output registers until they are replaced by the result of the next fully completed conversion. Reading the data output registers will not affect ongoing conversions.

The mode control in the Conversion Register (00h) allows to convert only shunt voltage or bus voltage, which is flexible for various application requirements. All current and power calculations are in background and do not contribute to conversion time.

In triggered mode, writing any of the triggered convert modes into the Configuration Register (00h) (that is, MODE bits of the Configuration Register (00h) are set to '001', '010', or '011') triggers a single-shot conversion. This action produces only a single set of measurements. If a second single-shot conversion is needed, the Configuration Register (00h) must be written to a second time, even if the mode does not change.

In addition to the two operating modes (continuous and triggered), the device also has a power-down mode that reduces the quiescent current and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. Full recovery from power-down mode requires 40µs. The registers of the device can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active modes settings are written into the Configuration Register (00h).

Although the device can be read at any time, and the data from the last conversion remain available, the Conversion Ready flag bit (Mask/Enable Register, CVRF bit) is provided to help coordinate one-shot or triggered conversions. The Conversion Ready flag (CVRF) bit is set after all conversions, averaging, and multiplication operations are completed.

The Conversion Ready flag (CVRF) bit clears under these conditions:

- Writing to the Configuration Register (00h), except when configuring the MODE bits for power-down mode; or

- Reading the Mask/Enable Register (06h).

7.3.1.1 POWER CALCULATION

The Current and Power are calculated following shunt voltage and bus voltage measurements as shown in Figure 18. Current is calculated following a shunt voltage measurement based on the value set in the Calibration Register. If no value is loaded into the Calibration Register, the current value stored is zero. Power is calculated following the bus voltage measurement based on the previous current calculation and bus voltage measurement. If no value is loaded in the Calibration Register, the power value stored is also zero. Again, these calculations are performed in the background and do not add to the overall conversion time. These current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register, not the corresponding output registers. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged based on the number of averages set in the Configuration Register (00h).
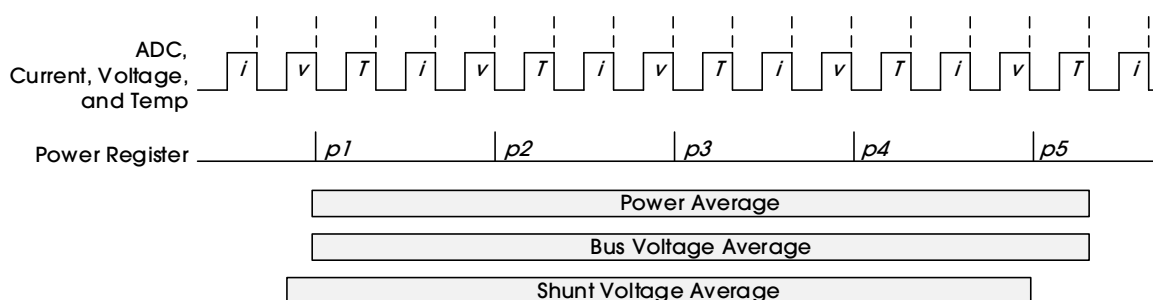
Figure 18. Power Calculation Scheme

In addition to the current and power accumulating after every sample, the shunt and bus voltage measurements are also collected. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers, where they can then be read.

7.3.1.2 ALERT PIN

The CSD202 has an Alert Limit Register (07h) for the Alert pin to be programmed to respond to a single user-defined event or to a Conversion Ready notification. Customer can select from one of the five available functions via the Mask/Enable register for monitoring and/or setting the Conversion Ready bit to control the response of the Alert pin. Based on monitored function, the user would then enter a value into the Alert Limit register to set the corresponding threshold value that asserts the Alert pin.

The Alert pin can monitor one of several available alert functions to determine whether a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt Voltage Over-Limit (SOL)
- Shunt Voltage Under-Limit (SUL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

The Alert pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable Register exceeds the value programmed into the Alert Limit Register. Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit Register value. For example, if the Shunt Voltage Over-Limit function and the Shunt Voltage Under-Limit function are both selected, the Alert pin asserts when the Shunt Voltage Register exceeds the value in the Alert Limit Register.

The Conversion Ready state of the device can also be monitored at the Alert pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. Conversion Ready can be monitored at the Alert pin along with one of the alert functions. If an alert function and the Conversion Ready are both enabled to be monitored at the Alert pin, after the Alert pin is asserted, the Mask/Enable Register must be read following the alert to determine the source of the alert. By reading the Conversion Ready Flag (CVRF, bit 3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register, the source of the alert can be determined.

If the alert function is not used, the Alert pin can be left floating without impacting the operation of the device.

Refer to Figure 18 to see the relative timing of when the value in the Alert Limit Register is compared to the corresponding converted value. For example, if the alert function that is enabled is Shunt Voltage Over-Limit (SOL), following every shunt voltage conversion the value in the Alert Limit Register is compared to the measured shunt voltage to determine if the measurements has exceeded the programmed limit. The AFF, bit 4 of the Mask/Enable Register, asserts high any time the measured voltage exceeds the value programmed into the Alert Limit Register. In addition to the AFF being asserted, the Alert pin is asserted based on the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch is enabled, the AFF and Alert pin remain asserted until either the Configuration Register (00h) is written to or the Mask/Enable Register is read.

The Bus Voltage alert functions compare the measured bus voltage to the Alert Limit Register following every bus voltage conversion and assert the AFF bit and Alert pin if the limit threshold is exceeded.

The Power Over-Limit alert function is also compared to the calculated power value following every bus voltage measurement conversion and asserts the AFF bit and Alert pin if the limit threshold is exceeded.

7.4 DEVICE FUNCTIONAL MODES

7.4.1 AVERAGING AND CONVERSION TIME CONSIDERATIONS

The CSD202 device offers programmable conversion times (t_{CT}) for both the shunt voltage and bus voltage measurements. The conversion times for these measurements can be selected from as fast as 140µs to as long as 8.244ms. The conversion time settings, along with the programmable averaging mode, allow the device to be configured to optimize the available timing requirements in a given application. For example, if a system requires that data be read every 5ms, the device could be configured with the conversion times set to 588µs for both shunt and bus voltage measurements and the averaging mode set to 4. This configuration results in the data updating approximately every 4.7ms. The device could also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation can allow for the time focused on the bus voltage measurement to be reduced relative to the shunt voltage measurement. The shunt voltage conversion time could be set to 4.156ms with the bus voltage conversion time set to 588µs, with the averaging mode set to 1. This configuration also results in data updating approximately every 4.7ms.

There are trade-offs associated with the settings for conversion time and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the device to reduce any noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the device to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an impact on the measurement accuracy. In order to achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on the timing requirements of the system.

7.4.2 FILTERING AND INPUT CONSIDERATIONS

Measuring current is often noisy, and such noise can be difficult to define. The CSD202 device offers several options for filtering by allowing the conversion times and number of averages to be selected independently in the Configuration Register (00h). The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility in configuring the monitoring of the power-supply bus.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500kHz (±10%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1MHz and higher, they can be managed by incorporating filtering at the input of the device. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. In general, filtering the device input is only necessary if there are transients at exact harmonics of the 500kHz (±10%) sampling rate (greater than 1MHz). Filter using the lowest possible series resistance (typically 10Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1µF and 1µF. Figure 18 shows the device with a filter added at the input.

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate 40V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). Removing a short to ground can result in inductive kickbacks that could exceed the 40V differential and common-mode rating of the device. Inductive kickback voltages are best controlled by Zener-type transient-absorbing devices (commonly called transzorbs) combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the device in systems where large currents are available. Testing demonstrates that the addition of 10Ω resistors in series with each input of the device sufficiently protects the inputs against this dV/dt failure up to the 40V rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.
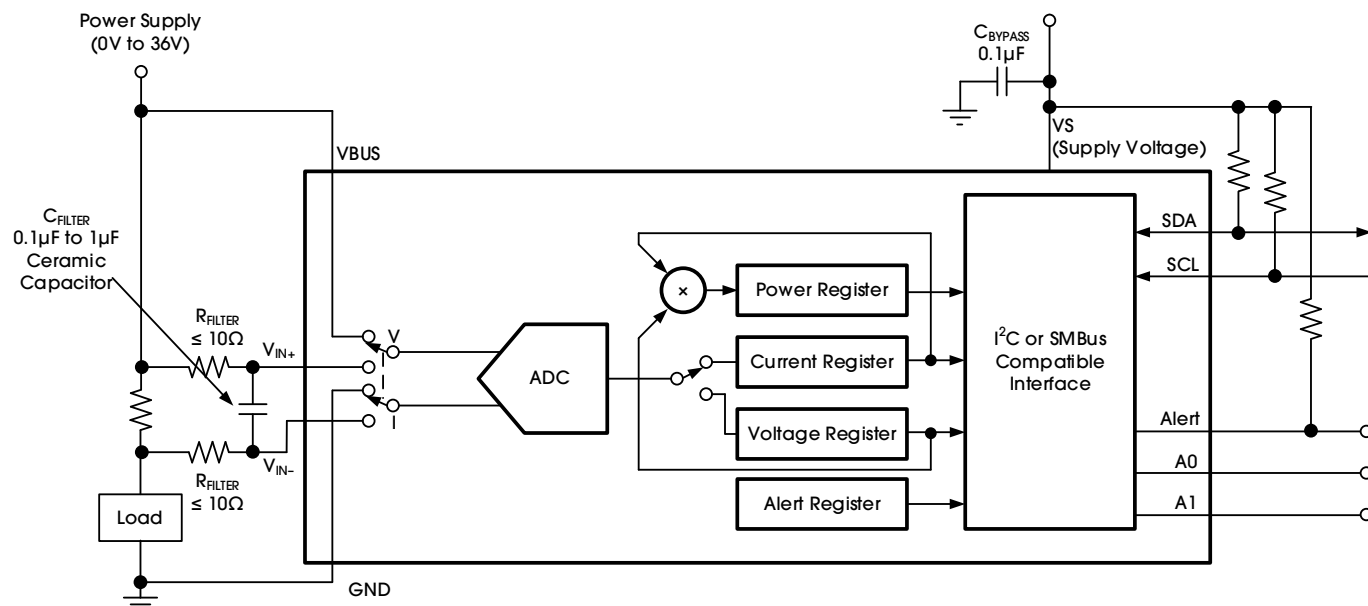

Figure 19. Input Filtering

7.5 PROGRAMMING

An important aspect of the CSD202 device is that it does not necessarily measure current or power. The device measures both the differential voltage applied between the IN+ and IN– input pins and the voltage applied to the VBUS pin. In order for the device to report both current and power values, the user must program the resolution of the Current Register (04h) and the value of the shunt resistor present in the application to develop the differential voltage applied between the input pins. The Power Register (03h) is internally set to be 25 times the programmed Current_LSB. Both the Current_LSB and shunt resistor value are used in the calculation of the Calibration Register value the device uses to calculate the corresponding current and power values based on the measured shunt and bus voltages.

The Calibration Register is calculated based on Equation 1. This equation includes the term Current_LSB, which is the programmed value for the LSB for the Current Register (04h). The user uses this value to convert the value in the Current Register (04h) to the actual current in amperes. The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively. The R_{SHUNT} term is the value of the external shunt used to develop the differential voltage across the input pins.

$$CAL = \frac{0.00512}{CURRENT\_LSB \times R_{SHUNT}} \tag{1}$$

Where:

- 0.00512 is an internal fixed value used to ensure scaling is maintained properly.

$$CURRENT\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \tag{2}$$

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) remain at zero.

7.5.1 PROGRAMMING THE CALIBRATION REGISTER

Figure 25 shows a nominal 10A load that creates a differential voltage of 20mV across a 2mΩ shunt resistor. The bus voltage for the CSD202 is measured at the external VBUS input pin, which in this example is connected to the IN– pin to measure the voltage level delivered to the load. For this example, the VBUS pin measures less than 12V because the voltage at the IN– pin is 11.98V as a result of the voltage drop across the shunt resistor.

For this example, assuming a maximum expected current of 15A, the Current_LSB is calculated to be 457.7µA/bit using Equation 2. Using a value for the Current_LSB of 500µA/Bit or 1mA/Bit would significantly simplify the conversion from the Current Register (04h) and Power Register (03h) to amperes and watts. For this example, a value of 1mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process on the user side. Using Equation 1 in this example with a Current_LSB value of 1mA/bit and a shunt resistor of 2mΩ results in a Calibration Register value of 2560, or A00h.

The Current Register (04h) is then calculated by multiplying the decimal value of the Shunt Voltage Register (01h) contents by the decimal value of the Calibration Register and then dividing by 2048, as shown in Equation 3. For this example, the Shunt Voltage Register contains a value of 8,000 (representing 20mV), which is multiplied by the Calibration Register value of 2560 and then divided by 2048 to yield a decimal value for the Current Register (04h) of 10000, or 2710h. Multiplying this value by 1mA/bit results in the original 10A level stated in the example.

$$CURRENT = \frac{ShuntVoltage \times CalibrationRegister}{2048} \tag{3}$$

The LSB for the Bus Voltage Register (02h) is a fixed 1.25mV/bit, which means that the 11.98V present at the VBUS pin results in a register value of 2570h, or a decimal equivalent of 9584. Note that the MSB of the Bus Voltage Register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

The Power Register (03h) is then calculated by multiplying the decimal value of the Current Register, 10000, by the decimal value of the Bus Voltage Register (02h), 9584, and then dividing by 20,000, as defined in Equation 4. For this example, the result for the Power Register (03h) is 12B8h, or a decimal equivalent of 4792. Multiplying this result by the power LSB (25 times the (1 × 10^{-3} Current_LSB)) results in a power calculation of (4792 × 25mW/bit), or 119.82W. The power LSB has a fixed ratio to the Current_LSB of 25. For this example, a programmed 1mA/bit Current_LSB results in a power LSB of 25mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98V (12V$_{CM}$ – 20mV shunt drop) multiplied by the load current of 10A to give a result of 119.8W.

$$Power = \frac{Current \times BusVoltage}{20,000} \tag{4}$$

Table 9 lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 9. Calculating Current and Power

STEP	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Step 1	Configuration Register	00h	4127h	—	—	—
Step 2	Shunt Register	01h	1F40h	8000	2.5µV	20mV
Step 3	Bus Voltage Register	02h	2570h	9584	1.25mV	11.98V
Step 4	Calibration Register	05h	A00h	2560	—	—
Step 5	Current Register	04h	2710	10000	1mA	10A
Step 6	Power Register	03h	12B8h	4792	25mW	119.82W

Note: Conditions: Load = 10A, V$_{CM}$ = 12V, R$_{SHUNT}$ = 2mΩ, and V$_{VBUS}$ = 12V.

7.5.2 PROGRAMMING THE POWER MEASUREMENT ENGINE

7.5.2.1 CALIBRATION REGISTER AND SCALING

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) to the most useful value for a given application. For example, set the Calibration Register such that the largest possible number is generated in the Current Register (04h) or Power Register (03h) at the expected full-scale point. This approach yields the highest resolution using the previously calculated minimum Current_LSB in the equation for the Calibration Register. The Calibration Register can also be selected to provide values in the Current Register (04h) and Power Register (03h) that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After these choices have been made, the Calibration Register also offers possibilities for end-user system-level calibration. After determining the exact current by using an external ammeter, the value of the Calibration Register can then be adjusted based on the measured current result of the CSD202 to cancel the total system error as shown in Equation 5.

$$Corrected\_Full\_Scale\_Cal = trunc \left[\frac{Cal \times MeasShuntCurrent}{CSD202\_Current} \right] \tag{5}$$

7.5.3 SIMPLE CURRENT SHUNT MONITOR USAGE (NO PROGRAMMING NECESSARY)

The device can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default power-on reset configuration and continuous conversion of shunt and bus voltages.

Without programming the device Calibration Register, the device is unable to provide either a valid current or power value, because these outputs are both derived using the values loaded into the Calibration Register.

7.5.4 DEFAULT SETTINGS

The default power-up states of the registers are shown in the REGISTER MAPS section of this datasheet. These registers are volatile, and if programmed to a value other than the default values shown in Table 12, they must be re-programmed at every device power-up. Detailed information on programming the Calibration Register specifically is given in the PROGRAMMING section and calculated based on Equation 1.

7.5.5 BUS OVERVIEW

The CSD202 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another.

The I²C interface is used throughout this datasheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two lines, SCL and SDA, connect the device to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

After all data have been transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The device includes a 28ms timeout on its interface to prevent locking up the bus.

7.5.5.1 SERIAL BUS ADDRESS

To communicate with the CSD202, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. Table 10 lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs.

Table 10. Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

7.5.5.2 SERIAL INTERFACE

The CSD202 operates only as a slave device on both the I²C bus and the SMBus. Connections to the bus are made via the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitively coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduces the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The CSD202 supports the transmission protocol for fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 2.94MHz). All data bytes are transmitted most significant byte first.

7.5.5.3 WRITING TO AND READING FROM THE CSD202

Accessing a specific register on the CSD202 is accomplished by writing the appropriate value to the register pointer. Refer to Table 12 for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in Figure 23) is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register which data is written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

Figure 20 shows the write operation timing diagram. Figure 21 shows the read operation timing diagram.

NOTE
Register bytes are sent most-significant byte first, followed by the least significant byte.
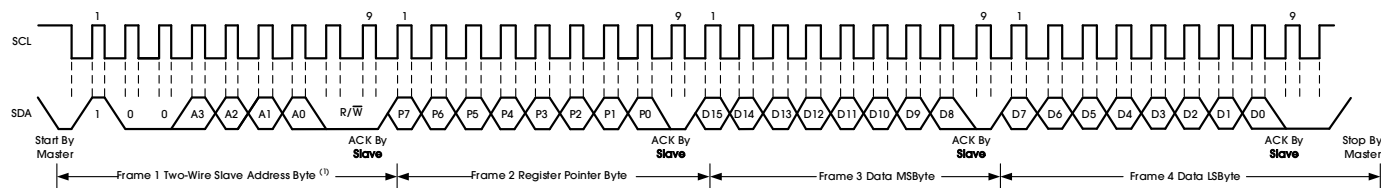
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(1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins.

Figure 20. Timing Diagram for Write Word Format

(1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins.
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated.
(3) ACK by Master can also be sent.

Figure 21. Timing Diagram for Read Word Format

Figure 22 shows the timing diagram for the SMBus Alert response operation. Figure 23 illustrates a typical register pointer configuration.

(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins.

Figure 22. Timing Diagram for SMBus ALERT

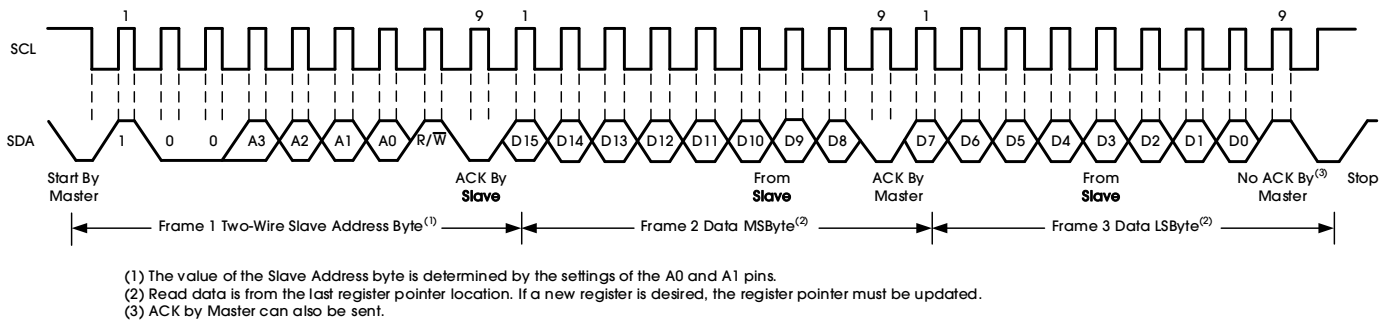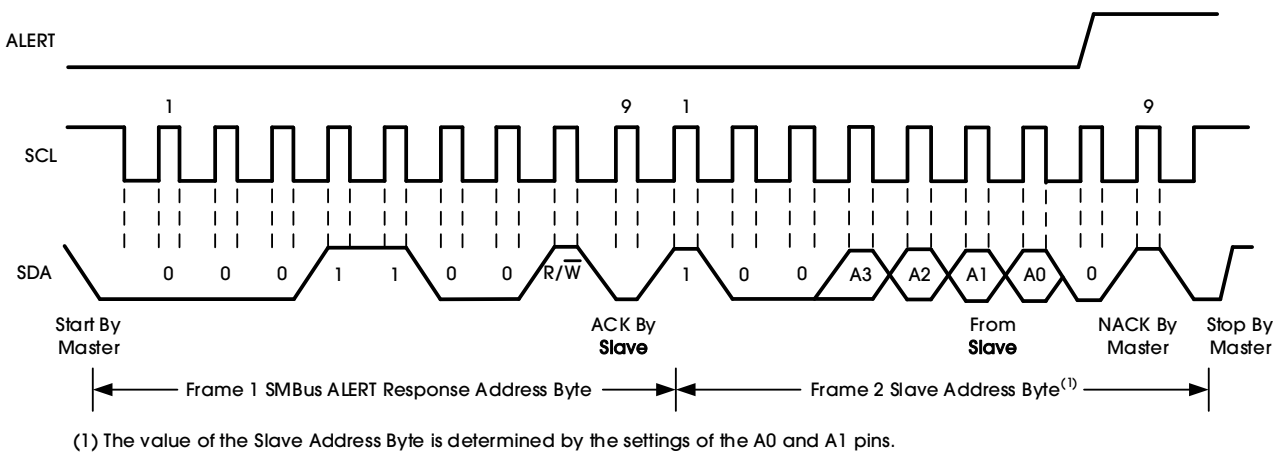(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins.
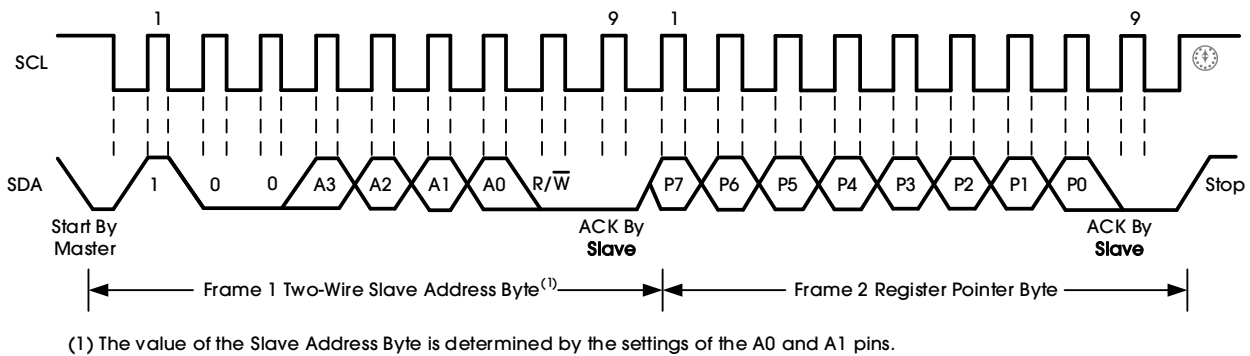
Figure 23. Typical Register Pointer Set

7.5.5.3.1 HIGH-SPEED I²C MODE

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code 00001XXX. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The device does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.94MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.
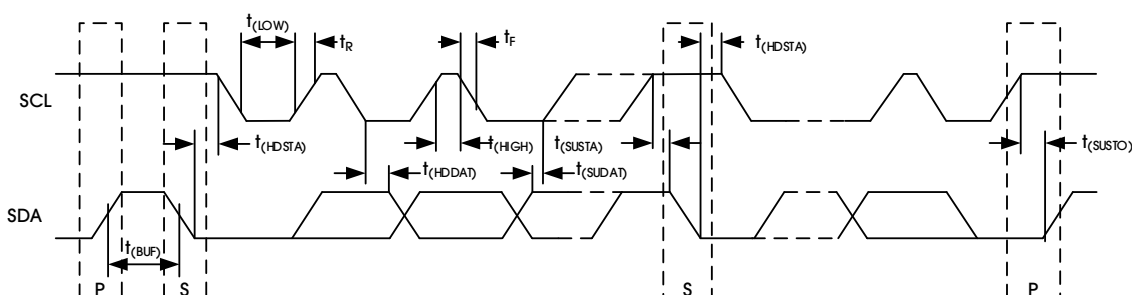
Figure 24. Bus Timing Diagram

Table 11. Bus Timing Diagram Definitions

PARAMETER	SYMBOL	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	2.94	MHz
Bus Free Time Between Stop and Start Conditions	$t_{(BUF)}$	600		160		ns
Hold Time after Repeated START Condition (After This Period, The First Clock is Generated.)	$t_{(HDSTA)}$	100		100		ns
Repeated Start Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	10	900	10	100	ns
Data Setup Time	$t_{(SUDAT)}$	100		20		ns
SCL Clock Low Period	$t_{(LOW)}$	1300		200		ns
SCL Clock High Period	$t_{(HIGH)}$	600		60		ns
Data Fall Time	t_F		300		80	ns
Clock Fall Time	t_F		300		40	ns
Clock Rise Time	t_R		300		40	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		1000			ns

Note: Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not guaranteed and not production tested.

7.5.5.4 SMBUS ALERT RESPONSE

The CSD202 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the Read/Write bit set high. Following this Alert Response, any slave device that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus. The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until the interrupt is cleared.

7.6 REGISTER MAPS

The CSD202 uses a bank of registers for holding configuration settings, measurement results, minimum/maximum limits, and status information. Table 12 summarizes the device registers; refer to the FUNCTIONAL BLOCK DIAGRAM section for an illustration of the registers.

All 16-bit device registers are two 8-bit bytes via the I2C interface.

Table 12. Register Set Summary

| POINTER ADDRESS | REGISTER NAME | FUNCTION | POWER-ON RESET | | TYPE[1] |
HEX			BINARY	HEX	
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	01000001 00100111	4127	R/$\overline{W}$
01h	Shunt Voltage Register	Shunt voltage measurement data	00000000 00000000	0000	R
02h	Bus Voltage Register	Bus voltage measurement data	00000000 00000000	0000	R
03h	Power Register[2]	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
04h	Current Register[2]	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/$\overline{W}$
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag	00000000 00000000	0000	R/$\overline{W}$
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function	00000000 00000000	0000	R/$\overline{W}$
FEh	Manufacturer ID Register	Contains unique manufacturer identification number	0101010001001001	4153	R
FFh	Die ID Register	Contains unique die identification number	0010001001100000	020X	R

Note 1: Type: R = Read-Only, R/$\overline{W}$ = Read/Write.
Note 2: The Current Register (04h) and Power Register (03h) default to '0' because the Calibration register defaults to '0', yielding zero current and power values until the Calibration register is programmed.

7.6.1 CONFIGURATION REGISTER (00H) (READ/WRITE)

The Configuration Register settings control the operating modes for the device. This register controls the conversion time settings for both the shunt and bus voltage measurements as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed resulting in a new conversion starting based on the new contents of the Configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion. Return to the SUMMARY TABLE.

Table 13. Configuration Register (00h) (Read/Write) Descriptions

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG 2	AVG 1	AVG 0	VBUS CT2	VBUS CT1	VBUS CT0	VSHC T2	VSHC T1	VSHC T0	MOD E3	MOD E2	MO DE1
POR VALUE	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

RST: Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset.
Bit 15:   Resets all registers to default values; this bit self-clears.

AVG: Averaging Mode. Determines the number of samples that are collected and averaged.
Bits 9–11:   Table 14 shows all the AVG bit settings and related number of averages for each bit setting.

Table 14. AVG Bit Settings (11:9) Combinations

AVG2 D11	AVG1 D10	AVG0 D9	NUMBER OF AVERAGES
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

Note: Shaded values are default.

VBUSCT: Bus Voltage Conversion Time
Bits 6–8:   Sets the conversion time for the bus voltage measurement. Table 15 shows the VBUSCT bit options and related conversion times for each bit setting.

Table 15. VBUSCT Bit Settings (8:6) Combinations

VBUSCT2 D8	VBUSCT1 D7	VBUSCT0 D6	CONVERSION TIME
0	0	0	140µs
0	0	1	204µs
0	1	0	332µs
0	1	1	588µs
1	0	0	1.1ms
1	0	1	2.116ms
1	1	0	4.156ms
1	1	1	8.244ms

Note: Shaded values are default.

VSHCT: Shunt Voltage Conversion Time
Bits 3–5:   Sets the conversion time for the shunt voltage measurement. Table 16 shows the VSHCT bit options and related conversion times for each bit setting.

Table 16. VSHCT Bit Settings (5:3) Combinations

VSHCT2 D8	VSHCT1 D7	VSHCT0 D6	CONVERSION TIME
0	0	0	140µs
0	0	1	204µs
0	1	0	332µs
0	1	1	588µs
1	0	0	1.1ms
1	0	1	2.116ms
1	1	0	4.156ms
1	1	1	8.244ms

Note: Shaded values are default.

MODE: Operating Mode
Bits 0-2:   Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 22.

Table 17. Mode Settings (2:0) Combinations

MODE3 D2	MODE2 D1	MODE1 D0	MODE
0	0	0	Power-Down (or Shutdown)
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	Power-Down (or Shutdown)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

Note: Shaded values are default.

7.6.2 SHUNT VOLTAGE REGISTER (01H) (READ-ONLY)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT}. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Example: For a value of V_{SHUNT} = –80mV:

1. Take the absolute value: 80mV.

2. Translate this number to a whole decimal number (80mV ÷ 2.5µV) = 32000.

3. Convert this number to binary = 0111 1101 0000 0000.

4. Complement the binary result = 1000 0010 1111 1111.

5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h.

If averaging is enabled, this register displays the averaged value. Full-scale range = 81.92mV (decimal = 7FFF); LSB: 2.5µV. Return to the SUMMARY TABLE.

Table 18. Shunt Voltage Register (01h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.3 BUS VOLTAGE REGISTER (02H) (READ-ONLY)

The Bus Voltage Register stores the most recent bus voltage reading, VBUS. If averaging is enabled, this register displays the averaged value. Full-scale range = 40.96V (decimal = 7FFF); LSB = 1.25mV. Return to the SUMMARY TABLE.

Table 19. Bus Voltage Register (02h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: D15 is always zero because bus voltage can only be positive.

7.6.4 POWER REGISTER (03H) (READ-ONLY)

If averaging is enabled, this register displays the averaged value.

The Power Register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB.

The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register according to Equation 4. Return to the SUMMARY TABLE.

Table 20. Power Register (03h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.5 CURRENT REGISTER (04H) (READ-ONLY)

If averaging is enabled, this register displays the averaged value.

The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register, according to Equation 3. Return to the SUMMARY TABLE.

Table 21. Current Register (04h) (Read-Only) Register Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.6 CALIBRATION REGISTER (05H) (READ/WRITE)

This register provides the device with the value of the shunt resistor that was present to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable for use in overall system calibration. See the PROGRAMMING THE CALIBRATION REGISTER for additional information on programming the Calibration Register. Return to the SUMMARY TABLE.

Table 22. Calibration Register (05h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.7 MASK/ENABLE REGISTER (06H) (READ/WRITE)

The Mask/Enable Register selects the function that is enabled to control the Alert pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (D15-D11) takes priority and responds to the Alert Limit Register. Return to the SUMMARY TABLE.

Table 23. Mask/Enable Register (06h) (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: Shunt Voltage Over-Voltage
Bit 15:   Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.

SUL: Shunt Voltage Under-Voltage
Bit 14:   Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.

BOL: Bus Voltage Over-Voltage
Bit 13:   Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.

BUL: Bus Voltage Under-Voltage
Bit 12:   Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.

POL: Power Over-Limit
Bit 11:   Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.

CNVR: Conversion Ready
Bit 10:   Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.

AFF: Alert Function Flag
Bit 4:   While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert.

              When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.

CVRF: Conversion Ready Flag
Bit 3:   Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions:
1.) Writing to the Configuration Register (except for Power-Down selection).
2.) Reading the Mask/Enable Register.

OVF: Math Overflow Flag
Bit 2:   This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.

APOL: Alert Polarity bit; sets the Alert pin polarity.
Bit 1:   1 = Inverted (active-high open collector)
            0 = Normal (active-low open collector) (default)

LEN: Alert Latch Enable; configures the latching feature of the Alert pin and Alert Flag bits.
Bit 0:   1 = Latch enabled
            0 = Transparent (default)
            When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

7.6.8 ALERT LIMIT REGISTER (07H) (READ/WRITE)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded. Return to the SUMMARY TABLE.

Table 24. Alert Limit Register (07h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.6.9 MANUFACTURER ID REGISTER (FEH) (READ-ONLY)

The Manufacturer ID Register stores a unique identification number for the manufacturer. Return to the SUMMARY TABLE.

Table 25. Manufacturer ID Register (FEh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
POR VALUE	0	1	0	0	0	0	0	1	0	1	0	1	0	0	1	1

ID: Manufacturer ID Bits
Bits 0-15:   Stores the manufacturer identification bits.

7.6.10 DIE ID REGISTER (FFH) (READ-ONLY)

The Die ID Register stores a unique identification number and the revision ID for the die. Return to the SUMMARY TABLE.

Table 26. Die ID Register (FFh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DID 11	DID 10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	RID3	RID2	RID1	RID0
POR VALUE	0	0	0	0	0	0	1	0	0	0	0	0	x	x	x	x

DID: Device ID Bits
Bits 15-4:   Stores the device identification bits.

RID: Reserved
Bit 3-0:   Reserved and do NOT care.

8. APPLICATION AND IMPLEMENTATION

NOTE

The information provided in this section is not part of the AnalogySemi component specification. Hence, AnalogySemi does not warrant its completeness or accuracy. Customers are responsible for determining suitability of components and system functionality for their applications. Validation and testing should be performed prior to design implementation.

8.1 APPLICATION INFORMATION

The CSD202 senses the bi-directional current on a high common-mode bus and monitors the bus voltage with an I2C™- or SMBUS-compatible digital interface. The programmable calibration value, conversion times, averaging, and an internal multiplier make it easy to read out current, bus voltage, and power values directly from registers.

8.2 TYPICAL APPLICATIONS

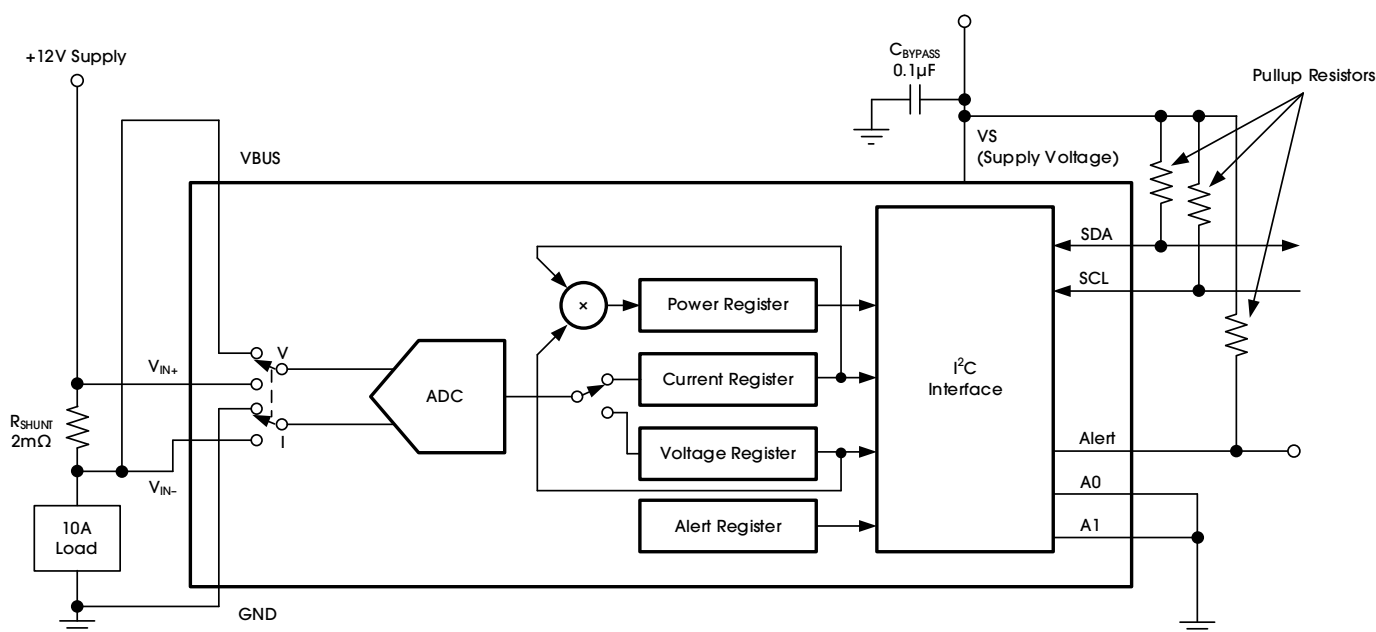### 8.2.1 HIGH-SIDE SENSING CIRCUIT APPLICATION

Figure 25. Typical Circuit Configuration, CSD202

8.2.1.1 DESIGN REQUIREMENTS

The CSD202 measures the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through it. The device also measures the bus supply voltage and can calculate power when calibrated. It comes with alert capability where the alert pin can be programmed to respond to a user-defined event or to a conversion ready notification. This design illustrates the ability of the alert pin to respond to a set threshold.

8.2.1.2 DETAILED DESIGN PROCEDURE

The Alert pin can be configured to respond to one of the five alert functions described in the ALERT PIN section. The alert pin must be pulled up to the V_{VS} pin voltage via the pull-up resistors. The configuration register is set based on the required conversion time and averaging. The Mask/Enable Register is set to identify the required alert function and the Alert Limit Register is set to the limit value used for comparison.

9. POWER SUPPLY RECOMMENDATIONS

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_{VS}. For example, the voltage applied to the V_{VS} power supply terminal can be 5V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 36V. Note also that the device can withstand the full 0V to 36V range at the input terminals, regardless of whether the device has power applied or not.

Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device to ensure stability. A typical value for this supply bypass capacitor is 0.1μF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10. LAYOUT

10.1 LAYOUT GUIDELINES

Connect the input pins (IN+ and IN−) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

10.2 LAYOUT EXAMPLE
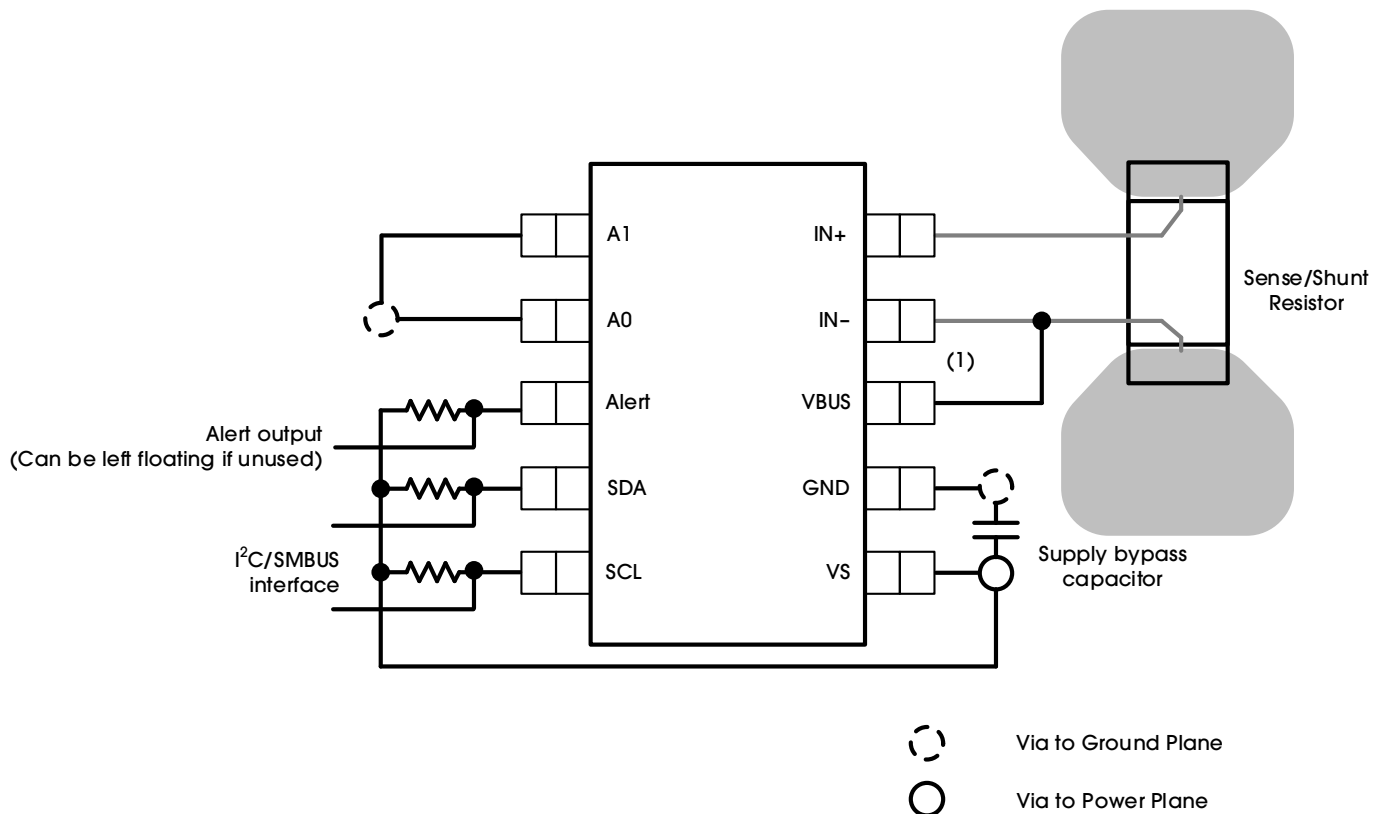
(1) connect the VBUS pin to the power supply rail.

Figure 26. CSD202 Layout Example

11. PACKAGE INFORMATION

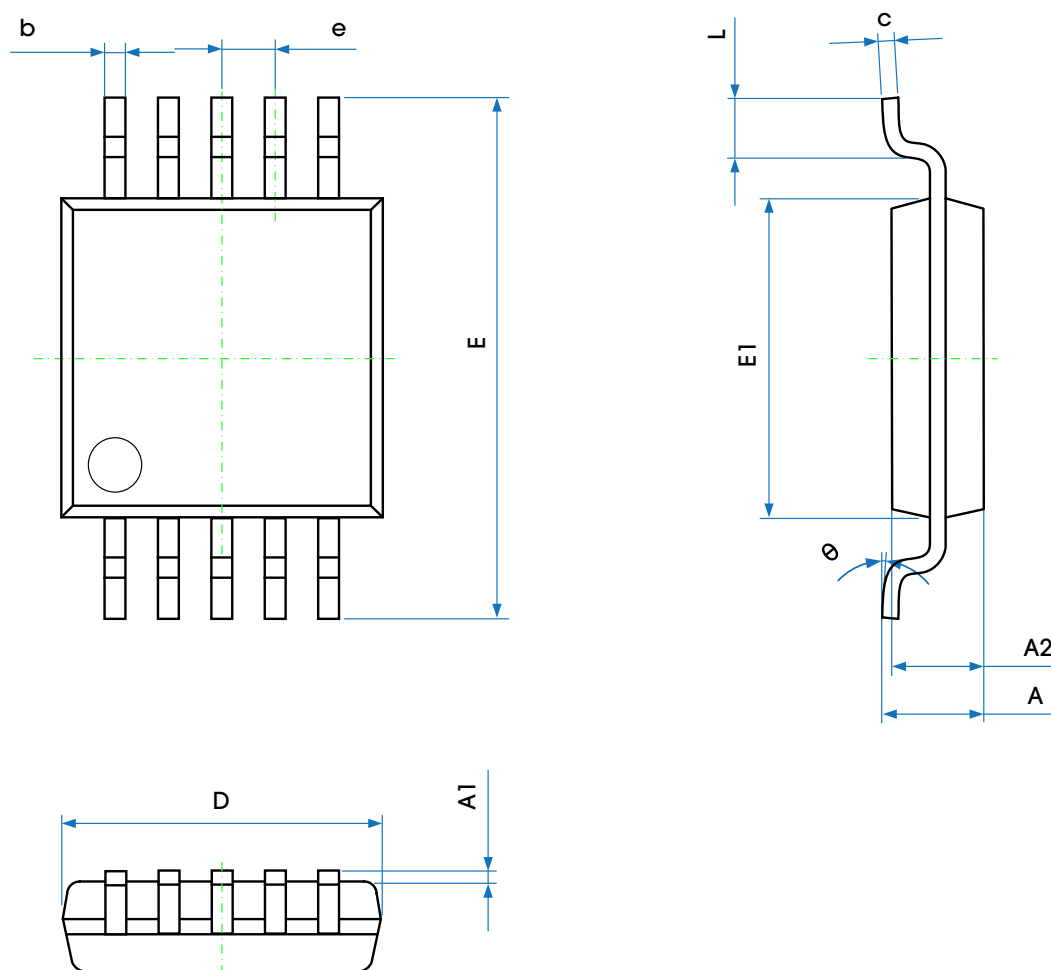The CSD202 is available in the MSOP-10 package. Figure 27 shows the package view.


Figure 27. Package View

Table 27 provides detailed information about the dimensions.

Table 27. Dimensions

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	—	1.100	—	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.330	0.007	0.013
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.500 (BSC)		0.020 (BSC)	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

12. TAPE AND REEL INFORMATION

Figure 28 illustrates the carrier tape.
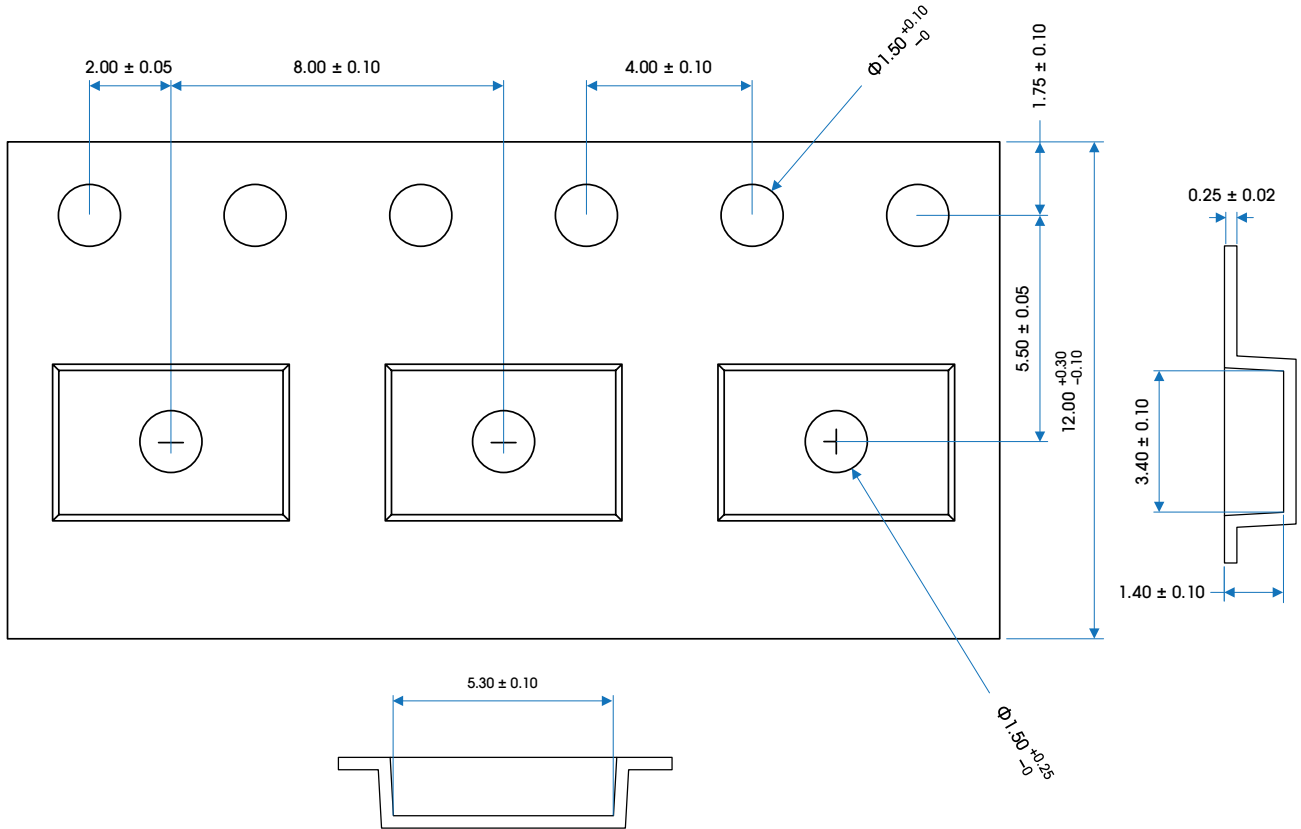
Notes:
1. Cover tape width: 9.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 250mm.
4. Mold#: MSOP-10.
5. All dimensions: mm.
6. Direction of view:

Figure 28. Carrier Tape Drawing

Table 28 provides information about tape and reel.

Table 28. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
MSOP-10	13''	3000	1	8	24000	358*340*50	430*380*390

Figure 29 shows the product loading orientation—pin 1 is assigned at Q1.

* Q: Pocket quadrant
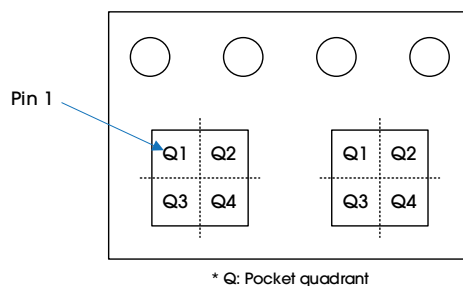
Figure 29. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	14 October 2022	Rev A release.
Rev B	16 December 2022	Updated the order information, and the tape and reel information.

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