Ultra-Low Noise, 150mA/200mA/250mA, CMOS Linear Regulator

1. FEATURES

- Ultra-low noise:
  - 13.5μV rms at V_{OUT} = 3.3V
  - 9.5μV rms at V_{OUT} = 1.1V
- No noise bypass capacitor required
- Stable with 1μF ceramic input and output capacitors
- Maximum output current:
  - 150mA (LD501L)
  - 200mA (LD501M)
  - 250mA (LD501P)
- Input voltage range: 2.2V to 5.5V
- Low quiescent current
  - I_{GND} = 12μA with I_{OUT} = 0mA
  - I_{GND} = 170μA with I_{OUT} = 150mA (LD501L)
  - I_{GND} = 200μA with I_{OUT} = 200mA (LD501M)
  - I_{GND} = 229μA with I_{OUT} = 250mA (LD501P)
- Low shutdown current: 0.25μA
- Low dropout voltage:
  - $V_{DROPOUT}$ = 70mV with I_{OUT} = 150mA (LD501L)
  - $V_{DROPOUT}$ = 94mV with I_{OUT} = 200mA (LD501M)
  - $V_{DROPOUT}$ = 118mV with I_{OUT} = 250mA (LD501P)
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature: ±2.5%
- More than 32 fixed output voltage options: 1.1V to 5.0V
- PSRR performance of 74dB at 10kHz
- Current-limit and thermal overload protection
- Logic controlled enable
- SOT23-5 package

2. APPLICATIONS

- RF, voltage controlled oscillator (VCO), and phase locked loop (PLL) power supplies
- Mobile phones
- Digital camera and audio devices
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Portable medical devices

3. DESCRIPTION

The LD501 is an ultra-low noise, low dropout (LDO) linear regulator that operates from 2.2V to 5.5V and provides output current up to 150mA (LD501L), 200mA (LD501M), or 250mA (LD501P).

The low dropout voltage—70mV at 150mA load (LD501L), 94mV at 200mA load (LD501M), or 118mV at 250mA load (LD501P), improves efficiency and allows operation over a wide input voltage range.

The LD501 achieves ultra-low noise performance without the bypass capacitor due to the optimized circuit topology, which makes the LD501 ideal for noise or space sensitive analog and RF applications. The LD501 also achieves ultra-low noise performance without compromising the power supply rejection ratio (PSRR) or transient line and load performance. The low operating supply current—170μA (LD501L), 200μA (LD501M), or 229μA (LD501P), makes the LD501 suitable for battery-operated portable equipment.

The LD501 is specifically designed for stable operation with tiny 1μF, ±30% ceramic input and output capacitors to address the needs of high performance, space constrained applications. In addition, the LD501 also includes an internal pull-down resistor on the EN input.

The LD501 is capable of more than 32 fixed output voltage options, ranging from 1.1V to 5.0V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions.

The LD501 is available in tiny SOT23-5 package for the smallest footprint solution to meet a variety of portable power application requirements. See Table 1 for the order information.

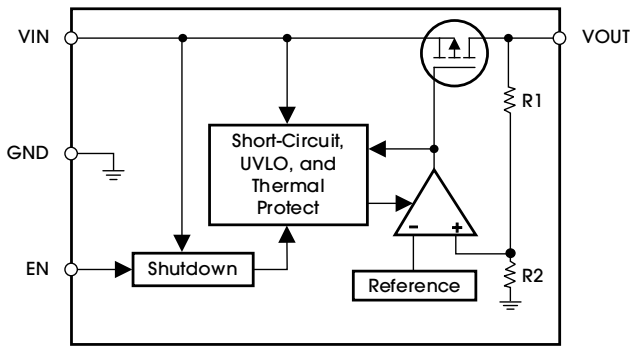


Table 1 lists the order information for the available devices.

Table 1. Order Information (Available)

ORDER NUMBER[1]	PART NUMBER	PACKAGE	MARKING	V_{OUT} (V)	I_{OUT} (MAX) (mA)	OPERATING TEMP (°C)	PACKAGE OPTION
LD501PCSOT-12	LD501P	SOT23-5	LD501P12	1.2	250	-40-125	T/R-3000
LD501PCSOT-18	LD501P	SOT23-5	LD501P18	1.8	250	-40-125	T/R-3000
LD501PCSOT-25	LD501P	SOT23-5	LD501P25	2.5	250	-40-125	T/R-3000
LD501PCSOT-30	LD501P	SOT23-5	LD501P30	3.0	250	-40-125	T/R-3000
LD501PCSOT-33	LD501P	SOT23-5	LD501P33	3.3	250	-40-125	T/R-3000

Table 2 lists the order information for the devices that will be available in the future.

Table 2. Order Information (Unavailable Now)

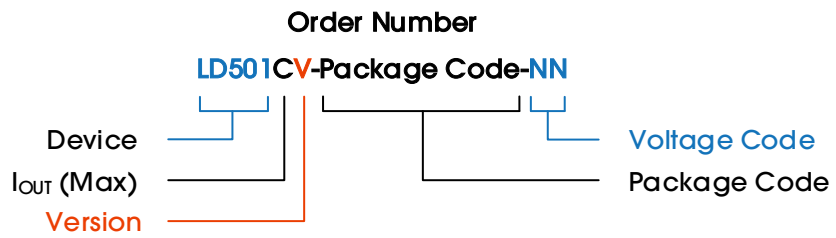
ORDER NUMBER[1]	PART NUMBER	PACKAGE	MARKING	V_{OUT} (V)	I_{OUT} (MAX) (mA)	OPERATING TEMP (°C)	PACKAGE OPTION
LD501LCSOT-11[2]	LD501L	SOT23-5	LD501L11	1.1	150	-40-125	T/R-3000
LD501LCSOT-12[2]	LD501L	SOT23-5	LD501L12	1.2	150	-40-125	T/R-3000
LD501LCSOT-13[2]	LD501L	SOT23-5	LD501L13	1.3	150	-40-125	T/R-3000
LD501LCSOT-14[2]	LD501L	SOT23-5	LD501L14	1.4	150	-40-125	T/R-3000
LD501LCSOT-15[2]	LD501L	SOT23-5	LD501L15	1.5	150	-40-125	T/R-3000
LD501LCSOT-16[2]	LD501L	SOT23-5	LD501L16	1.6	150	-40-125	T/R-3000
LD501LCSOT-17[2]	LD501L	SOT23-5	LD501L17	1.7	150	-40-125	T/R-3000
LD501LCSOT-18[2]	LD501L	SOT23-5	LD501L18	1.8	150	-40-125	T/R-3000
LD501LCSOT-19[2]	LD501L	SOT23-5	LD501L19	1.9	150	-40-125	T/R-3000
LD501LCSOT-20[2]	LD501L	SOT23-5	LD501L20	2.0	150	-40-125	T/R-3000
LD501LCSOT-21[2]	LD501L	SOT23-5	LD501L21	2.1	150	-40-125	T/R-3000
LD501LCSOT-22[2]	LD501L	SOT23-5	LD501L22	2.2	150	-40-125	T/R-3000
LD501LCSOT-23[2]	LD501L	SOT23-5	LD501L23	2.3	150	-40-125	T/R-3000
LD501LCSOT-24[2]	LD501L	SOT23-5	LD501L24	2.4	150	-40-125	T/R-3000
LD501LCSOT-25[2]	LD501L	SOT23-5	LD501L25	2.5	150	-40-125	T/R-3000
LD501LCSOT-26[2]	LD501L	SOT23-5	LD501L26	2.6	150	-40-125	T/R-3000
LD501LCSOT-27[2]	LD501L	SOT23-5	LD501L27	2.7	150	-40-125	T/R-3000
LD501LCSOT-275[2]	LD501L	SOT23-5	LD501L275	2.75	150	-40-125	T/R-3000
LD501LCSOT-28[2]	LD501L	SOT23-5	LD501L28	2.8	150	-40-125	T/R-3000
LD501LCSOT-285[2]	LD501L	SOT23-5	LD501L285	2.85	150	-40-125	T/R-3000
LD501LCSOT-29[2]	LD501L	SOT23-5	LD501L29	2.9	150	-40-125	T/R-3000
LD501LCSOT-30[2]	LD501L	SOT23-5	LD501L30	3.0	150	-40-125	T/R-3000
LD501LCSOT-31[2]	LD501L	SOT23-5	LD501L31	3.1	150	-40-125	T/R-3000
LD501LCSOT-32[2]	LD501L	SOT23-5	LD501L32	3.2	150	-40-125	T/R-3000
LD501LCSOT-33[2]	LD501L	SOT23-5	LD501L33	3.3	150	-40-125	T/R-3000
LD501LCSOT-34[2]	LD501L	SOT23-5	LD501L34	3.4	150	-40-125	T/R-3000
LD501LCSOT-35[2]	LD501L	SOT23-5	LD501L35	3.5	150	-40-125	T/R-3000
LD501LCSOT-36[2]	LD501L	SOT23-5	LD501L36	3.6	150	-40-125	T/R-3000
LD501LCSOT-37[2]	LD501L	SOT23-5	LD501L37	3.7	150	-40-125	T/R-3000
LD501LCSOT-38[2]	LD501L	SOT23-5	LD501L38	3.8	150	-40-125	T/R-3000
LD501LCSOT-39[2]	LD501L	SOT23-5	LD501L39	3.9	150	-40-125	T/R-3000
LD501LCSOT-40[2]	LD501L	SOT23-5	LD501L40	4.0	150	-40-125	T/R-3000
LD501LCSOT-41[2]	LD501L	SOT23-5	LD501L41	4.1	150	-40-125	T/R-3000
LD501LCSOT-42[2]	LD501L	SOT23-5	LD501L42	4.2	150	-40-125	T/R-3000
LD501LCSOT-43[2]	LD501L	SOT23-5	LD501L43	4.3	150	-40-125	T/R-3000
LD501LCSOT-44[2]	LD501L	SOT23-5	LD501L44	4.4	150	-40-125	T/R-3000
LD501LCSOT-45[2]	LD501L	SOT23-5	LD501L45	4.5	150	-40-125	T/R-3000

ORDER NUMBER[1]	PART NUMBER	PACKAGE	MARKING	V_{OUT} (V)	I_{OUT} (MAX) (mA)	OPERATING TEMP (°C)	PACKAGE OPTION
LD501LCSOT-46[2]	LD501L	SOT23-5	LD501L46	4.6	150	-40-125	T/R-3000
LD501LCSOT-47[2]	LD501L	SOT23-5	LD501L47	4.7	150	-40-125	T/R-3000
LD501LCSOT-48[2]	LD501L	SOT23-5	LD501L48	4.8	150	-40-125	T/R-3000
LD501LCSOT-49[2]	LD501L	SOT23-5	LD501L49	4.9	150	-40-125	T/R-3000
LD501LCSOT-50[2]	LD501L	SOT23-5	LD501L50	5.0	150	-40-125	T/R-3000
LD501MCSOT-11[2]	LD501M	SOT23-5	LD501M11	1.1	200	-40-125	T/R-3000
LD501MCSOT-12[2]	LD501M	SOT23-5	LD501M12	1.2	200	-40-125	T/R-3000
LD501MCSOT-13[2]	LD501M	SOT23-5	LD501M13	1.3	200	-40-125	T/R-3000
LD501MCSOT-14[2]	LD501M	SOT23-5	LD501M14	1.4	200	-40-125	T/R-3000
LD501MCSOT-15[2]	LD501M	SOT23-5	LD501M15	1.5	200	-40-125	T/R-3000
LD501MCSOT-16[2]	LD501M	SOT23-5	LD501M16	1.6	200	-40-125	T/R-3000
LD501MCSOT-17[2]	LD501M	SOT23-5	LD501M17	1.7	200	-40-125	T/R-3000
LD501MCSOT-18[2]	LD501M	SOT23-5	LD501M18	1.8	200	-40-125	T/R-3000
LD501MCSOT-19[2]	LD501M	SOT23-5	LD501M19	1.9	200	-40-125	T/R-3000
LD501MCSOT-20[2]	LD501M	SOT23-5	LD501M20	2.0	200	-40-125	T/R-3000
LD501MCSOT-21[2]	LD501M	SOT23-5	LD501M21	2.1	200	-40-125	T/R-3000
LD501MCSOT-22[2]	LD501M	SOT23-5	LD501M22	2.2	200	-40-125	T/R-3000
LD501MCSOT-23[2]	LD501M	SOT23-5	LD501M23	2.3	200	-40-125	T/R-3000
LD501MCSOT-24[2]	LD501M	SOT23-5	LD501M24	2.4	200	-40-125	T/R-3000
LD501MCSOT-25[2]	LD501M	SOT23-5	LD501M25	2.5	200	-40-125	T/R-3000
LD501MCSOT-26[2]	LD501M	SOT23-5	LD501M26	2.6	200	-40-125	T/R-3000
LD501MCSOT-27[2]	LD501M	SOT23-5	LD501M27	2.7	200	-40-125	T/R-3000
LD501MCSOT-275[2]	LD501M	SOT23-5	LD501M275	2.75	200	-40-125	T/R-3000
LD501MCSOT-28[2]	LD501M	SOT23-5	LD501M28	2.8	200	-40-125	T/R-3000
LD501MCSOT-285[2]	LD501M	SOT23-5	LD501M285	2.85	200	-40-125	T/R-3000
LD501MCSOT-29[2]	LD501M	SOT23-5	LD501M29	2.9	200	-40-125	T/R-3000
LD501MCSOT-30[2]	LD501M	SOT23-5	LD501M30	3.0	200	-40-125	T/R-3000
LD501MCSOT-31[2]	LD501M	SOT23-5	LD501M31	3.1	200	-40-125	T/R-3000
LD501MCSOT-32[2]	LD501M	SOT23-5	LD501M32	3.2	200	-40-125	T/R-3000
LD501MCSOT-33[2]	LD501M	SOT23-5	LD501M33	3.3	200	-40-125	T/R-3000
LD501MCSOT-34[2]	LD501M	SOT23-5	LD501M34	3.4	200	-40-125	T/R-3000
LD501MCSOT-35[2]	LD501M	SOT23-5	LD501M35	3.5	200	-40-125	T/R-3000
LD501MCSOT-36[2]	LD501M	SOT23-5	LD501M36	3.6	200	-40-125	T/R-3000
LD501MCSOT-37[2]	LD501M	SOT23-5	LD501M37	3.7	200	-40-125	T/R-3000
LD501MCSOT-38[2]	LD501M	SOT23-5	LD501M38	3.8	200	-40-125	T/R-3000
LD501MCSOT-39[2]	LD501M	SOT23-5	LD501M39	3.9	200	-40-125	T/R-3000
LD501MCSOT-40[2]	LD501M	SOT23-5	LD501M40	4.0	200	-40-125	T/R-3000
LD501MCSOT-41[2]	LD501M	SOT23-5	LD501M41	4.1	200	-40-125	T/R-3000
LD501MCSOT-42[2]	LD501M	SOT23-5	LD501M42	4.2	200	-40-125	T/R-3000
LD501MCSOT-43[2]	LD501M	SOT23-5	LD501M43	4.3	200	-40-125	T/R-3000
LD501MCSOT-44[2]	LD501M	SOT23-5	LD501M44	4.4	200	-40-125	T/R-3000
LD501MCSOT-45[2]	LD501M	SOT23-5	LD501M45	4.5	200	-40-125	T/R-3000
LD501MCSOT-46[2]	LD501M	SOT23-5	LD501M46	4.6	200	-40-125	T/R-3000
LD501MCSOT-47[2]	LD501M	SOT23-5	LD501M47	4.7	200	-40-125	T/R-3000
LD501MCSOT-48[2]	LD501M	SOT23-5	LD501M48	4.8	200	-40-125	T/R-3000
LD501MCSOT-49[2]	LD501M	SOT23-5	LD501M49	4.9	200	-40-125	T/R-3000
LD501MCSOT-50[2]	LD501M	SOT23-5	LD501M50	5.0	200	-40-125	T/R-3000
LD501PCSOT-11[2]	LD501P	SOT23-5	LD501P11	1.1	250	-40-125	T/R-3000
LD501PCSOT-13[2]	LD501P	SOT23-5	LD501P13	1.3	250	-40-125	T/R-3000
LD501PCSOT-14[2]	LD501P	SOT23-5	LD501P14	1.4	250	-40-125	T/R-3000

ORDER NUMBER[1]	PART NUMBER	PACKAGE	MARKING	V_{OUT} (V)	I_{OUT} (MAX) (mA)	OPERATING TEMP (°C)	PACKAGE OPTION
LD501PCSOT-15[2]	LD501P	SOT23-5	LD501P15	1.5	250	-40-125	T/R-3000
LD501PCSOT-16[2]	LD501P	SOT23-5	LD501P16	1.6	250	-40-125	T/R-3000
LD501PCSOT-17[2]	LD501P	SOT23-5	LD501P17	1.7	250	-40-125	T/R-3000
LD501PCSOT-19[2]	LD501P	SOT23-5	LD501P19	1.9	250	-40-125	T/R-3000
LD501PCSOT-20[2]	LD501P	SOT23-5	LD501P20	2.0	250	-40-125	T/R-3000
LD501PCSOT-21[2]	LD501P	SOT23-5	LD501P21	2.1	250	-40-125	T/R-3000
LD501PCSOT-22[2]	LD501P	SOT23-5	LD501P22	2.2	250	-40-125	T/R-3000
LD501PCSOT-23[2]	LD501P	SOT23-5	LD501P23	2.3	250	-40-125	T/R-3000
LD501PCSOT-24[2]	LD501P	SOT23-5	LD501P24	2.4	250	-40-125	T/R-3000
LD501PCSOT-26[2]	LD501P	SOT23-5	LD501P26	2.6	250	-40-125	T/R-3000
LD501PCSOT-27[2]	LD501P	SOT23-5	LD501P27	2.7	250	-40-125	T/R-3000
LD501PCSOT-275[2]	LD501P	SOT23-5	LD501P275	2.75	250	-40-125	T/R-3000
LD501PCSOT-28[2]	LD501P	SOT23-5	LD501P28	2.8	250	-40-125	T/R-3000
LD501PCSOT-285[2]	LD501P	SOT23-5	LD501P285	2.85	250	-40-125	T/R-3000
LD501PCSOT-29[2]	LD501P	SOT23-5	LD501P29	2.9	250	-40-125	T/R-3000
LD501PCSOT-31[2]	LD501P	SOT23-5	LD501P31	3.1	250	-40-125	T/R-3000
LD501PCSOT-32[2]	LD501P	SOT23-5	LD501P32	3.2	250	-40-125	T/R-3000
LD501PCSOT-34[2]	LD501P	SOT23-5	LD501P34	3.4	250	-40-125	T/R-3000
LD501PCSOT-35[2]	LD501P	SOT23-5	LD501P35	3.5	250	-40-125	T/R-3000
LD501PCSOT-36[2]	LD501P	SOT23-5	LD501P36	3.6	250	-40-125	T/R-3000
LD501PCSOT-37[2]	LD501P	SOT23-5	LD501P37	3.7	250	-40-125	T/R-3000
LD501PCSOT-38[2]	LD501P	SOT23-5	LD501P38	3.8	250	-40-125	T/R-3000
LD501PCSOT-39[2]	LD501P	SOT23-5	LD501P39	3.9	250	-40-125	T/R-3000
LD501PCSOT-40[2]	LD501P	SOT23-5	LD501P40	4.0	250	-40-125	T/R-3000
LD501PCSOT-41[2]	LD501P	SOT23-5	LD501P41	4.1	250	-40-125	T/R-3000
LD501PCSOT-42[2]	LD501P	SOT23-5	LD501P42	4.2	250	-40-125	T/R-3000
LD501PCSOT-43[2]	LD501P	SOT23-5	LD501P43	4.3	250	-40-125	T/R-3000
LD501PCSOT-44[2]	LD501P	SOT23-5	LD501P44	4.4	250	-40-125	T/R-3000
LD501PCSOT-45[2]	LD501P	SOT23-5	LD501P45	4.5	250	-40-125	T/R-3000
LD501PCSOT-46[2]	LD501P	SOT23-5	LD501P46	4.6	250	-40-125	T/R-3000
LD501PCSOT-47[2]	LD501P	SOT23-5	LD501P47	4.7	250	-40-125	T/R-3000
LD501PCSOT-48[2]	LD501P	SOT23-5	LD501P48	4.8	250	-40-125	T/R-3000
LD501PCSOT-49[2]	LD501P	SOT23-5	LD501P49	4.9	250	-40-125	T/R-3000
LD501PCSOT-50[2]	LD501P	SOT23-5	LD501P50	5.0	250	-40-125	T/R-3000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: Available in the future.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

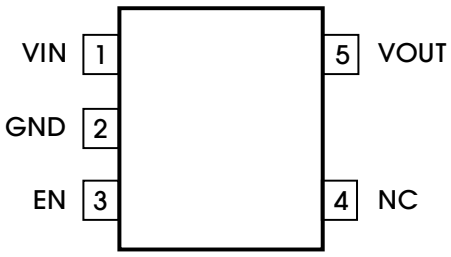


Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION	NAME	TYPE	DESCRIPTION
1	VIN	Input	Regulator input supply. Bypass VIN to GND with a 1μF or greater capacitor.
2	GND	Ground	Ground
3	EN	Input	Enable input. Drive EN high to turn on the regulator and drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	NC	NC	No connect. Not connected internally.
5	VOUT	Output	Regulated output voltage. Bypass VOUT to GND with a 1μF or greater capacitor.
—	NC	NC	No connect. Not connected internally.
—	EPAD	NC	Exposed pad. The exposed pad must be connected to ground. The exposed pad enhances the thermal performance of the package.

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the LD501.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	VIN to GND	–0.3	6.5	V
	VOUT to GND	–0.3	V_{IN}	
	EN to GND	–0.3	6.5	
Current	I_{OUT}	Internally limited		mA
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J	–40	125	
	Storage, T_{stg}	–65	150	
	Soldering	JEDEC J-STD-020		

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the LD501.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the LD501.

Table 6. Recommended Operating Conditions

PARAMETER		SYMBOL	MIN	NOM	MAX	UNITS
Input Voltage Range		V_{IN}	2.2		5.5	V
Output Voltage Range		V_{OUT}	1.1		5.0	V
Output Current Range	LD501L	I_{OUT}	0		150	mA
	LD501M		0		200	mA
	LD501P		0		250	mA
EN Voltage		V_{EN}	0		V_{IN}	V
Output Capacitor		C_{OUT}	0.7	1		μF
Output Capacitor ESR		R_{ESR}	0.001		0.2	Ω
Junction Temperature		T_J	–40		125	°C

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the LD501.

Table 7. Thermal Information

PARAMETER	SYMBOL	SOT23-5	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	168	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	103	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	39	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	10	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	36	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	66	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of the LD501. V_{IN} = (V_{OUT} + 0.4V) or 2.2V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	T_J = –40°C to 125°C	2.2		5.5	V
Operating Supply Current	I_{GND}	I_{OUT} = 0μA		12		μA
		I_{OUT} = 0μA, T_J = –40°C to 125°C			25	μA
		I_{OUT} = 100μA		28		μA
		I_{OUT} = 100μA, T_J = –40°C to 125°C			54	μA
		I_{OUT} = 10mA		61		μA
		I_{OUT} = 10mA, T_J = –40°C to 125°C			100	μA
		I_{OUT} = 150mA		170		μA
		I_{OUT} = 150mA, T_J = –40°C to 125°C			215	μA
		I_{OUT} = 200mA		200		μA
		I_{OUT} = 200mA, T_J = –40°C to 125°C			253	μA
		I_{OUT} = 250mA		229		μA
		I_{OUT} = 250mA, T_J = –40°C to 125°C			291	μA
Shutdown Current	I_{GND-SD}	EN = GND		0.25		μA
		EN = GND, T_J = –40°C to 125°C			1.8	μA
OUTPUT VOLTAGE ACCURACY						
SOT23-5	V_{OUT}	I_{OUT} = 10mA	–1		1	%
		T_J = –40°C to 125°C				
		V_{OUT} < 1.8V, 100μA < I_{OUT} < 150mA (200mA, 250mA), V_{IN} = (V_{OUT} + 0.4V) to 5.5V	–3		2	%
		V_{OUT} ≥1.8V, 100μA < I_{OUT} < 150mA (200mA, 250mA), V_{IN} = (V_{OUT} + 0.4V) to 5.5V	–2.5		1.5	%
REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4V) to 5.5V, T_J = –40°C to 125°C		0.02		%/V
Load Regulation (SOT23-5)[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{OUT} < 1.8V				
		I_{OUT} = 100μA to 150mA (200mA, 250mA)		0.005		%/mA
		I_{OUT} = 100μA to 150mA (200mA, 250mA), T_J = –40°C to 125°C			0.008	%/mA
		V_{OUT} ≥ 1.8V				
		I_{OUT} = 100μA to 150mA (200mA, 250mA)		0.002		%/mA
		I_{OUT} = 100μA to 150mA (200mA, 250mA), T_J = –40°C to 125°C			0.005	%/mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DROPOUT VOLTAGE(3)						
SOT23-5	$V_{DROPOUT}$	I_{OUT} = 150mA		70		mV
		I_{OUT} = 150mA, T_J = –40°C to 125°C			105	mV
		I_{OUT} = 200mA		94		mV
		I_{OUT} = 200mA, T_J = –40°C to 125°C			140	mV
		I_{OUT} = 250mA		118		mV
		I_{OUT} = 250mA, T_J = –40°C to 125°C			117	mV
Start-Up Time(4)	$t_{START-UP}$	V_{OUT} = 3.3V		180		μs
Current-Limit Threshold(5)	I_{LIMIT}	T_J = 0°C to 125°C, LD501L	160	260	360	mA
		T_J = 0°C to 125°C, LD501M	210	290	400	mA
		T_J = 0°C to 125°C, LD501P	260	350	385	mA
UNDERVOLTAGE LOCKOUT						
Input Voltage Rising	$UVLO_{RISE}$	T_J = –40°C to 125°C			2.1	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = –40°C to 125°C	1.75		2.0	V
Hysteresis	$UVLO_{HYS}$	T_J = –40°C to 125°C		102		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		155		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}	T_J rising		20		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.2V ≤ V_{IN} ≤ 5.5V	1.2			V
EN Input Logic Low	V_{IL}	2.2V ≤ V_{IN} ≤ 5.5V			0.4	V
EN Input Leakage Current	I_{EN}	V_{IN} = V_{EN} = 5.5V		0.001		μA
Output Noise	OUT_{NOISE}	10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 3.3V		13.5		μV rms
		10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 2.5V		12.5		μV rms
		10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 1.1V		9.5		μV rms
POWER SUPPLY REJECTION RATIO						
V_{IN} = V_{OUT} + 0.5V	PSRR	10kHz, V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 10mA		74		dB
		100kHz, V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 10mA		57		dB
V_{IN} = V_{OUT} + 1V	PSRR	10kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA		71		dB
		100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA		58		dB
		10kHz, V_{IN} = 2.2V, V_{OUT} = 1.1V, I_{OUT} = 10mA		68		dB
		100kHz, V_{IN} = 2.2V, V_{OUT} = 1.1V, I_{OUT} = 10mA		51		dB

Note 1: Unless otherwise specified, 150mA in this table corresponds to LD501L, 200mA corresponds to LD501M, and 250mA corresponds to LD501P.
Note 2: Based on an end-point calculation using 0.1mA and 150mA (200mA, 250mA) loads.
Note 3: Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This voltage applies only for output voltages above 2.2V.
Note 4: Start-up time is defined as the time between the rising edge of EN and V_{OUT} being at 90% of its nominal value.
Note 5: Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0V (that is, 2.7V).

5.6 TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.

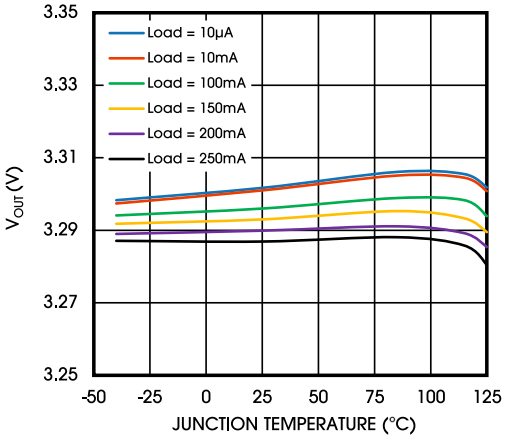


Figure 2. V_{OUT} vs. Junction Temperature

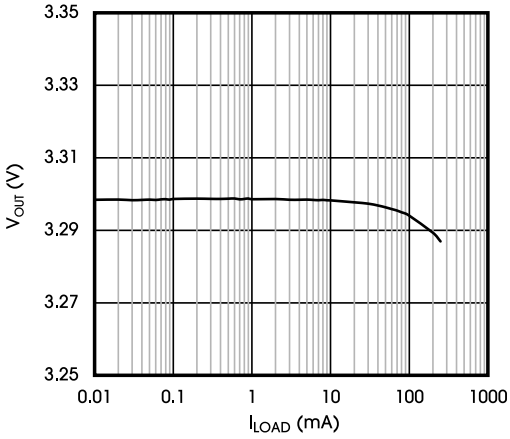


Figure 3. V_{OUT} vs. Load Current (I_{LOAD})

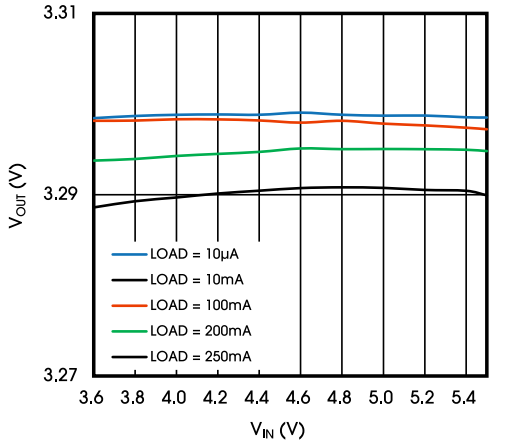


Figure 4. V_{OUT} vs. V_{IN}

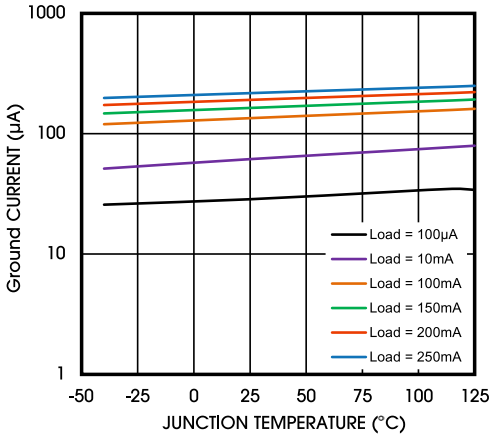


Figure 5. Ground Current vs. Junction Temperature

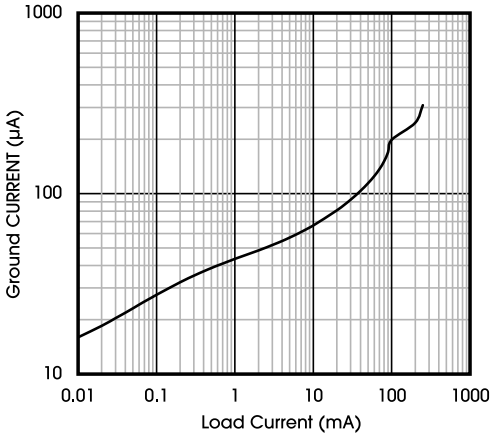


Figure 6. Ground Current vs. I_{LOAD}

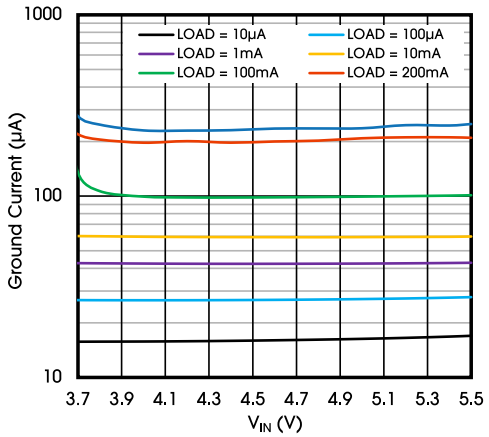


Figure 7. Ground Current vs. V_{IN}

5.7 TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.

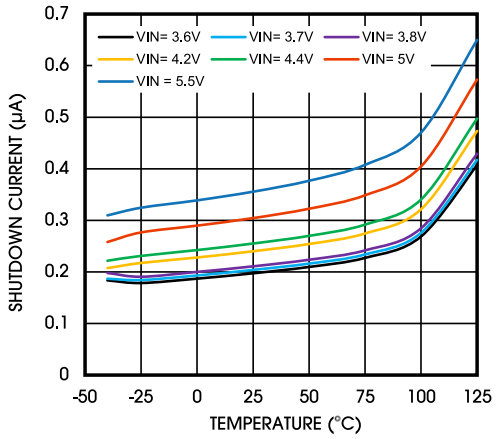


Figure 8. Shutdown Current vs. Temperature at Various Input Voltages

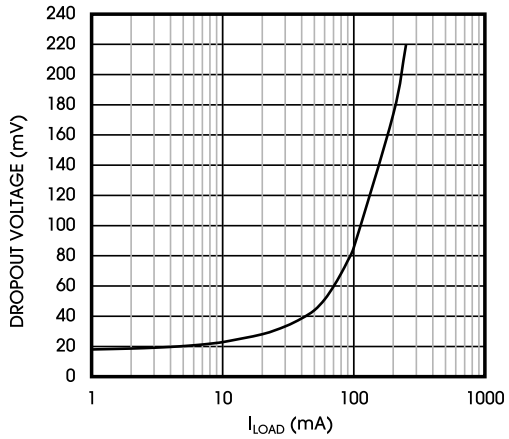


Figure 9. Dropout Voltage vs. I_{LOAD}

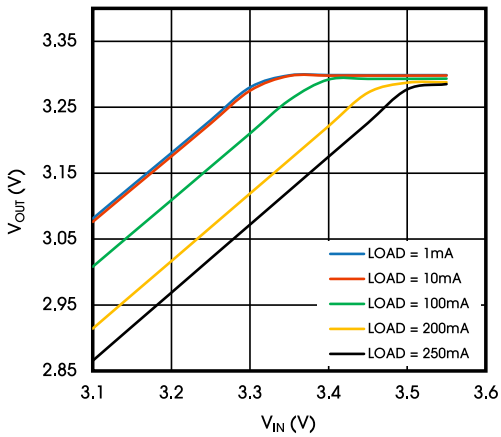


Figure 10. V_{OUT} vs. V_{IN} (in Dropout)

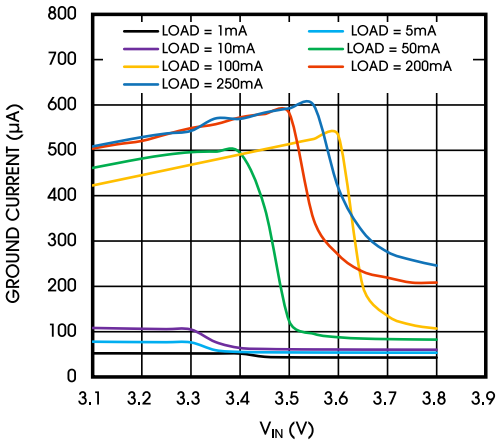


Figure 11. Ground Current vs. V_{IN} (in Dropout)

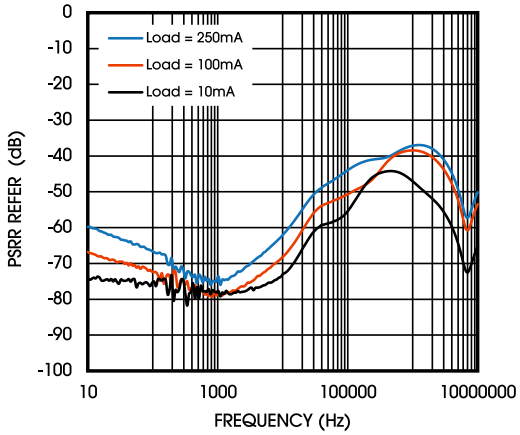


Figure 12. PSRR vs. Frequency, V_{OUT} = 1.2V, V_{IN} = 2.2V

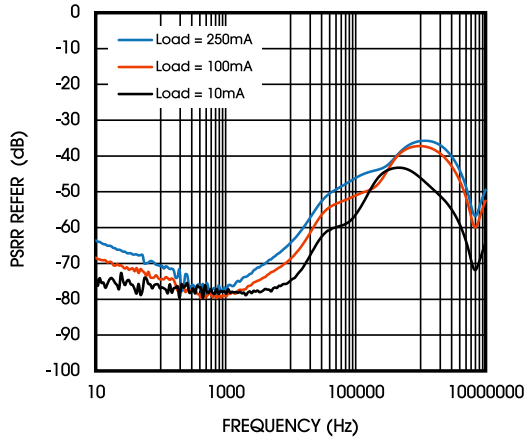


Figure 13. PSRR vs. Frequency, V_{OUT} = 1.8V, V_{IN} = 3.0V

5.8 TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.

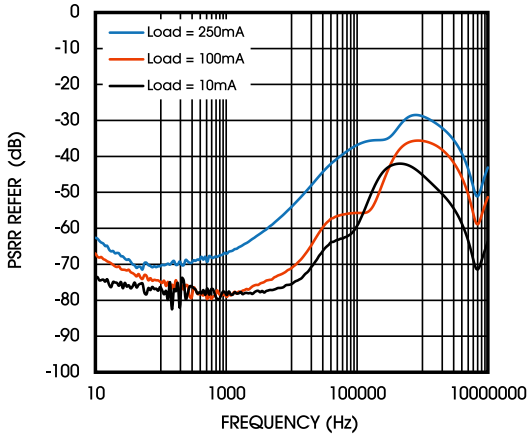


Figure 14. PSRR vs. Frequency, V_{OUT} = 3.3V, V_{IN} = 3.7V

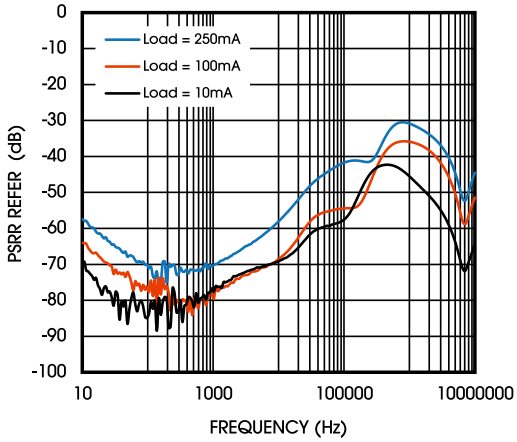


Figure 15. PSRR vs. Frequency, V_{OUT} = 5V, V_{IN} = 5.5V

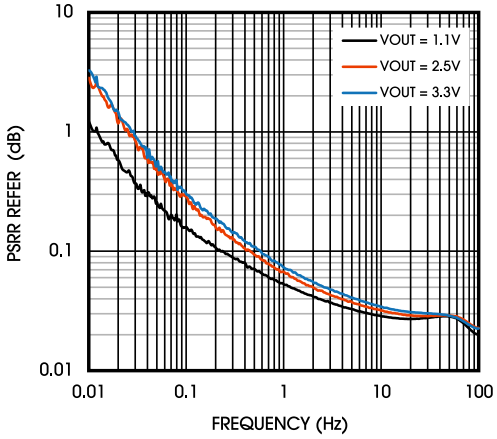


Figure 16. Output Noise vs. Load Current for Various Output Voltages, V_{IN} = 5V, C_{OUT} = 1μF

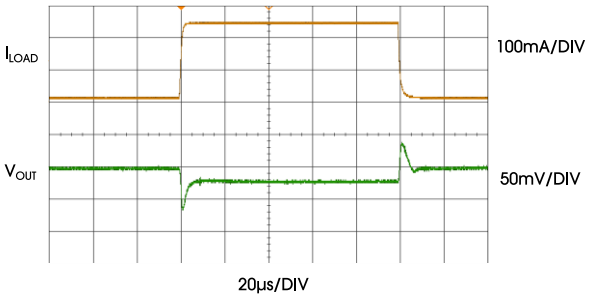


Figure 17. Load Transient Response, C_{IN}, C_{OUT} = 1μF, I_{LOAD} = 1mA to 250mA

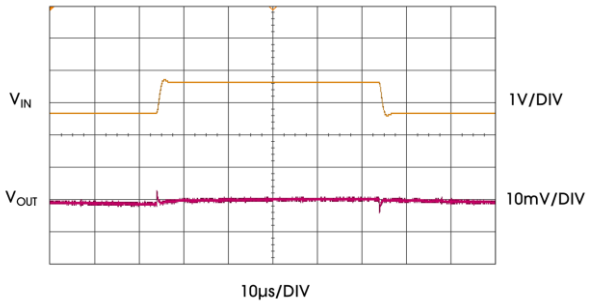


Figure 18. Line Transient Response, C_{IN}, C_{OUT} = 1μF, I_{LOAD} = 250mA

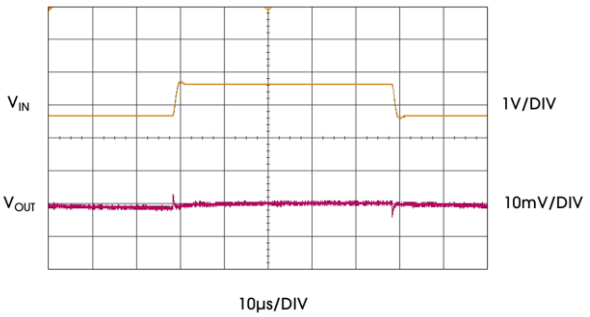


Figure 19. Line Transient Response, C_{IN}, C_{OUT} = 1μF, I_{LOAD} = 1mA

5.9 TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = (V_{OUT} + 0.4V) or 2.2V, EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.

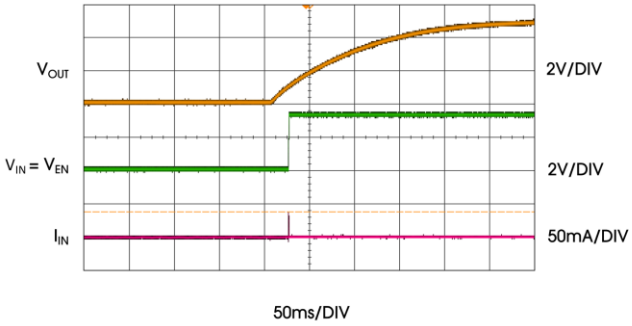


Figure 20. Inrush Current

6. DETAILED DESCRIPTION

6.1 OVERVIEW

The LD501 is an ultra-low noise, low quiescent current, LDO linear regulator that operates from 2.2V to 5.5V and it can provide up to 150mA (LD501L), 200mA (LD501M), or 250mA (LD501P) of output current. As most battery operated, portable equipment applications usually need around 0.3μA shutdown current consumption, LD501 is the ideal option that draws a low operating supply current (typical) at full load—170μA (LD501L), 200μA (LD501M), or 229μA (LD501P).

Using an optimized architecture, the LD501 provides superior noise performance for noise or space sensitive analog and RF applications without the need for a noise bypass capacitor. The LD501 is also optimized for use with small 1μF ceramic capacitors.

6.2 FUNCTIONAL BLOCK DIAGRAM

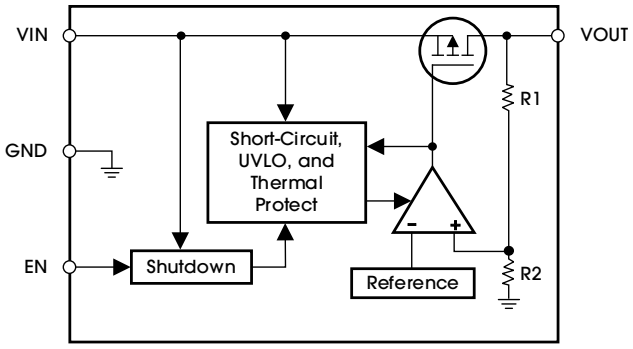


Figure 21. Functional Block Diagram

6.3 FEATURE DESCRIPTION

The LD501 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. The error amplifier compares the reference voltage with the output feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device pulls lower to allow more current to pass and increases the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device pulls higher, allowing less current to pass and decreasing the output voltage. The LD501 supports more than 32 output voltage options, ranging from 1.1V to 5.0V.

The LD501 enables or disables the VOUT pin through the EN pin. To reduce the power consumption, there is no pull-down resistor on the EN pin, hence it is not suggested to leave the EN pin floating at any time.

7. APPLICATION AND IMPLEMENTATION

NOTE

The information provided in this section is not part of the AnalogySemi component specification. Hence, AnalogySemi does not warrant its completeness or accuracy. Customers are responsible for determining suitability of components and system functionality for their applications. Validation and testing should be performed prior to design implementation.

7.1 OUTPUT CAPACITOR

The LD501 supports design with the space-saving ceramic capacitors for most of applications. During the design, the effective series resistance (ESR) value is the key parameter as it affects the stability of the LDO control loop. Usually, a minimum of 1μF capacitor with a 1Ω or less ESR is recommended. A larger capacitance can improve the transient response. Figure 22 shows the transient responses for an output capacitance value of 1μF.

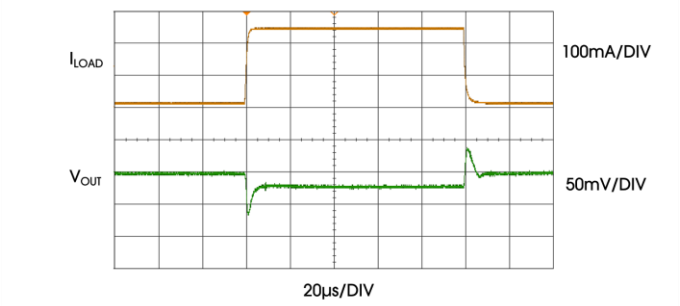


Figure 22. Output Transient Response, C_{OUT} = 1μF

7.2 INPUT BYPASS CAPACITOR

Usually, a 1μF capacitor on the VIN pin helps to reduce the circuit sensitivity to PCB layout. It is always suggested to match the input capacitance of VIN with VOUT capacitance.

7.3 INPUT AND OUTPUT CAPACITOR PROPERTIES

There is no other special requirements of the capacitors for LD501 if the minimum capacitance and the maximum ESR requirements are met. To ensure the minimum capacitance of the ceramic capacitor across temperature range and dc bias condition, the adequate dielectric must be taken into consideration. Usually, X5R or X7R dielectrics rather than Y5V/Z5U with a voltage rating of 6.3V or 10V are recommended.

Equation 1 below is often used to determine the worst case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

Where:

- C_{BIAS} is the effective capacitance at the operating voltage.
- TEMPCO is the worst-case capacitor temperature coefficient.
- TOL is the worst-case component tolerance.

For example, if the worst-case temperature coefficient (TEMPCO) over –40°C to 85°C is 15% for an X5R dielectric, the tolerance of the capacitor (TOL) is 10%, and C_{BIAS} is 0.94μF at 1.8V, which can be obtained from the datasheet of the capacitors.

Substituting these values in Equation 1 yields the following:

$$C_{EFF} = 0.94\mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the LD501, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

7.4 ENABLE FEATURE

The LD501 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. The EN pin has hysteresis to avoid oscillations caused by noise. Figure 23 shows typical active and inactive thresholds of EN when the input voltage varies from 2.2V to 5.5V.

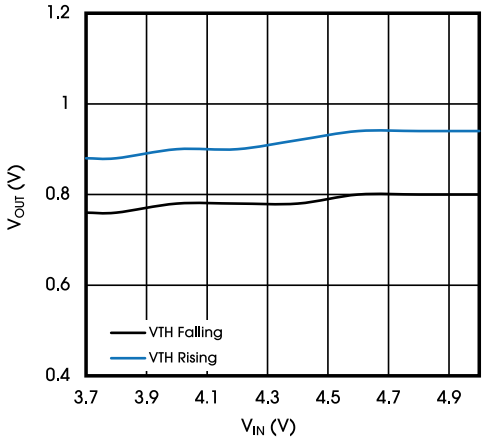


Figure 23. Typical EN Pin Thresholds vs. Input Voltage

The LD501 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3V option is approximately 160μs from the time the EN active threshold is crossed to when the output reaches 90% of its final value.

7.5 ADJUSTABLE OUTPUT VOLTAGE OPERATION

LD501 is possible to implement an adjustable regulator with solution as below:

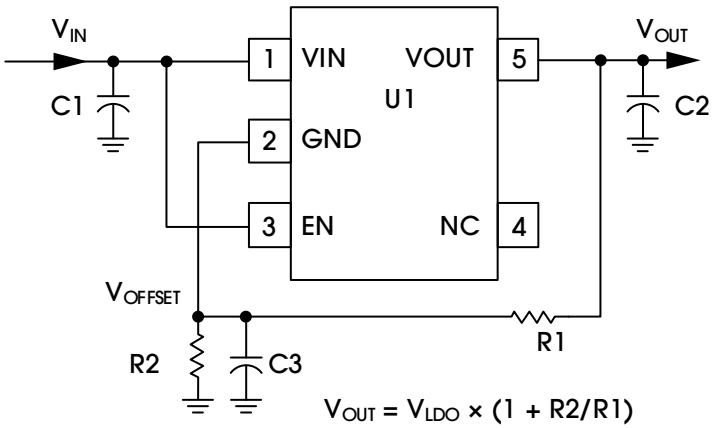


Figure 24. Adjustable LDO Using the LD501

As can be seen in Figure 24 above, the offset voltage (V_{OFFSET}) at GND pin makes the output of LD501 to be VOUT + V_{OFFSET}. The output voltage can be changed by adjusting the V_{OFFSET} even though the VOUT is fixed. However it increases the quiescent current. To minimize the effect variation of the LD501 ground current (I_{GND}) with load, it is best to keep R1 as small as possible. Usually it is suggested to size the current through R2 to at least 20× greater than the maximum expected ground current.

For example, to create a 4V LDO, a 3.3V version of LD501 is more suitable to be chosen as it minimizes value of R2. Because VOUT is 4V, V_{OFFSET} must be 0.7V, and the current through R2 must be 7mA. R1 is, therefore, 3.3V/7mA or 471Ω. A 470Ω standard value introduces less than 1% error and capacitor C3 is necessary to stabilize the LDO. A value of 1μF is adequate.

Note that the method above usually brings worse noise performance, larger quiescent current, and worse PSRR.

The PSRR of the 4V circuit is as much as 10dB poorer than the 3.3V LDO with 500mV of headroom, because the ground current of the LDO varies slightly with input voltage. This, in turn, modulates V_{OFFSET} and reduces the PSRR of the regulator. By increasing the headroom to 1V, the PSRR performance is nearly restored to the performance of the fixed output LDO.

7.6 CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The LD501 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The LD501 is designed to current limit when the output load reaches a typical of 260mA (LD501L), 290mA (LD501M), or 350mA (LD501P). When the output load exceeds 300mA, the output voltage is reduced to maintain a constant current limit.

The LD501 limits the junction temperature to a maximum of 150°C with thermal shutdown function. When the junction temperature starts to rise above 150°C, the output is turned off and the output current is reduced to 0. After the junction temperature drops below 135°C, the output is turned on automatically.

Current limit and thermal limit protections protect the LD501 against accidental overload conditions. It is suggested to limit the power dissipation strictly so that junction temperatures is always below 125°C.

7.6.1 THERMAL CONSIDERATIONS

In most applications, the LD501 does not dissipate much heat due to its high efficiency. However, in applications with a high ambient temperature and a high supply voltage to output voltage differential, the heat dissipated in the package can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. The converter recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the LD501 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 9 shows typical θ_{JA} values of the SOT23-5 for various PCB copper sizes. Table 10 shows the typical Ψ_{JB} values of the SOT23-5.

Table 9. Typical θ_{JA} Values

COPPER SIZE (mm^2)	Θ_{JA} (°C/W)
0(1)	170
50	152
100	146
300	134
500	131

Note: Device soldered to minimum size pin traces.

Table 10. Typical Ψ_{JB} Values

Model	Ψ_{JB} (°C/W)
SOT23-5	36

To calculate the junction temperature of the LD501, use the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

Where:

- T_A is the ambient temperature.
- P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{OUT}) \times I_{LOAD}) + (V_{IN} \times I_{GND}) \quad (3)$$

Where:

- V_{IN} and V_{OUT} are input and output voltages, respectively.
- I_{LOAD} is the load current.
- I_{GND} is the ground current.

Power dissipation due to ground current is small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \left(((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \theta_{JA}\right) \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C.

8. LAYOUT

8.1 LAYOUT GUIDELINES

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the LD501. However, as listed in Table 9, a point of diminishing returns is eventually reached beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and the GND pins. Place the output capacitor as close as possible to the VOUT and the GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

8.2 LAYOUT EXAMPLE

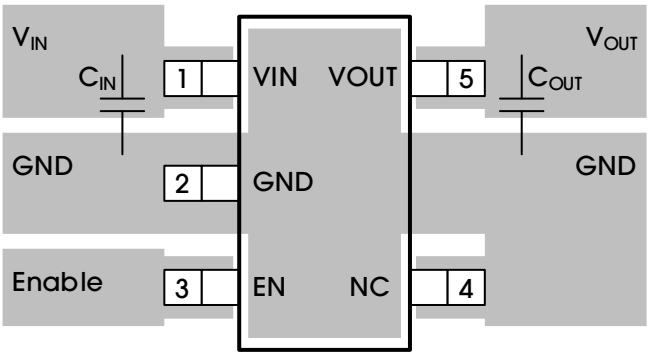


Figure 25. Layout Example

9. PACKAGE INFORMATION

The LD501 family is available in the SOT23-5 package. Figure 26 shows the package view.

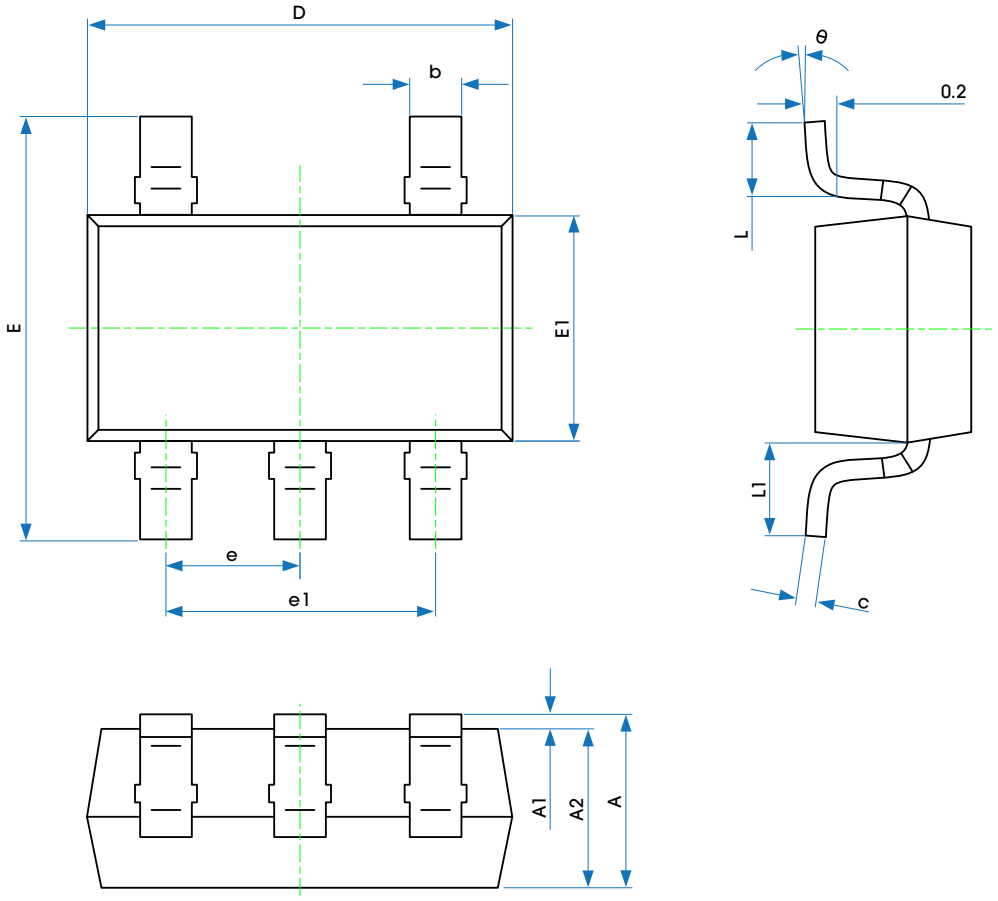


Figure 26. Package View

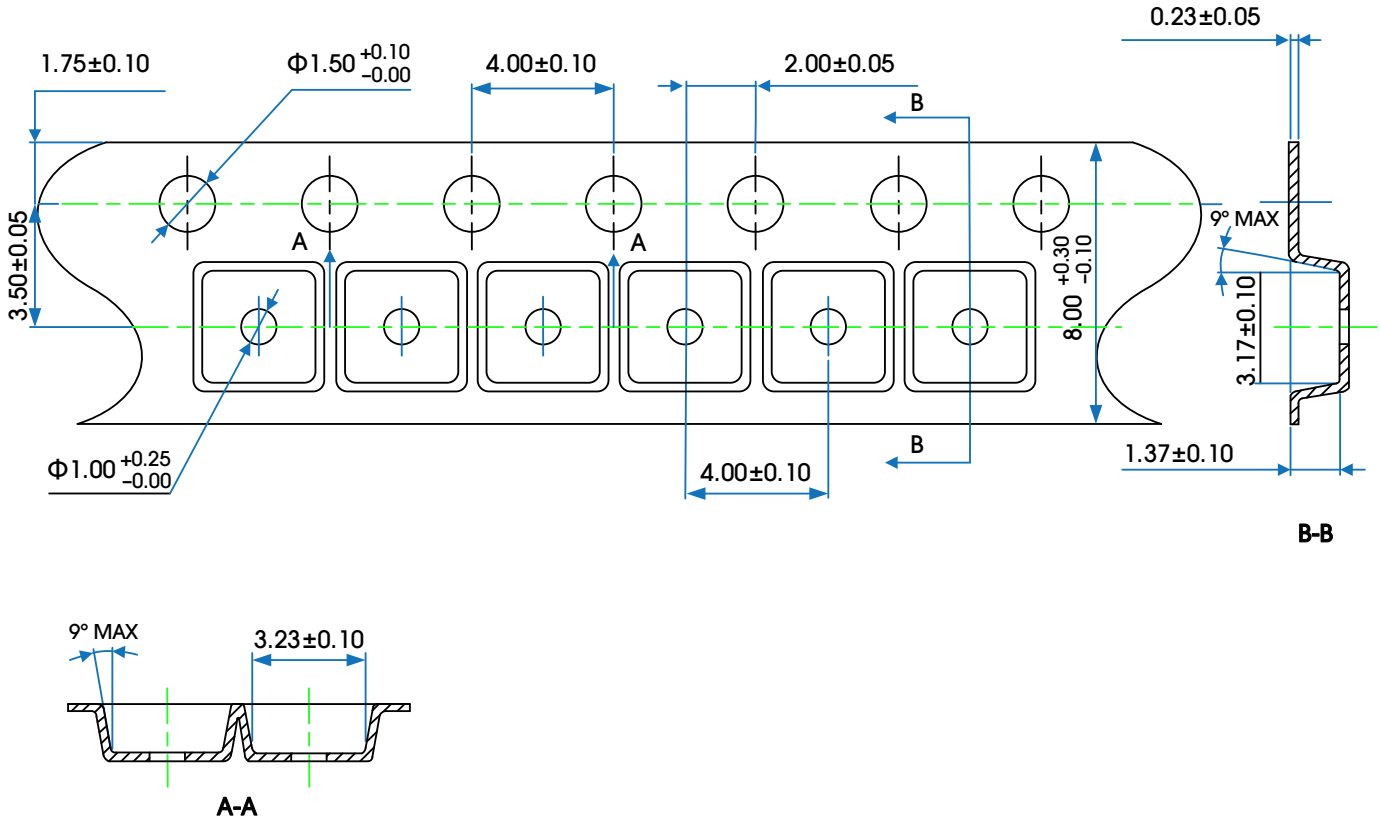
Table 11 provides detailed information about the dimensions.

Table 11. Dimensions

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600 REF.		0.024 REF.	
θ	0°	8°	0°	8°

10. TAPE AND REEL INFORMATION

Figure 27 illustrates the carrier tape.



Notes:
1. Cover tape width: 5.50 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 2mm in 250mm.
4. Mold#: SOT23-5.
5. All dimensions: mm.
6. Direction of view:

Figure 27. Carrier Tape Drawing

Table 12 provides information about tape and reel.

Table 12. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOT23-5	7''	3000	10	4	120000	210*208*203	440*440*230

Figure 28 shows the product loading orientation—pin 1 is assigned on the lower left corner.

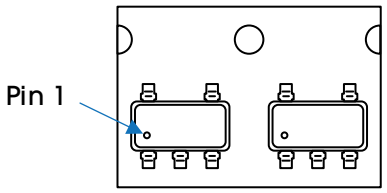


Figure 28. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	21 July 2022	Rev A release.

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