40V, High-Performance, General-Purpose, Zero-Drift Operational Amplifiers

1. FEATURES

- Low offset voltage: 10μV (max)
- Zero-drift: 0.2μV/°C (max)
- Low noise: 17.6nV/$\sqrt{Hz}$
  - 0.1Hz to 10Hz noise: 0.36μV_{PP}
- Excellent DC precision:
  - PSRR: 146dB
  - CMRR: 149dB
  - Open-loop gain: 164dB
- Gain bandwidth: 1MHz
- Quiescent current: 300μA (typ)
- Wide supply range: ±2.25V to ±20V
- Rail-to-rail output
- Input includes negative rail
- RFI filtered inputs
- 1/2 channel

2. APPLICATIONS

- Bridge amplifiers
- Strain gauges
- Transducer applications
- Temperature measurement
- Electronic scales
- Medical instrumentation
- Resistance temperature detectors

3. DESCRIPTION

The OPZ202/2022 devices are high-performance, general-purpose operational amplifiers that support 4.5V to 40V supply range. With extremely low input offset voltage of 10μV (maximum) and a high CMRR of 149dB, the OPZ202/2022 operational amplifiers provide excellent initial accuracy and rail-to-rail output. The devices work well with both single-supply convenient portable equipment and differential output scenarios.

The OPZ202/2022 family provides up to 1MHz bandwidth, 2.8V/μs slew rate, and outstanding DC performance, which is rather suitable for active filter circuits.

The OPZ202/2022 operational amplifiers are offered in the SOT23-5 and SOIC-8 packages. All versions are specified from –40°C to 125°C. See Table 1 for the order information.

Bridge Amplifier

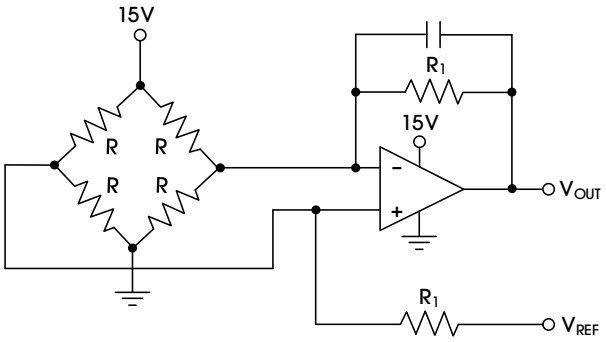


Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER	CH (#)	PACKAGE	MARK	V_{OS} (MAX) (μV)	V_{CC} (V)	I_Q PER CH (TYP) (μA)	GBW (kHz)	SLEW RATE (TYP) (V/μs)	NOISE (TYP) (nV/√Hz)	RAIL-TO-RAIL	OP. TEMP (°C)	RATING	PKG. OPTION
OPZ202BSOT235	1	SOT23-5	OPZ202	±10	4.5-40	300	1000	2.8	17.6	IN/OUT	-40-125	Industry	T/R-3000
OPZ202BSOIC8	1	SOIC-8	OPZ202	±10	4.5-40	300	1000	2.8	17.6	IN/OUT	-40-125	Industry	T/R-4000
OPZ2022BSOIC8	2	SOIC-8	OPZ2022	±10	4.5-40	300	1000	2.8	17.6	IN/OUT	-40-125	Industry	T/R-4000

Table 2. Family Selection Guide

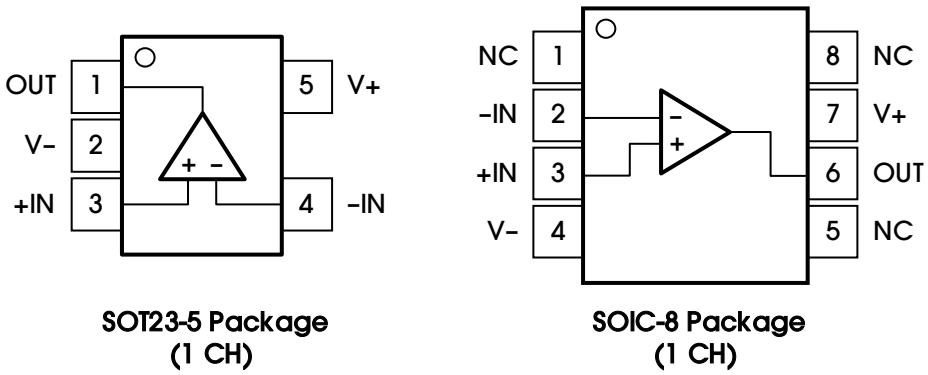
ORDER NUMBER	CH (#)	PACKAGE	MARK	V_{OS} (MAX) (μV)	V_{CC} (V)	I_Q PER CH (TYP) (μA)	GBW (kHz)	SLEW RATE (TYP) (V/μs)	NOISE (TYP) (nV/√Hz)	RAIL-TO-RAIL	OP. TEMP (°C)	RATING	PKG. OPTION
OPZ102BSOT235	1	SOT23-5	OPZ102	±15	4.5-40	150	300	0.8	35	IN/OUT	-40-125	Industry	T/R-3000
OPZ102BSOIC8	1	SOIC-8	OPZ102	±15	4.5-40	150	300	0.8	35	IN/OUT	-40-125	Industry	T/R-4000
OPZ1022BSOIC8	2	SOIC-8	OPZ1022	±15	4.5-40	150	300	0.8	35	IN/OUT	-40-125	Industry	T/R-4000
OPZ302BSOT235	1	SOT23-5	OPZ302	±10	4.5-40	600	2200	3.8	11.6	IN/OUT	-40-125	Industry	T/R-3000
OPZ302BSOIC8	1	SOIC-8	OPZ302	±10	4.5-40	600	2200	3.8	11.6	IN/OUT	-40-125	Industry	T/R-4000
OPZ3022BSOIC8	2	SOIC-8	OPZ3022	±10	4.5-40	600	2200	3.8	11.6	IN/OUT	-40-125	Industry	T/R-4000

Devices can be ordered via the following two ways:

1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration (1 CH devices).



SOT23-5 Package
(1 CH)

SOIC-8 Package
(1 CH)

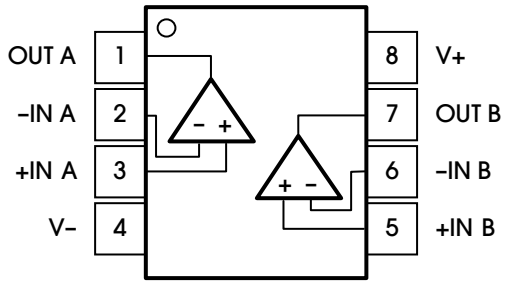
Figure 1. Pin Configuration (1 CH Devices)

Table 3 lists the pin functions (1 CH devices).

Table 3. Pin Functions (1 CH Devices)

POSITION		NAME	TYPE	DESCRIPTION
SOT23-5	SOIC-8			
1	6	OUT	Output	Output
2	4	V–	Power	Negative (lowest) power supply
3	3	+IN	Input	Positive (non-inverting) input
4	2	–IN	Input	Negative (inverting) input
5	7	V+	Power	Positive (highest) power supply
—	1, 5, 8	NC	I/O	No internal connection (can be left floating)

Figure 2 illustrates the pin configuration (2 CH devices).



SOIC-8 Package
(2 CH)

Figure 2. Pin Configuration (2 CH Devices)

Table 4 lists the pin functions (2 CH devices).

Table 4. Pin Functions (2 CH Devices)

POSITION	NAME	TYPE	DESCRIPTION
1	OUT A	Ouput	Output, channel A
2	–IN A	Input	Inverting input, channel A
3	+IN A	Input	Non-inverting input, channel A
4	V–	Power	Negative (lowest) power supply
5	+IN B	Input	Non-inverting input, channel B
6	–IN B	Input	Inverting input, channel B
7	OUT B	Output	Output, channel B
8	V+	Power	Positive (highest) power supply

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 5 lists the absolute maximum ratings of the OPZ202/2022.

Table 5. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Supply	Split	±2.25	±20	V
		Single	4.5	40	
	Signal input pins(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential		±0.7	
Current	Signal input pins			±10	mA
	Output short-circuit(3)		Continuous		
Temperature	Operating, T_A(4)		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

Note 1: Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 7. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
Note 3: Short-circuit to ground, V–, or V+.
Note 4: Provided device does not exceed maximum junction temperature (T_J) at any time.

5.2 ESD RATINGS

Table 6 lists the ESD ratings of the OPZ202/2022.

Table 6. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 7 lists the recommended operating conditions for the OPZ202/2022.

Table 7. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNITS
Operating Voltage Range	Split supply	±2.25		±20	V
	Single supply	4.5		40	V
Specified Temperature Range		–40		125	°C

5.4 THERMAL INFORMATION

Table 8 lists the thermal information for the OPZ202/2022.

Table 8. Thermal Information

PARAMETER	SYMBOL	SOT23-5	SOIC-8	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	168	90.6	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	39	47.6	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	10	3.6	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	36	47	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	103	35	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	66	50.8	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 9 lists the electrical characteristics of the OPZ202/2022. T_A = 25°C, V_S = ±4V to ±20V (V_S = 8V to 40V), R_L = 10kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

Table 9. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}			±1.7	±10	μV
		T_A = –40°C to 125°C		±0.03	±0.2	μV/°C
Power-Supply Rejection Ratio	PSRR	V_S = 4.5V to 40V, T_A = –40°C to 125°C		±0.05	±0.25	μV/V
Long-Term Stability(2)				4		μV
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S / 2		±100	±1000	pA
		T_A = –40°C to 125°C			±15	nA
Input Offset Current	I_{OS}			±250	±2500	pA
		T_A = –40°C to 125°C			±6	nA
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz		360		nV_{P-P}
		f = 0.1Hz to 10Hz		55		nVrms
Input Voltage Noise Density		f = 1kHz		17.6		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1kHz		214		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	T_A = –40°C to 125°C	V–		(V+) – 1.5	V
Common-Mode Rejection Ratio	CMRR	(V–) < V_{CM} < (V+) – 1.5V	135	153		dB
		(V–) + 0.5V < V_{CM} < (V+) – 1.5V, V_S = ±20V	136	149		dB
		(V–) + 0.5V < V_{CM} < (V+) – 1.5V, V_S = ±20V, T_A = –40°C to 125°C	133			dB
INPUT IMPEDANCE						
Differential	Z_{ID}			100 || 6		MΩ || pF
Common-Mode	Z_{IC}			6 || 9.5		10^{12}Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.5V < V_O < (V+) – 0.5V	135	164		dB
		(V–) + 0.5V < V_O < (V+) – 0.5V, T_A = –40°C to 125°C	128			dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			1		MHz
Slew Rate	SR	G = 1		2.8		V/μs
Settling Time 0.1%	t_S	V_S = ±20V, G = 1, 10V step		10		μs
Settling Time 0.01%	t_S	V_S = ±20V, G = 1, 10V step		50		μs
Overload Recovery Time	t_{OR}	V_{IN} × G = V_S		1		μs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT						
Voltage Output Swing from Rail		No load		5	15	mV
		R_L = 10kΩ		100	200	mV
		T_A = –40°C to 125°C			260	mV
Short-Circuit Current	I_{SC}	Sinking		–20		mA
		Sourcing		29		mA
Open-Loop Output Resistance	R_O	f = 1MHz, I_O = 0		120		Ω
Capacitive Load Drive	C_{LOAD}			1		nF
POWER SUPPLY						
Quiescent Current per Amplifier	I_Q	V_S = ±4.5V to V_S = ±20V		300	362	μA
		I_O = 0mA, T_A = –40°C to 125°C			420	μA

Note 1: V_S / 2 = mid-supply.
Note 2: 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4μV.

6. TYPICAL CHARACTERISTICS

V_S = ±18V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF, unless otherwise noted.

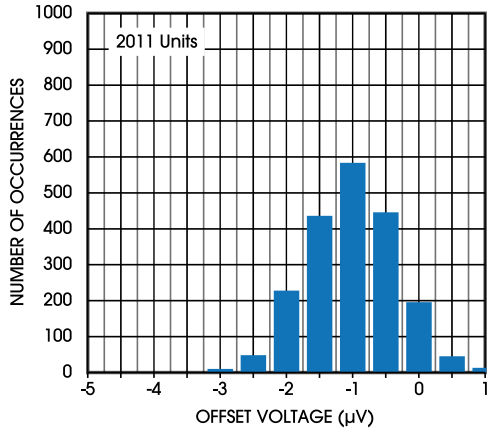


Figure 3. Offset Voltage Production Distribution

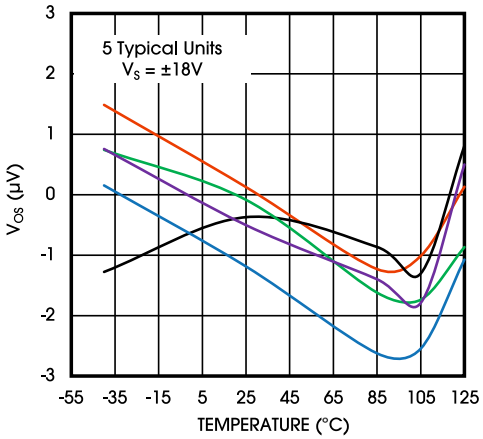


Figure 4. Offset Voltage vs. Temperature

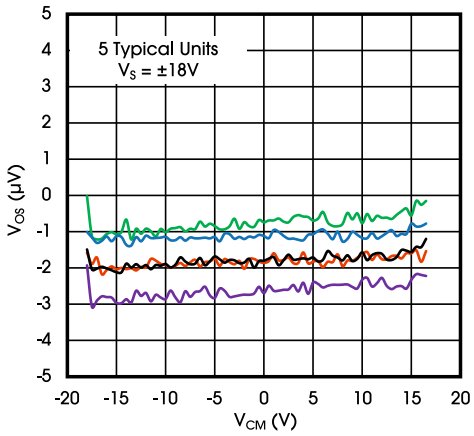


Figure 5. Offset Voltage vs. Common-Mode Voltage (±18V)

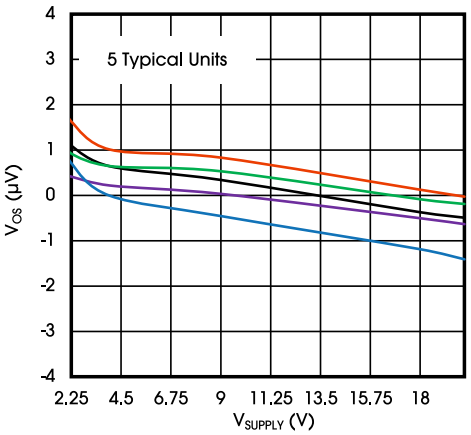


Figure 6. Offset Voltage vs. Power Supply

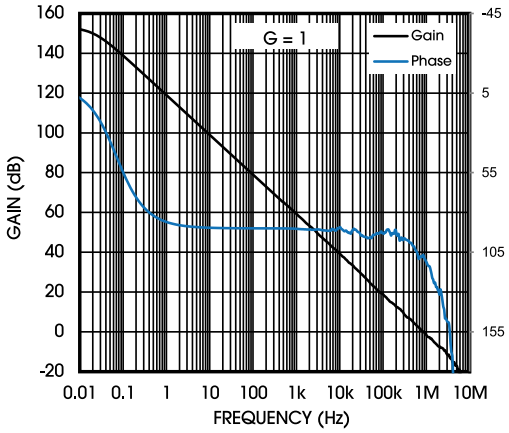


Figure 7. Open-Loop Gain and Phase vs. Frequency

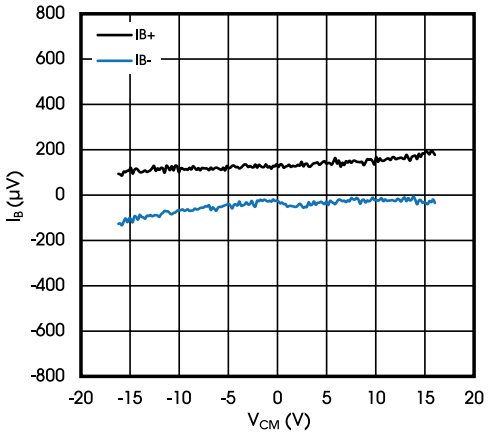


Figure 8. I_B and I_{OS} vs. Common-Mode Voltage

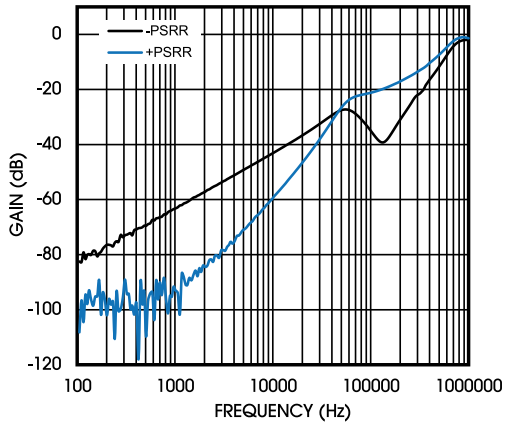


Figure 9. PSRR vs. Frequency (Referred-to-Input)

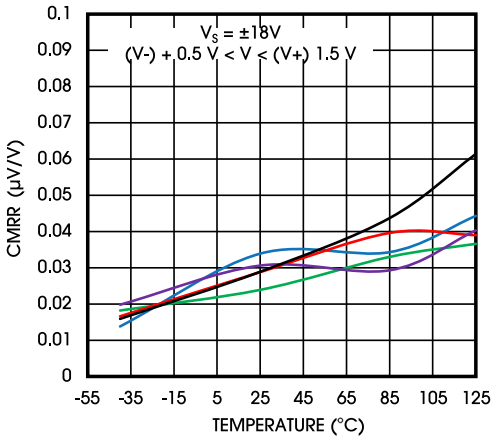


Figure 10. CMRR vs. Temperature

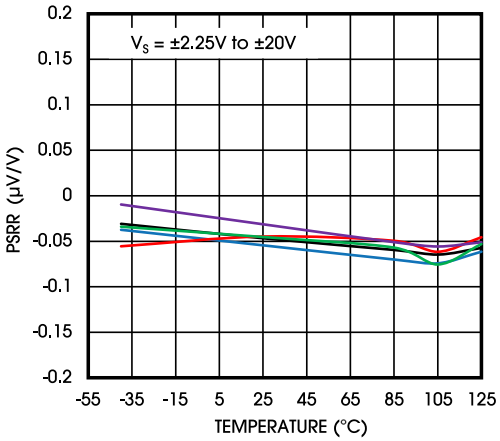


Figure 11. PSRR vs. Temperature

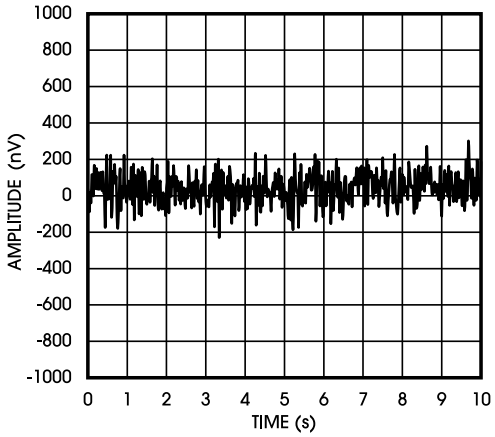


Figure 12. Noise (0.1Hz to 10Hz)

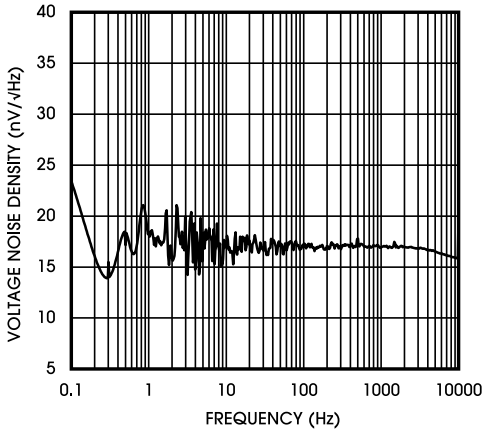


Figure 13. Input Voltage Noise Spectral Density vs. Frequency

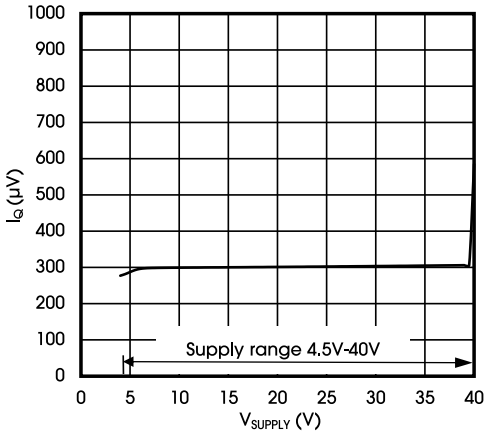


Figure 14. Quiescent Current vs. Supply Voltage

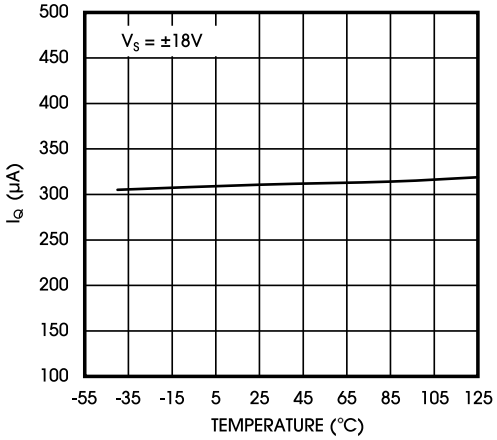


Figure 15. Quiescent Current vs. Temperature

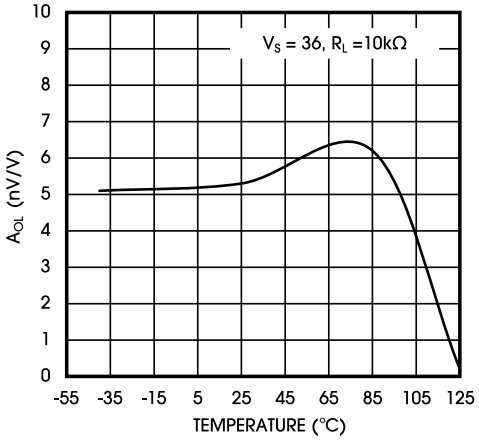


Figure 16. Open-Loop Gain vs. Temperature

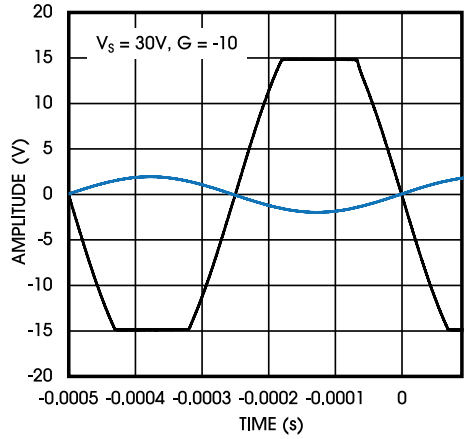


Figure 17. No Phase Reversal

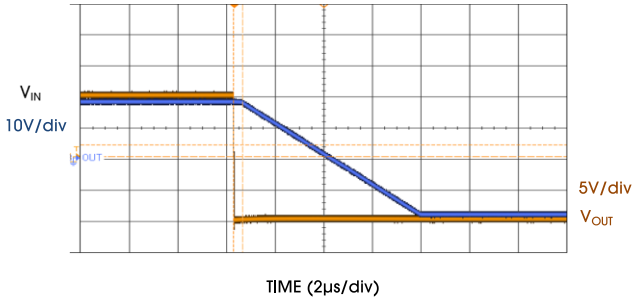


Figure 18. Positive Overload Recovery

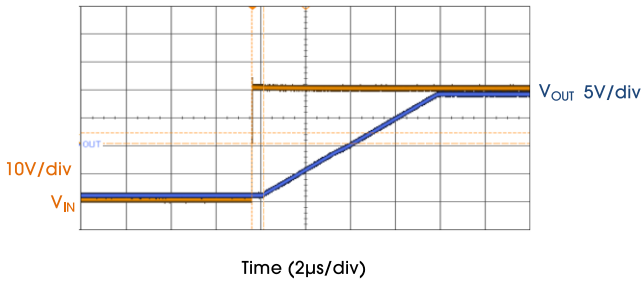


Figure 19. Negative Overload Recovery

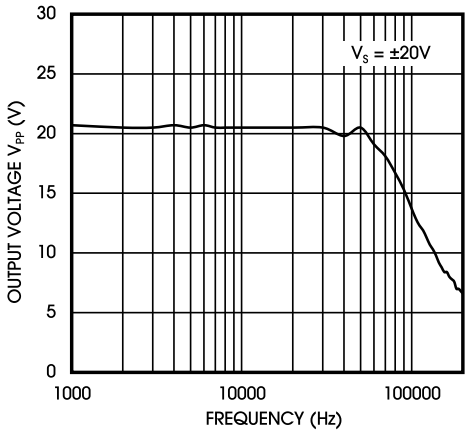


Figure 20. Maximum Output Voltage vs. Frequency

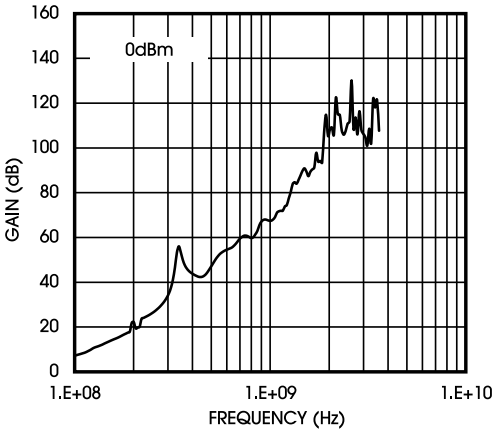


Figure 21. EMIRR IN+ vs. Frequency

7. DETAILED DESCRIPTION

7.1 OVERVIEW

The OPZ202/2022 devices are high-performance, zero-drift operational amplifiers that support 4.5V-40V supply range. With extremely low input offset voltage of max 10μV, 0.2μV/°C and excellent high CMRR, PSRR, and A_{OL}, the OPZ202/2022 devices provide excellent initial accuracy and rail-to-rail output. The devices also provide up to 1MHz bandwidth, and 2.8V/μs slew rate. The OPZ202/2022 devices are part of the zero-drift, low-power operational amplifiers family. Their architecture can also provide outstanding AC performance like ultra-low broadband noise and zero flicker noise.

7.2 FUNCTIONAL BLOCK DIAGRAM

Figure 22 shows the OPZ202/2022 functional block diagram.

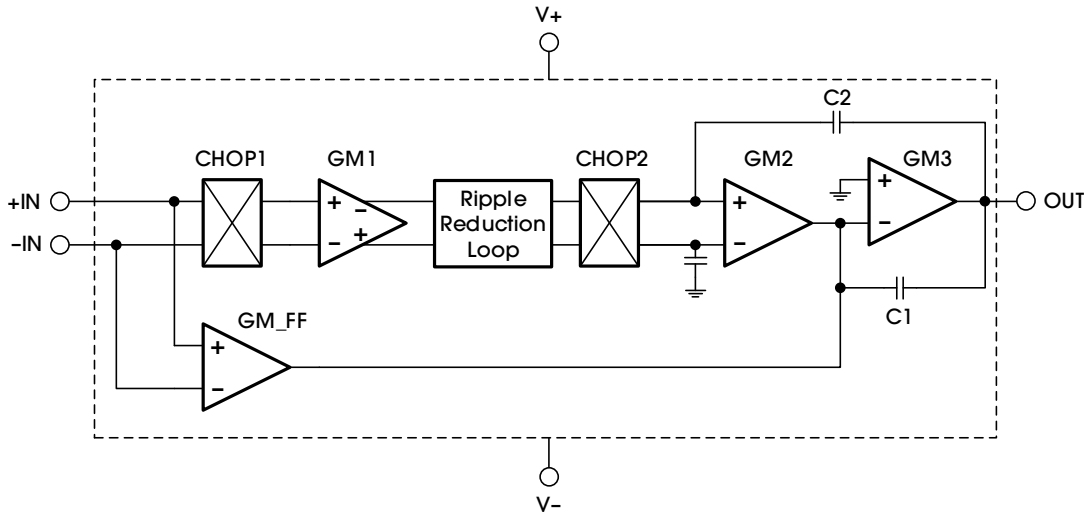


Figure 22. Functional Block Diagram

7.3 FEATURE DESCRIPTION

The OPZ202/2022 devices are unity-gain stable and use an auto-calibration technique to provide low offset voltage and very low drift over time and temperature. In order to achieve better precision performance, it is suggested to avoid temperature gradients, dissimilar metals, and direct air currents in design.

7.3.1 OPERATING CHARACTERISTICS

The OPZ202/2022 devices are specified for operation from 4.5V to 40V (±2.25V to ±20V). Many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in TYPICAL CHARACTERISTICS.

7.3.2 PHASE-REVERSAL PROTECTION

Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPZ202/2022 input prevents phase reversal with excessive common-mode voltage.

7.3.3 INPUT BIAS CURRENT CLOCK FEEDTHROUGH

The OPZ202/2022 devices use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. The switches on the input can introduce short transients in the input bias current that may be coupled to the output of the amplifiers. When the issue is found, it is suggested to add RC low-power filter in the output of the amplifier.

7.3.4 INTERNAL OFFSET CORRECTION

The OPZ202/2022 operational amplifiers use an auto-calibration technique to obtain low offset. Upon power-up, the auto-calibration circuit works to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.5 CAPACITIVE LOAD AND STABILITY

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50Ω) in series with the output.

7.3.6 ELECTRICAL OVERSTRESS

The OPZ202/2022 devices are designed to withstand high electrical overstress and accidental ESD events. Usually, the input pins of device are the most challenging for designers. The OPZ202/2022 devices have enhanced the protection from both overstress and ESD side. However, to avoid overstress failure or ESD events, keep the OPZ202/2022 work within the specifications.

7.4 DEVICE FUNCTIONAL MODES

The OPZ202/2022 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The maximum power supply voltage for the OPZ202/2022 is 40V (±20V).

8. APPLICATION AND IMPLEMENTATION

NOTE

The information provided in this section is not part of the AnalogySemi component specification. Hence, AnalogySemi does not warrant its completeness or accuracy. Customers are responsible for determining suitability of components and system functionality for their applications. Validation and testing should be performed prior to design implementation.

8.1 APPLICATION INFORMATION

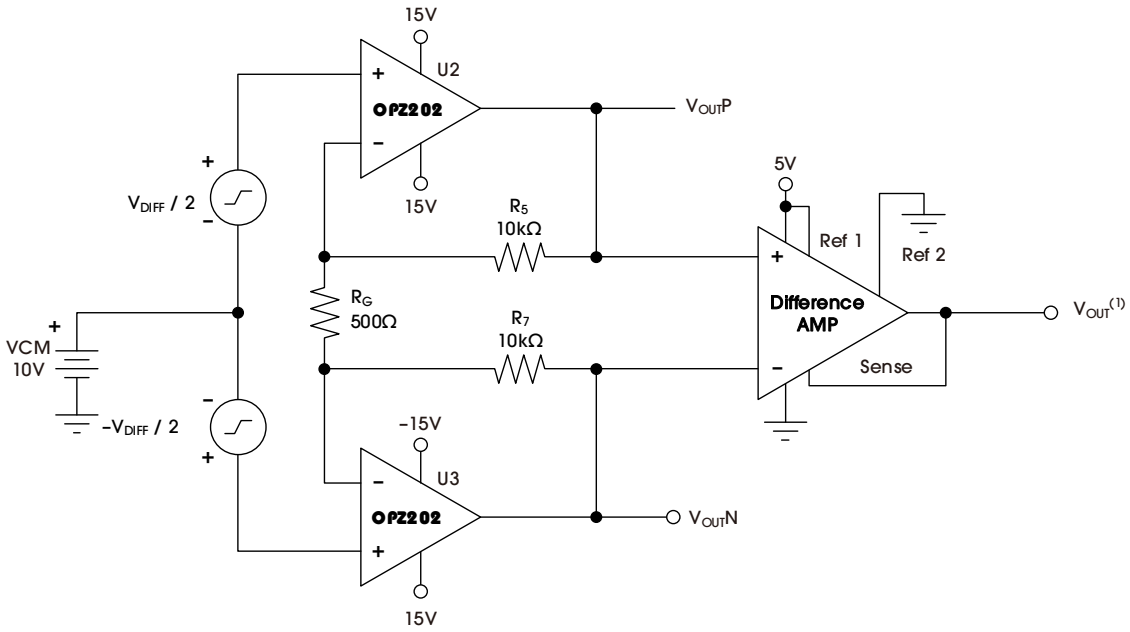
The OPZ202/2022 operational amplifier combines precision offset and drift with excellent overall performance, making this device an excellent choice for many precision applications. The precision offset drift of only 0.2μV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1μF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPZ202/2022 can be used.

8.2 TYPICAL APPLICATIONS

8.2.1 DISCRETE INA + ATTENUATION FOR ADC WITH 3.3V SUPPLY

Figure 23 shows an example of how the OPZ202/2022 is used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. A difference amplifier provides the attenuation that allows this circuit to easily interface with 3.3V or 5V analog-to-digital converters (ADCs).



(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref\ 1) / 2$.

Figure 23. Discrete INA + Attenuation for ADC With 3.3V Supply

8.2.2 BRIDGE AMPLIFIER

Figure 24 shows the basic configuration for a bridge amplifier.

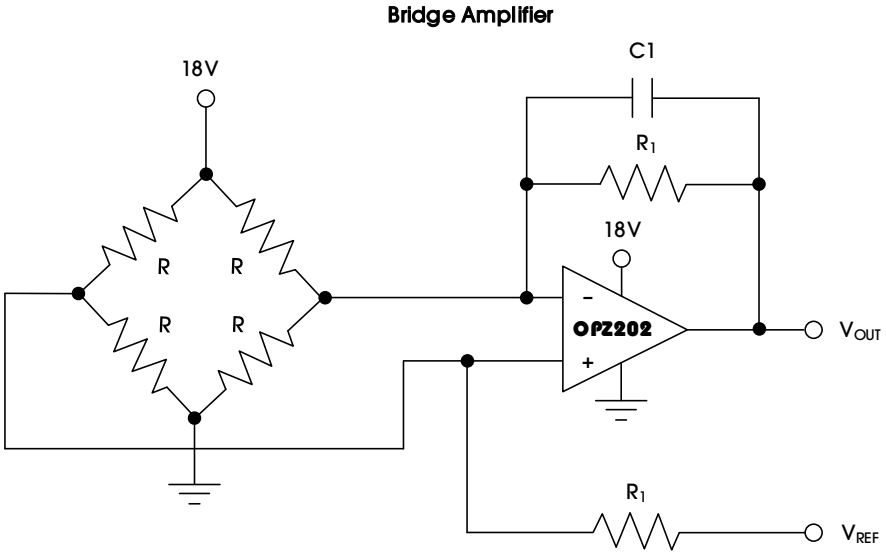


Figure 24. Bridge Amplifier

8.2.3 LOW-SIDE CURRENT MONITOR

Figure 25 shows the OPZ202/2022 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPZ202/2022, with a gain of 201. The load current is set from 0A to 500mA, which corresponds to an output voltage range from 0V to 10V. The output range can be adjusted by changing the shunt resistor or gain of the configuration.

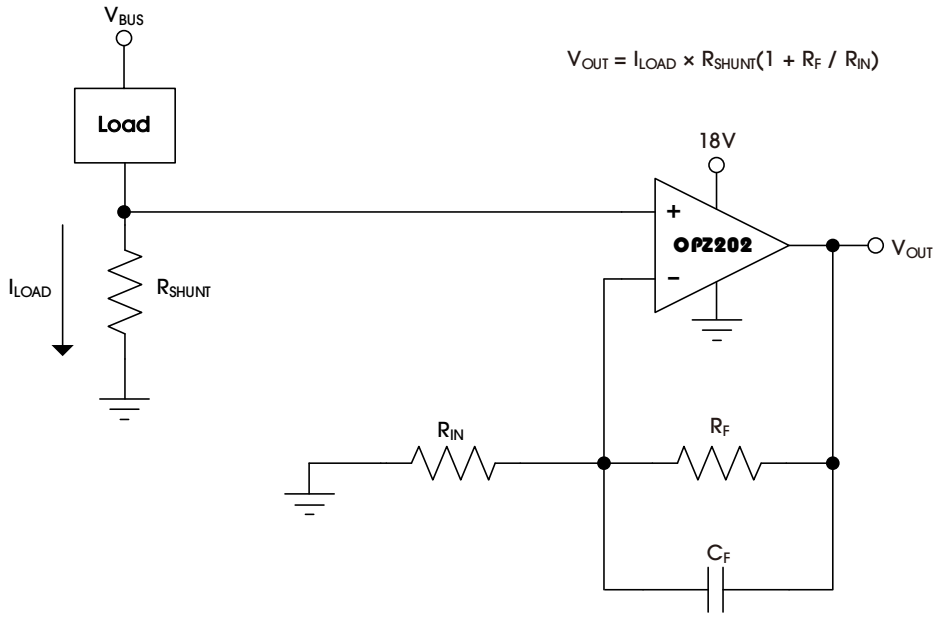
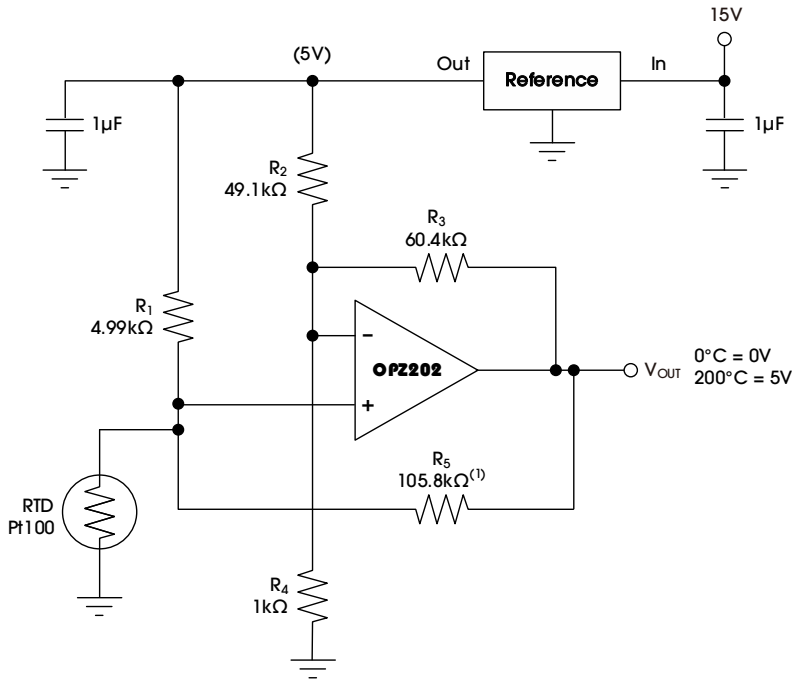


Figure 25. Low-Side Current Monitor

8.2.4 RTD AMPLIFIER WITH LINEARIZATION

See Analog Linearization Of Resistance Temperature Detectors for an in-depth analysis of Figure 26.



(1) R_5 provides positive-varying excitation to linearize output.

Figure 26. RTD Amplifier With Linearization

9. POWER SUPPLY RECOMMENDATIONS

The OPZ202/2022 devices are specified for operation from 4V to 40V (±2V to ±20V); many specifications apply from –40°C to 125°C. TYPICAL CHARACTERISTICS presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40V can permanently damage the device (see the ABSOLUTE MAXIMUM RATINGS).

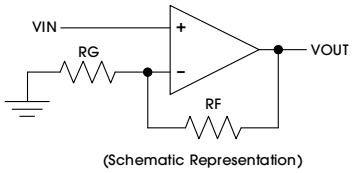
10. LAYOUT

10.1 LAYOUT GUIDELINES

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect Low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- Use a ground plane to help distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 LAYOUT EXAMPLE



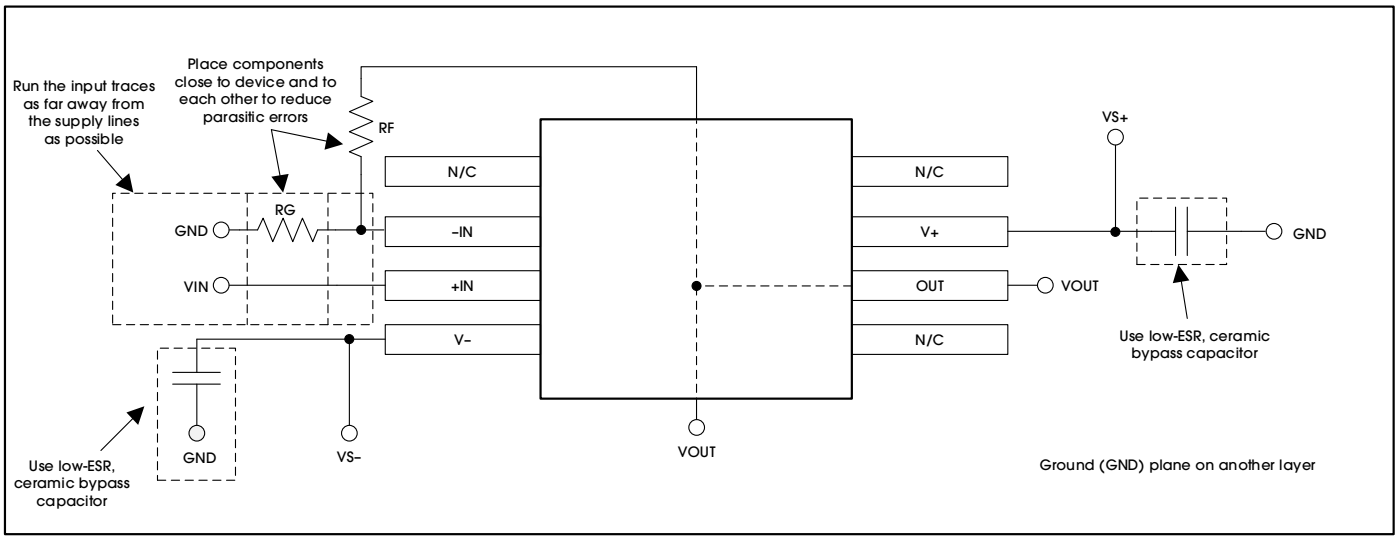


Figure 27. Layout Example

11. PACKAGE INFORMATION

The OPZ202/2022 devices are available in the SOT23-5 and SOIC-8 packages.

11.1 SOT23-5 PACKAGE

Figure 28 shows the SOT23-5 package view.

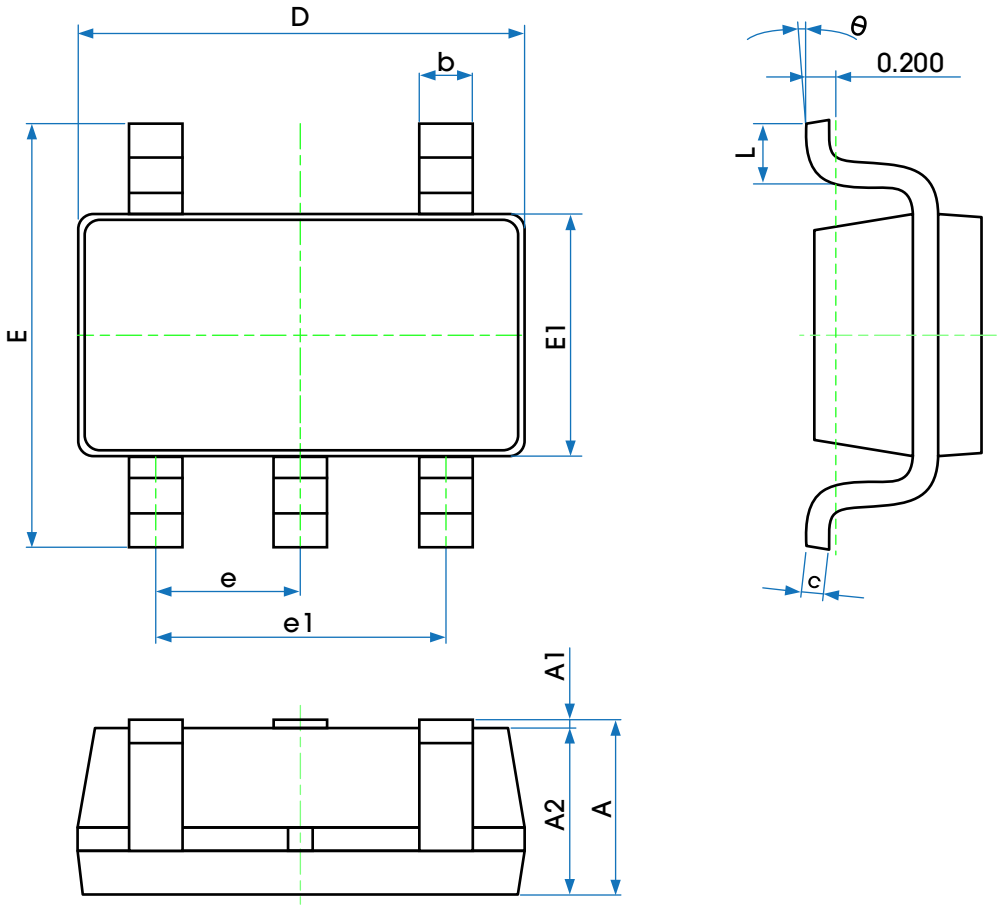


Figure 28. SOT23-5 Package View

Table 10 provides detailed information about the dimensions of the SOT23-5 package.

Table 10. Dimensions of the SOT23-5 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

11.2 SOIC-8 PACKAGE

Figure 29 shows the SOIC-8 package view.

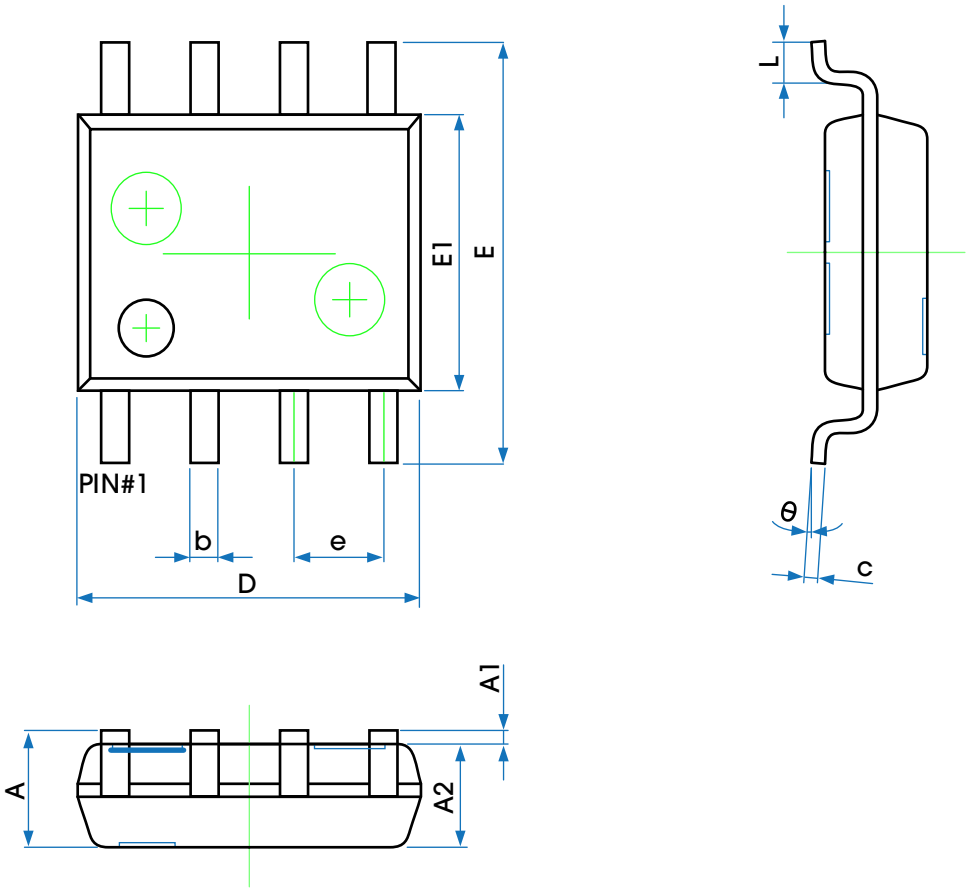


Figure 29. SOIC-8 Package View

Table 11 provides detailed information about the dimensions of the SOIC-8 package.

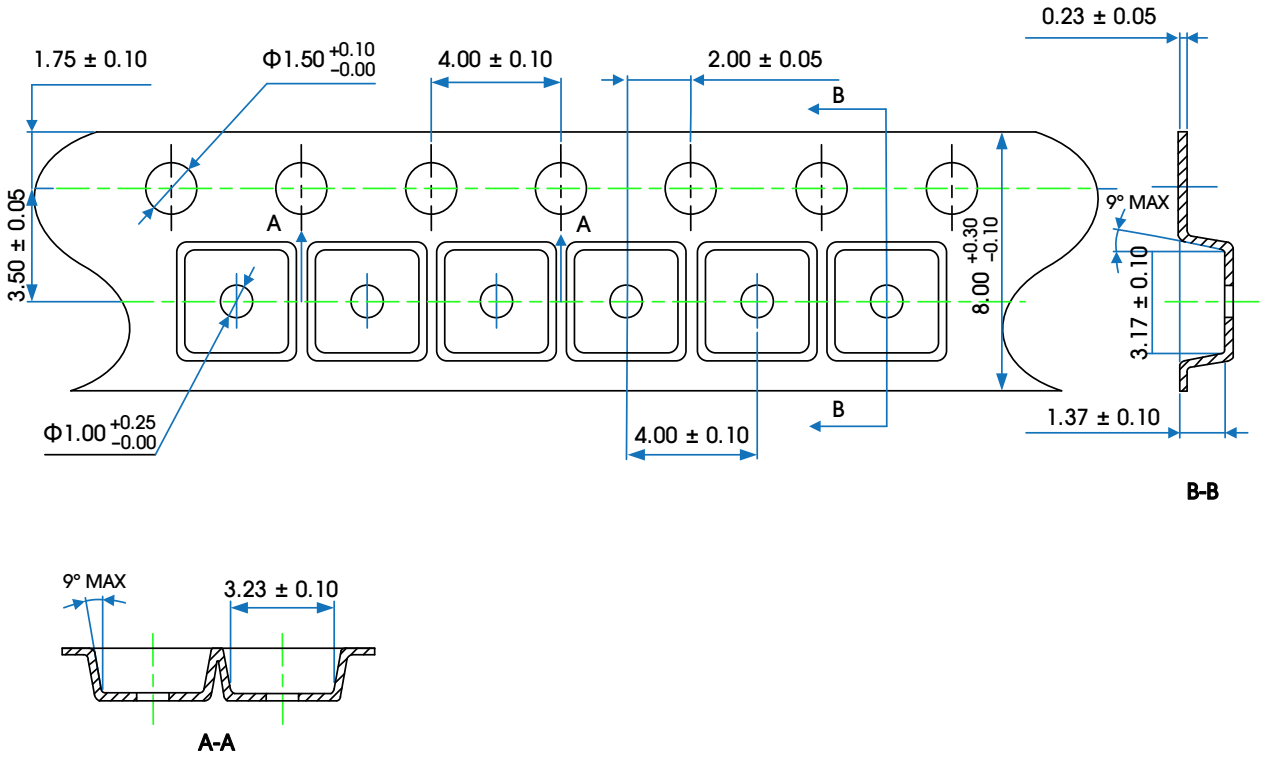
Table 11. Dimensions of the SOIC-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

12. TAPE AND REEL INFORMATION

12.1 SOT23-5 PACKAGE

Figure 30 illustrates the carrier tape.



Notes:
1. Cover tape width: 5.50 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 2mm in 250mm.
4. Mold#: SOT23-5.
5. All dimensions: mm.
6. Direction of view:

Figure 30. Carrier Tape Drawing

Table 12 provides information about tape and reel.

Table 12. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOT23-5	7''	3000	10	4	120000	210*208*203	440*440*230

Figure 31 shows the product loading orientation—pin 1 is assigned at Q3.

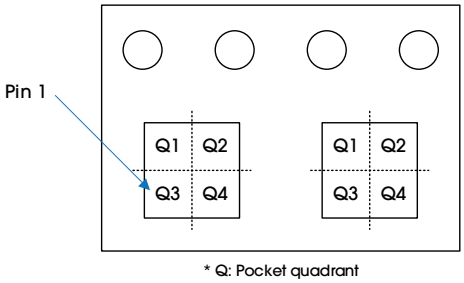
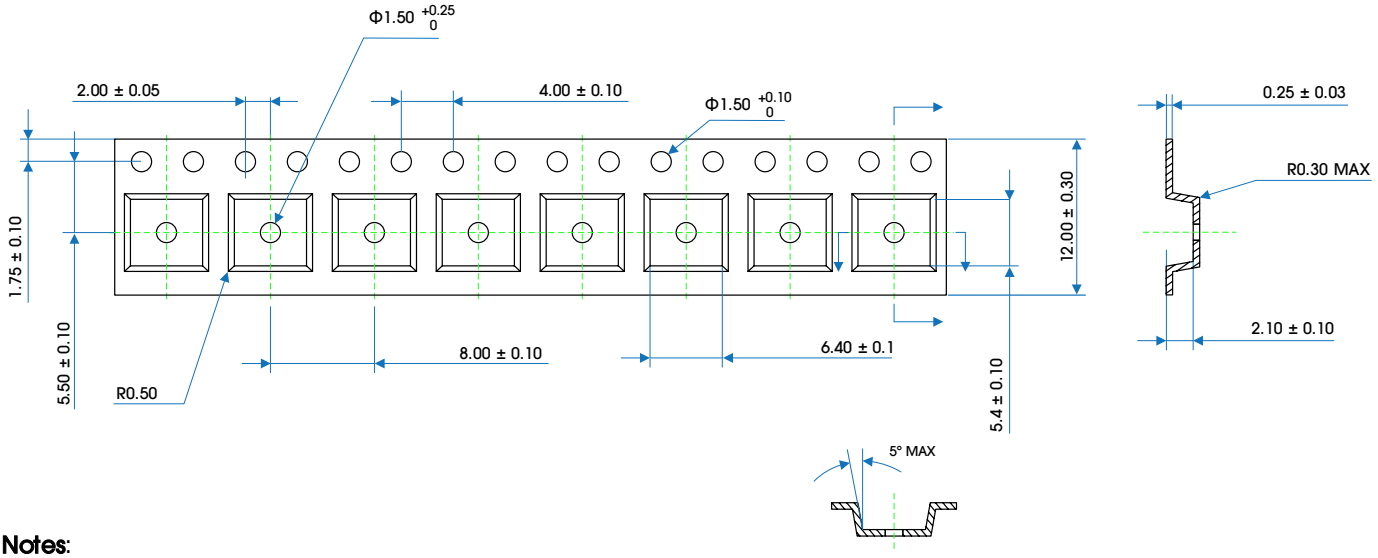


Figure 31. Product Loading Orientation

12.2 SOIC-8 PACKAGE

Figure 32 illustrates the carrier tape.



Notes:
1. Cover tape width: 9.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: SOIC-8.
5. All dimensions: mm.
6. Direction of view:

Figure 32. Carrier Tape Drawing

Table 13 provides information about tape and reel.

Table 13. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOIC-8	13''	4000	1	8	32000	358*340*50	430*380*390

Figure 33 shows the product loading orientation—pin 1 is assigned at Q1.

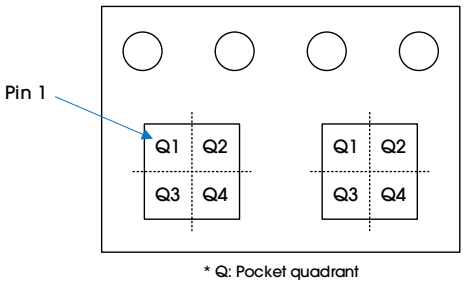


Figure 33. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	14 December 2022	Rev A release.

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