



Analog Semiconductor IC

VDD Series

Low voltage, Low power, $\pm 1\%$ High detect accuracy
CMOS Voltage Detector with Delay circuit

(IMPORTANT: Please check the last page for Genuine Product Labeling)

Rev. E13-01

Website: www.anasemi.com
Tel: +852-3590-8442
Email: sales@anasemi.com

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Low voltage, Low power, $\pm 1\%$ High detect accuracy with delay circuit CMOS Voltage Detector

VDD Series

GENERAL DESCRIPTIONS

The VDD series are delay circuit built-in voltage detectors with low voltage, low power consumption and high accuracy. The accuracy of the detection voltage is detected based on a voltage reference of high accuracy that the temperature coefficient is controlled. The detection voltage is made in high accuracy by using the laser trimming technology. Because the delay circuit is built-in, delay time can be set without any external components.



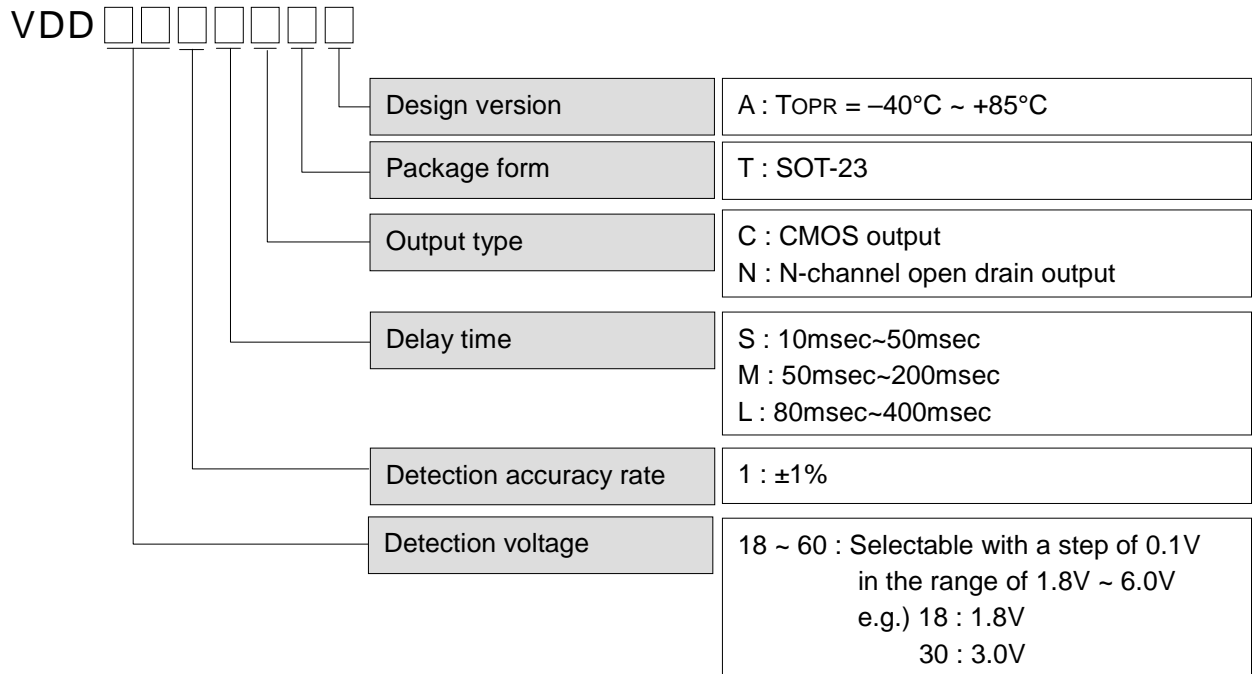
FEATURES

- Detection voltage range 1.8V~6.0V (selectable with a step of 0.1V)
- Operating voltage range 0.7V~6.0V
- High accuracy detection voltage $\pm 1\%$ ($V_{DET}=1.8V\sim 6.0V$)
- Detection voltage temperature characteristics Typ. $\pm 20\text{ppm}/^\circ\text{C}$ ($V_{DET}=1.8V\sim 6.0V$)
- Delay time S/10~50ms, M/50~200ms, L/80~400ms
- Output types CMOS or N-channel open drain
- Low current consumption Typ. $0.6\mu\text{A}$ ($V_{IN}=1.5V$)
- Operating temperature range $-40^\circ\text{C} \sim +85^\circ\text{C}$
- Small package SOT-23 (2.9x2.8x1.1mm)

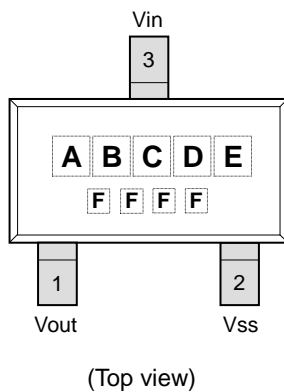
APPLICATIONS

- Reset of microprocessor
- Power-on reset of system
- Charge detection of battery
- Battery back-up of memory
- Monitoring of battery life time
- Delay circuit

PRODUCTS NUMBERING GUIDE



PIN CONFIGURATION / MARKING SPECIFICATION (SOT-23)



● **Pin Configuration**

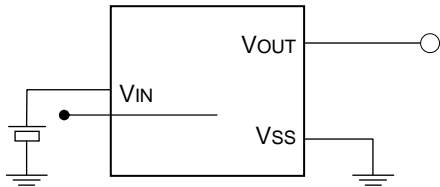
| No. | Symbol | Descriptions |
|-----|--------|---------------|
| 1 | VOUT | Output |
| 2 | VSS | Power ground |
| 3 | VIN | Voltage input |

● **Marking Specification**

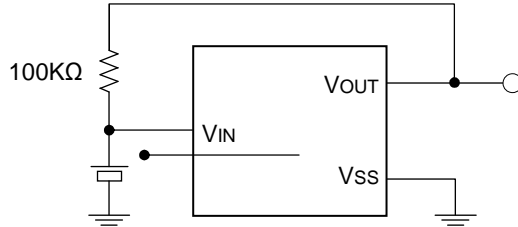
| Code | Mark | Contents |
|------|---------------|-------------------|
| A | C or N | Output type |
| BC | 18~60 | Detection voltage |
| D | S, M or L | Delay time |
| E | A | Version |
| F | Internal rule | Lot number |

TYPICAL APPLICATION CIRCUITS

- CMOS output

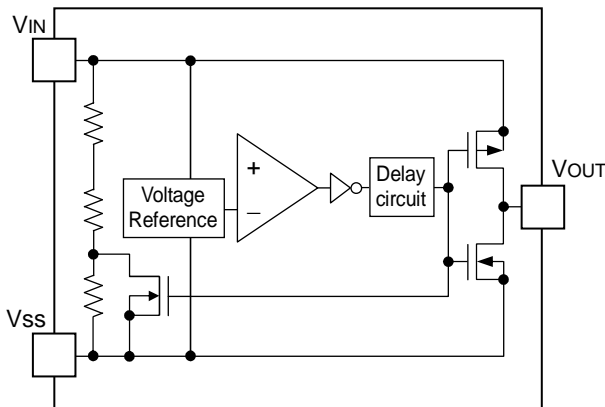


- N-channel open drain output

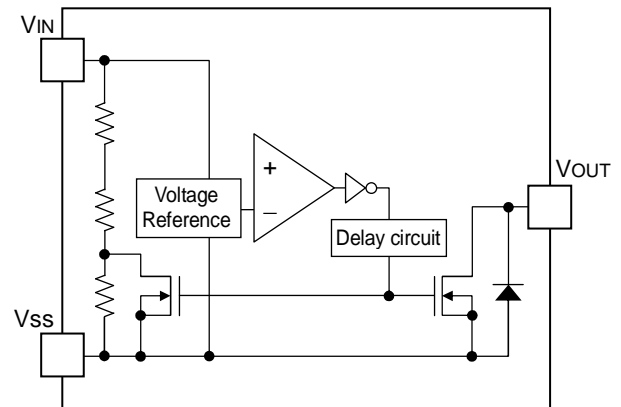


BLOCK DIAGRAM

- CMOS output



- N-channel open drain output



ABSOLUTE MAXIMUM RATINGS

| Items | Symbol | Ratings | Unit |
|--------------------------------|------------------|---|------|
| Input voltage range | V _{IN} | -0.3 ~ +7.0 | V |
| Output current | I _{OUT} | 50 | mA |
| Output voltage range | V _{OUT} | V _{SS} -0.3 ~ V _{IN} +0.3 | V |
| Power dissipation ※1) SOT-23 | P _D | 400 | mW |
| Operating temperature range | T _{OPR} | -40 ~ +85 | °C |
| Storage temperature range | T _{STG} | -55 ~ +125 | °C |

Note :

※1) Power dissipation depends on conditions of mounting on boards.

PCB dimension is 50mm×50mm×1.6mm.

ELECTRICAL CHARACTERISTICS

(Ta=25°C unless otherwise specified)

| Items | Symbol | Conditions | Min. | Typ. | Max. | Unit | Test circuit | |
|--|---|--|---------------------------|---------------------------|---------------------------|--------|--------------|---|
| Operating voltage | V _{IN} | V _{DET} = 1.8V ~ 6.0V | 0.7 | - | 6.0 | V | 1 | |
| Detection voltage | V _{DET} | V _{DET} = 1.8V ~ 6.0V Ta = -40°C ~ +85°C | V _{DET} x0.99 | V _{DET} | V _{DET} x1.01 | V | 1 | |
| Hysteresis range | V _{HYS} | | V _{DET} x0.02 | V _{DET} x0.05 | V _{DET} x0.08 | V | 1 | |
| Output current | I _{OUT} | N-ch V _{DS} =0.5V | V _{IN} =0.7V | 0.1 | 0.4 | - | mA | 3 |
| | | | V _{IN} =1.0V | 1.0 | 2.3 | - | mA | |
| | | | V _{IN} =2.0V | 3.0 | 8.2 | - | mA | |
| | | | V _{IN} =3.0V | 5.0 | 11.1 | - | mA | |
| | | | V _{IN} =4.0V | 6.0 | 12.8 | - | mA | |
| | | | V _{IN} =5.0V | 7.0 | 13.8 | - | mA | |
| | | CMOS P-ch V _{DS} =2.1V | V _{IN} =6.0V | - | -9.5 | -1.5 | mA | 4 |
| CMOS N-ch V _{DS} =2.1V | V _{IN} =6.0V | 1.5 | 9.5 | - | mA | 3 | | |
| Current consumption | I _{SS} | | V _{IN} =1.5V | - | 0.6 | 2.1 | μA | 2 |
| | | | V _{IN} =2.0V | - | 0.7 | 2.5 | μA | |
| | | | V _{IN} =3.0V | - | 0.8 | 2.8 | μA | |
| | | | V _{IN} =4.0V | - | 0.9 | 3.0 | μA | |
| | | | V _{IN} =5.0V | - | 1.0 | 3.4 | μA | |
| Leak current | I _{LEAK} | V _{IN} =6.0V V _{OUT} =6.0V | - | 10 | 100 | nA | 3 | |
| Detection voltage temperature coefficient | $\frac{\Delta V_{DET}}{\Delta T_a \cdot V_{DET}}$ | V _{DET} = 1.8V ~ 6.0V Ta = -40°C ~ +85°C | - | ±20 | - | ppm/°C | 1 | |
| Delay time V _{REL} →V _{OUT} inversion | T _{DLY} | V _{IN} = 0.7V ~ 6.0V | 10 | - | 50 | ms | 5 | |
| | | | 50 | - | 200 | ms | | |
| | | | 80 | - | 400 | ms | | |

TEST CIRCUITS

- **Circuit (1)** – Operating voltage, Detection voltage, Hysteresis range, Detection voltage temperature coefficient



Note 1) :
The resistor (100kΩ) is not necessary for CMOS output products.

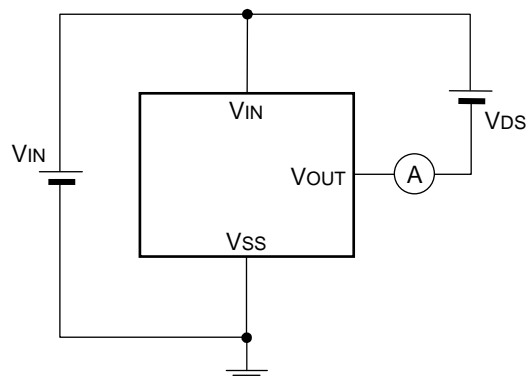
- **Circuit (2)** – Current consumption



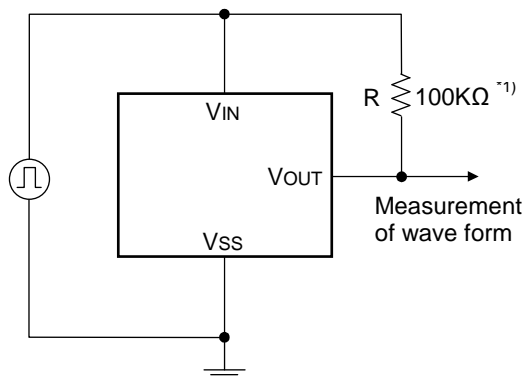
- **Circuit (3)** – N-ch driver output current



- **Circuit (4)** – P-ch driver output current



- **Circuit (5)** – Delay time (V_{REL}→V_{OUT} inversion)

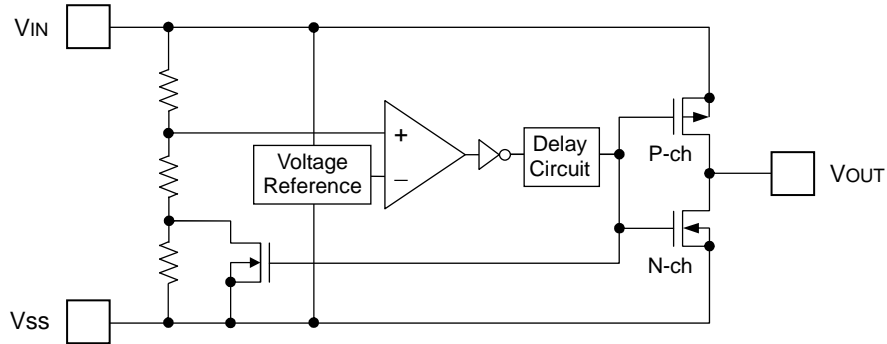


Note 1) :
The resistor (100kΩ) is not necessary for CMOS output products.

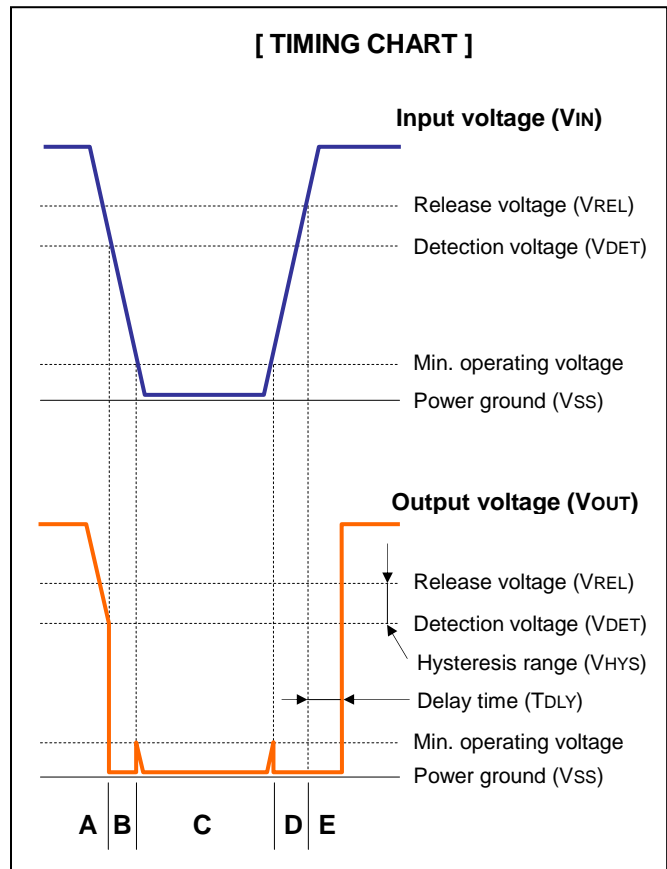
DESCRIPTION OF OPERATION

- **General operation (CMOS Output)**

In reference to following the block diagram of CMOS output VDD series ;

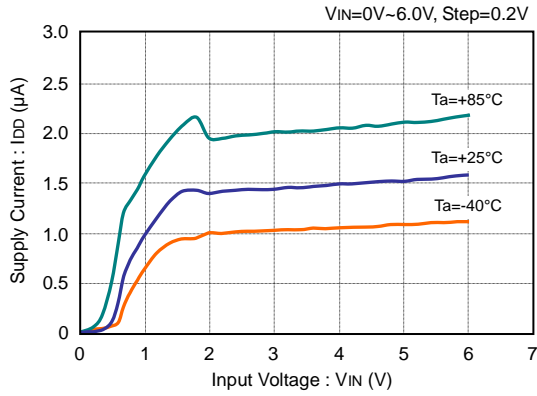


- When the input voltage (V_{IN}) is higher than the release voltage (V_{REL}), the input voltage (V_{IN}) is provided at the output terminal because N-ch transistor is OFF and the P-ch transistor is ON. And, the output maintains the same level of input as long as the input voltage remains above the detection voltage (V_{DET}).
- When the input voltage (V_{IN}) falls below the detection voltage (V_{DET}), the N-ch transistor is ON and the P-ch transistor is OFF. And, the output voltage (V_{OUT}) is same as ground level (V_{SS}).
- When the input voltage (V_{IN}) falls below the min. operating voltage, the output becomes unstable, or goes to V_{IN} when the output is pulled up to V_{IN} .
- When the input voltage (V_{IN}) rises above the minimum voltage, the ground voltage (V_{SS}) level is maintained even though the input voltage (V_{IN}) rises above the detection voltage (V_{DET}) as long as it does not exceed the release voltage (V_{REL}) level.
- Following delay time, the N-ch transistor becomes OFF when the input voltage (V_{IN}) rises above the release voltage (V_{REL}), and the P-Ch transistor becomes ON. And, the output voltage (V_{OUT}) is equal to input voltage (V_{IN}). This difference between V_{DET} and V_{REL} is hysteresis range (V_{HYS}).

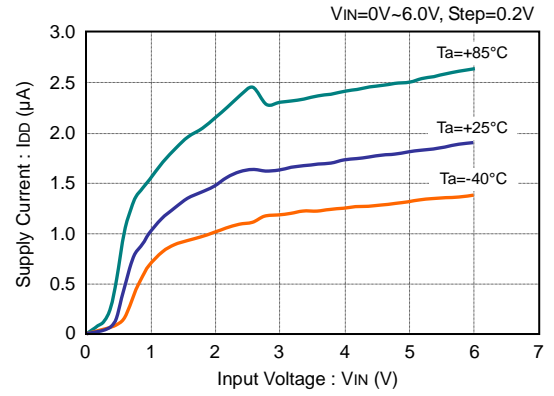


TYPICAL CHARACTERISTICS – Supply Current vs. Input Voltage

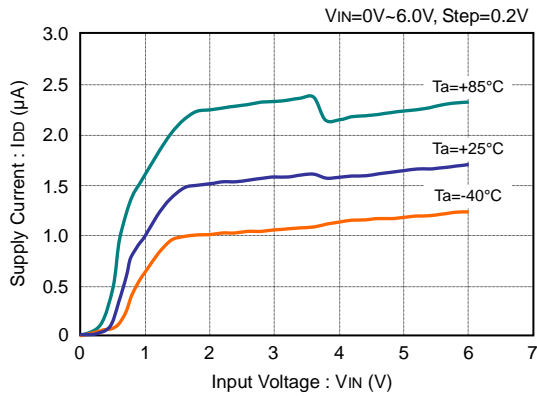
● **VDD181SCTA (CMOS 1.8V)**



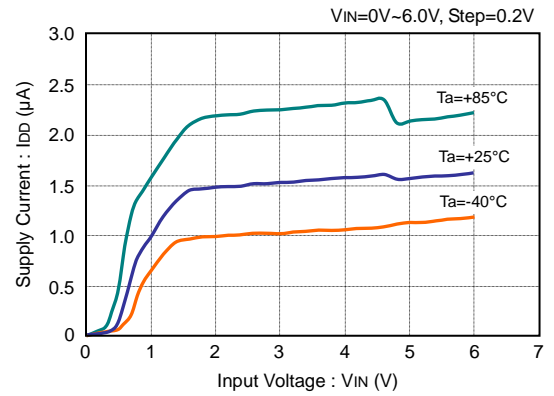
● **VDD251SCTA (CMOS 2.5V)**



● **VDD351SCTA (CMOS 3.5V)**

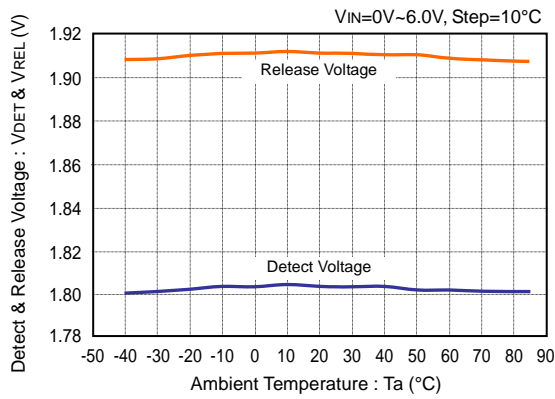


● **VDD451SCTA (CMOS 4.5V)**

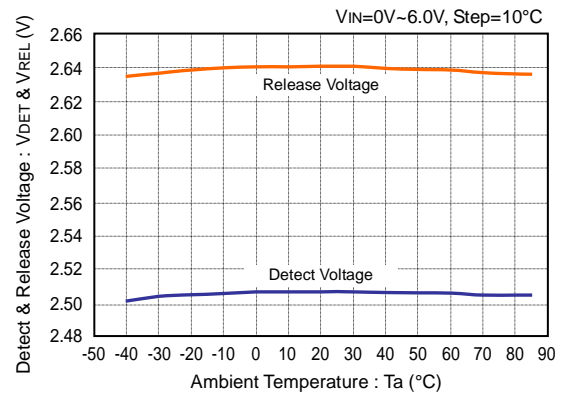


TYPICAL CHARACTERISTICS – Detect & Release Voltage vs. Ambient Temperature

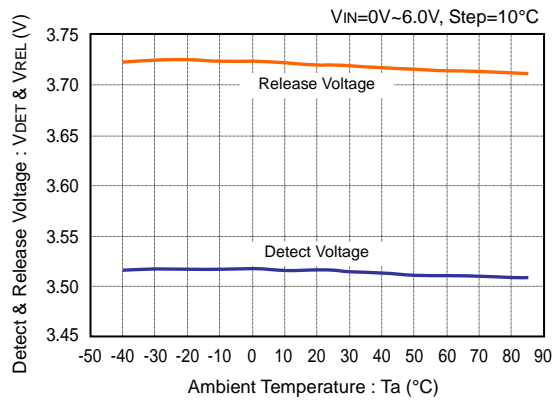
● **VDD181SCTA (CMOS 1.8V)**



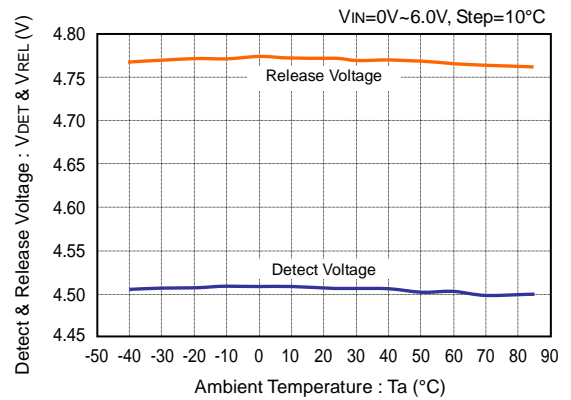
● **VDD251SCTA (CMOS 2.5V)**



● **VDD351SCTA (CMOS 3.5V)**

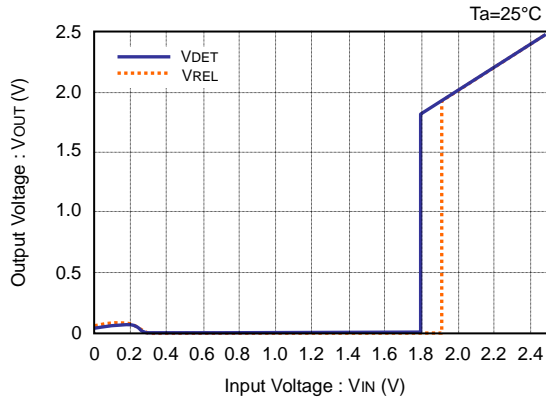


● **VDD451SCTA (CMOS 4.5V)**

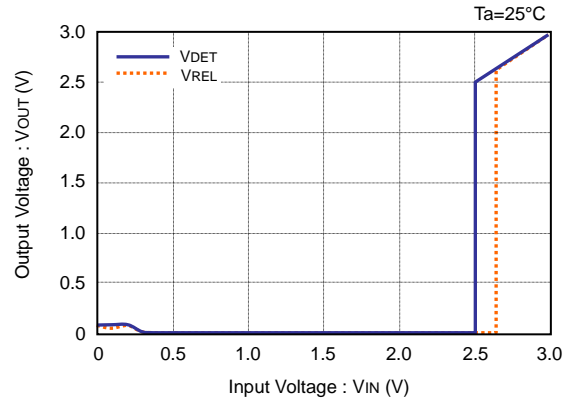


TYPICAL CHARACTERISTICS – Output Voltage vs. Input Voltage

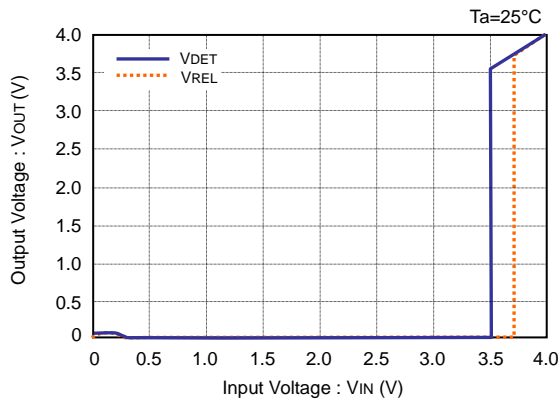
● **VDD181SCTA (CMOS 1.8V)**



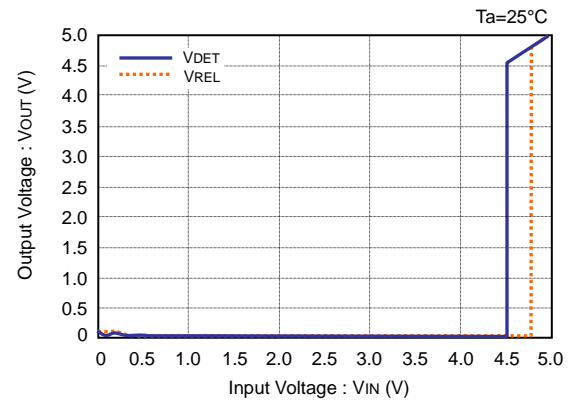
● **VDD251SCTA (CMOS 2.5V)**



● **VDD351SCTA (CMOS 3.5V)**

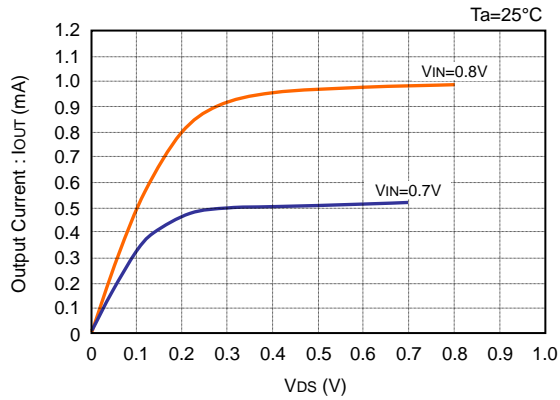


● **VDD451SCTA (CMOS 4.5V)**

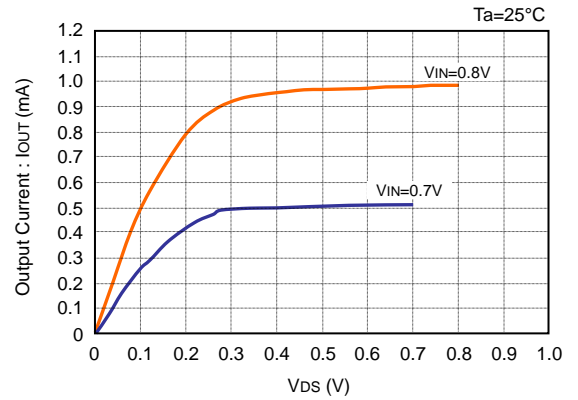


TYPICAL CHARACTERISTICS – N-ch Driver Output Current vs. V_{DS}

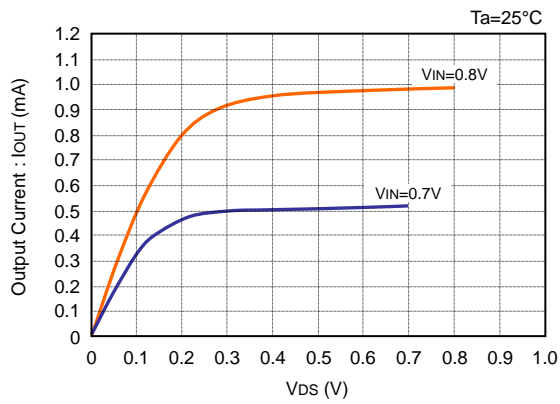
● **VDD181SCTA (CMOS 1.8V)**



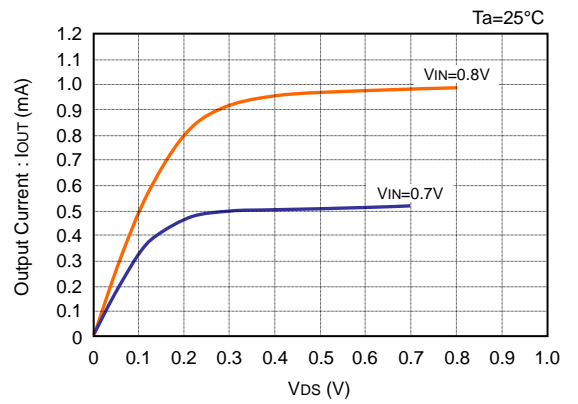
● **VDD251SCTA (CMOS 2.5V)**



● **VDD351SCTA (CMOS 3.5V)**

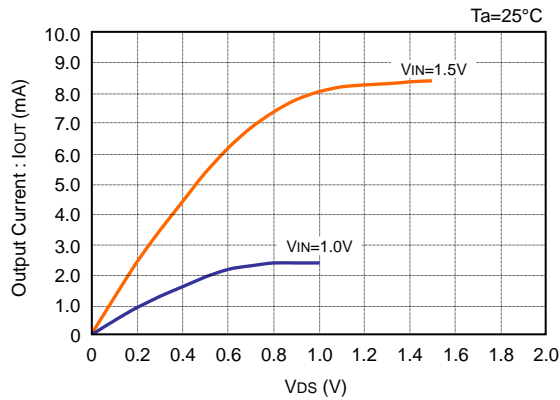


● **VDD451MCTA (CMOS 4.5V)**

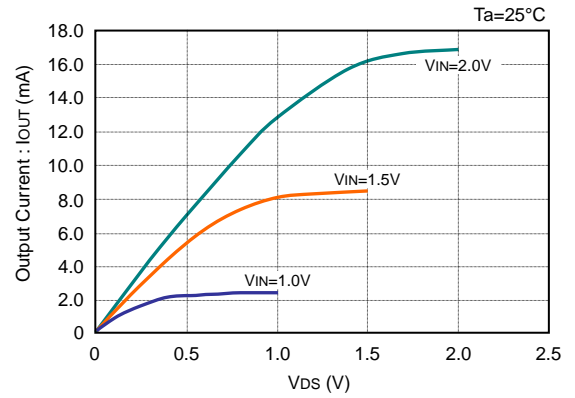


TYPICAL CHARACTERISTICS – N-ch Driver Output Current vs. V_{DS} (continued)

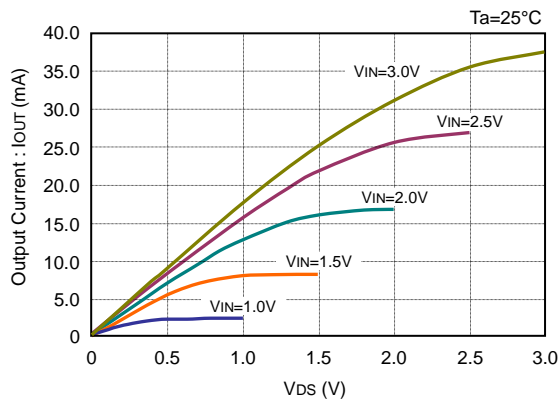
● **VDD181SCTA (CMOS 1.8V)**



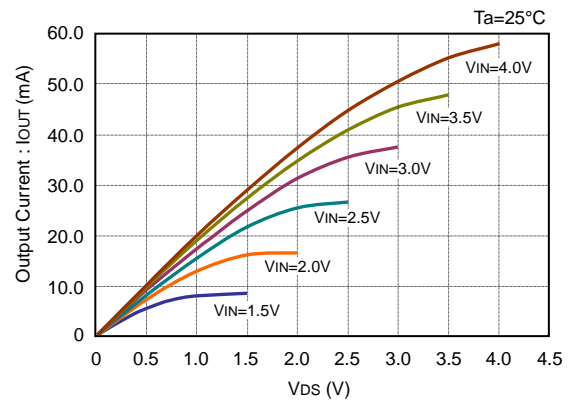
● **VDD251SCTA (CMOS 2.5V)**



● **VDD351SCTA (CMOS 3.5V)**

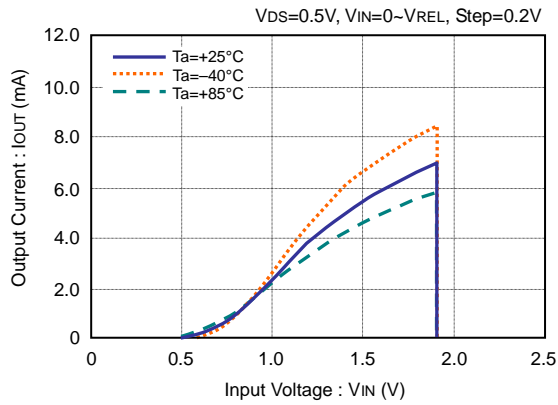


● **VDD451MCTA (CMOS 4.5V)**

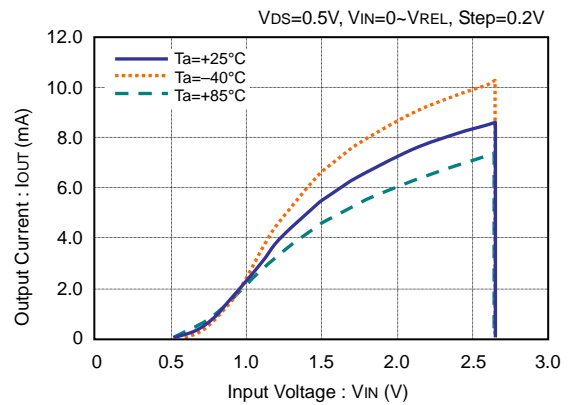


TYPICAL CHARACTERISTICS – N-ch Driver Output Current vs. Input Voltage

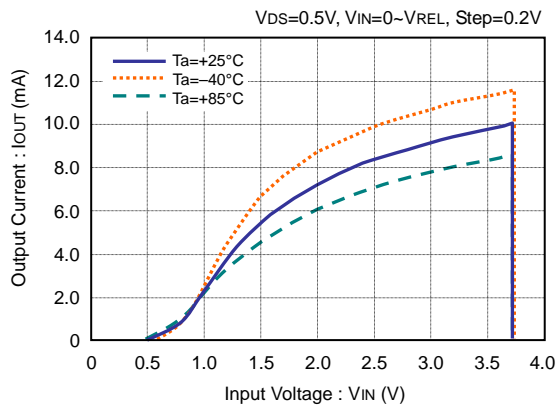
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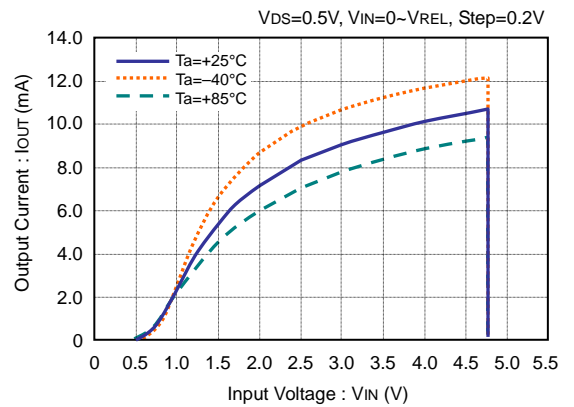
● **VDD251SCTA (CMOS 2.5V)**



● **VDD351SCTA (CMOS 3.5V)**

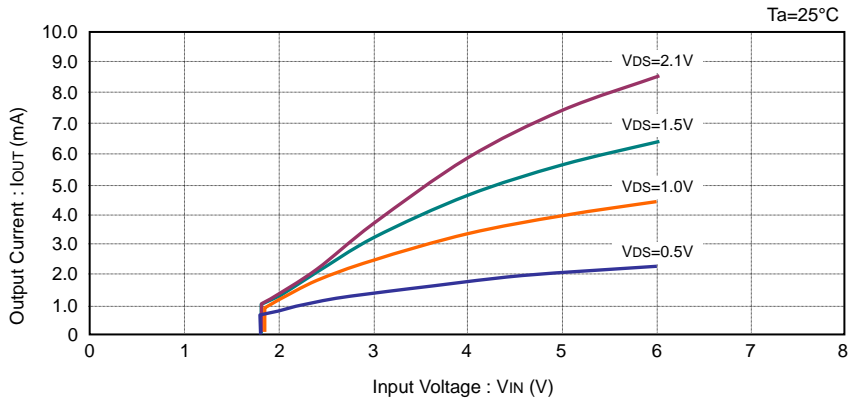


● **VDD451SCTA (CMOS 4.5V)**

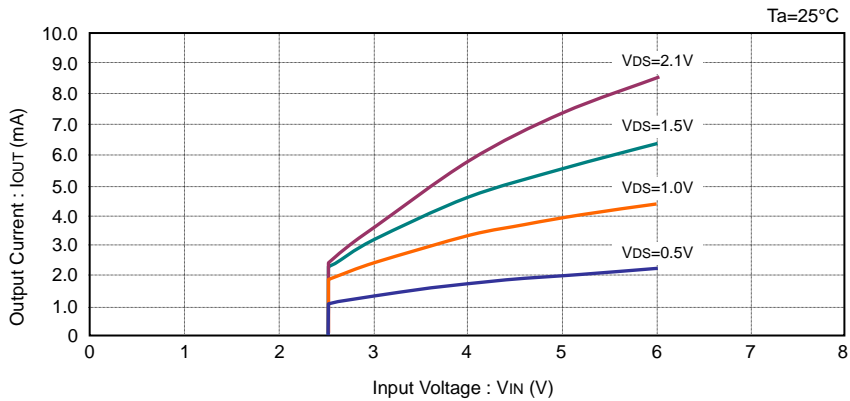


TYPICAL CHARACTERISTICS – P-ch Driver Output Current vs. Input Voltage

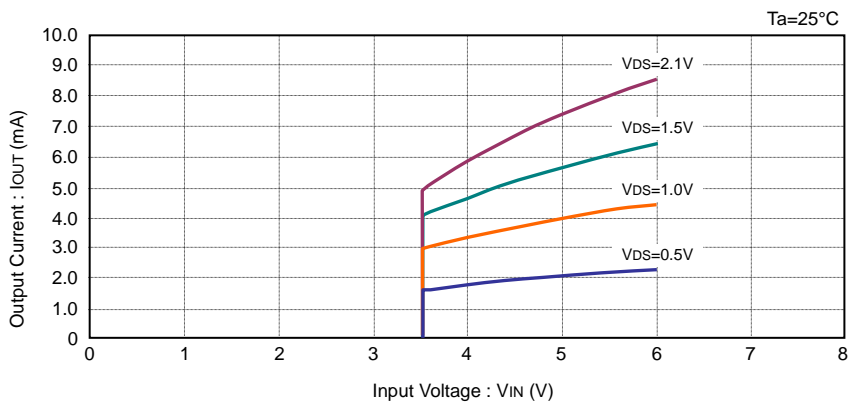
● **VDD181SCTA (CMOS 1.8V)**



● **VDD251SCTA (CMOS 2.5V)**

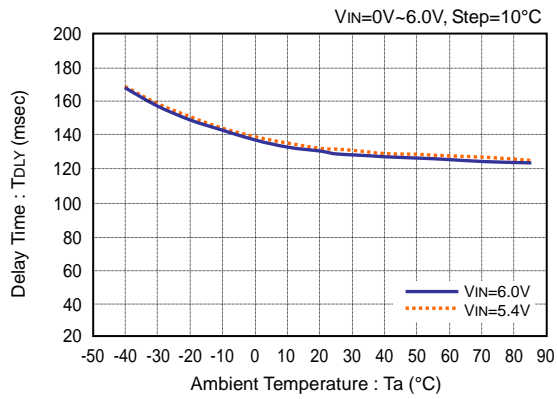


● **VDD351SCTA (CMOS 3.5V)**

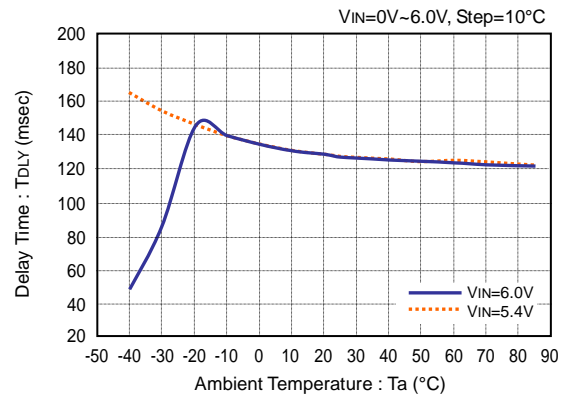


TYPICAL CHARACTERISTICS – Delay Time vs. Ambient Temperature

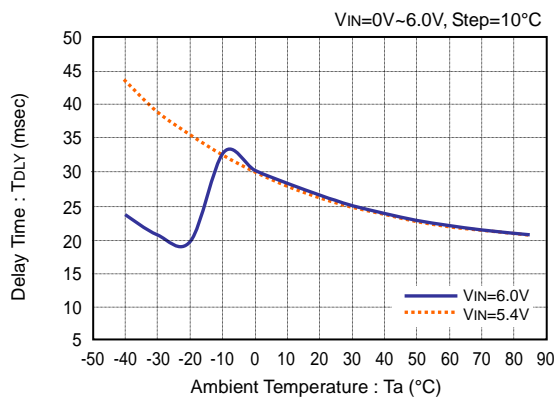
● VDD221MCTA (CMOS 2.2V)



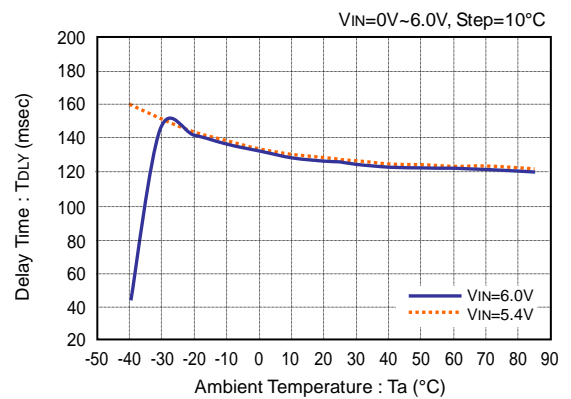
● VDD271MCTA (CMOS 2.7V)



● VDD271SNTA (N-ch 2.7V)

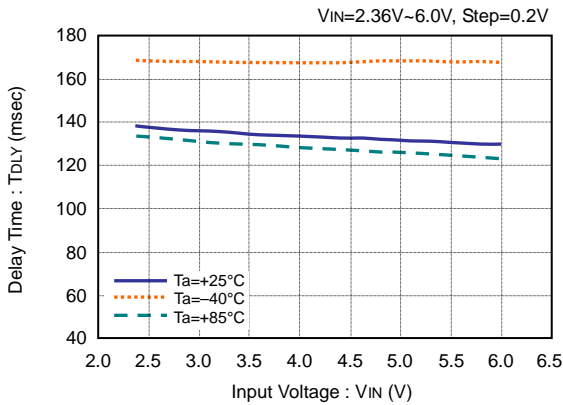


● VDD301MCTA (CMOS 3.0V)

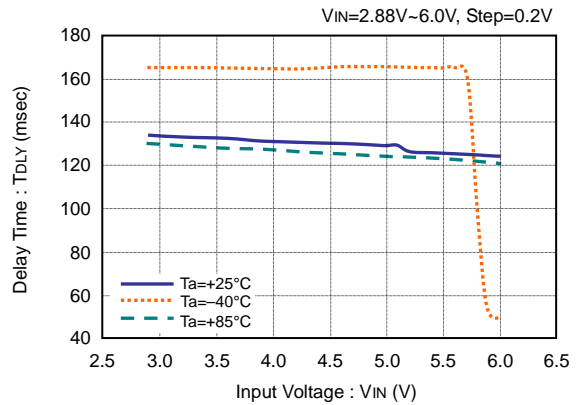


TYPICAL CHARACTERISTICS – Delay Time vs. Input Voltage

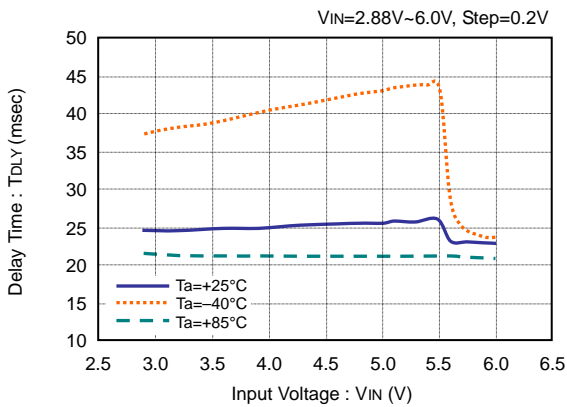
● **VDD221MCTA (CMOS 2.2V)**



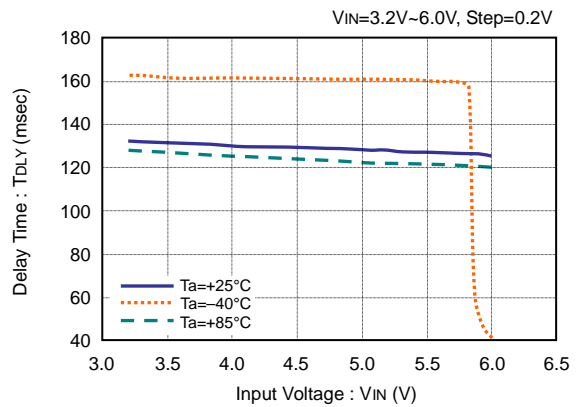
● **VDD271MCTA (CMOS 2.7V)**



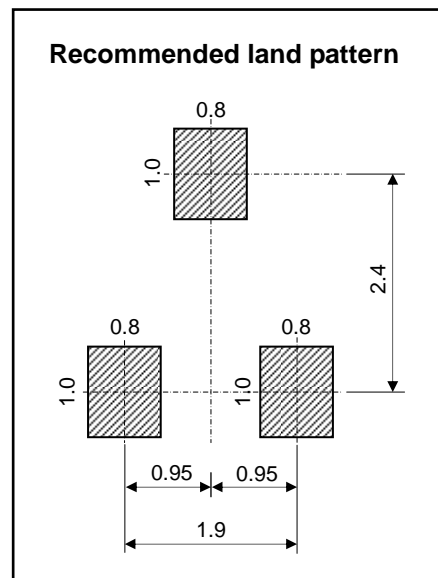
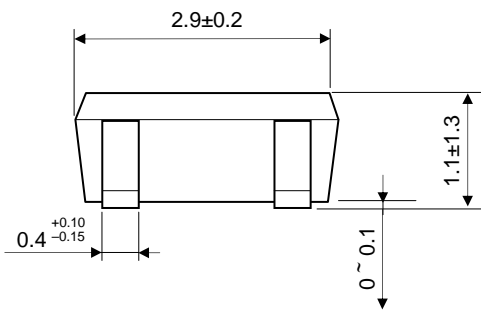
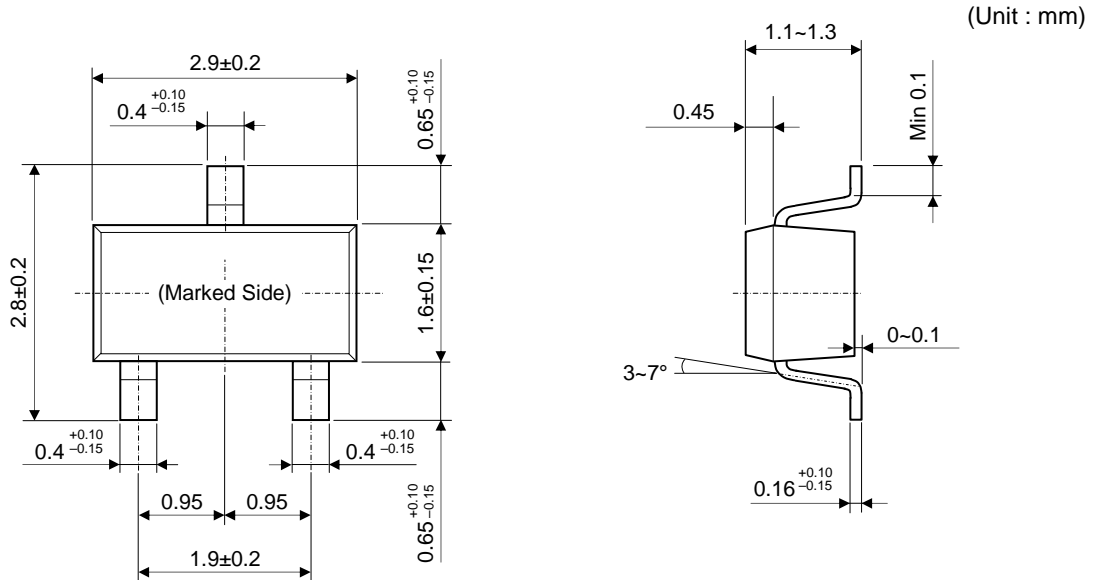
● **VDD271SNTA (N-ch 2.7V)**



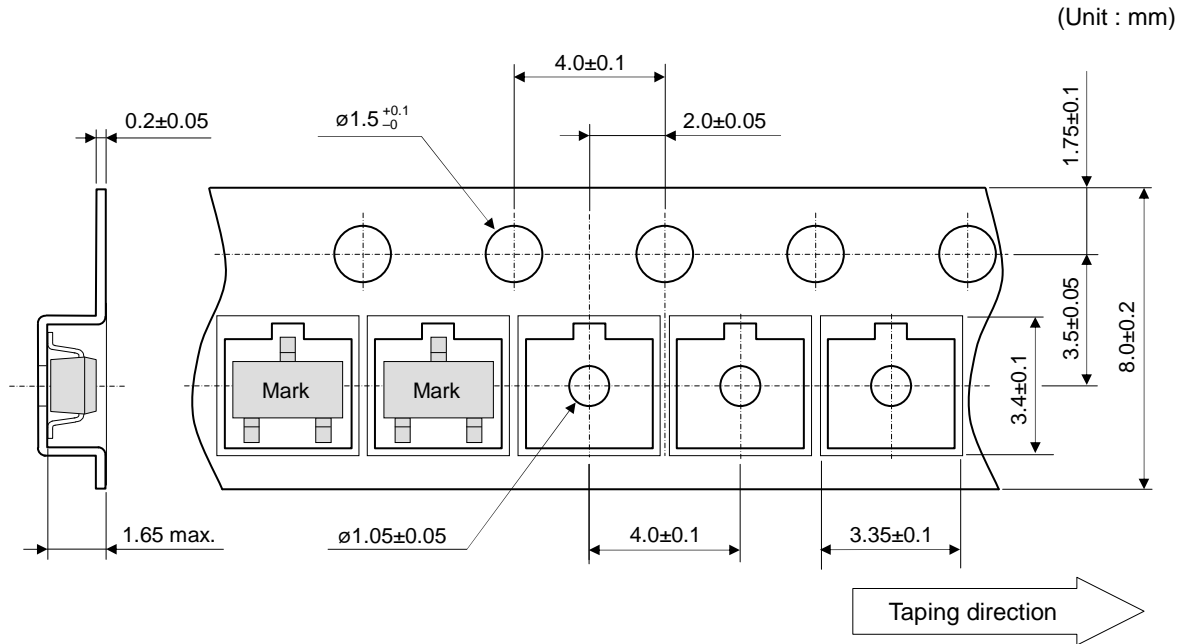
● **VDD301MCTA (CMOS 3.0V)**



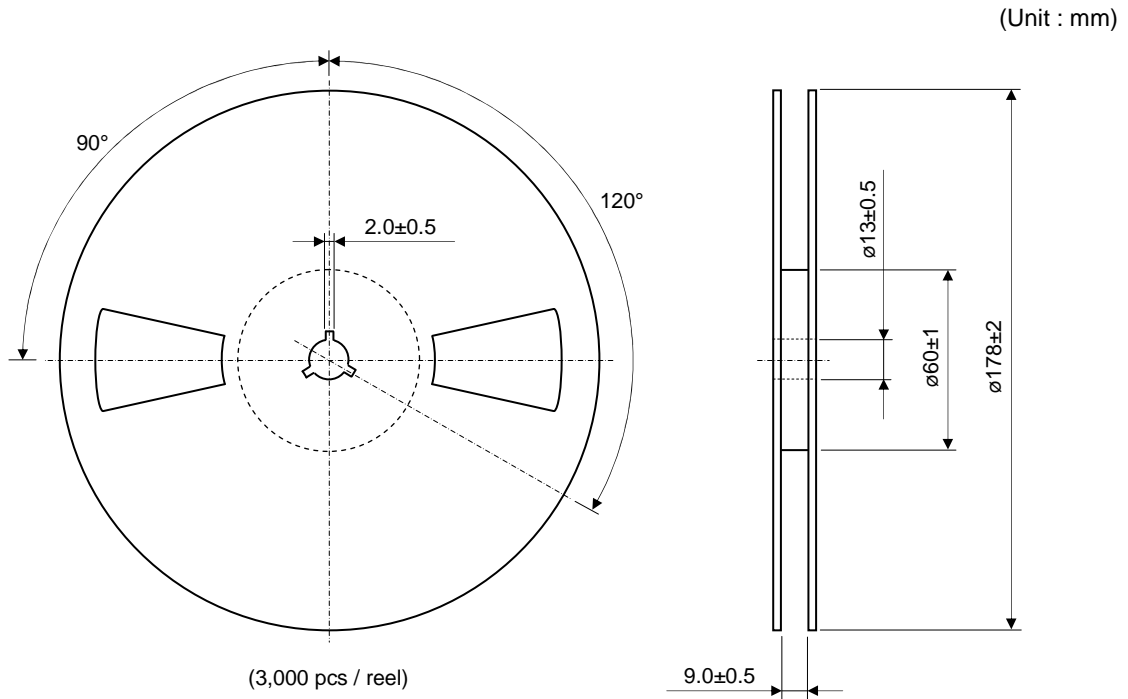
PACKAGE DIMENSIONS (SOT-23)

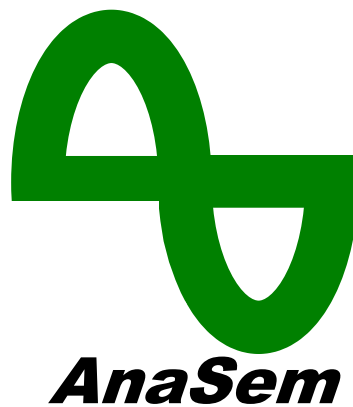


TAPING AND LOADING SPECIFICATIONS (SOT-23)



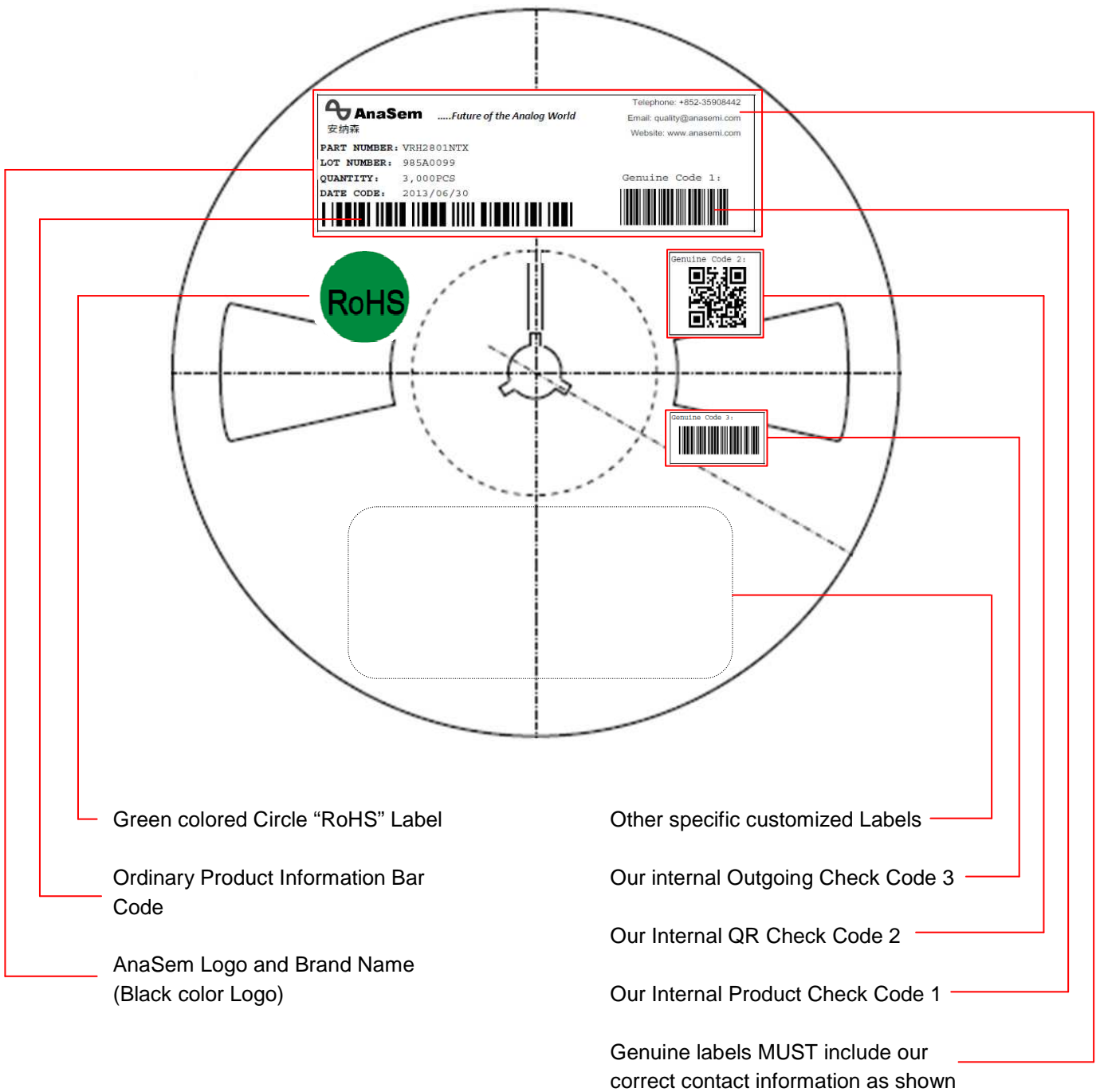
REEL DIMENSIONS (SOT-23)





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[NCP305LSQ16T1G](#) [NCP305LSQ17T1G](#) [NCP305LSQ18T1G](#) [NCP305LSQ24T1G](#) [NCP305LSQ25T1G](#) [NCP305LSQ29T1G](#)
[NCP305LSQ31T1G](#) [NCP305LSQ32T1G](#) [NCP308MT250TBG](#) [NCP308SN300T1G](#) [NCP391FCALT2G](#) [NCV303LSN42T1G](#)
[NCV308SN330T1G](#) [CAT1161LI-25-G](#) [CAT853STBI-T3](#) [MAX1232CPA](#) [MAX705CPA](#) [CAT1026LI-30-G](#) [CAT1320LI-25-G](#) [CAT872-30ULGT3](#) [LA-ispPAC-POWR1014-01TN48E](#) [NCP304HSQ18T1G](#) [NCP304HSQ29T1G](#) [NCP304LSQ27T1G](#) [NCP304LSQ29T1G](#)
[NCP304LSQ45T1G](#) [NCP305LSQ26T1G](#) [NCP305LSQ35T1G](#) [NCP305LSQ37T1G](#) [NCP308MT300TBG](#) [NCV300LSN36T1G](#)
[NCV302LSN30T1G](#) [NCV303LSN16T1G](#) [NCV303LSN22T1G](#) [NCV303LSN27T1G](#) [NCV33161DMR2G](#) [TC54VN2402EMB713](#)
[MCP1316T-44NE/OT](#) [MCP1316MT-45GE/OT](#) [MCP1316MT-23LI/OT](#) [MCP1316T-26LE/OT](#) [MAX8997EWW+](#) [MAX821RUS+T](#)
[MAX6725AKASYD3-LF-T](#)