

MOSFET Silicon N-Channel MOS



1. Applications

Boost PFC switch, Half bridge or Asymmetric half bridge or Series resonance half bridge and full bridge topologies.
Server power, Telecom power, EV charging, Solar inverter, UPS Application.

2. Features

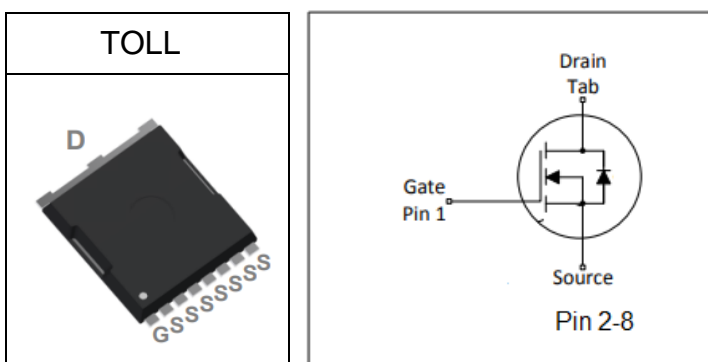
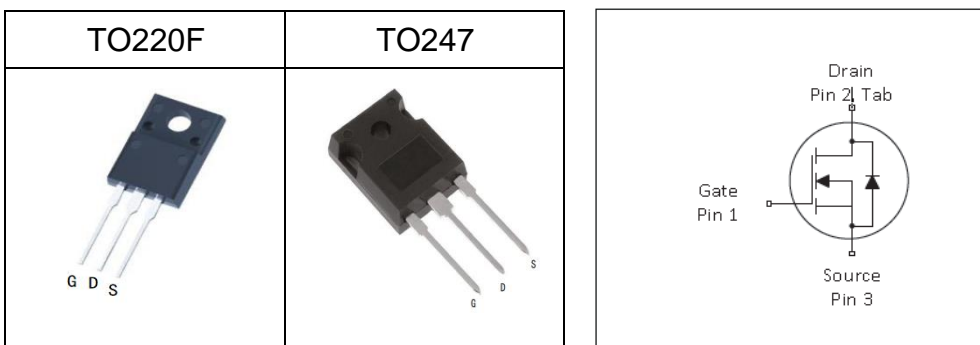
Low drain-source on-resistance: $R_{DS(on)} = 0.105\Omega$ (typ.)
Easy to control Gate switching
Enhancement mode: $V_{th} = 3$ to 5 V

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	120	m Ω
$Q_{g,typ}$	55.4	nC
$I_{D,pulse}$	90	A
Body diode dv/dt	50	V/ns

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R120EFD	TO247	ASW65R120EFD
ASA65R120EFD	TO220F	ASA65R120EFD
ASR65R120EFD	TOLL-8L	ASR65R120EFD



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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	30	A	$T_C=25^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	90	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	1216	mJ	$T_C=25^\circ\text{C}, V_{DD}=50\text{V}, L=10\text{mH}, R_G=25\Omega$
Avalanche current, single pulse	I_{AR}	-	-	10.9	A	$T_C=25^\circ\text{C}, V_{DD}=50\text{V}, L=10\text{mH}, R_G=25\Omega$
MOSFET dv/dt ruggedness	dv/dt	-	-	36.2	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1\text{ Hz}$)
Power dissipation(TO247)	P_{tot}	-	-	277.8	W	$T_C=25^\circ\text{C}$
Power dissipation (TO220F)	P_{tot}	-	-	36.5	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			260	$^\circ\text{C}$	
Reverse diode dv/dt ³⁾	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots400\text{V}, I_{SD} \leq I_D, T_j=25^\circ\text{C}$ see table 8

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¹⁾Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾Pulse width t_p limited by $T_{j,max}$

³⁾Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (TO220F)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.4	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Thermal characteristics(TO247)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.45	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	57	°C/W	device on PCB, minimal footprint

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3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	3		5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	2	μA	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.105	0.120	Ω	$V_{GS}=10V, I_D=14A, T_j=25^\circ C$
Gate resistance (Intrinsic)	R_G	-	12.6	-	Ω	$f=1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2657	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	C_{oss}	-	89	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Reverse transfer capacitance	C_{rss}	-	2	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Turn-on delay time	$t_{d(on)}$	-	29.6	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=19A, R_G=2\Omega; \text{see table 9}$
Rise time	t_r	-	31.3	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=19A, R_G=2\Omega; \text{see table 9}$
Turn-off delay time	$t_{d(off)}$	-	94.6	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=19A, R_G=2\Omega; \text{see table 9}$
Fall time	t_f	-	9.1	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=19A, R_G=2\Omega; \text{see table 9}$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	15	-	nC	$V_{DD}=400V, I_D=19A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	20.2	-	nC	$V_{DD}=400V, I_D=19A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	55.4	-	nC	$V_{DD}=400V, I_D=19A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.9	-	V	$V_{DD}=400V, I_D=19A, V_{GS}=0 \text{ to } 10V$

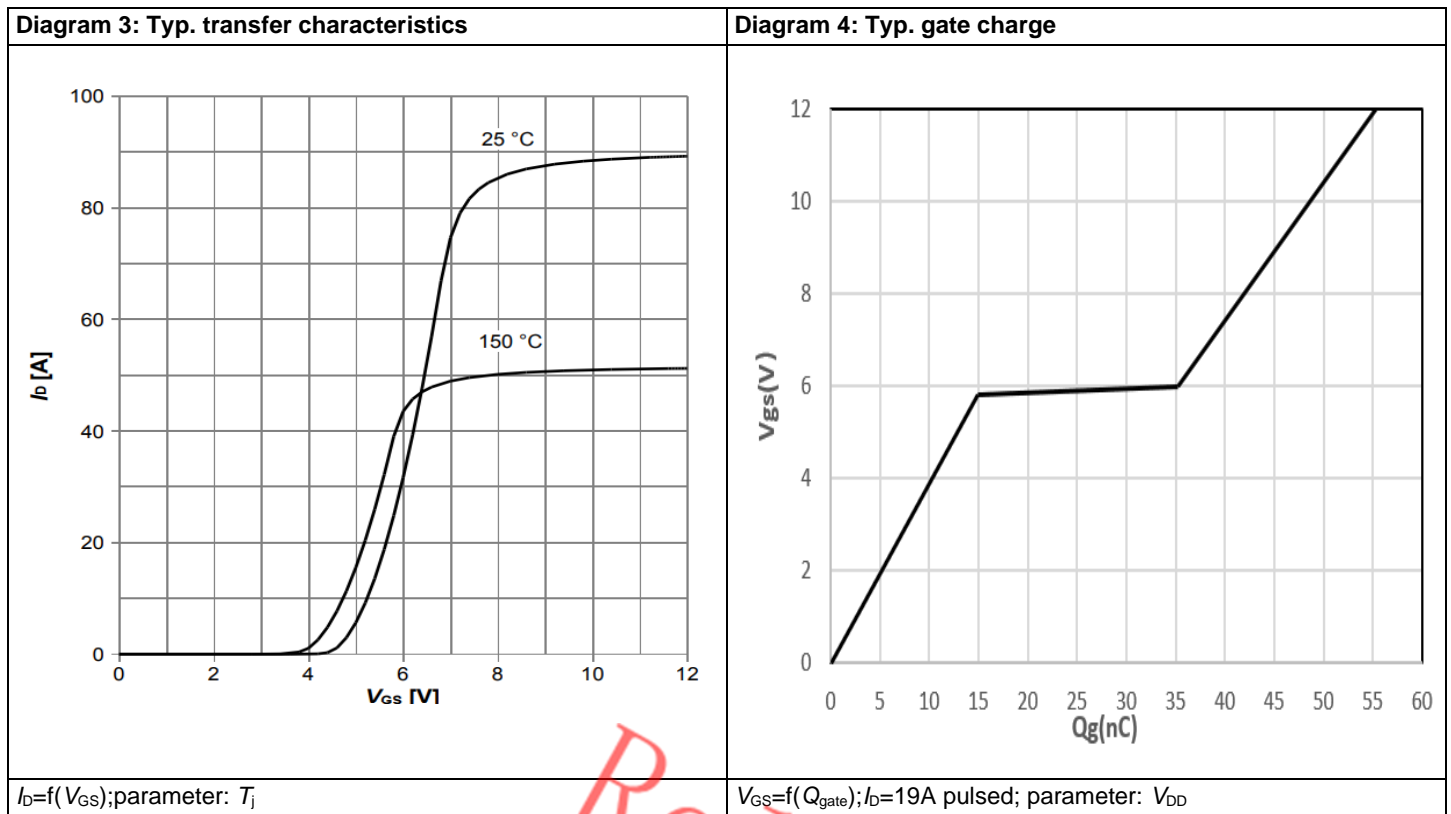
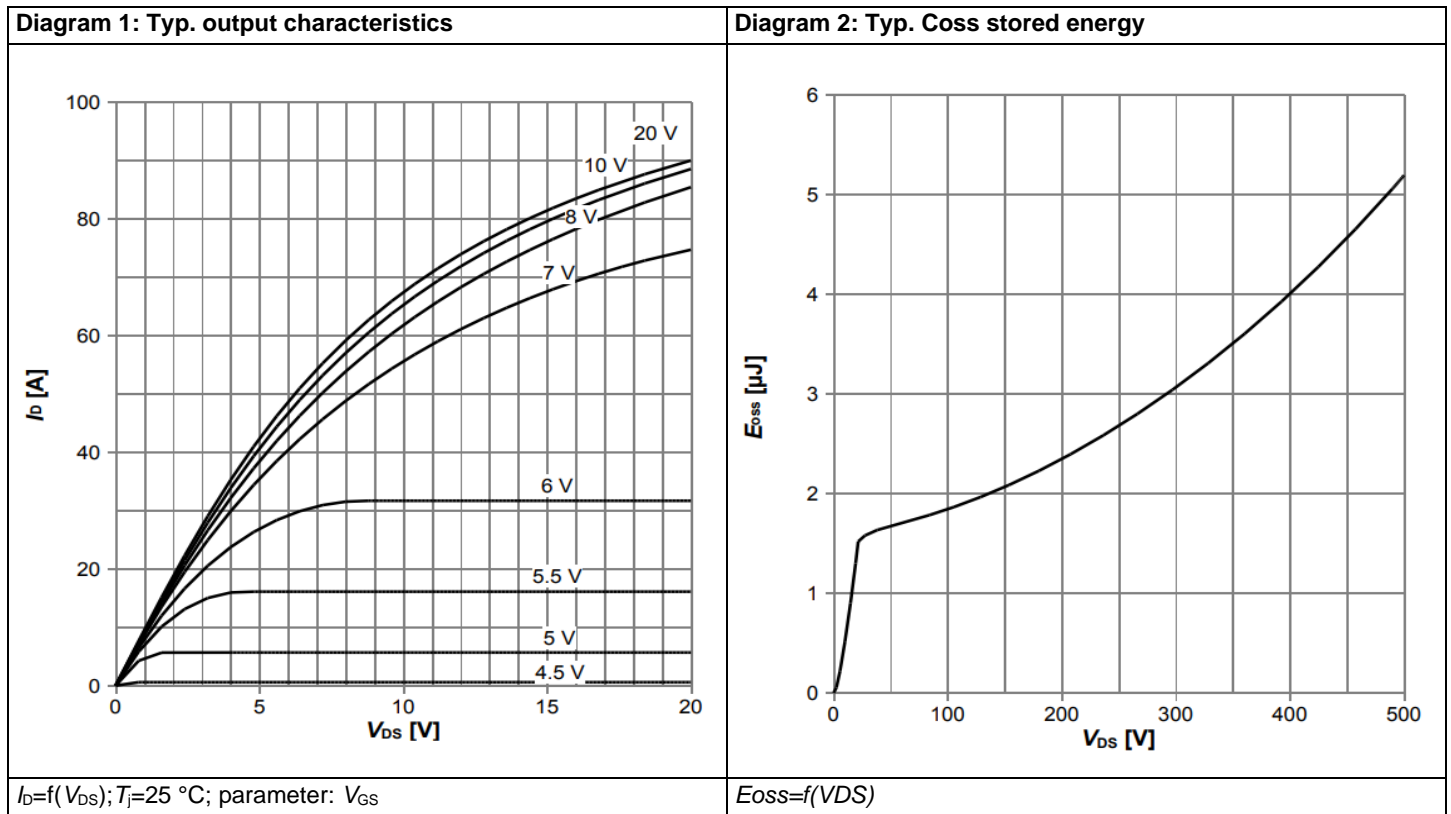
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Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.67	-	V	$V_{GS}=0V, I_F=1A, T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	136.7	-	ns	$V_R=400V, I_F=17A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.741	-	μC	$V_R=400V, I_F=17A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	10.28	-	A	$V_R=400V, I_F=17A, di_F/dt=100A/\mu s$; see table 8

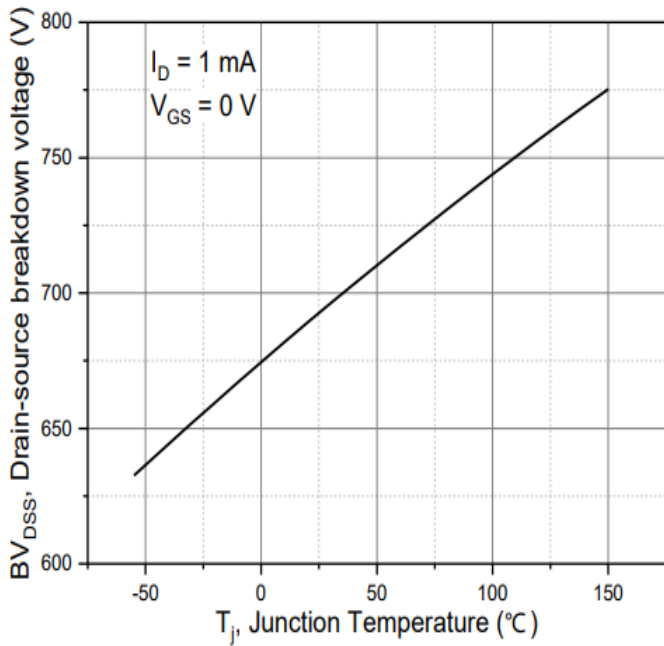
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4 Electrical characteristics diagram



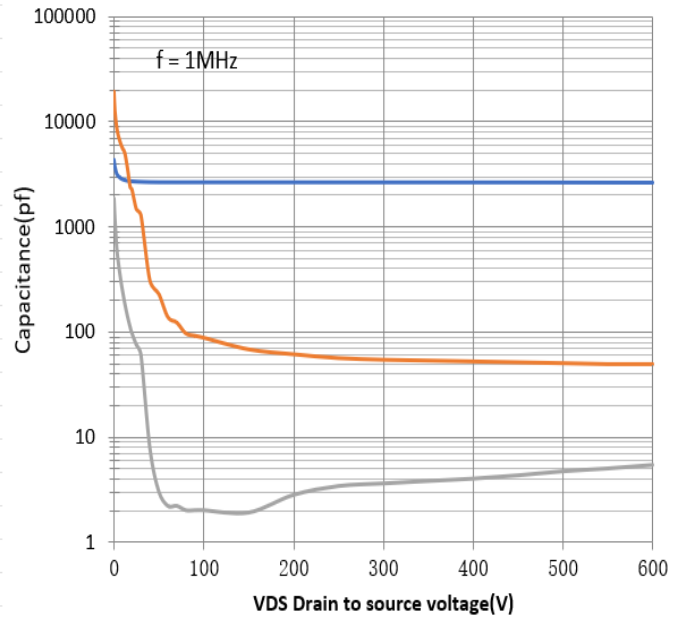
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Diagram 5: Drain-source breakdown voltage



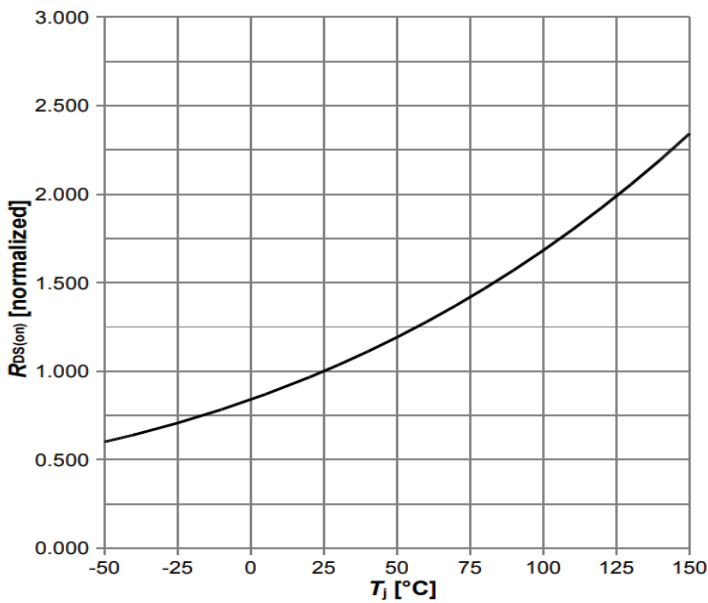
$V_{BR(DSS)}=f(T_j); I_D=1\text{mA}$

Diagram 6: Typ. capacitances



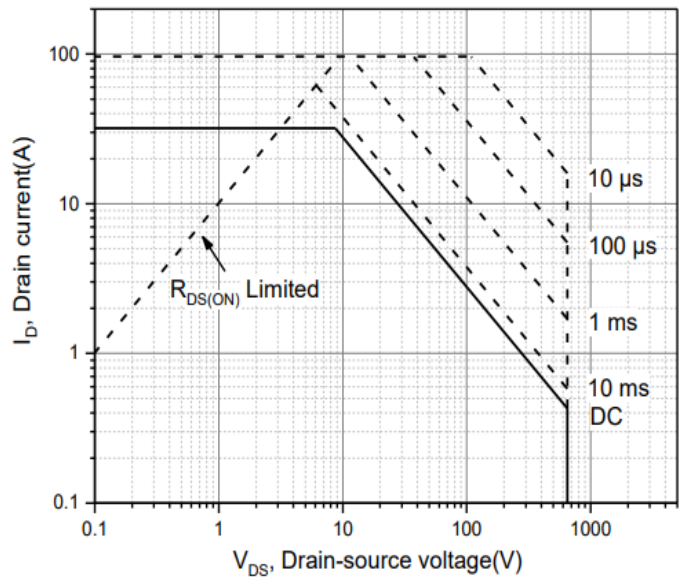
$C=f(V_{DS}); V_{GS}=0V; f=1\text{MHz}$

Diagram 7: Typ. On-Resistance vs. Junction Temperature



$R_{ds(on)}=f(T_j); V_{GS}=10V/I_D=14A$

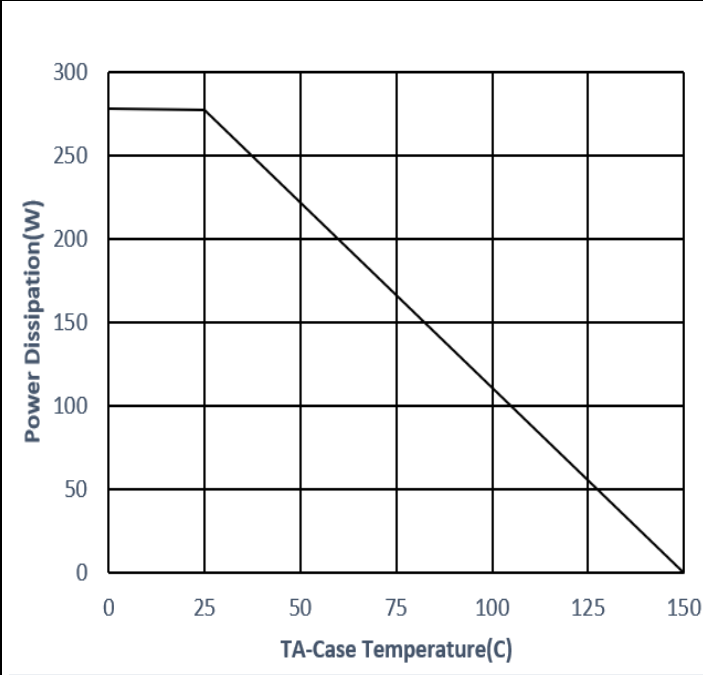
Diagram 8: Safe operating area $T_C=25^\circ\text{C}$,



$I_D=f(V_{DS}); T_C=25^\circ\text{C}; V_{GS}>7V; D=0; \text{parameter } tp$

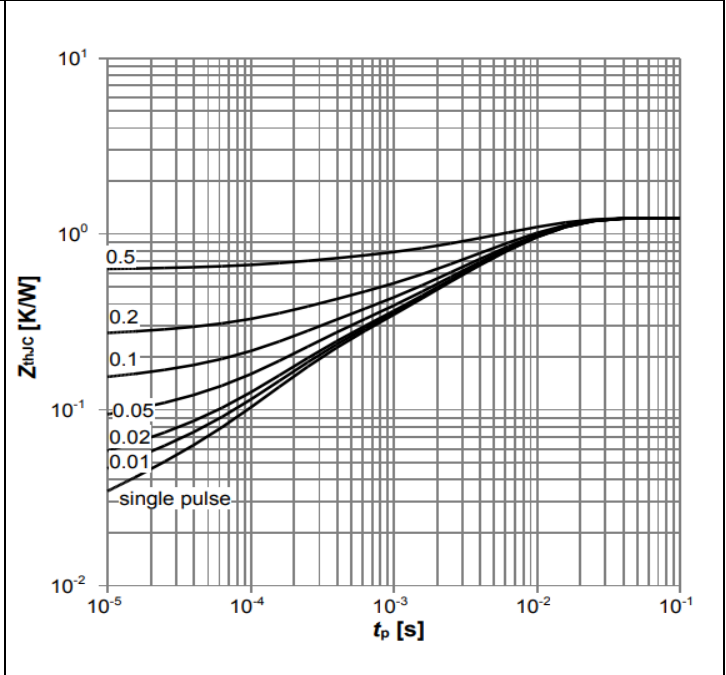
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Diagram 9: Typ. Power Dissipation



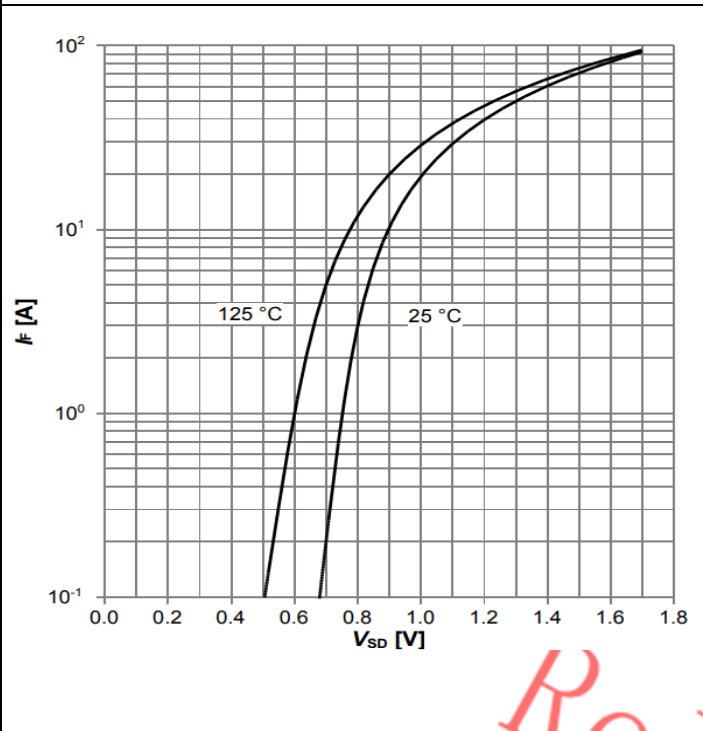
$P_{tot}=f(T_C)$

Diagram 10: Max. transient thermal impedance



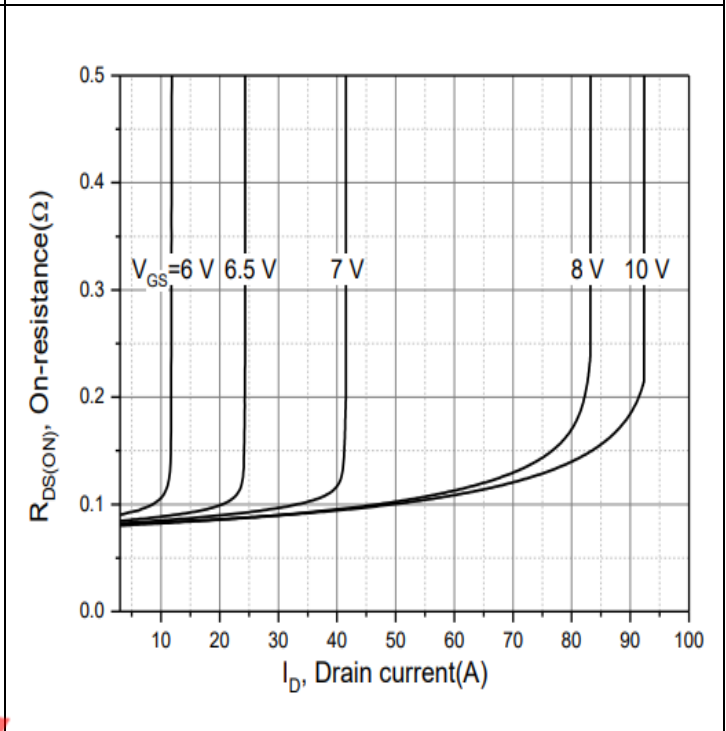
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 11: Forward characteristics of reverse diode



$I_f=f(V_{DS});$ parameter: T_j

Diagram 12: Typ. Drain-source on-state resistance



$R_{ds(on)}=f(T_j); T_j=25C,$ Parameter : V_{GS}

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5 Test Circuits

Table 8 Diode characteristics

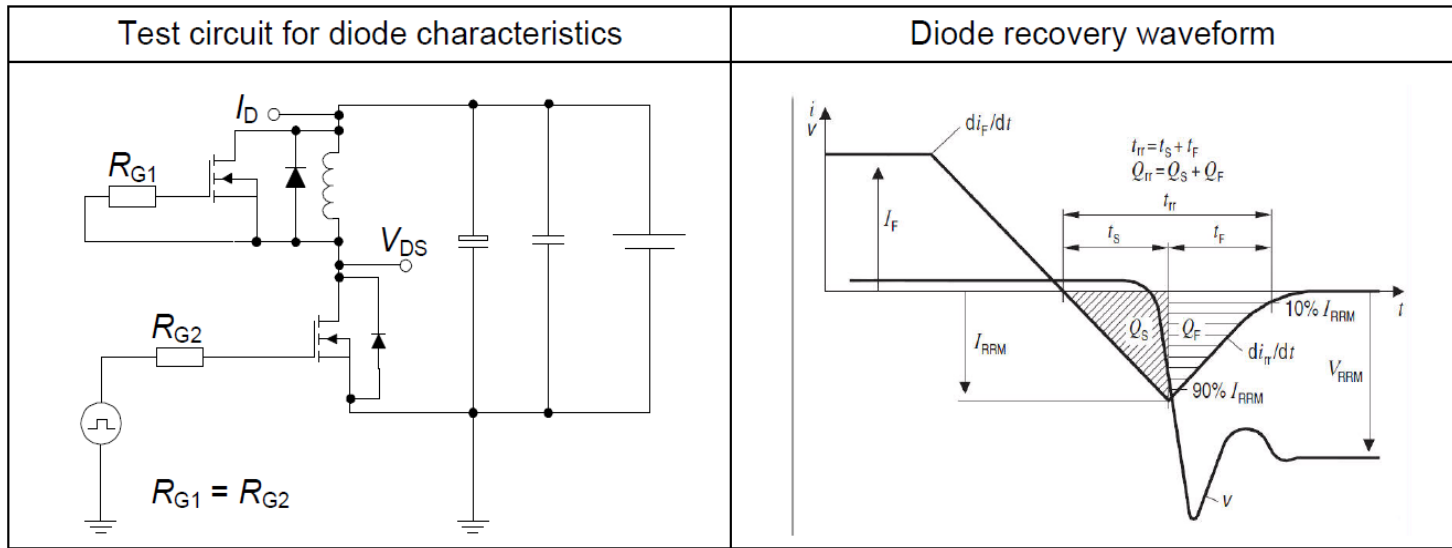


Table 9 Switching times

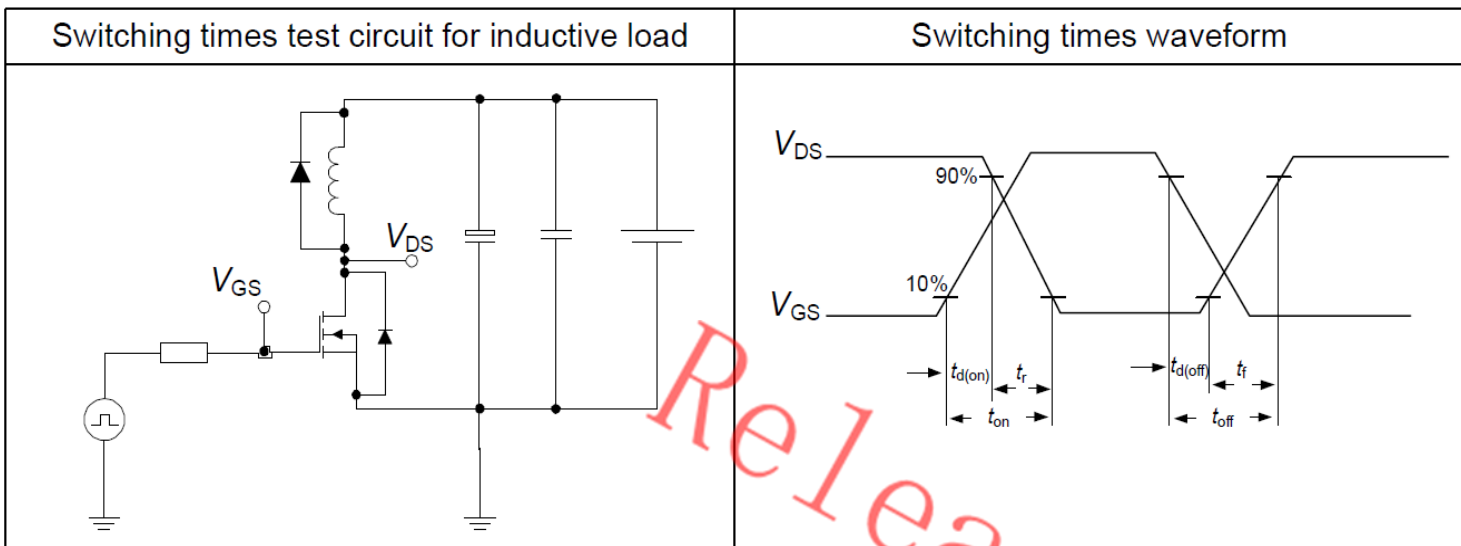
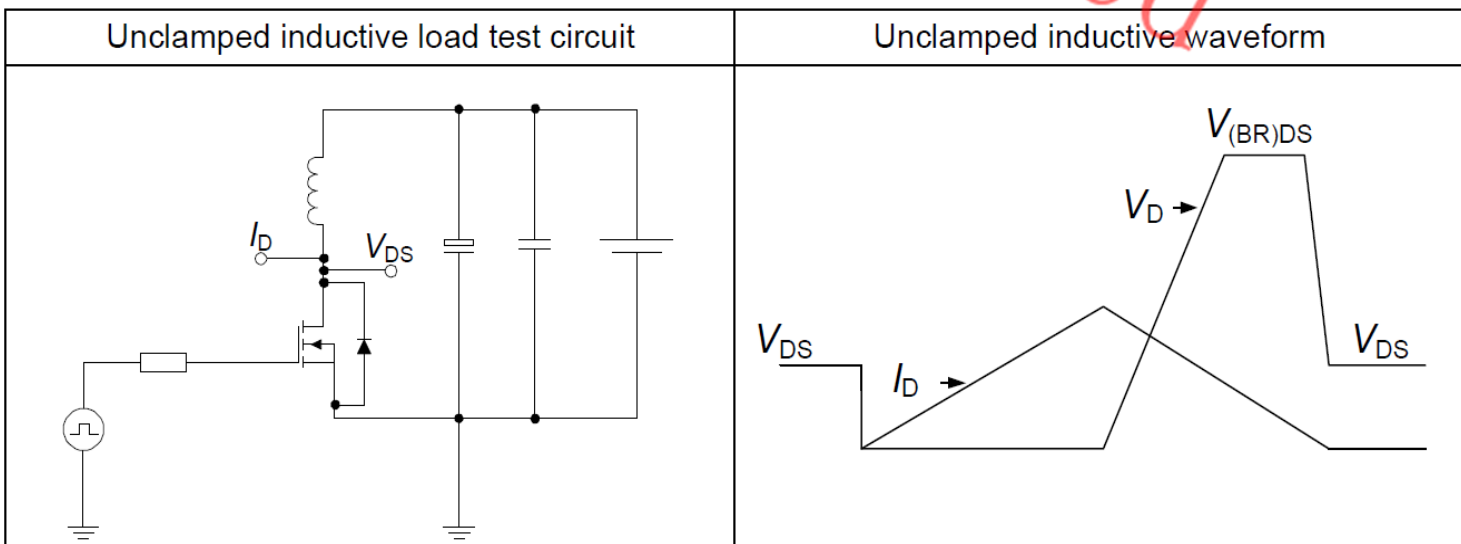
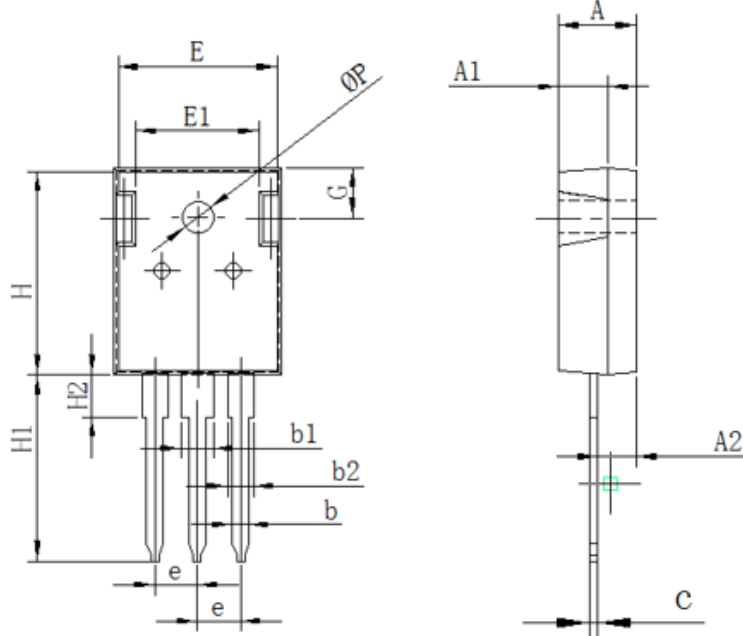


Table 10 Unclamped inductive load



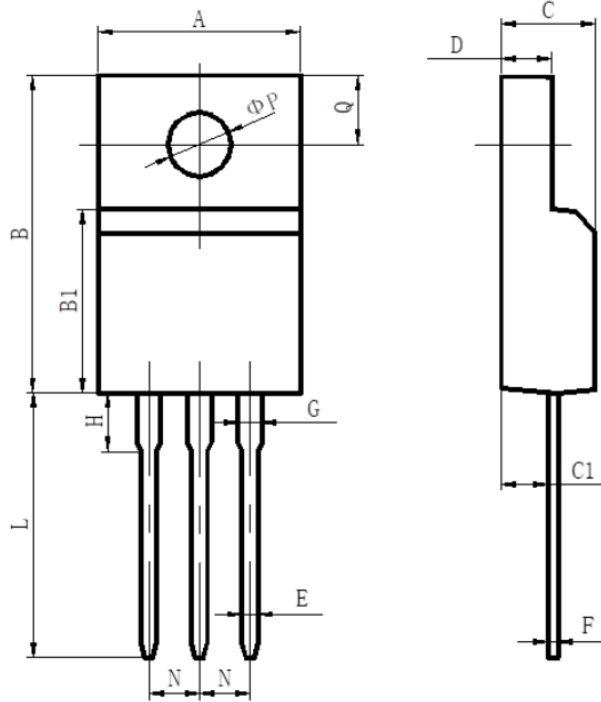
6 Package Outlines



Symbol	单位 mm		
	Min	Nom	Max
A	4.8	5.00	5.20
A1	3.3	3.5	3.7
A2	2.20	2.40	2.60
b	1.00	1.2	1.40
b1	2.90	3.10	3.30
b2	1.90	2.10	2.30
c	0.50	0.60	0.70
e	5.25	5.45	5.65
E	15.2	15.7	16.2
E1	10.2	10.7	11.2
H	20.8	21	21.2
H1	19.5	20.0	20.5
H2	4.00	4.20	4.40
G	5.60	5.80	600
ΦP	3.50	3.70	3.90

Figure1: Outline PG-T0247(CD&HT)

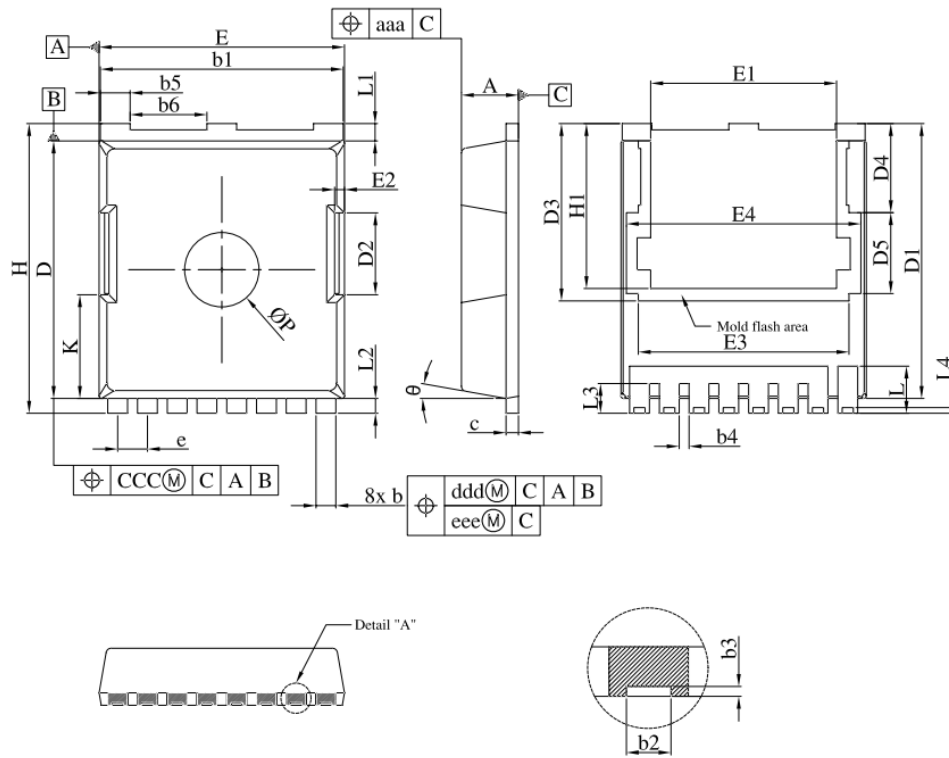
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项目	规范(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
B1	8.99	9.39
C	4.40	4.80
C1	2.15	2.55
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
Q	3.15	3.55
ϕP	3.00	3.30

Figure2: Outline PG-T0220F(HT)

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SYMBOL	COMMON		
	MILLIMETER		
	MIN.	NOMINAL	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.45	0.55
b3	0.05	0.100	?
b4	0.30	0.40	0.50
b5	1.10	1.20	1.30
b6	3.00	3.10	3.20
c	0.40	0.50	0.60
D	10.28	10.38	10.55
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	7.15		
D4	3.59		
D5	3.26		
e	1.10	1.20	1.30
E	9.80	9.90	10.00
E1	7.40	7.50	7.60
E2	0.30	0.40	0.50
E3	8.50		
E4	9.46		
H	11.50	11.68	11.85
H1	6.55	6.65	6.75
K	4.08	4.18	4.28
L	1.60	1.90	2.10
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.30
L4	0.13	0.23	0.33
P	2.85	3.00	3.15
θ	10° REF		
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.20		

Figure3: Outline PG-TOLL(JQ)

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Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2020-09-15	Release version
1.1	2022-06-18	Updated TO247 POD to CD
1.2	2022-12-23	Updated Ciss/Coss/Crss&Trr/Qrr/Irrm, and added electrical characteristics diagram
1.3	2023-04-26	Added TO220F package
1.4	2023-08-22	Added TOLL-8L package

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