

## MOSFET Silicon N-Channel MOS



### 1. Applications

Single-ended flyback or two-transistor forward topologies.  
PC power, PD Adaptor, LCD & PDP TV and LED lighting.

### 2. Features

Low drain-source on-resistance:  $R_{DS(ON)} = 236\text{m}\Omega$  (typ.)  
Easy to control Gate switching  
Enhancement mode:  $V_{th} = 2.8$  to  $4.2$  V

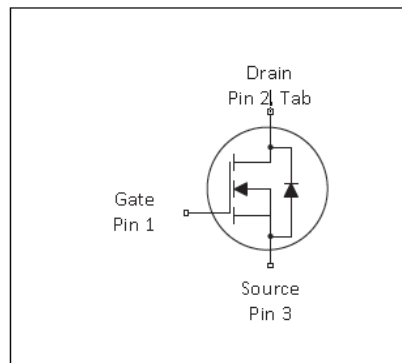
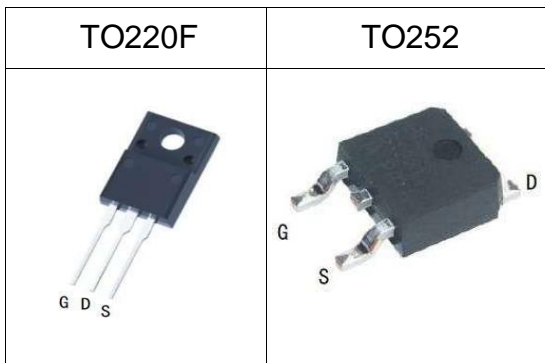


**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	270	m $\Omega$
$Q_{g,typ}$	23.2	nC
$I_{D,pulse}$	58	A
Body diode dv/dt	50	V/ns

### 3. Packaging and Internal Circuit

Part Name	Package	Marking
ASD65R270E	TO252	ASD65R270E
ASA65R270E	TO220F	ASA65R270E



## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$		-	15	A	$T_C = 25^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	58	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	88	mJ	$T_C = 25^\circ\text{C}$ , $V_{DD} = 50\text{V}$ , $I_{av} = 4.2\text{A}$ , $L = 10\text{mH}$ , $R_G = 25\Omega$
Avalanche current, single pulse	$I_{AR}$	-	-	4.2	A	$T_C = 25^\circ\text{C}$ , $V_{DD} = 50\text{V}$ , $L = 10\text{mH}$ , $R_G = 25\Omega$
MOSFET dv/dt ruggedness	dv/dt	-	-	80	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f > 1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	125	W	$T_C = 25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	
Soldering Temperature Distance of 1.6mm from case for 10s	$T_L$			260	$^\circ\text{C}$	
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq 58\text{A}$ , $T_j = 25^\circ\text{C}$

<sup>1)</sup>Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$

<sup>2)</sup>Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup>Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

### Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.99	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint

### 3 Electrical characteristics

at  $T_j=25^{\circ}\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=650V, V_{GS}=0V, T_j=25^{\circ}\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	236	270	m $\Omega$	$V_{GS}=10V, I_D=5.5A, T_j=25^{\circ}\text{C}$
Gate resistance (Intrinsic)	$R_G$	-	32	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1160	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	29.1	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Reverse transfer capacitance	$C_{rss}$	-	0.8	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Turn-on delay time	$t_{d(on)}$	-	21.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=10.2\Omega$
Rise time	$t_r$	-	23.4	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=10.2\Omega$
Turn-off delay time	$t_{d(off)}$	-	122.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=10.2\Omega$
Fall time	$t_f$	-	21.4	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=10.2\Omega$

**Table 6 Gate charge characteristics**

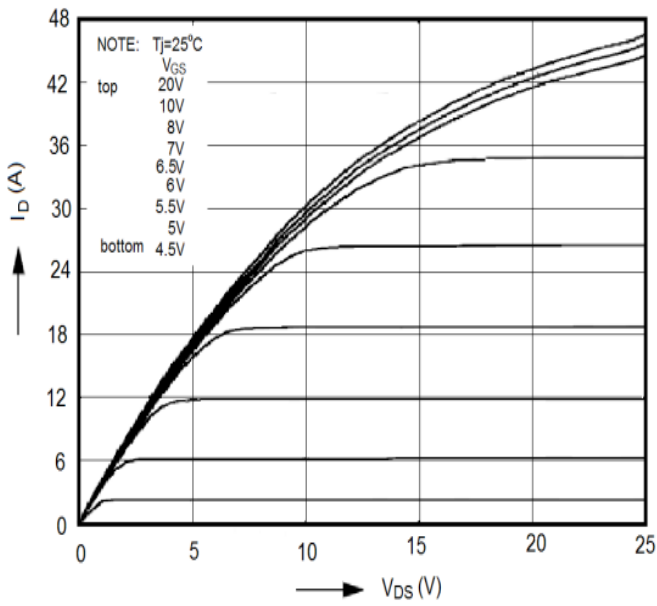
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	5.4	-	nC	$V_{DD}=400V, I_D=5.2A, V_{GS}=0$ to 10V
Gate to drain charge	$Q_{gd}$	-	8.1	-	nC	$V_{DD}=400V, I_D=5.2A, V_{GS}=0$ to 10V
Gate charge total	$Q_g$	-	23.2	-	nC	$V_{DD}=400V, I_D=5.2A, V_{GS}=0$ to 10V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.74	-	V	$V_{GS}=0V, I_F=1A, T_J=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	210.5	-	ns	$V_R=400V, I_F=5.2A, di_F/dt=100A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	1.7	-	$\mu C$	$V_R=400V, I_F=5.2A, di_F/dt=100A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	18	-	A	$V_R=400V, I_F=5.2A, di_F/dt=100A/\mu s$

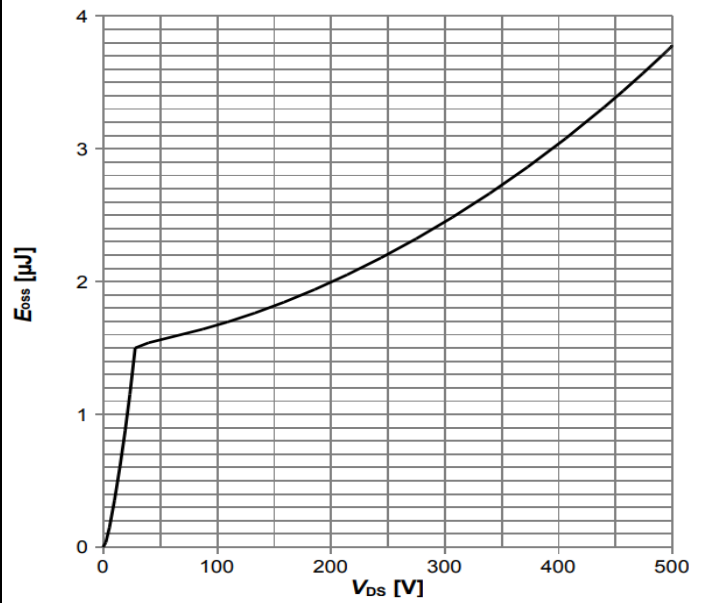
## 4 Electrical characteristics diagram

Diagram 1: Typ. output characteristics



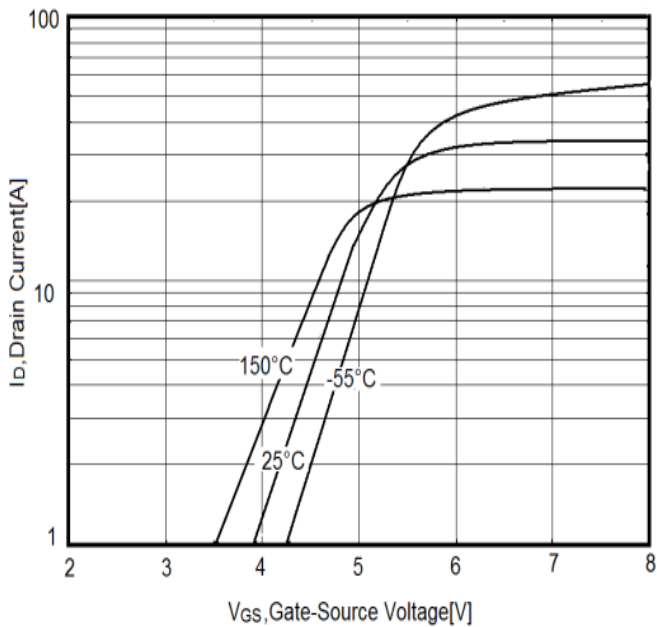
$I_D=f(V_{DS}); T_j=25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 2: Typ. Coss stored energy



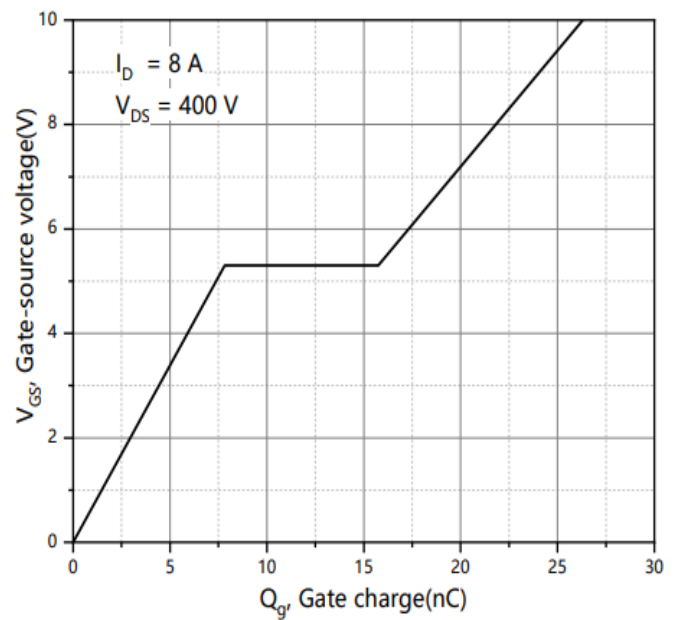
$E_{oss}=f(V_{DS})$

Diagram 3: Typ. transfer characteristics



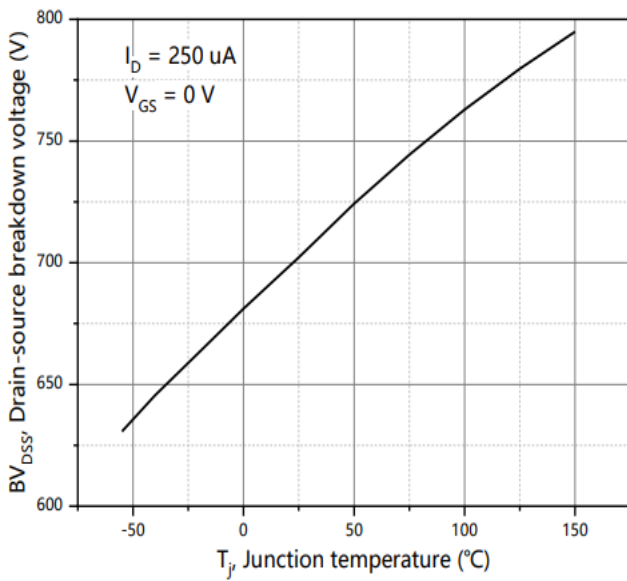
$I_D=f(V_{GS}); \text{parameter: } T_j$

Diagram 4: Typ. gate charge



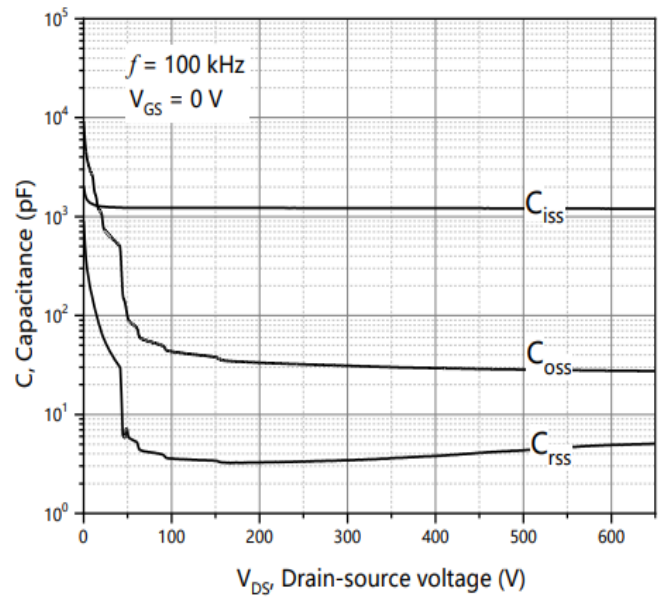
$V_{GS}=f(Q_{gate}); I_D=8\text{A pulsed}; \text{parameter: } V_{DD}$

**Diagram 5: Drain-source breakdown voltage**



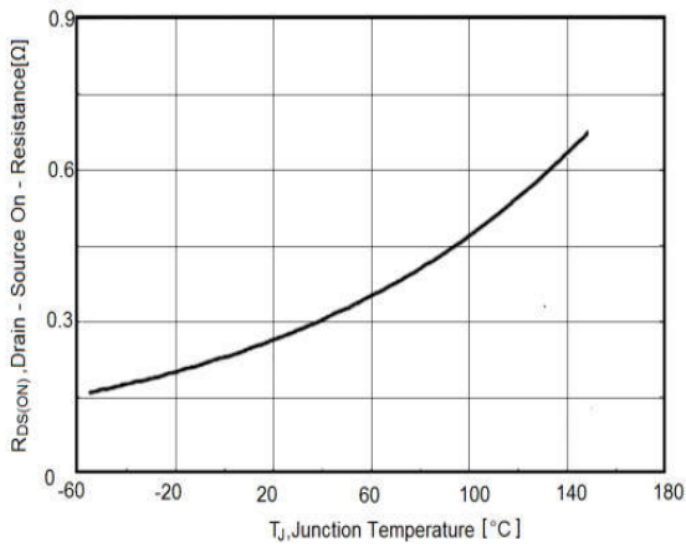
$$V_{BR(DSS)} = f(T_j); I_D = 250 \mu A$$

**Diagram 6: Typ. capacitances**



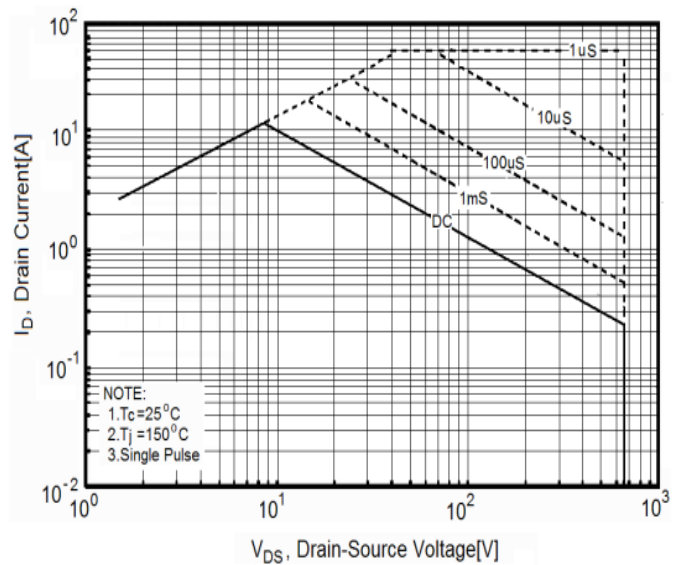
$$C = f(V_{DS}); V_{GS} = 0V; f = 0.1MHz$$

**Diagram 7: Typ. On-Resistance vs. Junction Temperature**



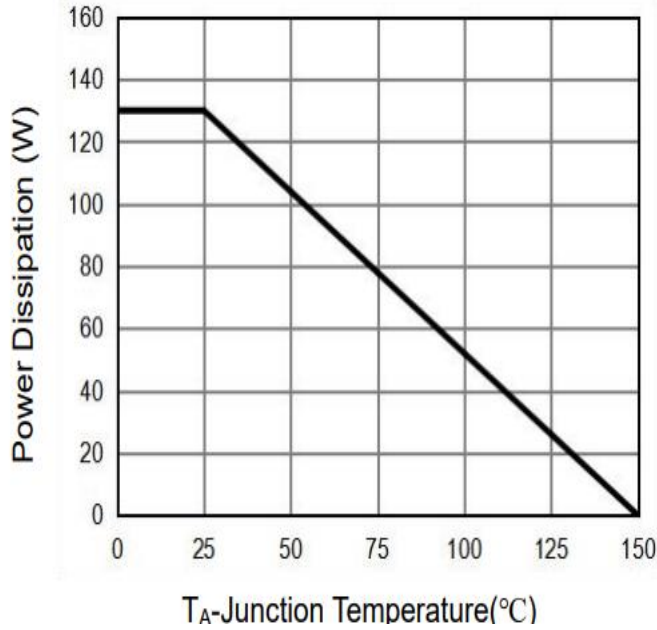
$$R_{ds(on)} = f(T_j); V_{GS} = 10V; I_D = 5.5A$$

**Diagram 8: Safe operating area  $T_C = 25^\circ C$ ,**



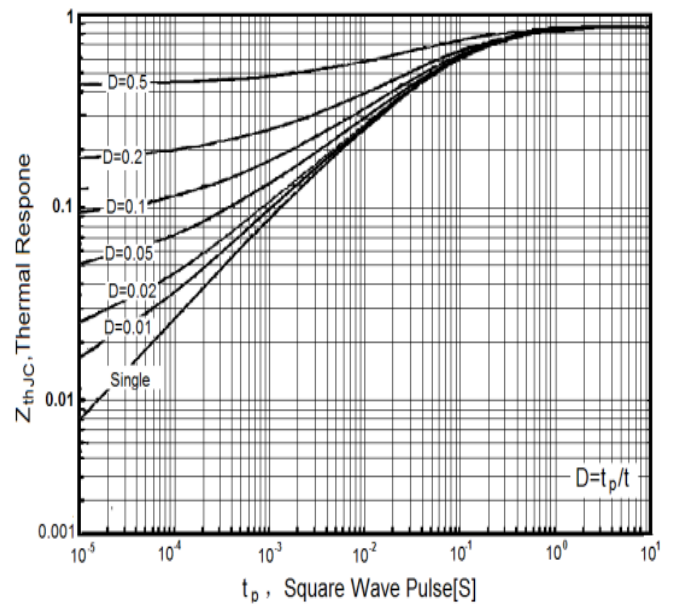
$$I_D = f(V_{DS}); T_C = 25^\circ C; V_{GS} > 7V; D = 0; \text{parameter } tp$$

Diagram 9: Typ. Power Dissipation



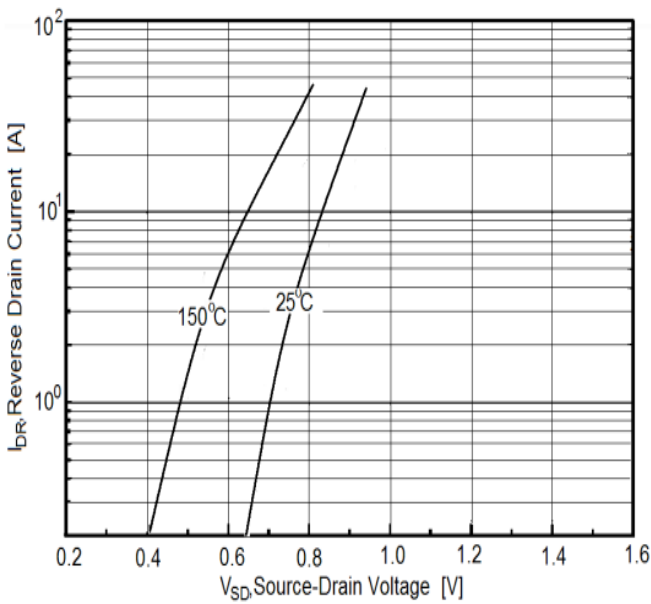
$P_{tot}=f(T_C)$

Diagram 10: Max. transient thermal impedance



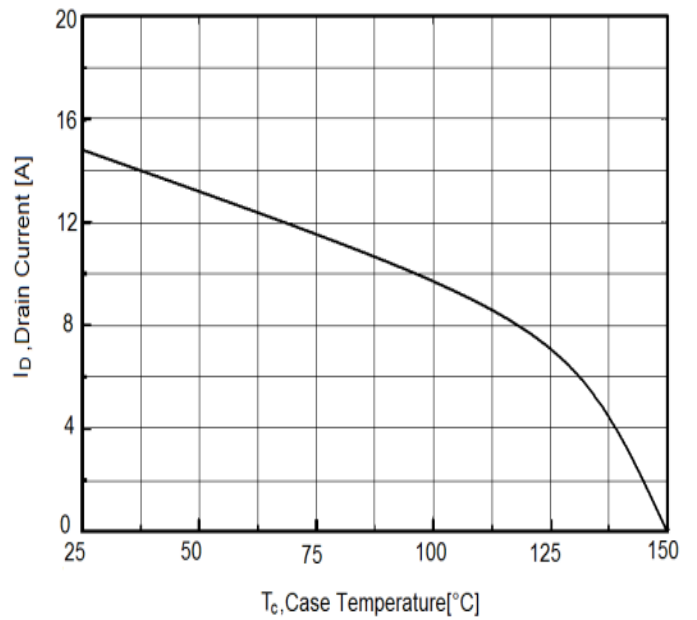
$Z_{thJC}=f(t_p)$ ; parameter:  $D=t_p/T$

Diagram 11: Forward characteristics of reverse diode



$I_F=f(V_{DS})$ ; parameter:  $T_j$

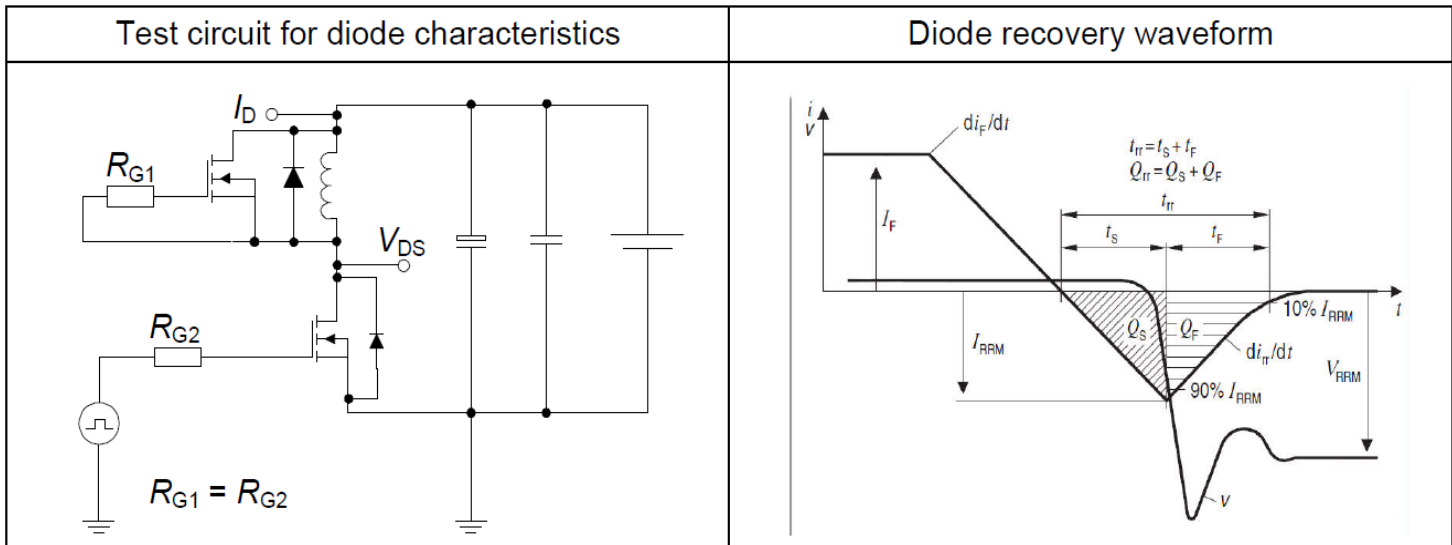
Diagram 12: Maximum Id vs Junction Temperature



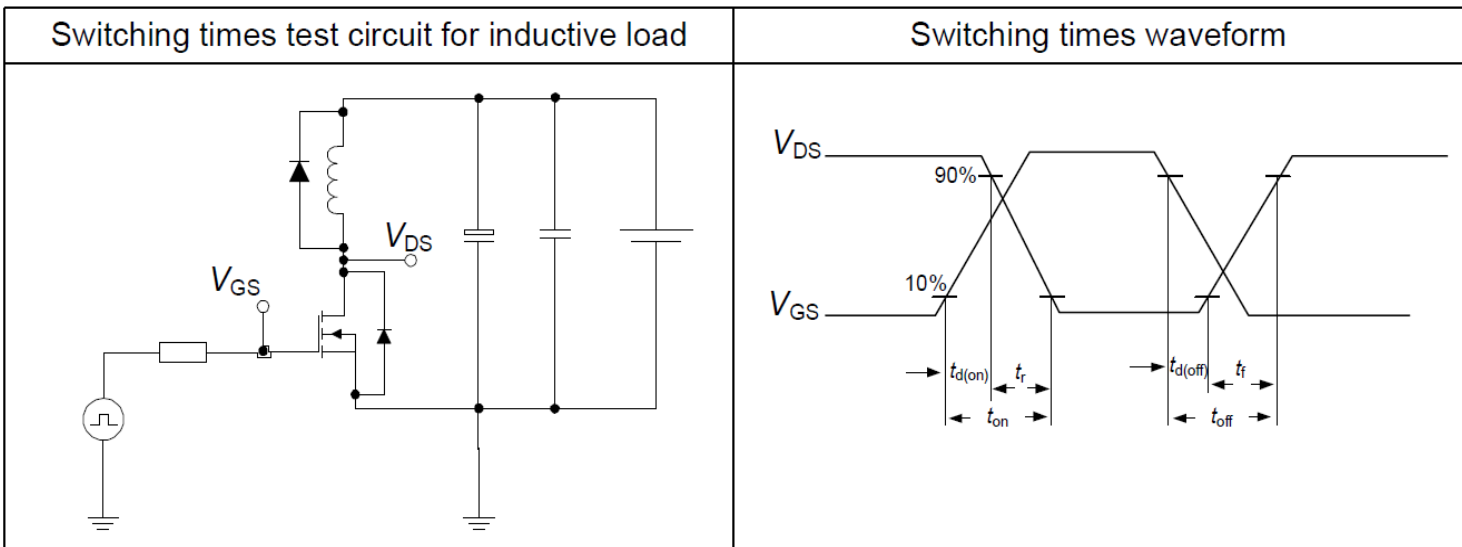


## 5 Test Circuits

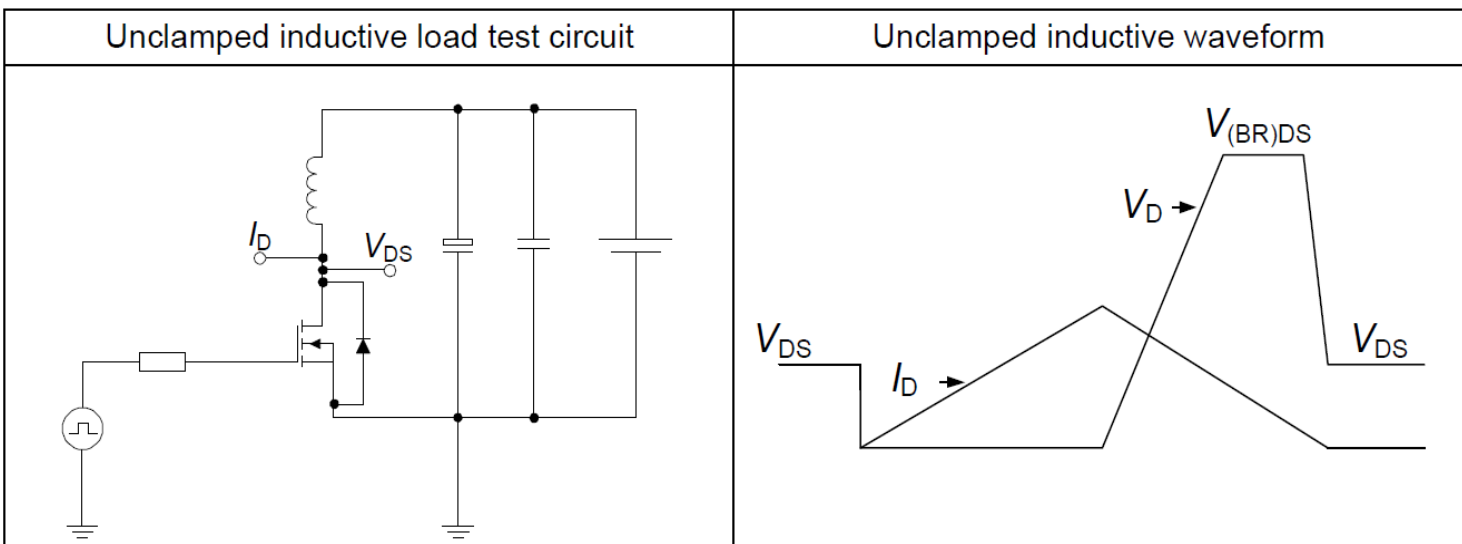
**Table 8 Diode characteristics**



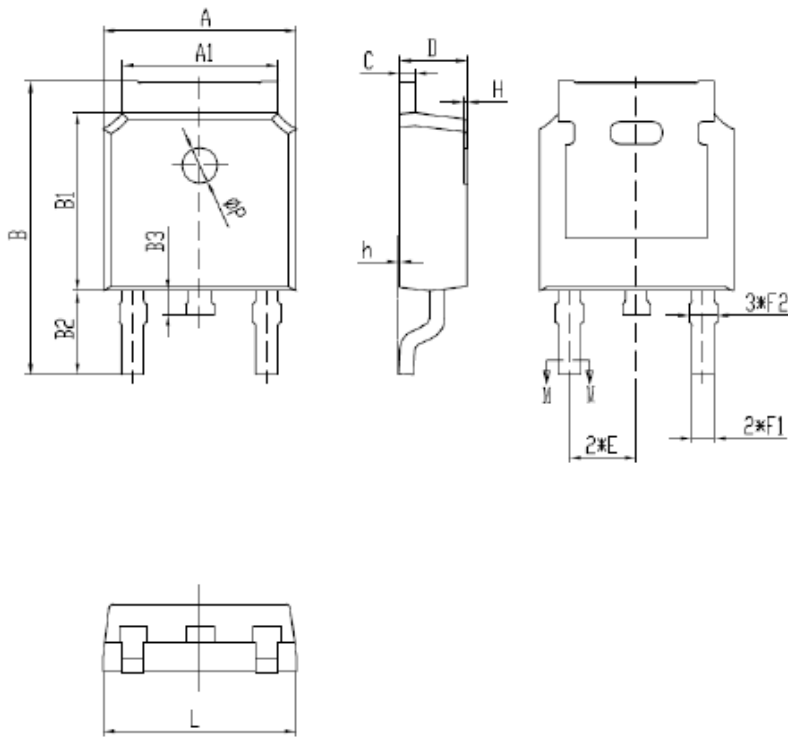
**Table 9 Switching times**



**Table 10 Unclamped inductive load**

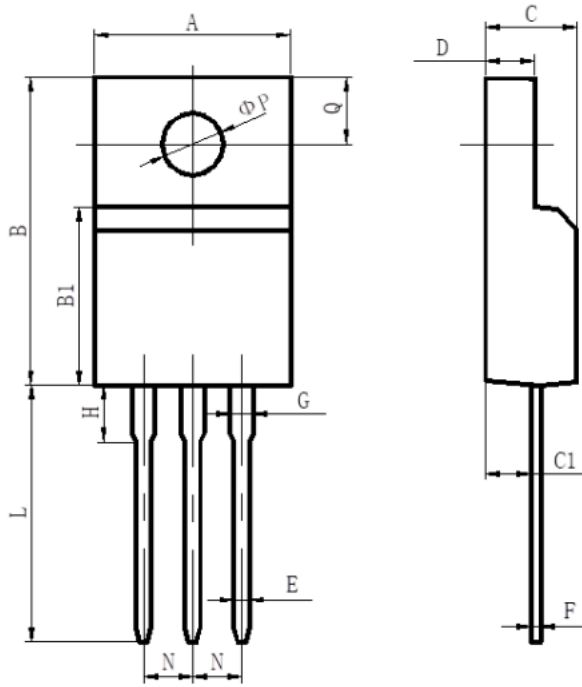


6 Package Outlines



项目	规范(mm)	
	MIN	MAX
A	6.50	6.70
A1	5.16	5.46
B	9.77	10.17
B1	6.00	6.20
B2	2.60	3.00
B3	0.70	0.90
C	0.45	0.61
D	2.20	2.40
E	2.186	2.386
F1	0.67	0.87
F2	0.76	0.96
H	0.00	0.30
h	0.00	0.127
L	6.50	6.70
φ P	1.10	1.30

Figure1: Outline PG-T0252(HT)



项目	规范(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
B1	8.99	9.39
C	4.40	4.80
C1	2.15	2.55
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
Q	3.15	3.55
$\phi P$	3.00	3.30

Figure2: Outline PG-TO220F(HT)

## Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2021-11-12	Preliminary version
1.1	2022-02-21	Added diagram of characterization
1.2	2023-07-31	Added ASA65R270E TO220F

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