

MOSFET Silicon N-Channel MOS



1. Applications

Single-ended flyback or two-transistor forward topologies.
PC power, PD Adaptor, LCD & PDP TV and LED lighting.

2. Features

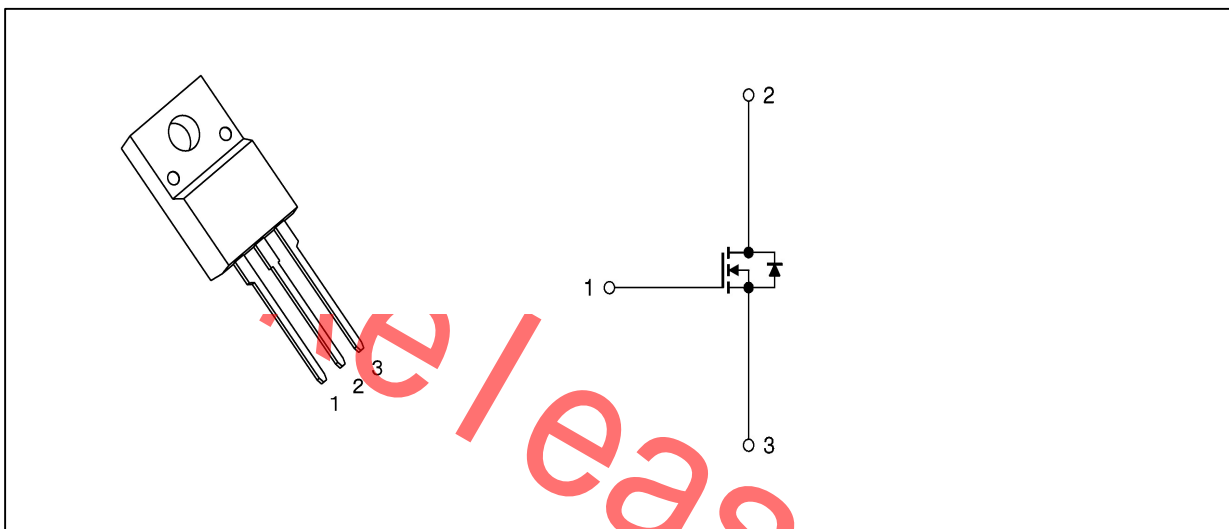
Low drain-source on-resistance: $R_{DS(ON)} = 0.211\Omega$ (typ.)
Easy to control Gate switching
Enhancement mode: $V_{th} = 2.8$ to 4.2 V



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	750	V
$R_{DS(on),max}$	240	m Ω
$Q_{g,typ}$	32.23	nC
$I_{D,pulse}$	60	A

3. Packaging and Internal Circuit



1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	20	A	$T_C = 25^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	60	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	898	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	69	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	33	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq 48\text{A}$, $T_j = 25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

Not for release

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

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3 Electrical characteristics

at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	705	-	-	V	$V_{GS}=0V, I_D=10mA$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	100	nA	$V_{DS}=700V, V_{GS}=0V, T_j=25^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.211	0.24	Ω	$V_{GS}=10V, I_D=10A, T_j=25^{\circ}\text{C}$
Gate resistance (Intrinsic)	R_G	-	11.1	-	Ω	$f=1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1547	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Output capacitance	C_{oss}	-	134	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Reverse transfer capacitance	C_{rss}	-	5.28	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Turn-on delay time	$t_{d(on)}$	-	12.4	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9
Rise time	t_r	-	21.6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	52	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9
Fall time	t_f	-	18.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.242	-	nC	$V_{DD}=400V, I_D=8A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	10.85	-	nC	$V_{DD}=400V, I_D=8A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	32.23	-	nC	$V_{DD}=400V, I_D=8A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V, I_D=8A, V_{GS}=0 \text{ to } 10V$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.72	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	275	-	ns	$V_R=400V, I_F=8 A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	3.809	-	uC	$V_R=400V, I_F=8 A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	25.6	-	A	$V_R=400V, I_F=8 A, di_F/dt=100A/\mu s$; see table 8

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4 Test Circuits

Table 8 Diode characteristics

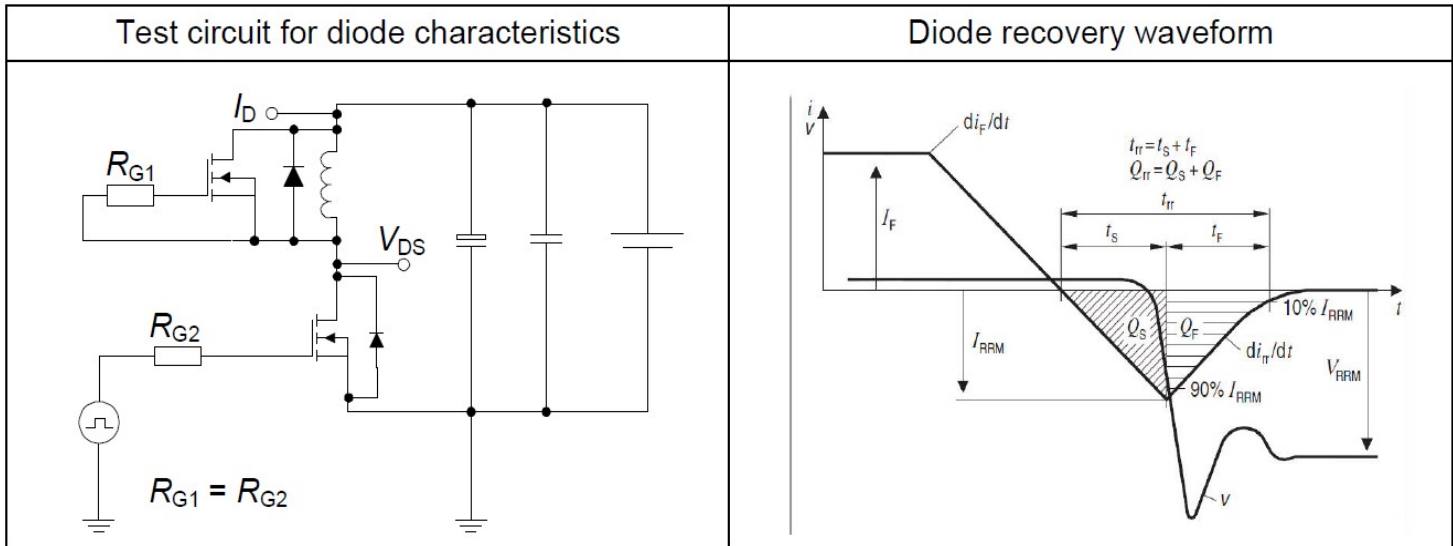


Table 9 Switching times

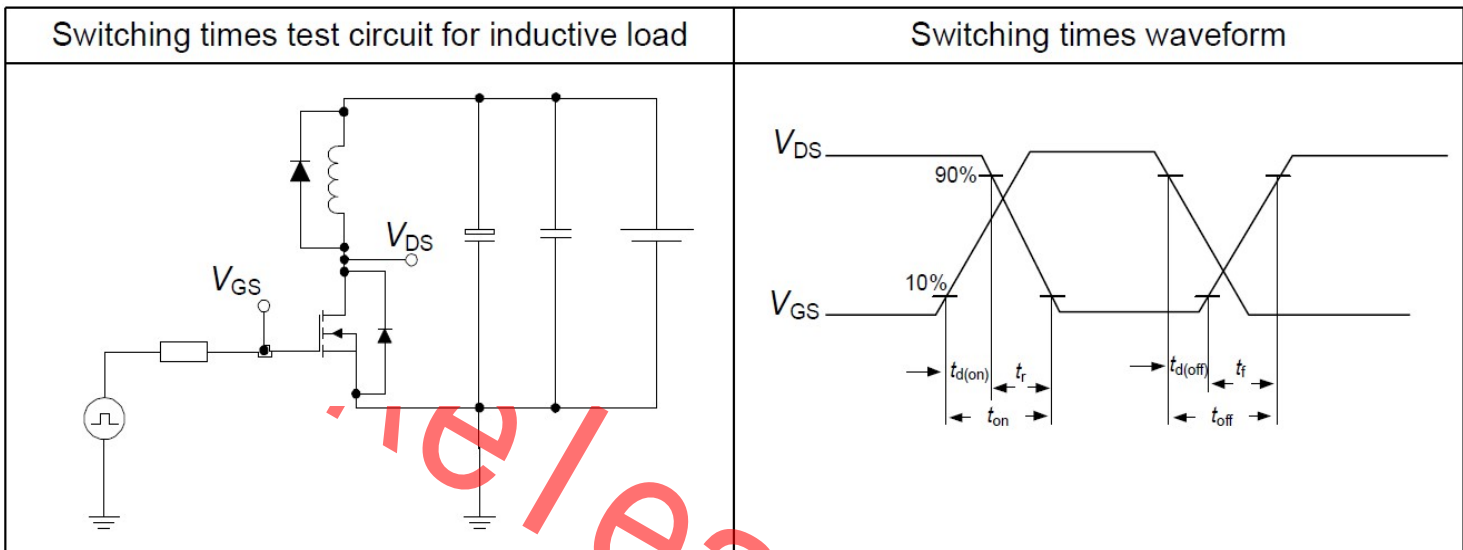
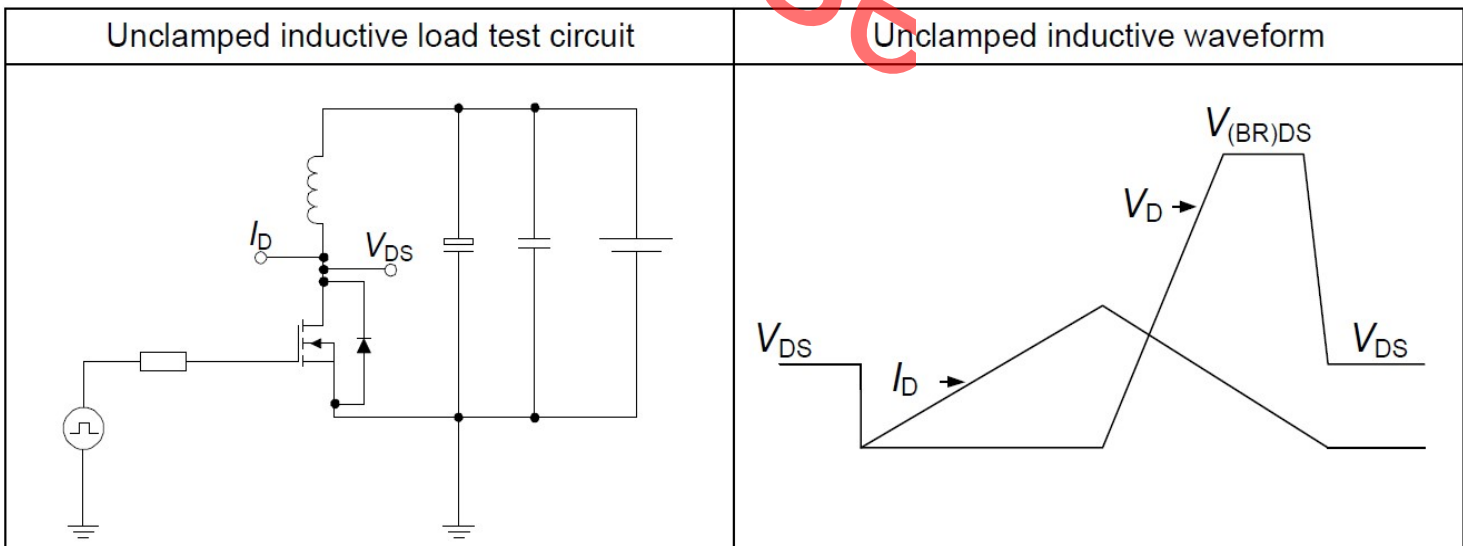


Table10 Unclamped inductive load



5 Package Outlines

TO-220F

单位: mm

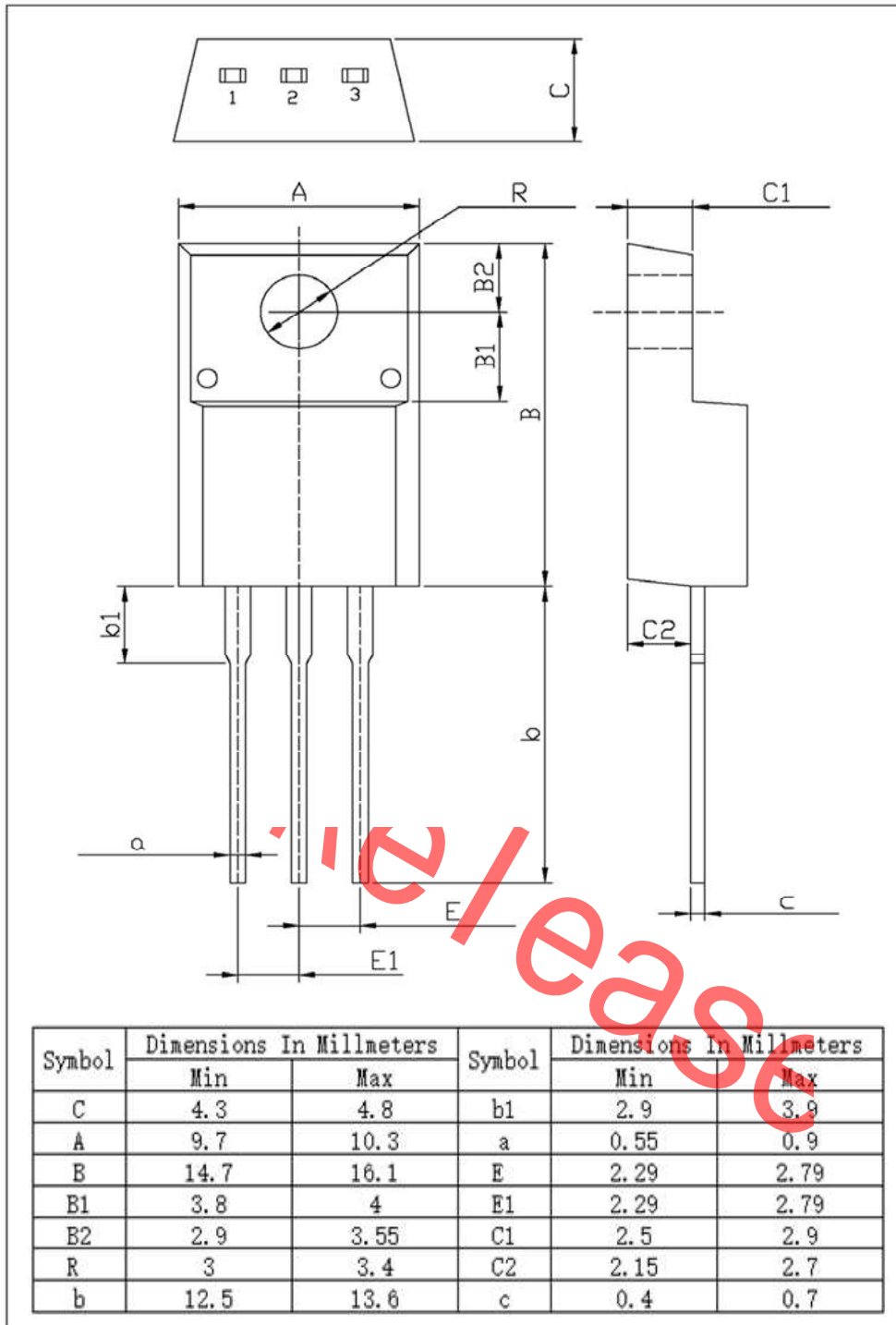


Figure1: Outline PG-T0220F

Revision History

ASA70R240E

Revision	Date	Subjects (major changes since last revision)
0.1	2019-5-08	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc

Pre-release

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