

MOSFET Silicon N-Channel MOS

1. Applications

Single-ended flyback or two-transistor forward topologies.
PC power, PD Adaptor, LCD & PDP TV and LED lighting.



2. Features

Low drain-source on-resistance: $R_{DS(ON)} = 620\text{m}\Omega$ (typ.)
Easy to control Gate switching
Enhancement mode: $V_{th} = 2.8$ to 4.2 V

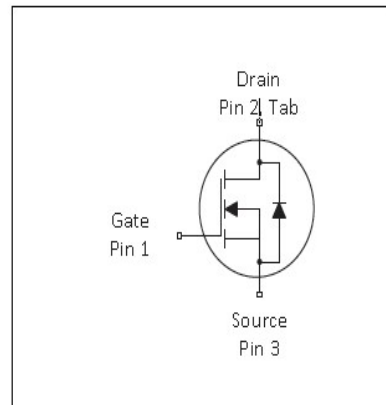


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	850	V
$R_{DS(on),max}$	710	$\text{m}\Omega$
$Q_{g,typ}$	18.5	nC
$I_{D,pulse}$	35	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA80R900E	TO220F	ASA80R900E



1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	8.5	A	$T_C=25^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	35	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	88	mJ	$T_C=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $I_{av}=4.2\text{A}$, $L=10\text{mH}$, $R_G=25\Omega$
Avalanche current, single pulse	I_{AR}	-	-	4.2	A	$T_C=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $L=10\text{mH}$, $R_G=25\Omega$
Gate source voltage (static)	V_{GS}	-30	-	30	V	static;
Power dissipation	P_{tot}	-	-	43	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.26	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	76	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=800V, V_{GS}=0V, T_j=25^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	620	710	m Ω	$V_{GS}=10V, I_D=6A, T_j=25^{\circ}\text{C}$
Gate resistance (Intrinsic)	R_G	-	25	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	850.8	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Output capacitance	C_{oss}	-	34.4	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Reverse transfer capacitance	C_{rss}	-	0.92	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	-	40.6	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=4.1A, R_G=50\Omega$
Rise time	t_r	-	34.8	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=4.1A, R_G=50\Omega$
Turn-off delay time	$t_{d(off)}$	-	128	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=4.1A, R_G=50\Omega$
Fall time	t_f	-	31	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=4.1A, R_G=50\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.0	-	nC	$V_{DD}=400V, I_D=4.1A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	6.6	-	nC	$V_{DD}=400V, I_D=4.1A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	18.5	-	nC	$V_{DD}=400V, I_D=4.1A, V_{GS}=0$ to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.75	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	266.5	-	ns	$V_R=400V, I_F=4.1A, di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	2.2	-	uC	$V_R=400V, I_F=4.1A, di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	14	-	A	$V_R=400V, I_F=4.1A, di_F/dt=100A/\mu s$

4 Test Circuits

Table 8 Diode characteristics

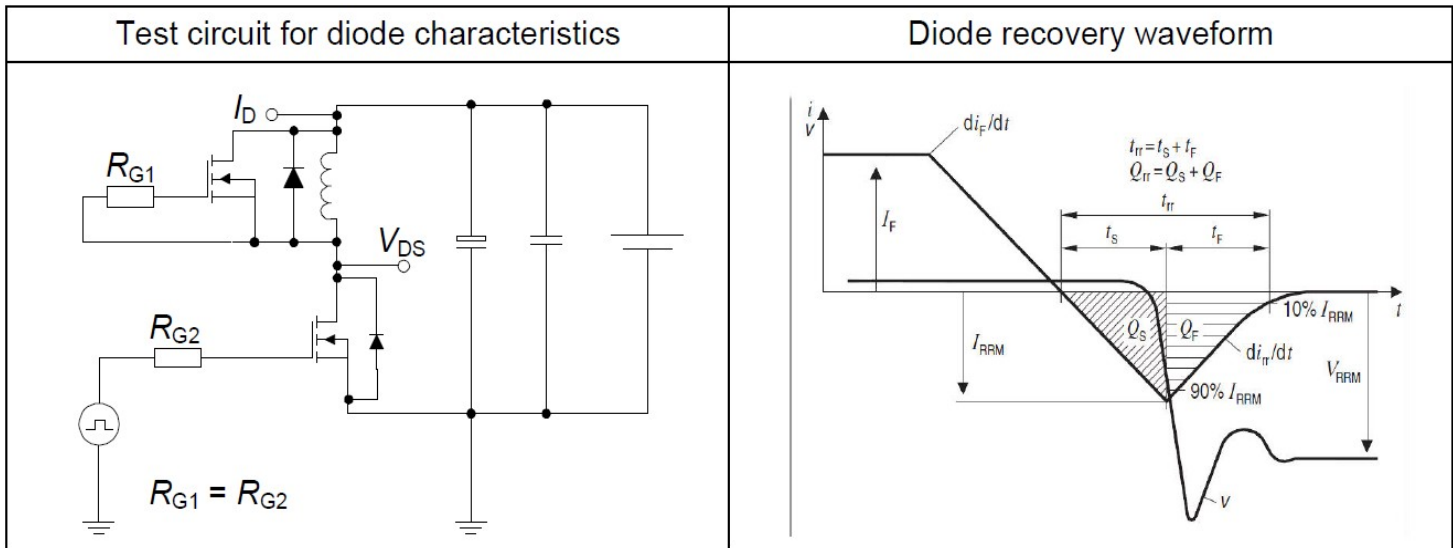


Table 9 Switching times

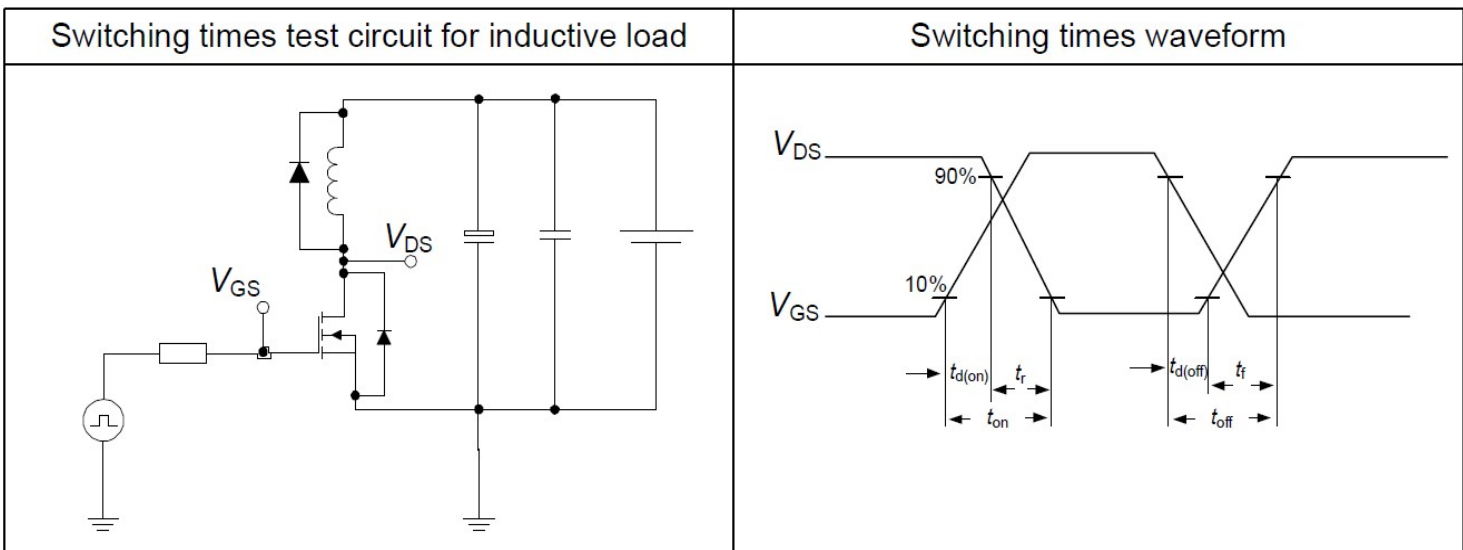
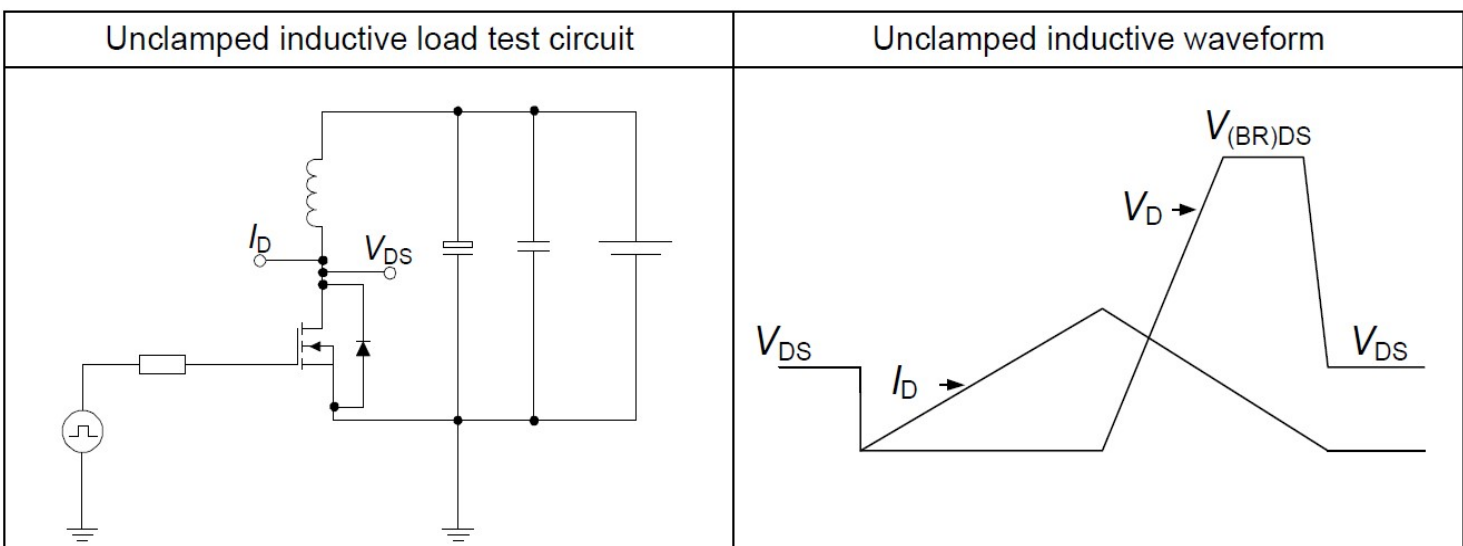
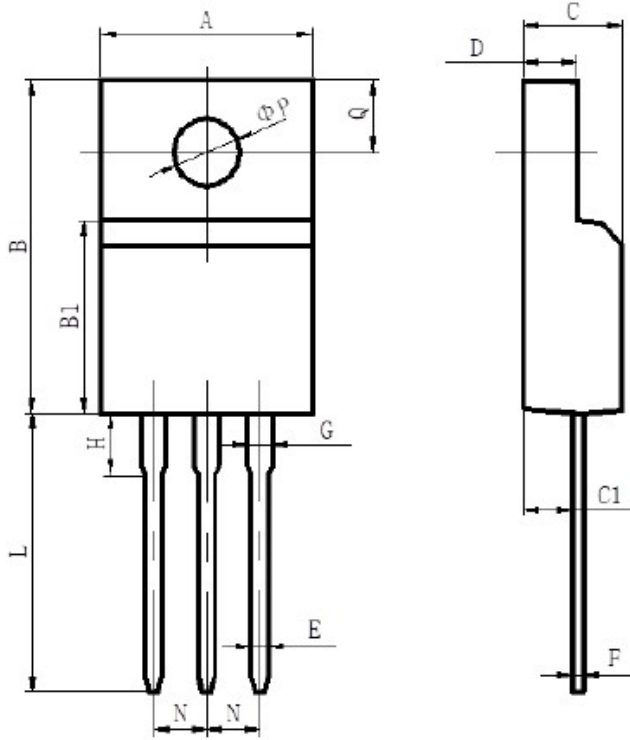


Table 10 Unclamped inductive load



5 Package Outlines



項目	規格(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
B1	8.99	9.39
C	4.40	4.80
C1	2.15	2.55
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
Q	3.15	3.55
ϕP	3.00	3.30

Outline PG-TO220F

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2021-11-4	Preliminary version

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