

MOSFET Silicon N-Channel MOS



1. Applications

Boost PFC switch, single-ended flyback or two-transistor forward, Half bridge or Asymmetric half bridge or Series resonance half bridge topologies. PC power, Adaptor, LCD & PDP TV, LED Lighting, Server power, Telecom power and UPS application.



2. Features

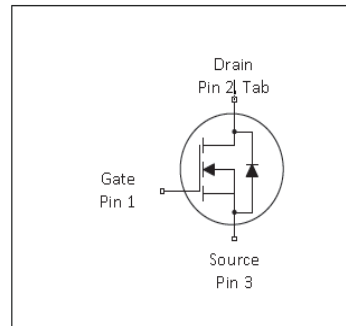
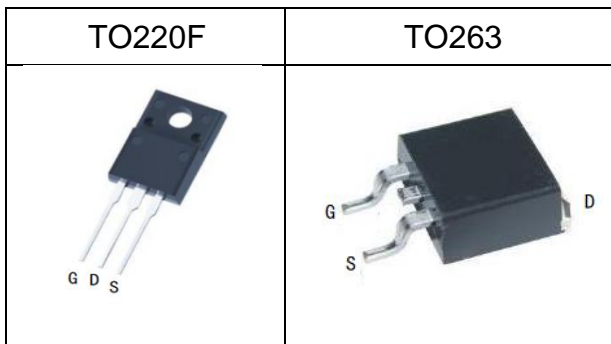
Low drain-source on-resistance: $R_{DS(ON)} = 0.19\Omega$ (typ.)
 Easy to control Gate switching
 Enhancement mode: $V_{th} = 2.8$ to 4.2 V

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	220	m Ω
$Q_{g,typ}$	32.23	nC
$I_{D,pulse}$	60	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA65R220E	TO220F	ASA65R220E
ASB65R220E	TO263	ASB65R220E



1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	20	A	$T_C = 25^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	60	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	830	mJ	$T_C = 25^\circ\text{C}, V_{DD} = 50\text{V}, L = 10\text{mH},$ $RG = 25\Omega$
Avalanche current, single pulse	I_{AR}	-	-	3	A	$T_C = 25^\circ\text{C}, V_{DD} = 50\text{V}, L = 10\text{mH},$ $RG = 25\Omega$
MOSFET dv/dt ruggedness	dv/dt	-	-	69	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	V_{GS}	-30	-	30	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC($f > 1\text{Hz}$)
Power dissipation (TO220F)	P_{tot}	-	-	33	W	$T_C = 25^\circ\text{C}$
Power dissipation (TO263)	P_{tot}	-	-	126	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}, I_{SD} \leq 48\text{A}, T_j = 25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high sides witch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (T0220 FullPAK)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

Thermal characteristics (T0263)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.99	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650V, V_{GS}=0V, T_j=25^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.19	0.22	Ω	$V_{GS}=10V, I_D=7A, T_j=25^{\circ}\text{C}$
Gate resistance	R_G	-	11	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1547	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10\text{kHz}$
Output capacitance	C_{oss}	-	134	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10\text{kHz}$
Reverse transfer capacitance	C_{rss}	-	5.28	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10\text{kHz}$
Turn-on delay time	$t_{d(on)}$	-	12.4	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9
Risetime	t_r	-	21.6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	52	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9
Fall time	t_f	-	18.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.242	-	nC	$V_{DD}=400V, I_D=8A, V_{GS}=0\text{to }10V$
Gate to drain charge	Q_{gd}		10.85	-	nC	$V_{DD}=400V, I_D=8A, V_{GS}=0\text{to }10V$
Gate charge total	Q_g	-	32.23	-	nC	$V_{DD}=400V, I_D=8A, V_{GS}=0\text{to }10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V, I_D=8A, V_{GS}=0\text{to }10V$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.72	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	275	-	ns	$V_R=400V, I_F=8A, di_F/dt=100A/\mu s$; seetable8
Reverse recovery charge	Q_{rr}	-	3.809	-	μC	$V_R=400V, I_F=8A, di_F/dt=100A/\mu s$; seetable8
Peak reverse recovery current	I_{rrm}	-	25.6	-	A	$V_R=400V, I_F=8A, di_F/dt=100A/\mu s$; seetable8

4 Electrical characteristics diagram

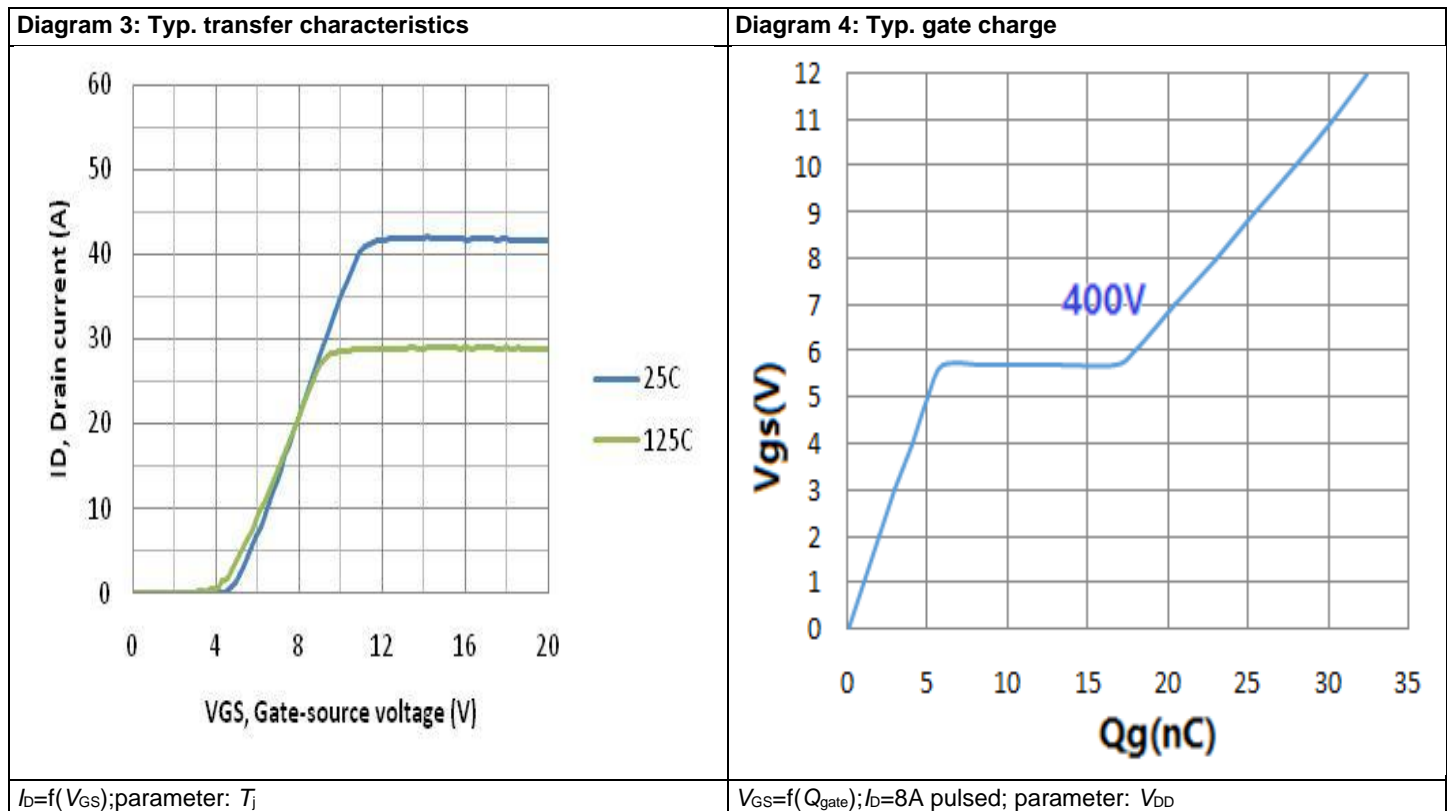
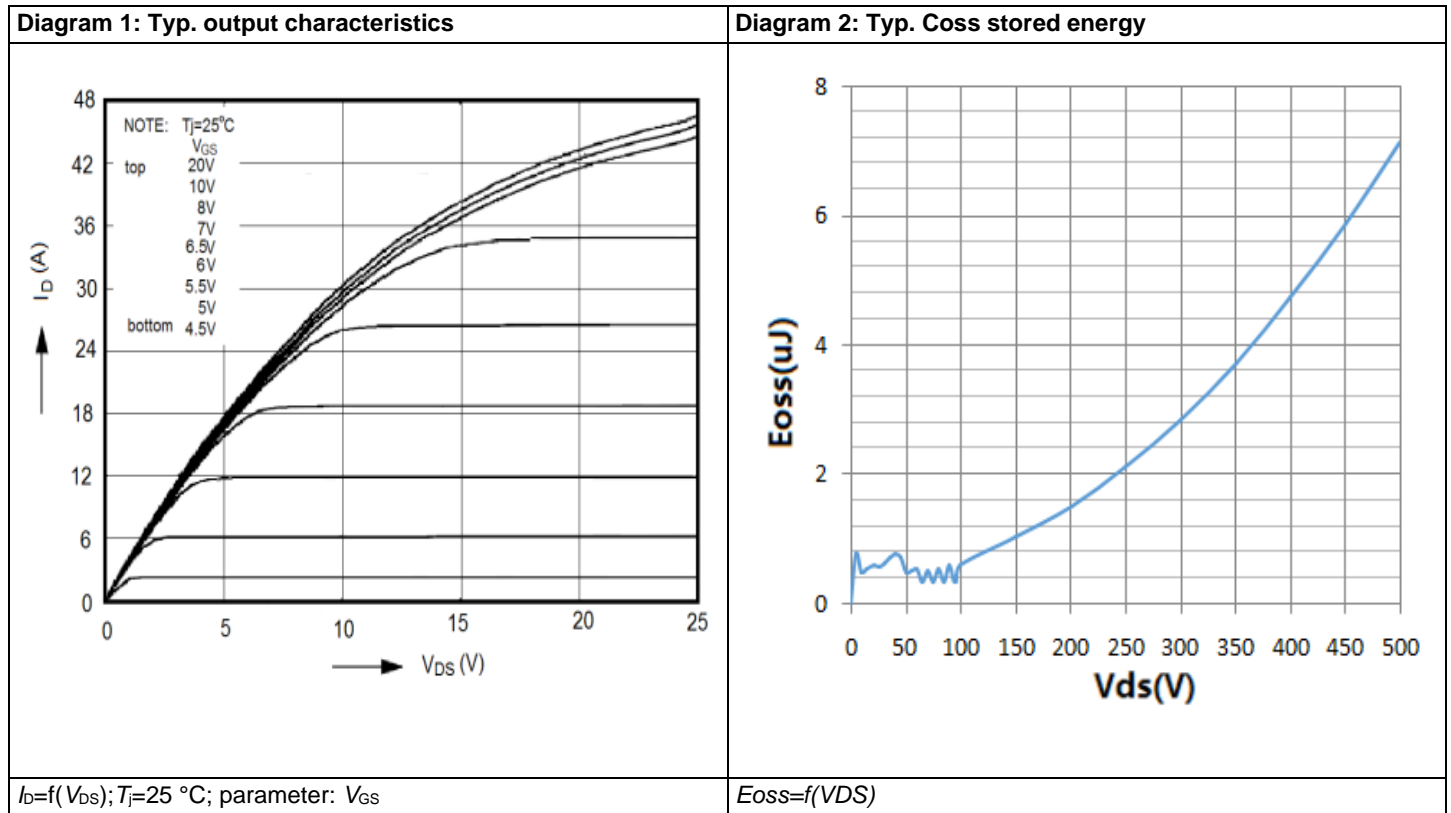
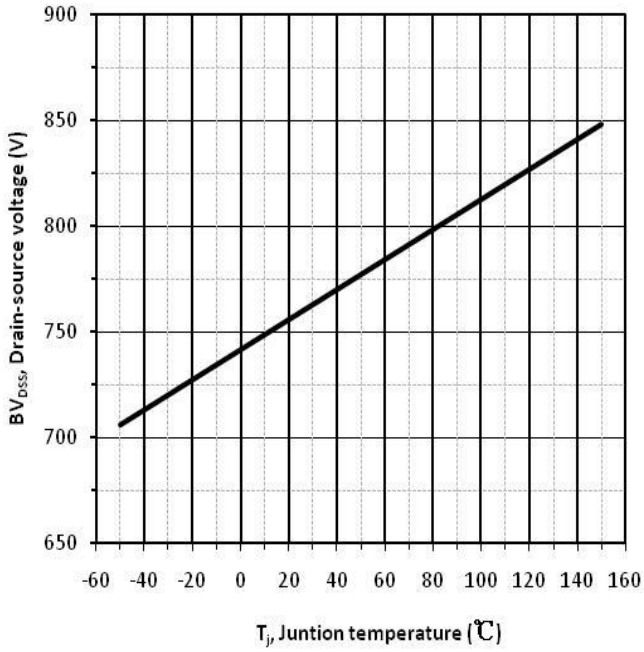
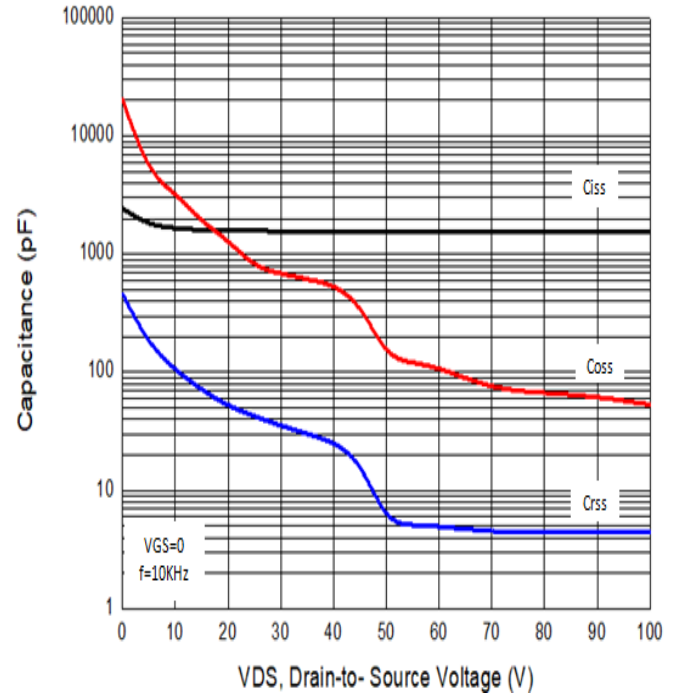


Diagram 5: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_b=10mA$

Diagram 6: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0V; f=10\text{ kHz}$

5 Test Circuits

Table 8 Diode characteristics

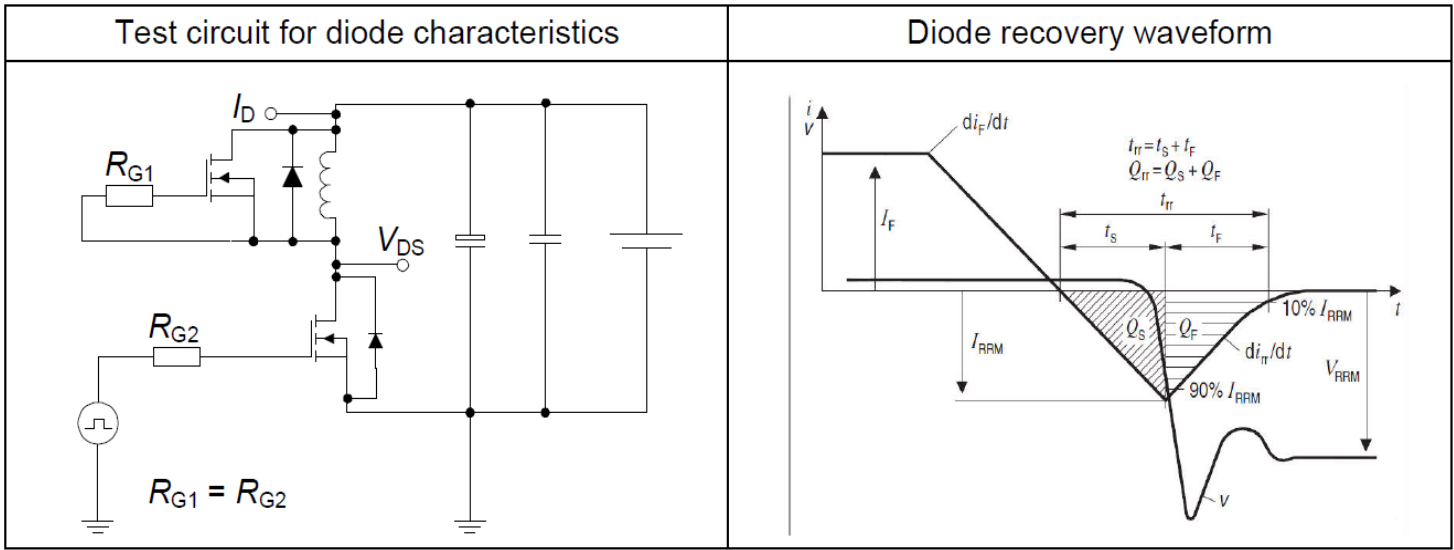


Table 9 Switching times

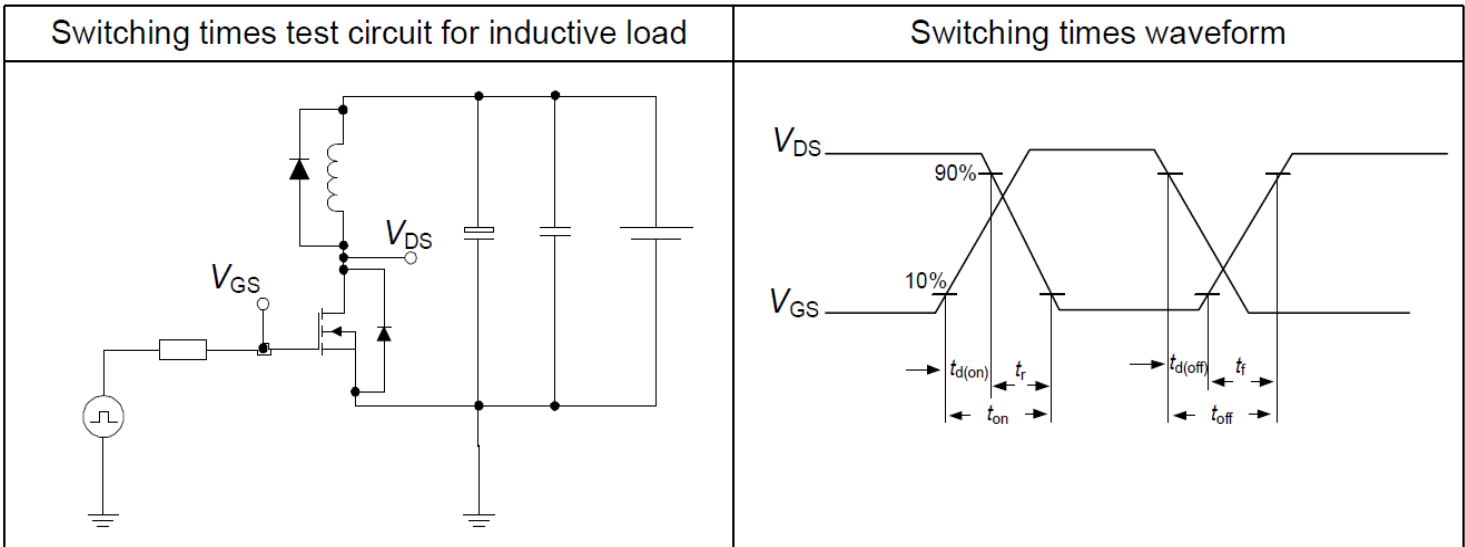
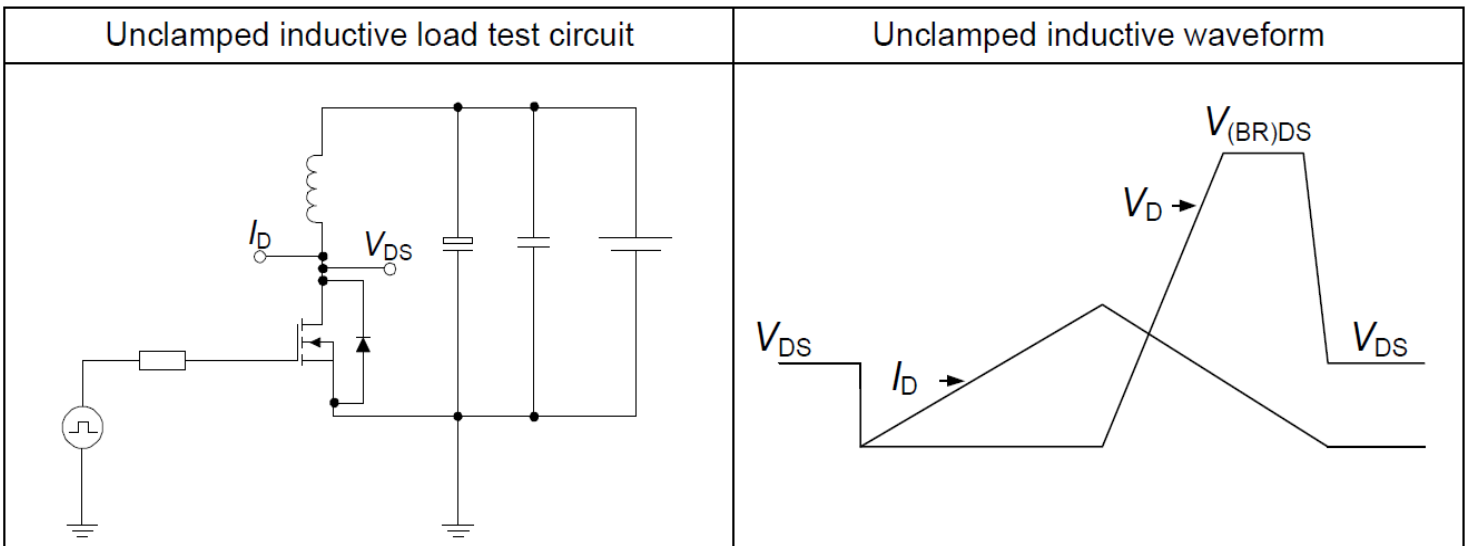
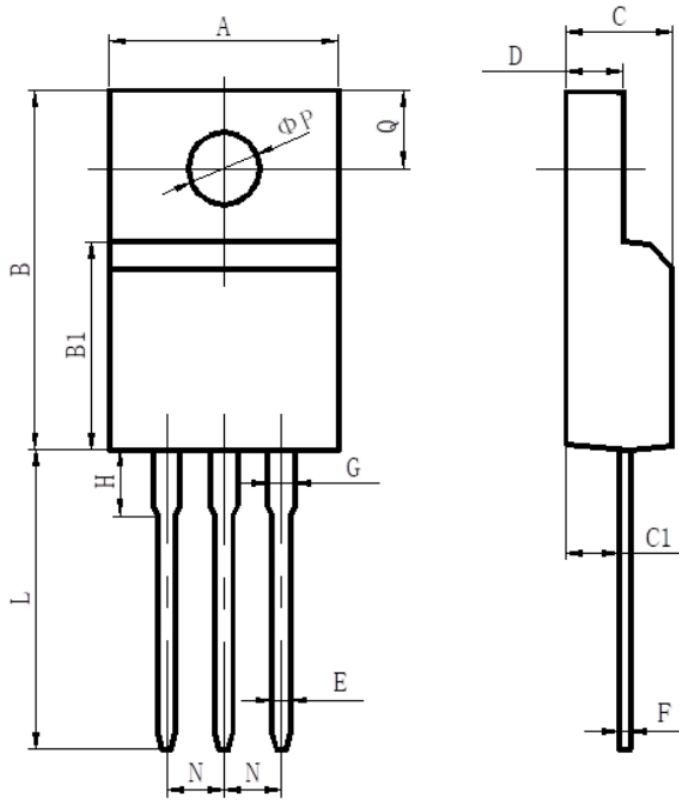


Table 10 Unclamped inductive load





项目	规范(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
B1	8.99	9.39
C	4.40	4.80
C1	2.15	2.55
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
Q	3.15	3.55
ϕP	3.00	3.30

Figure1: Outline PG-TO220F(HT)

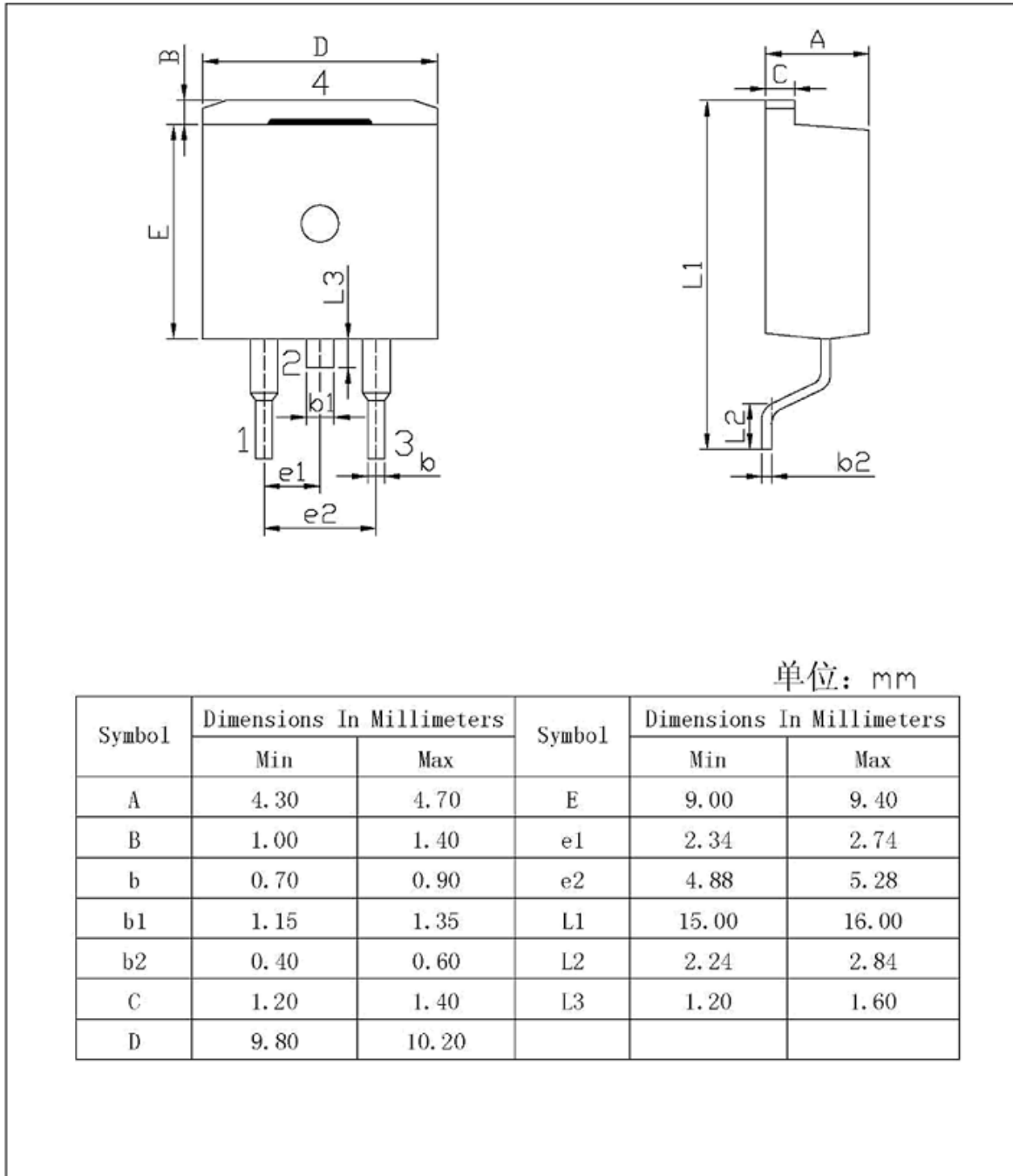


Figure2: Outline PG-T0263(FS)

Revision History

Revision	Date	Subjects (major changes since last revision)
0.1	2019-05-27	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc
1.1	2020-03-16	Update key Parameters
1.2	2020-03-31	Add Electrical characteristics Curve
1.3	2020-04-18	Add avalanche energy test condition, avalanche current data and test condition
1.4	2022-09-19	Updated Idss limit, Vth test condition and TO220F POD to HT

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