

## MOSFET Silicon N-Channel MOS

### 1. Applications

Boost PFC switch, single-ended flyback or two-transistor forward topologies.  
PC power, PD Adaptor, LCD & PDP TV and LED lighting.



### 2. Features

Low drain-source on-resistance:  $R_{DS(ON)} = 0.750\Omega$  (typ.)  
Easy to control Gate switching  
Enhancement mode:  $V_{th} = 2.8$  to  $4.2$  V

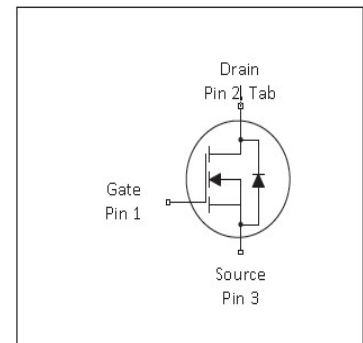
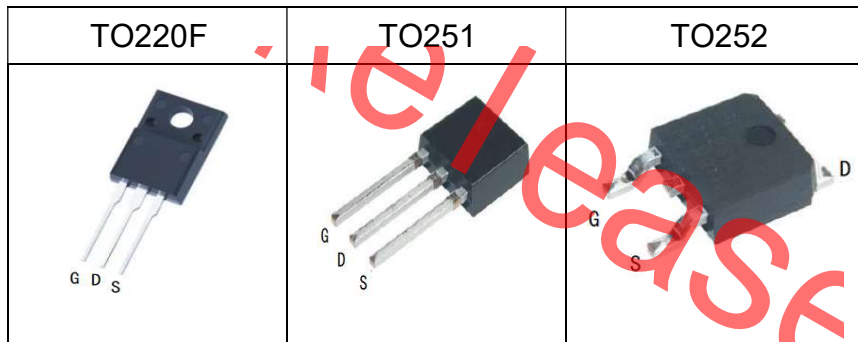


**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	850	m $\Omega$
$Q_{g,typ}$	10.3	nC
$I_{D,pulse}$	18	A

### 3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA65R850E	TO220F	ASA65R850E
ASU65R850E	TO251	ASU65R850E
ASD65R850E	TO252	ASD65R850E



## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$		-	6	A	$T_C = 25^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	18	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	624	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	36	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f > 1\text{ Hz}$ )
Power dissipation (TO220F)	$P_{tot}$	-	-	27	W	$T_C = 25^\circ\text{C}$
Power dissipation (TO252&TO251)	$P_{tot}$	-	-	74	W	$T_C = 25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq 48\text{A}$ , $T_j = 25^\circ\text{C}$ see table 8

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<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics (T0220 FullPAK)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	4.6	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	°C/W	device on PCB, minimal footprint

**Thermal characteristics (T0251 and T0252)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.7	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint

Not for release

### 3 Electrical characteristics

at  $T_j=25^{\circ}\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	$V_{GS}=0\text{V}$ , $I_D=10\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	100	nA	$V_{DS}=650\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=25^{\circ}\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=30\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.75	0.85	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=2.5\text{A}$ , $T_j=25^{\circ}\text{C}$
Gate resistance	$R_G$	-	33.7	-		$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	377	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=50\text{V}$ , $f=10\text{kHz}$
Output capacitance	$C_{oss}$	-	33	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=50\text{V}$ , $f=10\text{kHz}$
Reverse transfer capacitance	$C_{rss}$	-	4.55	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=50\text{V}$ , $f=10\text{kHz}$
Turn-on delay time	$t_{d(on)}$	-	8.4	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.5\text{A}$ , $R_G=6.8\Omega$ ; see table 9
Rise time	$t_r$	-	21.6	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.5\text{A}$ , $R_G=6.8\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	45.2	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.5\text{A}$ , $R_G=6.8\Omega$ ; see table 9
Fall time	$t_f$	-	24.4	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=2.5\text{A}$ , $R_G=6.8\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.845	-	nC	$V_{DD}=400\text{V}$ , $I_D=2.5\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	2.723	-	nC	$V_{DD}=400\text{V}$ , $I_D=2.5\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	10.3	-	nC	$V_{DD}=400\text{V}$ , $I_D=2.5\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	$V_{DD}=400\text{V}$ , $I_D=2.5\text{A}$ , $V_{GS}=0$ to $10\text{V}$

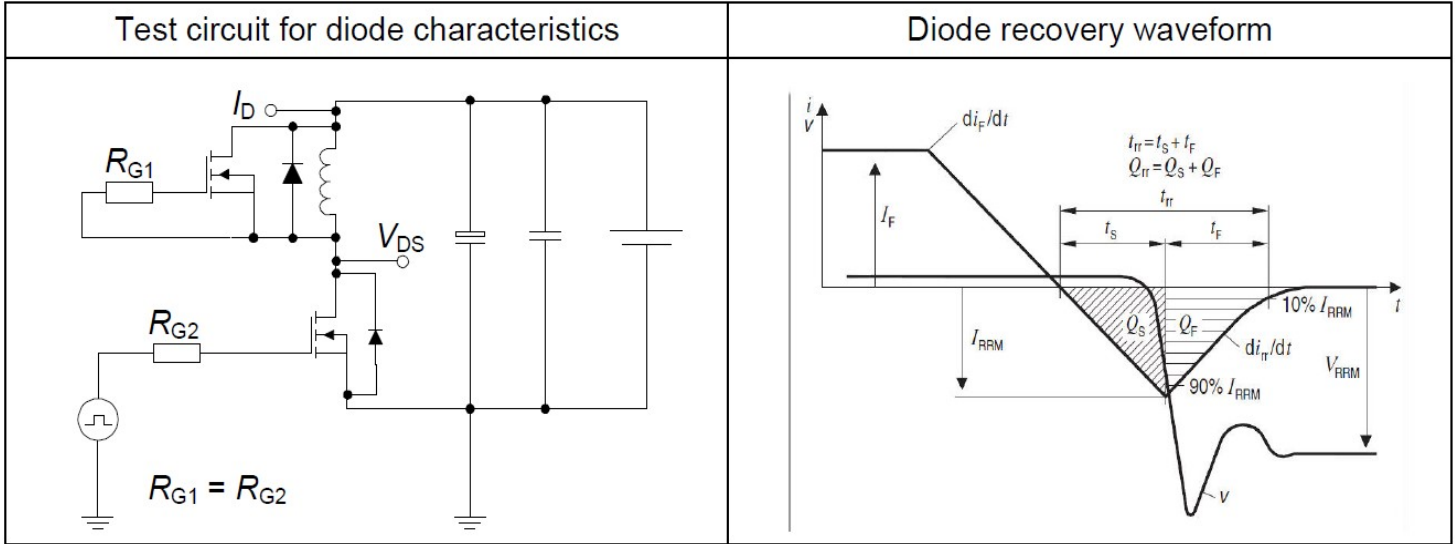
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.78	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	124	-	ns	$V_R=400V, I_F=2.5 A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	0.88	-	uC	$V_R=400V, I_F=2.5 A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	10	-	A	$V_R=400V, I_F=2.5 A, di_F/dt=100A/\mu s$ ; see table 8

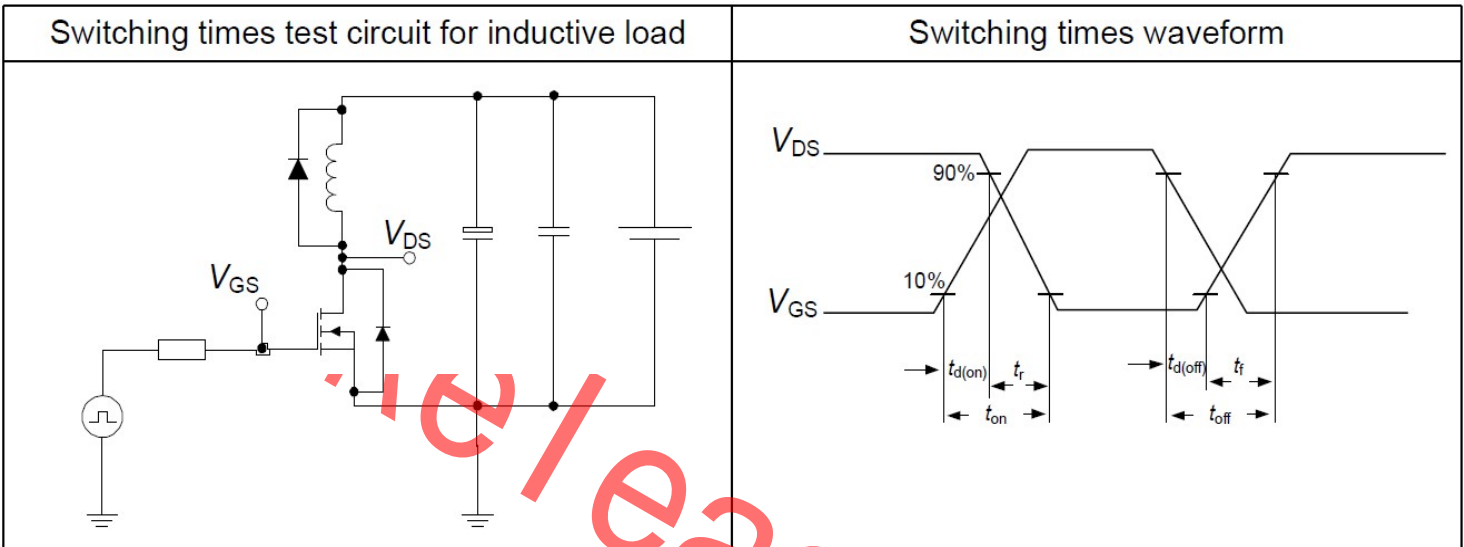
release

## 4 Test Circuits

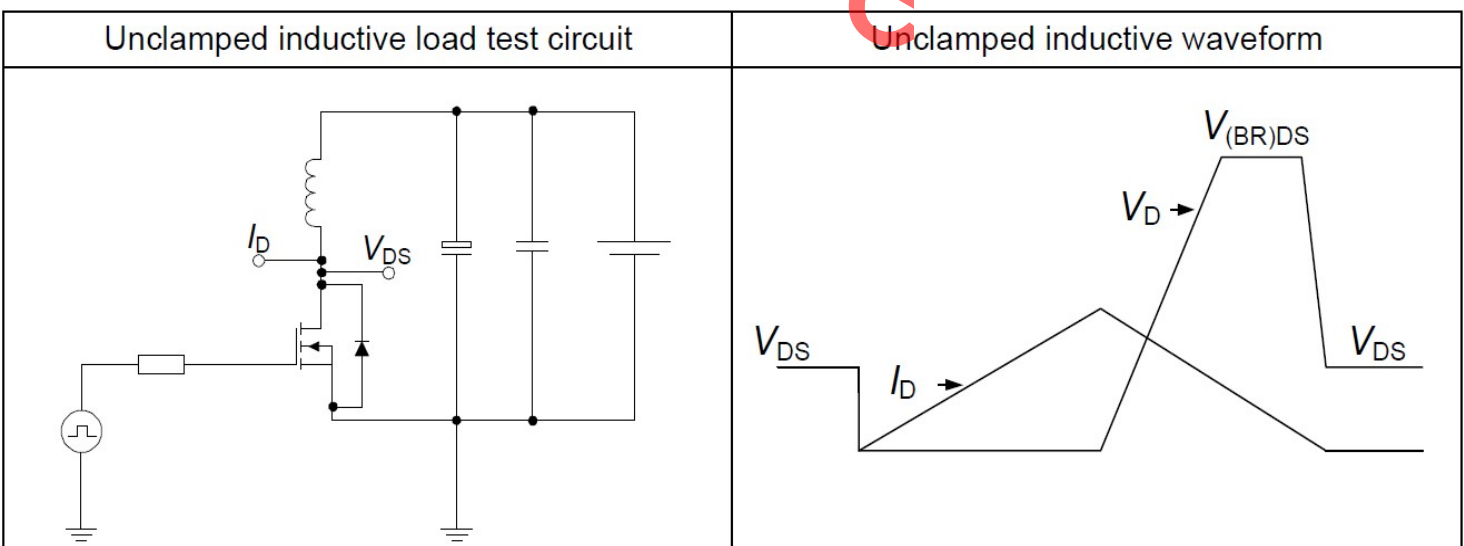
**Table 8 Diode characteristics**



**Table 9 Switching times**



**Table 10 Unclamped inductive load**



5 Package Outlines

TO-220F

单位: mm

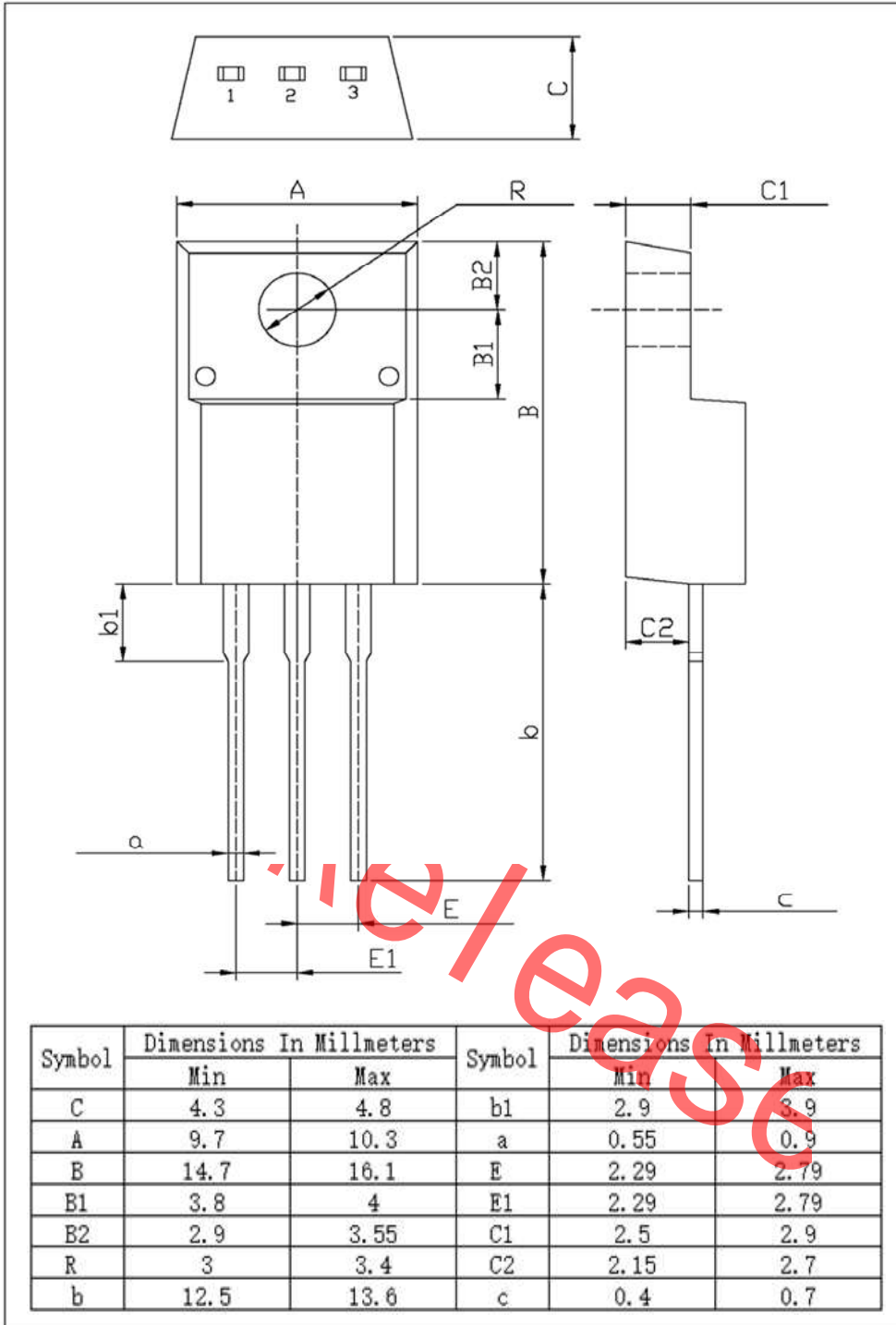
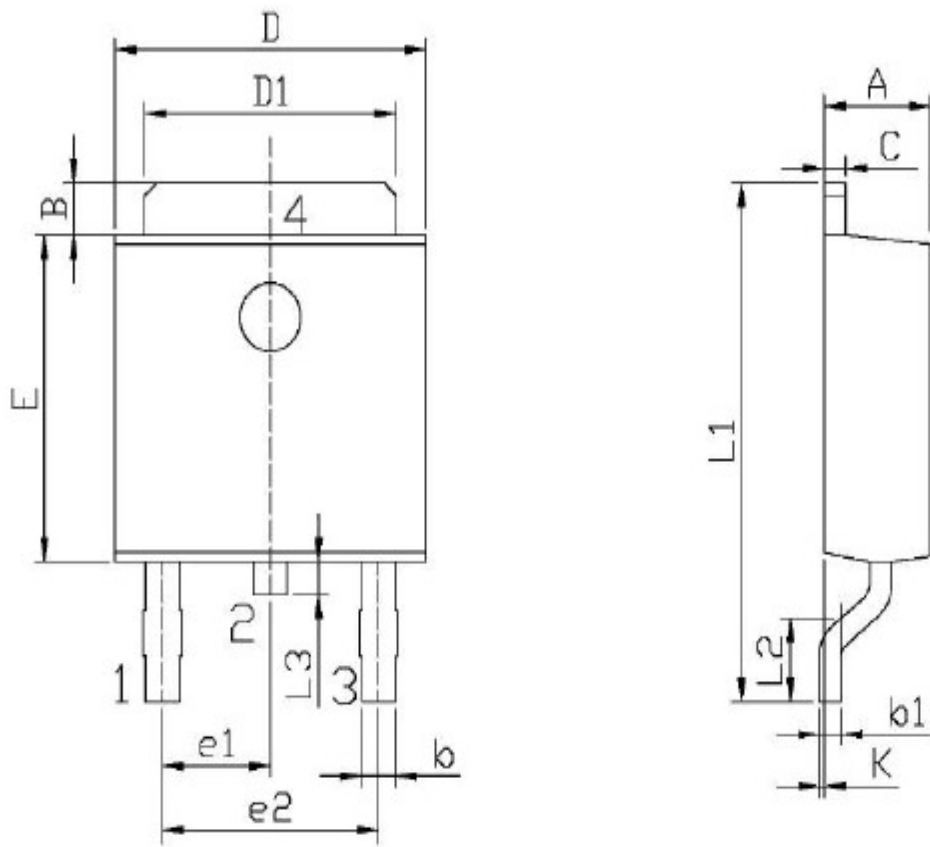


Figure1: Outline PG-TO220F

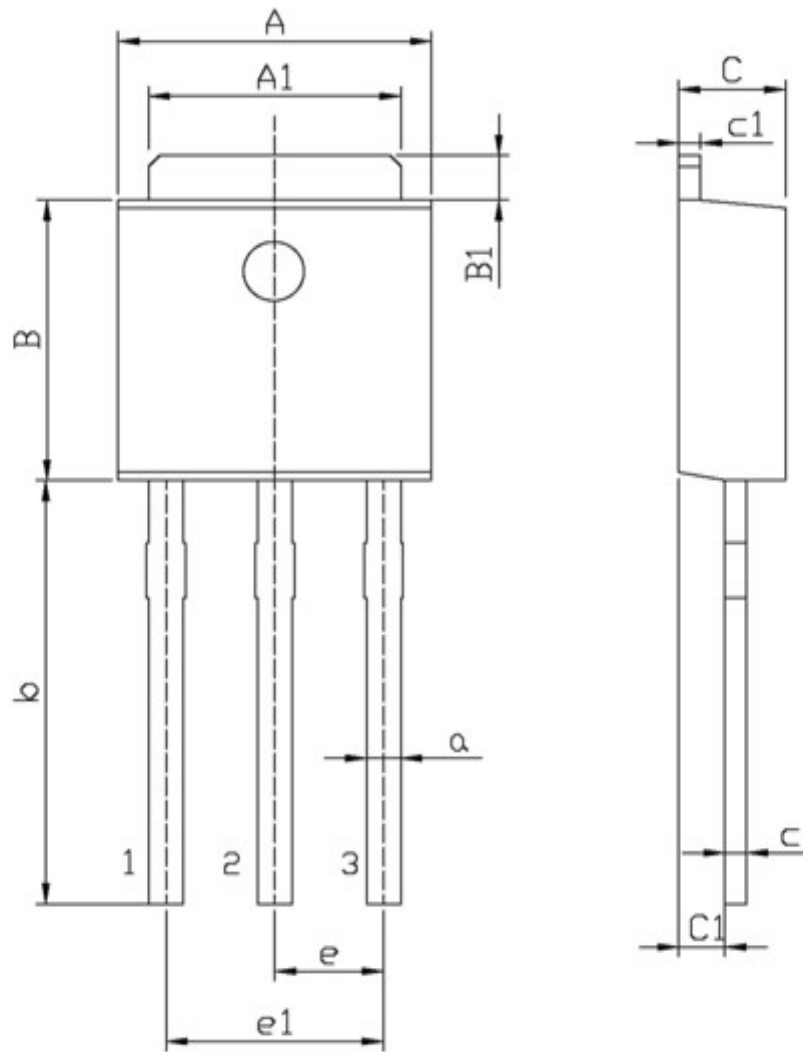


单位: mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	2.20	2.40	E	5.95	6.25
B	0.95	1.25	e1	2.24	2.34
b	0.50	0.70	e2	4.43	4.73
b1	0.45	0.55	L1	9.45	9.95
C	0.45	0.55	L2	1.25	1.75
D	6.45	6.75	L3	0.60	0.90
D1	5.10	5.50	K	0.00	0.10

Figure2: OutlinePG-T0252





单位: mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	6.45	6.75	a	0.50	0.70
A1	5.10	5.50	b	9.00	9.40
B	5.95	6.25	c	0.45	0.55
B1	0.95	1.25	c1	0.45	0.55
C	2.20	2.40	e	2.24	2.34
C1	0.95	1.15	e1	4.43	4.73

Figure3: OutlinePG-T0251

Revision History

**ASA65R850E**

Revision	Date	Subjects (major changes since last revision)
0.1	2019-04-11	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc

Pre-release

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