

## MOSFET Silicon N-Channel MOS



### 1. Applications

For Soft Switching Boost PFC switch, HB or AHB or LLC half bridge and full bridge topologies.  
Such as phase-shift-bridge(ZVS),LLC Application-Server Power, Telecom Power, EV Charging, Solar inverter.

### 2. Features

Low drain-source on-resistance:  $R_{DS(ON)} = 0.034\Omega$  (typ.)  
Easy to control Gate switching  
Enhancement mode:  $V_{th} = 3$  to  $5$  V

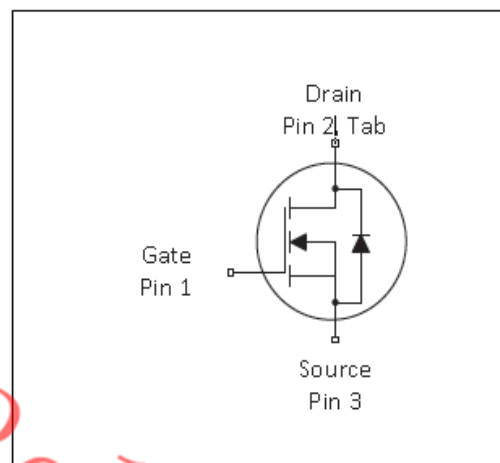
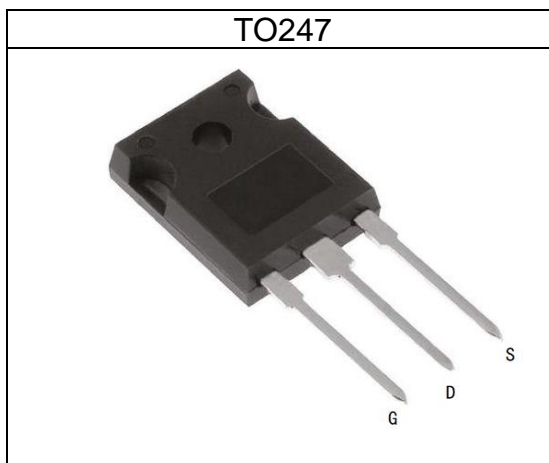


**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	38	m $\Omega$
$Q_{g,typ}$	158.2	nC
$I_{D,pulse}$	240	A
Body diode dv/dt	50	V/ns

### 3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R038EFD	TO247	ASW65R038EFD



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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$		-	80	A	$T_C=25^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	240	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	2560	mJ	$T_C=25^\circ\text{C}$ , $V_{DD}=50\text{V}$ , $L=20\text{mH}$ , $R_G=25\Omega$
Avalanche current, single pulse	$I_{AR}$	-	-	16	A	$T_C=25^\circ\text{C}$ , $V_{DD}=50\text{V}$ , $L=20\text{mH}$ , $R_G=25\Omega$
MOSFET dv/dt ruggedness	dv/dt	-	-	26	V/ns	$V_{DS}=0\dots150\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	500	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	
Soldering Temperature Distance of 1.6mm from case for 10s	$T_L$			260	$^\circ\text{C}$	
Reverse diode dv/dt <sup>3)</sup>	dv/dt		-	50	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 48\text{A}$ , $T_j=25^\circ\text{C}$ see table 8

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<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

Table 3 Thermal characteristics

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Thermal resistance, junction	- case	$R_{thJC}$	-	-	0.205	°C/W	-
Thermal resistance, junction	- ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint

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### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	3		5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	$I_{DSS}$	-	-	5	$\mu A$	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.034	0.038	$\Omega$	$V_{GS}=10V, I_D=28A, T_j=25^\circ\text{C}$
Gate resistance (Intrinsic)	$R_G$	-	1.2	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	6033	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1\text{MHz}$
Output capacitance	$C_{oss}$	-	169	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1\text{MHz}$
Reverse transfer capacitance	$C_{rss}$	-	12.1	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	-	67.6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=44.2A$ $R_G=1.8\Omega$ ; see table 9
Rise time	$t_r$	-	29.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=44.2A$ $R_G=1.8\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=44.2A$ $R_G=1.8\Omega$ ; see table 9
Fall time	$t_f$	-	325.4	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=44.2A$ $R_G=1.8\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	45	-	nC	$V_{DD}=480V, I_D=44.2A, V_{GS}=10V$
Gate to drain charge	$Q_{gd}$	-	61	-	nC	$V_{DD}=480V, I_D=44.2A, V_{GS}=10V$
Gate charge total	$Q_g$	-	158.2	-	nC	$V_{DD}=480V, I_D=44.2A, V_{GS}=10V$
Gate plateau voltage	$V_{plateau}$	-	6.14	-	V	$V_{DD}=480V, I_D=44.2A, V_{GS}=10V$

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Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.61	-	V	$V_{GS}=0V, I_F=1A, T_J=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	173.5	-	ns	$V_r=400v, I_F=44.2A, di/dt=100A/us$ see table 8
Reverse recovery charge	$Q_{rr}$	-	1.19	-	$\mu C$	$V_r=400v, I_F=44.2A, di/dt=100A/us$ see table 8
Peak reverse recovery current	$I_{rm}$	-	12.7	-	A	$V_r=400v, I_F=44.2A, di/dt=100A/us$ see table 8

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### 4 Electrical characteristics diagram

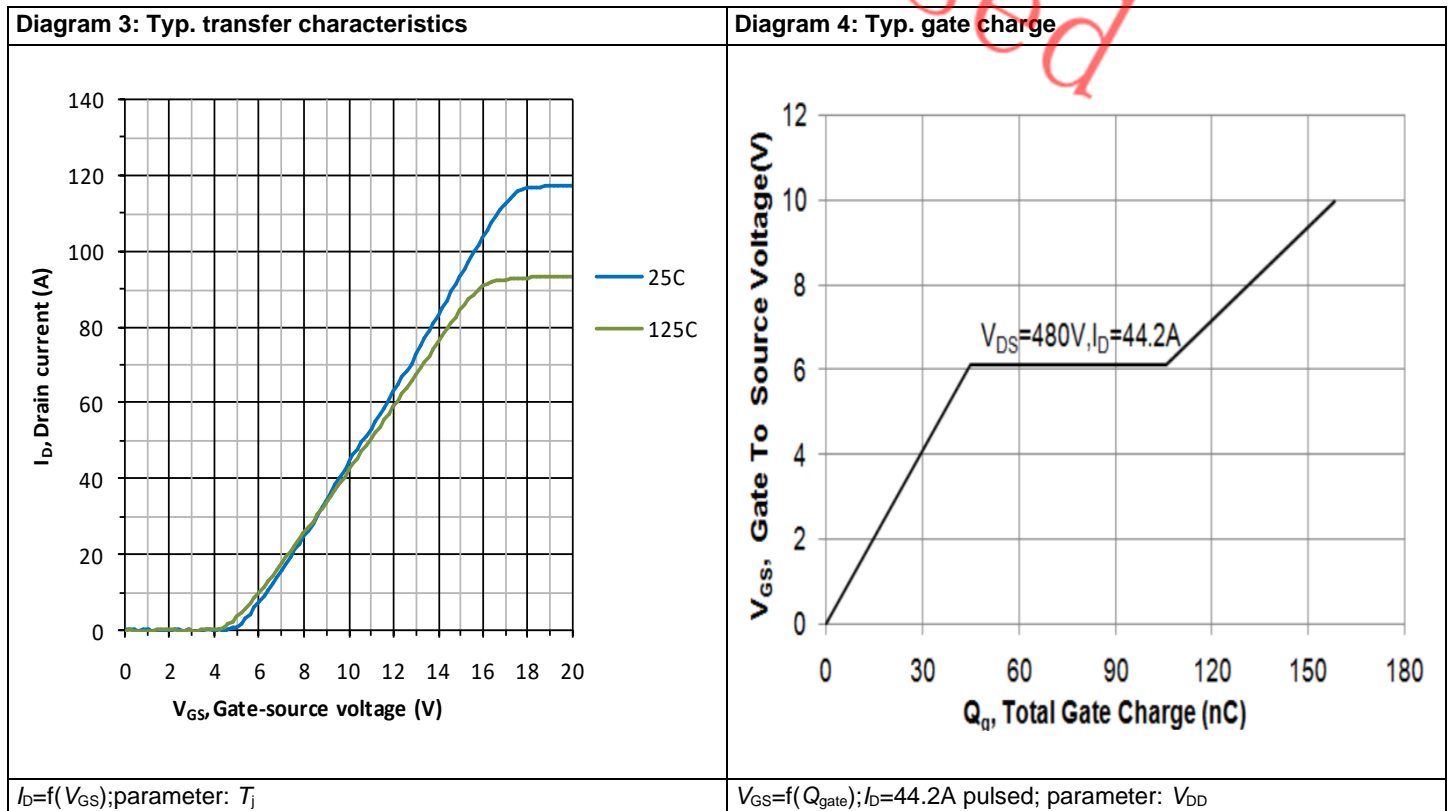
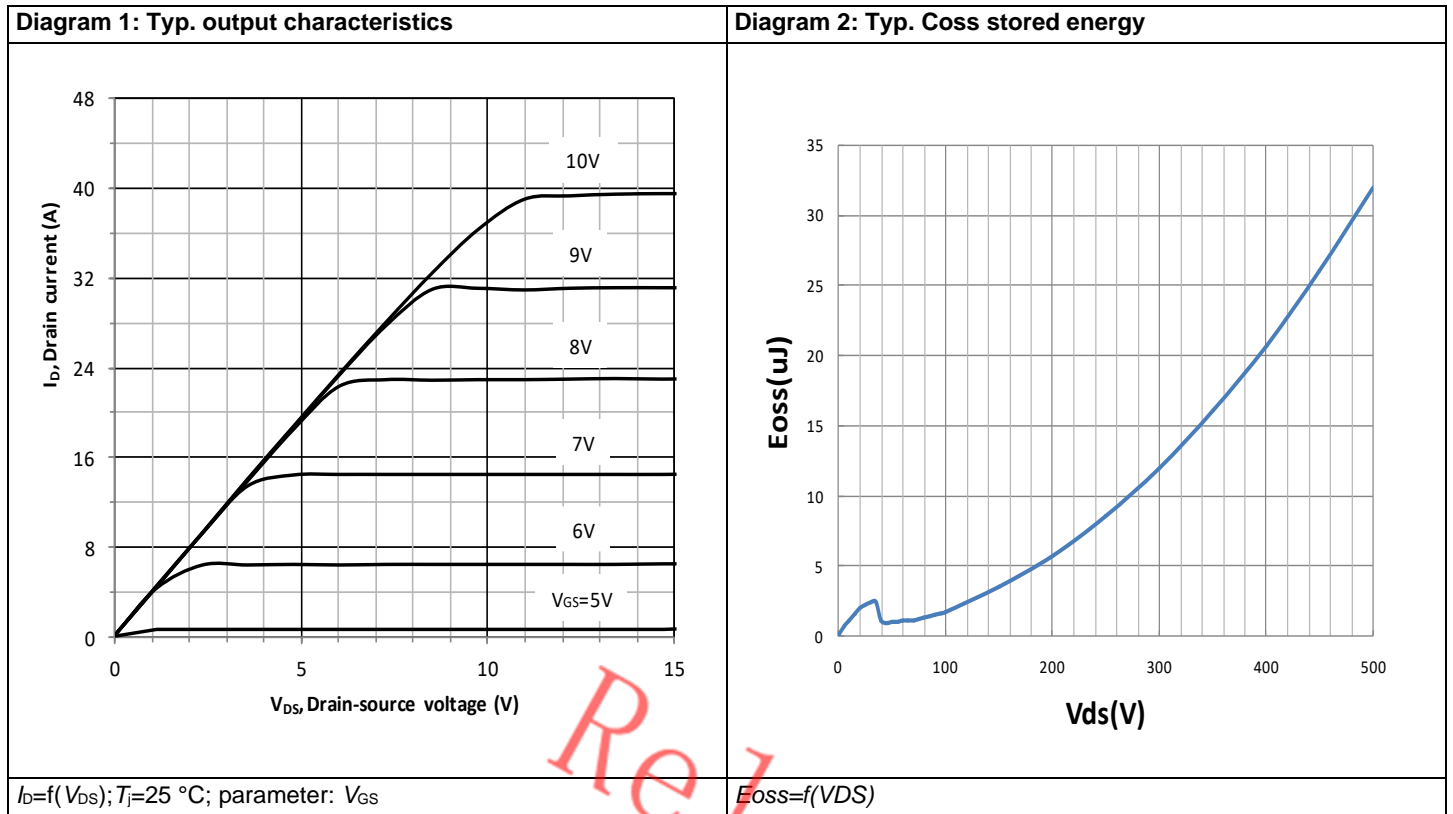
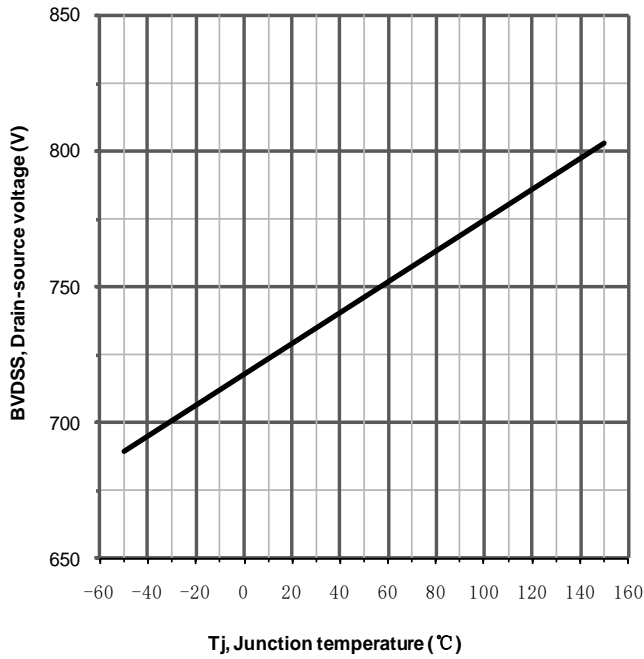
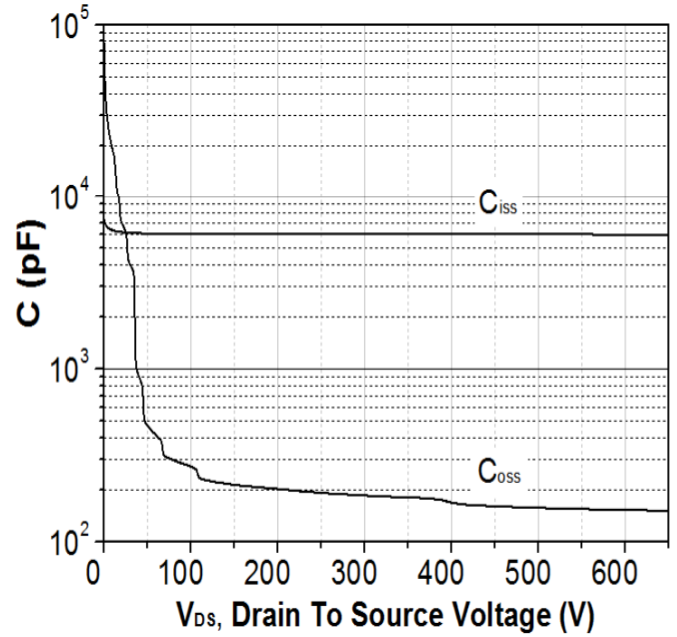


Diagram 5: Drain-source breakdown voltage



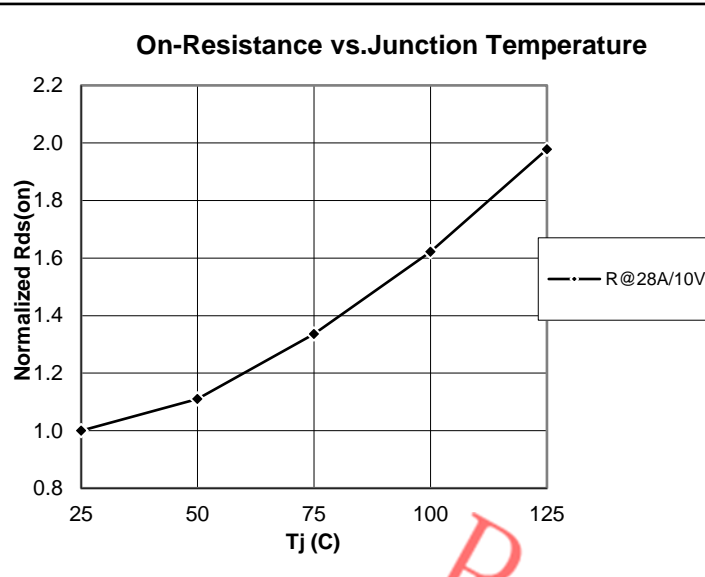
$V_{BR(DSS)}=f(T_j); I_D=10mA$

Diagram 6: Typ. capacitances



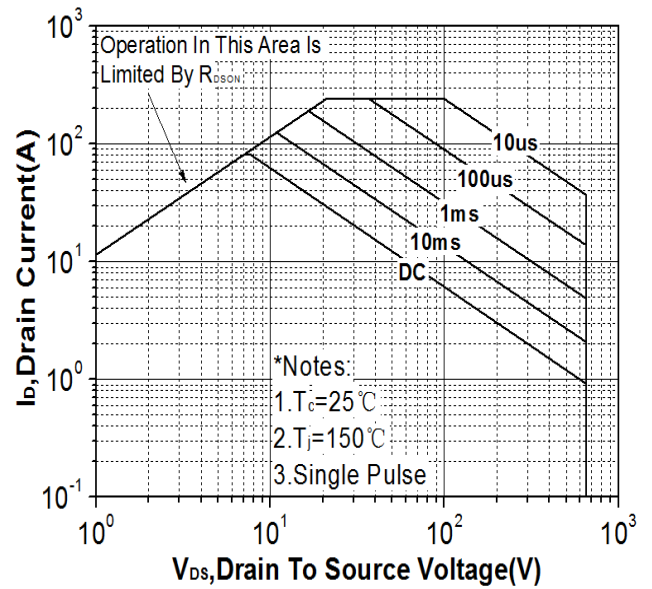
$C=f(V_{DS}); V_{GS}=0V; f=10kHz$

Diagram 7: Typ. On-Resistance vs. Junction Temperature



$R_{ds(on)}=f(T_j); V_{GS}=10V/I_D=28A$

Diagram 8: Safe operating area Tc=25 °C, TO247

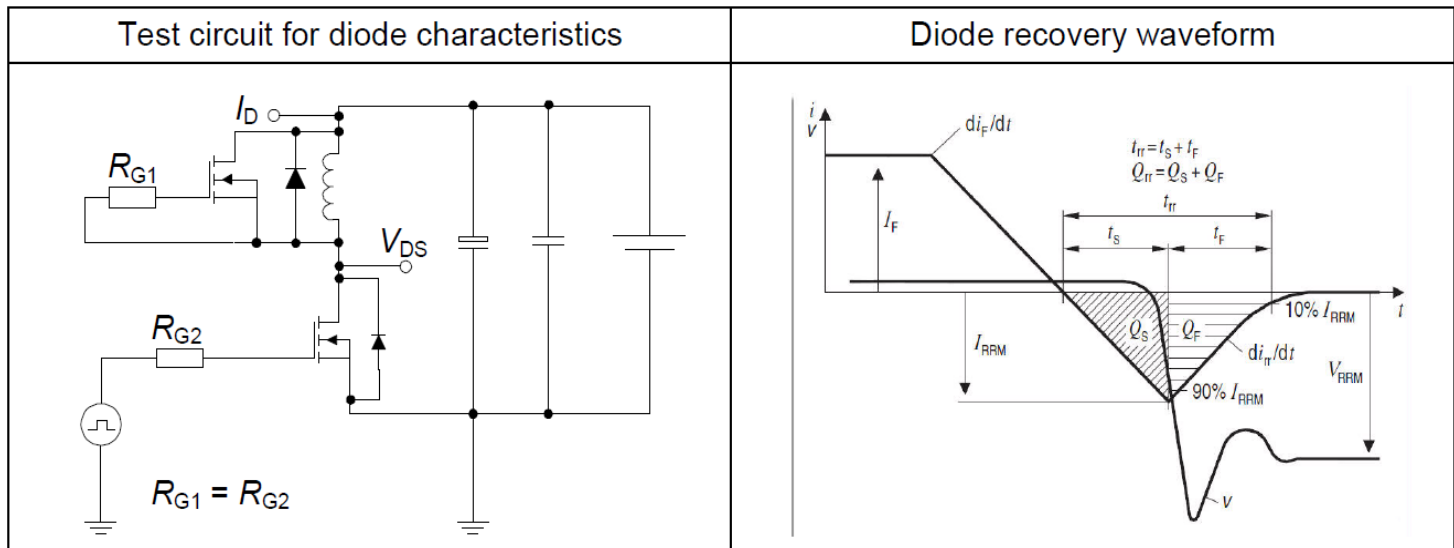


$I_D=f(V_{DS}); T_c=25^\circ C; V_{GS}>7V; D=0; \text{parameter } tp$

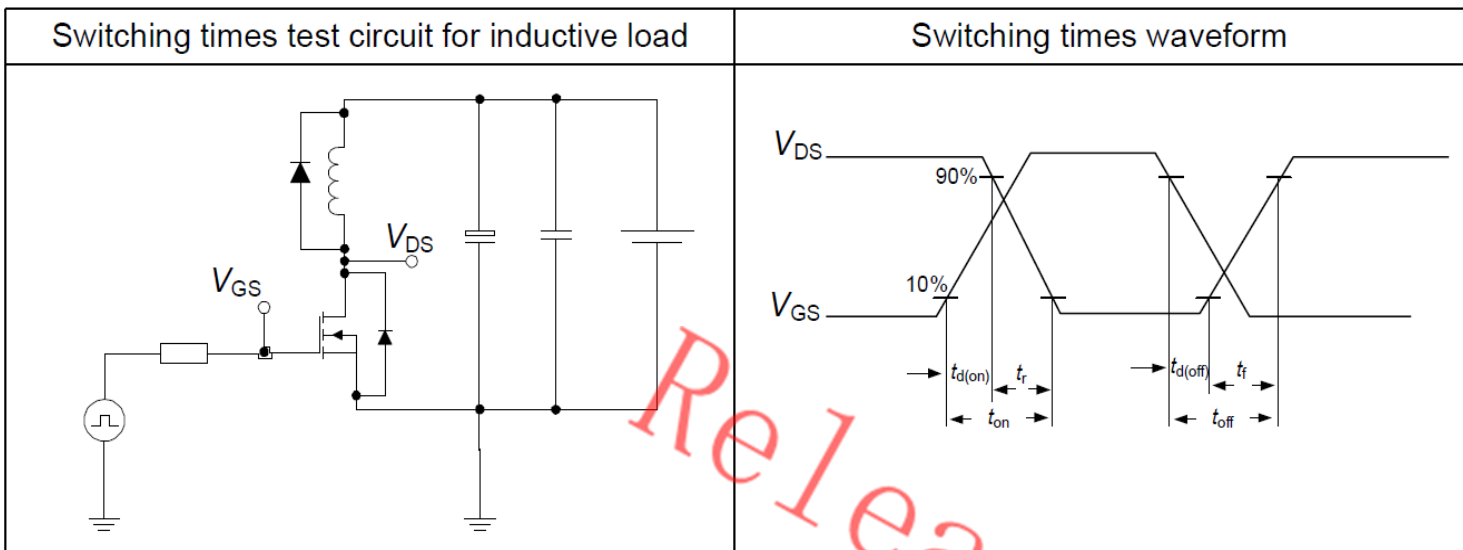
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## 5 Test Circuits

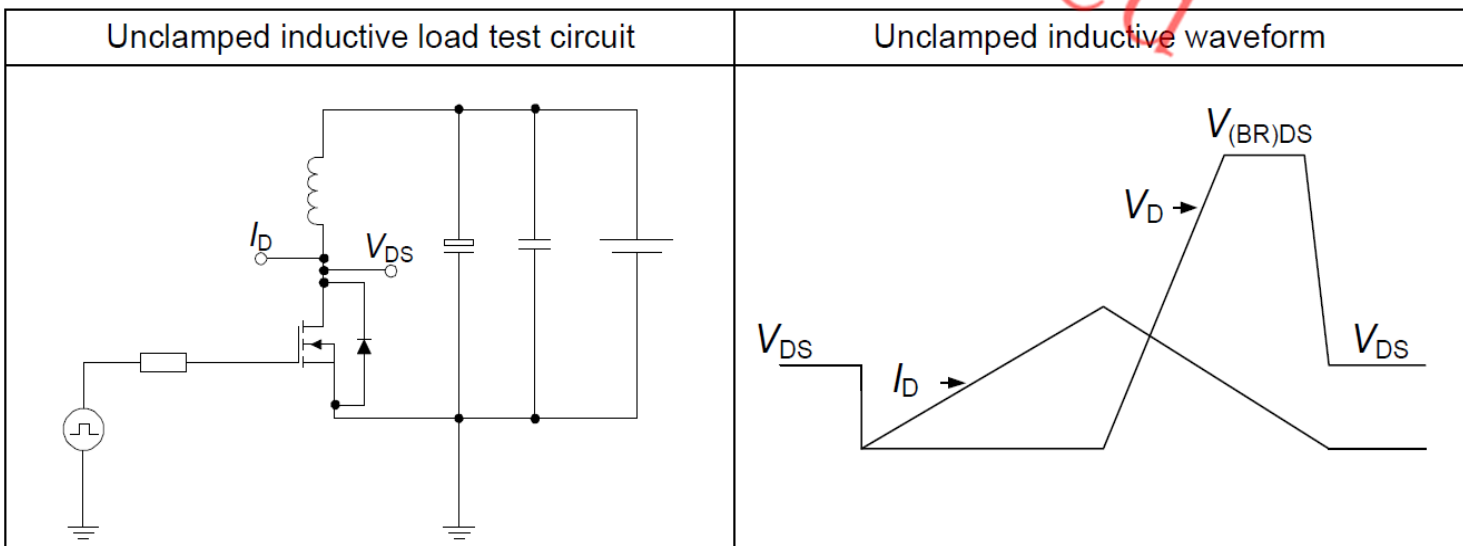
**Table 8 Diode characteristics**



**Table 9 Switching times**



**Table 10 Unclamped inductive load**





6 Package Outlines

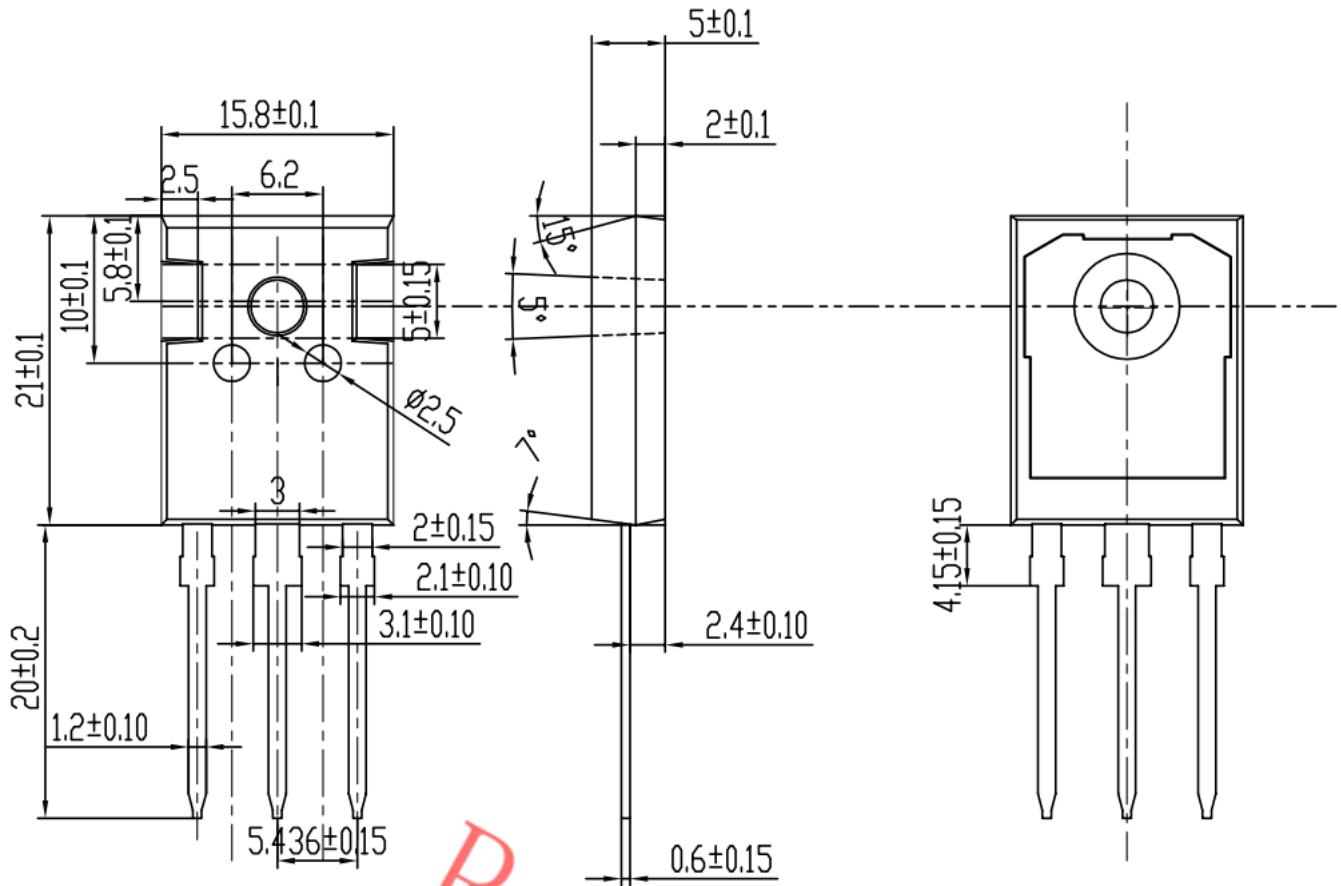


Figure: Outline PG-T0247(HT)

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## Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2022-06-27	Preliminary version

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