

MOSFET Silicon N-Channel MOS



1. Applications

Boost PFC switch, Half bridge or Asymmetric half bridge or Series resonance half bridge and full bridge topologies.
 Server power, Telecom power, EV charging, Solar inverter, UPS Application.

2. Features

Low drain-source on-resistance: $R_{DS(ON)} = 0.082\Omega$ (typ.)
 Easy to control Gate switching
 Enhancement mode: $V_{th} = 3$ to 5 V

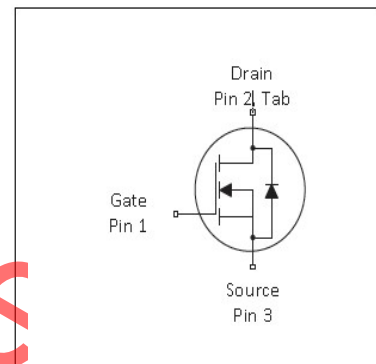
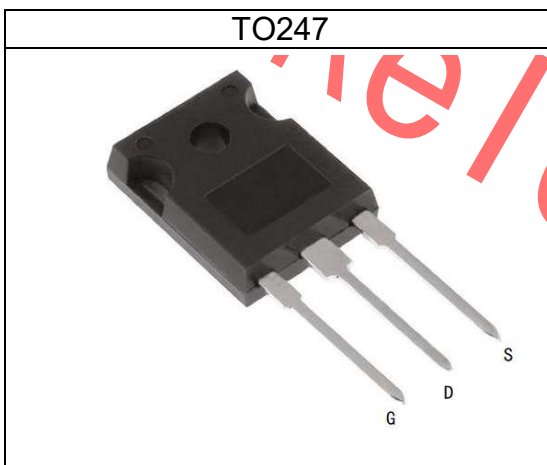


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	95	m Ω
$Q_{g,typ}$	85	nC
$I_{D,pulse}$	141	A
Body diode dv/dt	50	V/ns

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R095EFD	TO247	ASW65R095EFD



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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	47	A	$T_C = 25^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	141	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	4623	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	57	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	391	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	
Reverse diode dv/dt ³⁾	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq 48\text{A}$, $T_j = 25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

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2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.32	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

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3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	$V_{GS}=0V, I_D=10mA$
Gate threshold voltage	$V_{(GS)th}$	3		5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	5	μA	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.082	0.095	Ω	$V_{GS}=10V, I_D=14A, T_j=25^\circ\text{C}$
Gate resistance	R_G	-	13	-	Ω	$f=1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4799	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Output capacitance	C_{oss}	-	482	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Reverse transfer capacitance	C_{rss}	-	4.6	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Turn-on delay time	$t_{d(on)}$	-	38.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7\Omega$; see table 9
Rise time	t_r	-	26.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	134.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7\Omega$; see table 9
Fall time	t_f	-	20	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	$V_{DD}=400V, I_D=25.8A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	30	-	nC	$V_{DD}=400V, I_D=25.8A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	85	-	nC	$V_{DD}=400V, I_D=25.8A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	7.4	-	V	$V_{DD}=400V, I_D=25.8A, V_{GS}=0 \text{ to } 10V$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.66	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	124.8	-	ns	$V_r=400v, I_F=9.6A, di/dt=100A/us$
Reverse recovery charge	Q_{rr}	-	0.754	-	uC	$V_r=400v, I_F=9.6A, di/dt=100A/us$
Peak reverse recovery current	I_{rrm}	-	11.5	-	A	$V_r=400v, I_F=9.6A, di/dt=100A/us$

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4 Test Circuits

Table 8 Diode characteristics

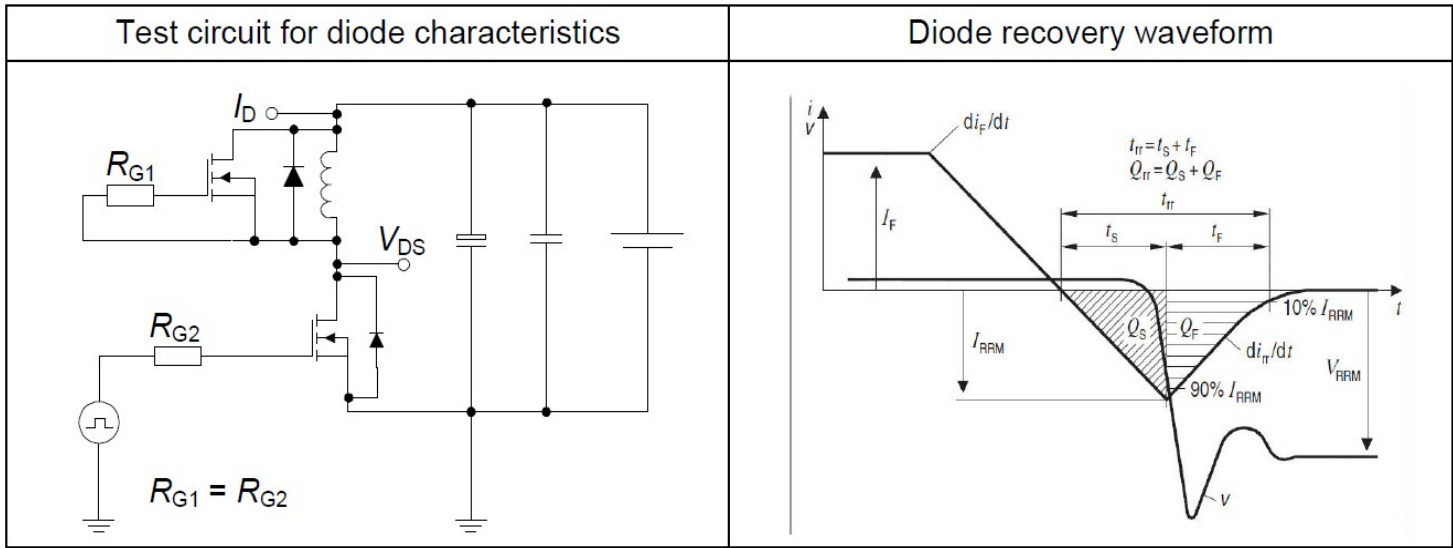


Table 9 Switching times

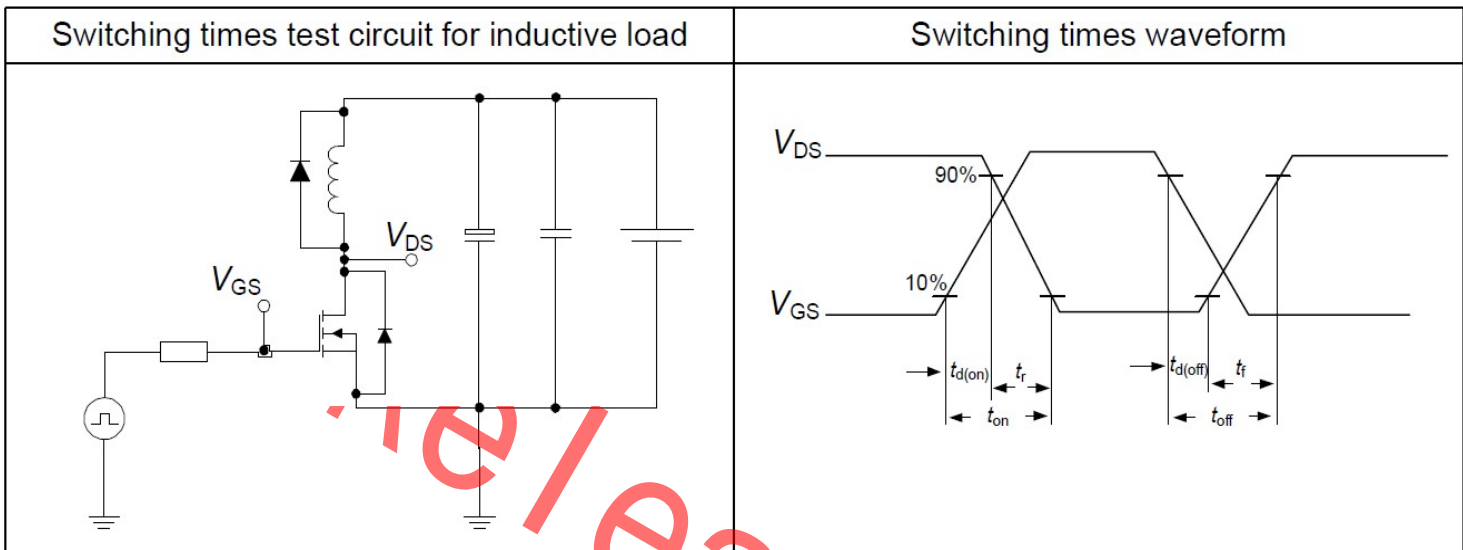
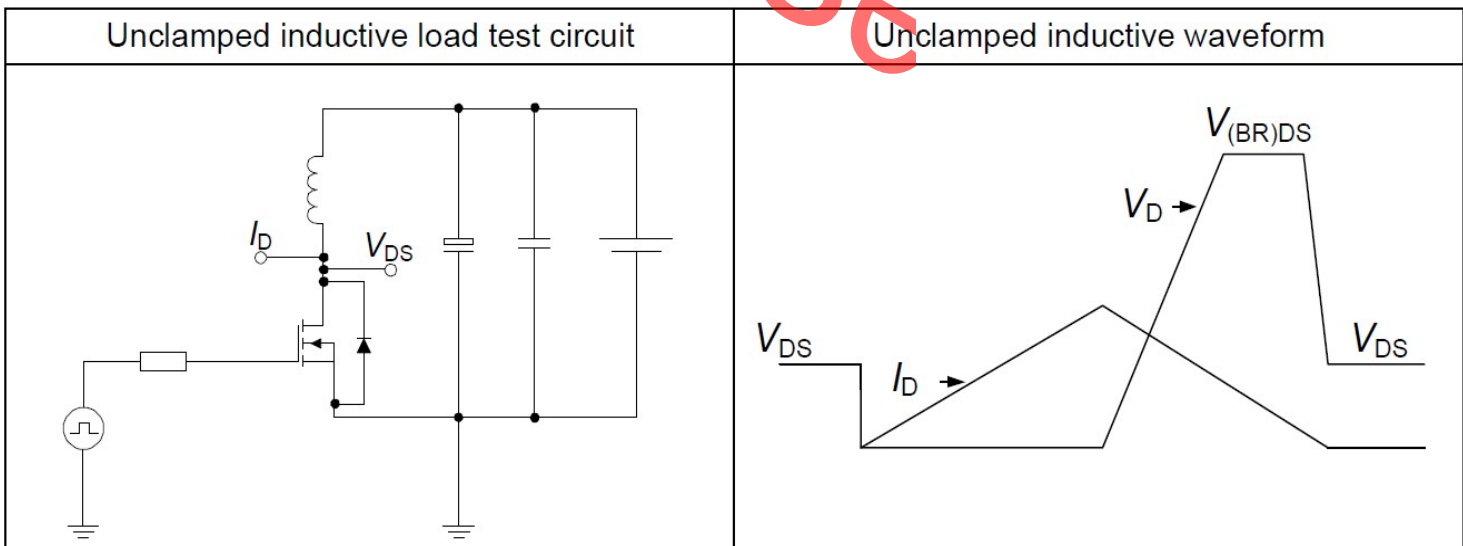


Table10 Unclamped inductive load



5 Package Outlines

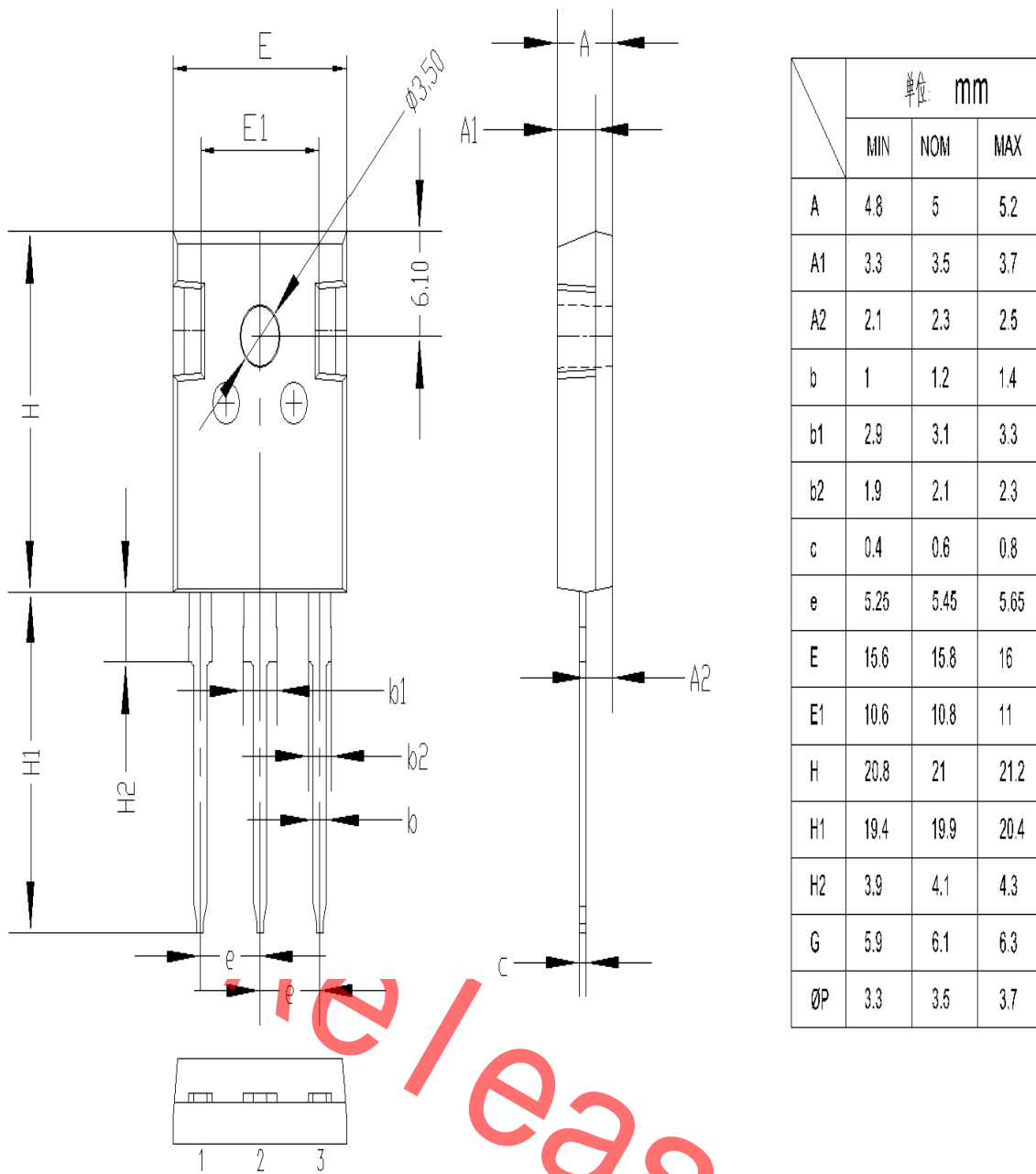


Figure1: Outline PG-T0247

Revision History

ASW65R095EFD

Revision	Date	Subjects (major changes since last revision)
0.1	2019-05-21	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc
1.1	2020-03-13	Change Marking

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