

MOSFET Silicon N-Channel MOS

1. Applications

Single-ended flyback or two-transistor forward topologies.
PC power, PD Adaptor, LCD & PDP TV and LED lighting.



2. Features

Low drain-source on-resistance: $R_{DS(ON)} = 4.2\text{m}\Omega$ (typ.)
Easy to control Gate switching
Enhancement mode: $V_{th} = 2.5$ to 3.5 V

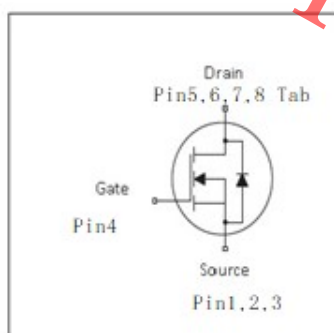
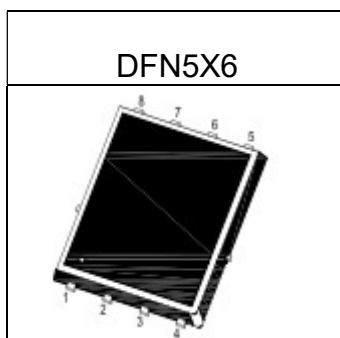
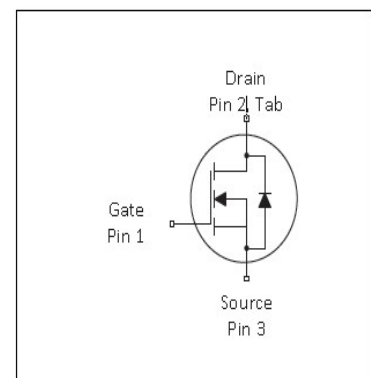
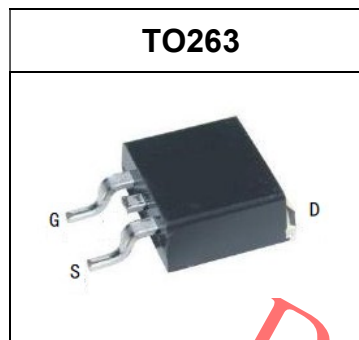


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	85	V
$R_{DS(on),max}$	5.2	$\text{m}\Omega$
$Q_{g,typ}$	68.4	nC
$I_{D,pulse}$	480	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
AUP052N085	TO220	AUP052N085
AUB050N085	TO263	AUB050N085
AUN045N085	DFN5X6	AUN045N085



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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	119	A	$T_C = 25^\circ\text{C}$
Continuous drain current	I_D		-	89	A	$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	480	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	420	mJ	$T_C = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $I = 41\text{A}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$
Avalanche current, single pulse	I_{AR}	-	-	41	A	$T_C = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Power dissipation	P_{tot}	-	-	183	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	
Transconductance	GFS	-	76	-	S	$V_{DS} = 5\text{V}$ $I_{DS} = 50\text{A}$

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

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2 Thermal characteristics

Thermal characteristics (TO220)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.9	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Thermal characteristics (TO263)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.0	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	60	°C/W	device on PCB, minimal footprint

Thermal characteristics (DFN5X6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.3	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	50	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	85	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	2.5		3.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=85V, V_{GS}=0V, T_j=25^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.2	5.2	m Ω	$V_{GS}=10V, I_D=20A, T_j=25^{\circ}\text{C}(\text{TO220})$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.9	5.0	m Ω	$V_{GS}=10V, I_D=20A, T_j=25^{\circ}\text{C}(\text{TO263})$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.7	4.5	m Ω	$V_{GS}=10V, I_D=20A, T_j=25^{\circ}\text{C}(\text{DFN5X6})$
Gate resistance (Intrinsic)	R_G	-	1.8	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4587	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$
Output capacitance	C_{oss}	-	824	-	pF	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$
Reverse transfer capacitance	C_{rss}	-	5.5	-	pF	$V_{GS}=0V, V_{DS}=40V, f=0.7\text{MHz}$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=56A, R_G=1.6\Omega$
Rise time	t_r	-	33.6	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=56A, R_G=1.6\Omega$
Turn-off delay time	$t_{d(off)}$	-	34.6	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=56A, R_G=1.6\Omega$
Fall time	t_f	-	17.4	-	ns	$V_{DD}=40V, V_{GS}=10V, I_D=56A, R_G=1.6\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24.6	-	nC	$V_{DD}=40V, I_D=56A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	15.5	-	nC	$V_{DD}=40V, I_D=56A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	68.4	-	nC	$V_{DD}=40V, I_D=56A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	$V_{DD}=40V, I_D=56A, V_{GS}=0 \text{ to } 10V$

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Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.7	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	44	-	ns	$V_R=40V, I_F=56A, di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	42	-	nC	$V_R=40V, I_F=56A, di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	1.9	-	A	$V_R=40V, I_F=56A, di_F/dt=100A/\mu s$

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4. Electrical characteristics diagram

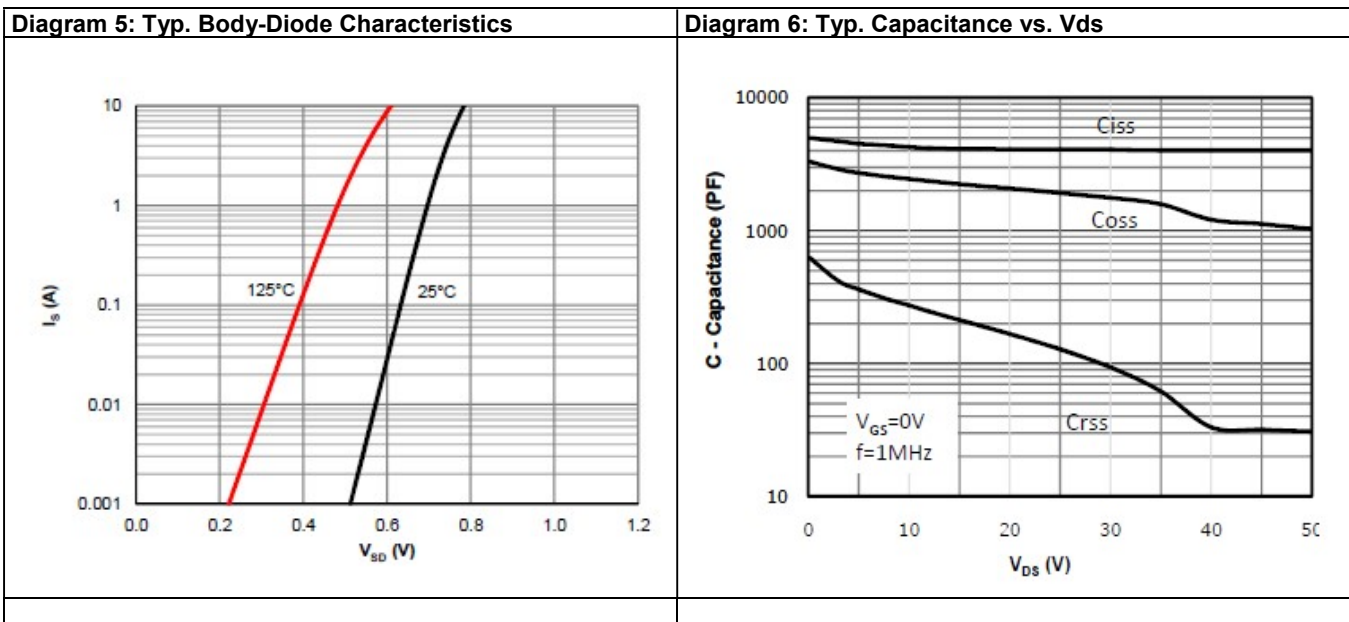
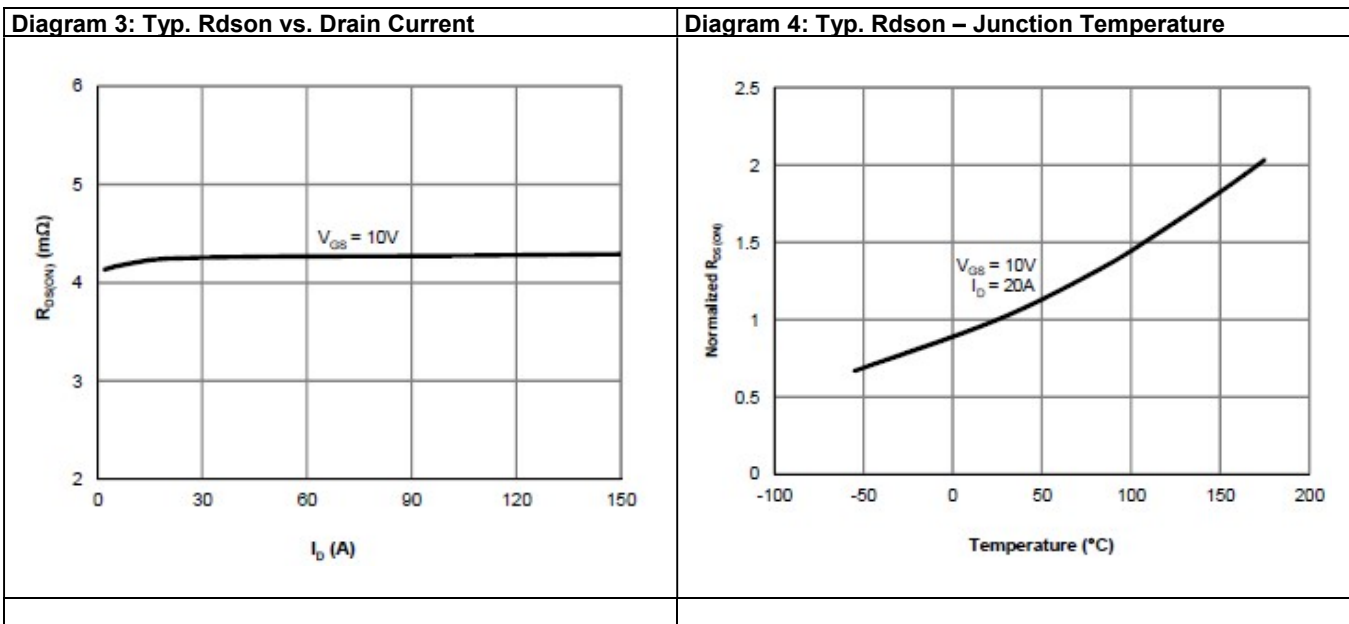
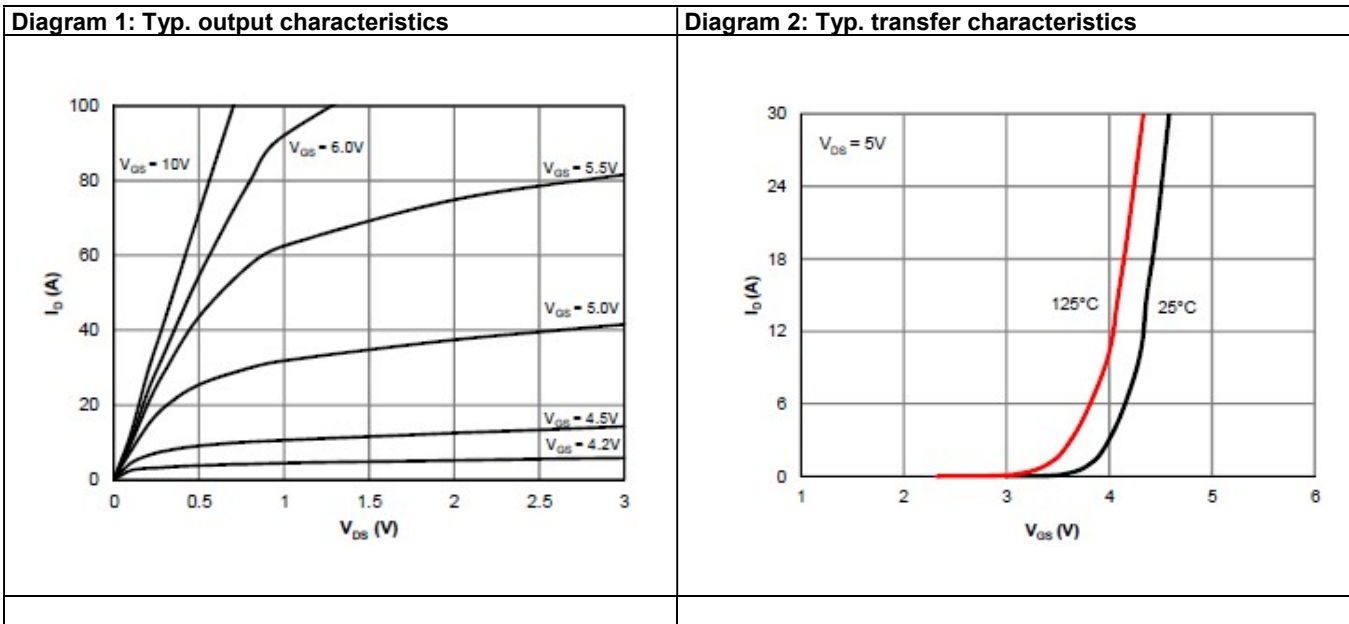


Diagram 7: Typ. Power Dissipation

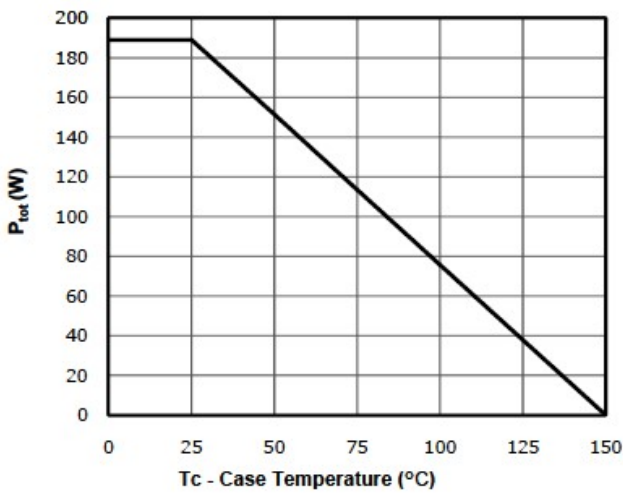


Diagram 8: Typ. Drain Current De-rating

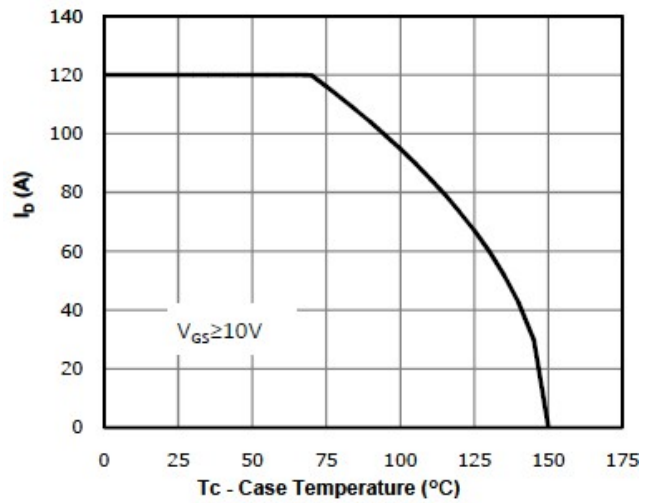


Diagram 9: Typ. Gate charge

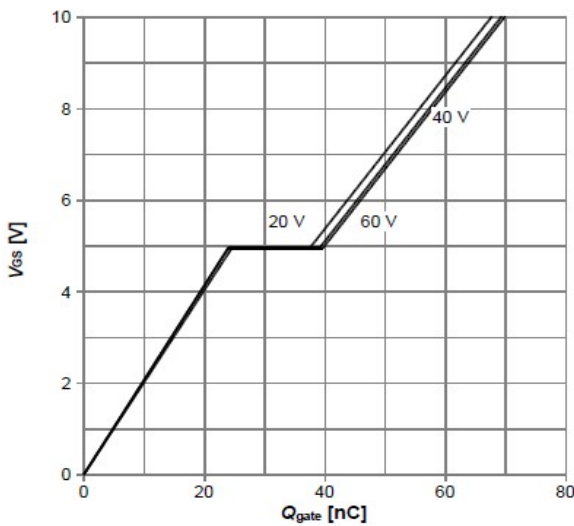


Diagram 10: Typ. Rds(on) vs Gate Voltage

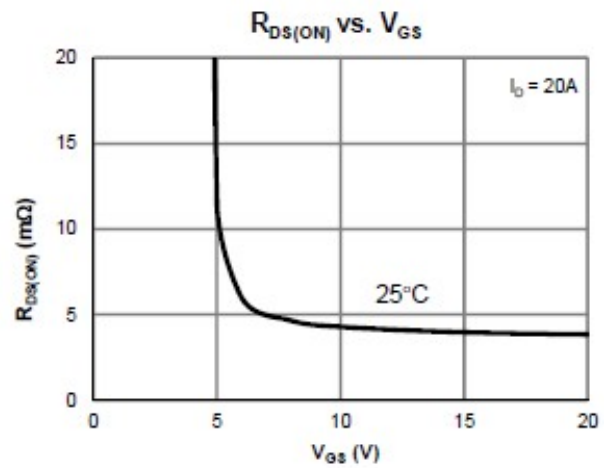


Diagram 11: Typ. Maximum Safe Operating Area

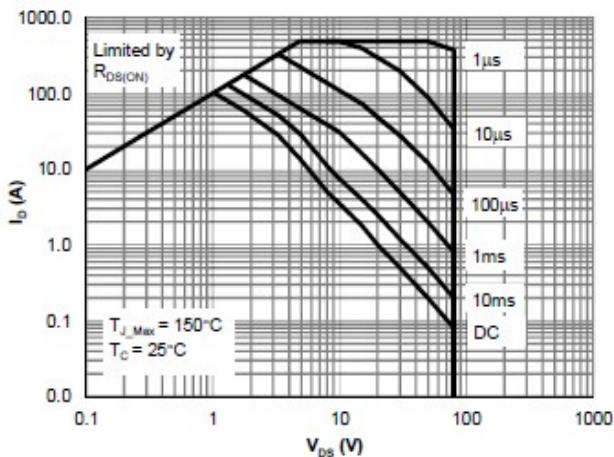


Diagram 12: Single Pulse Power Rating, Junction-to-Case

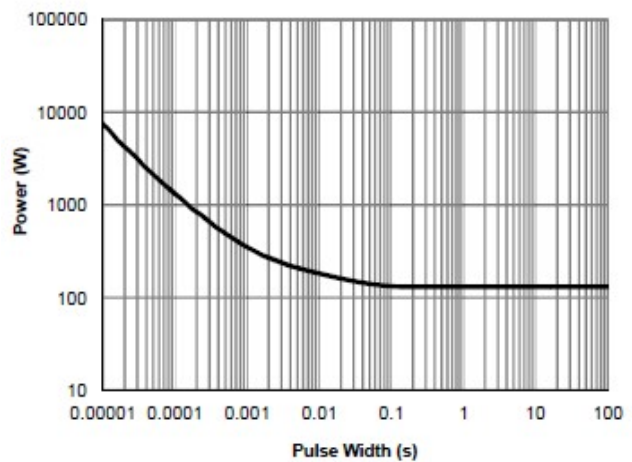
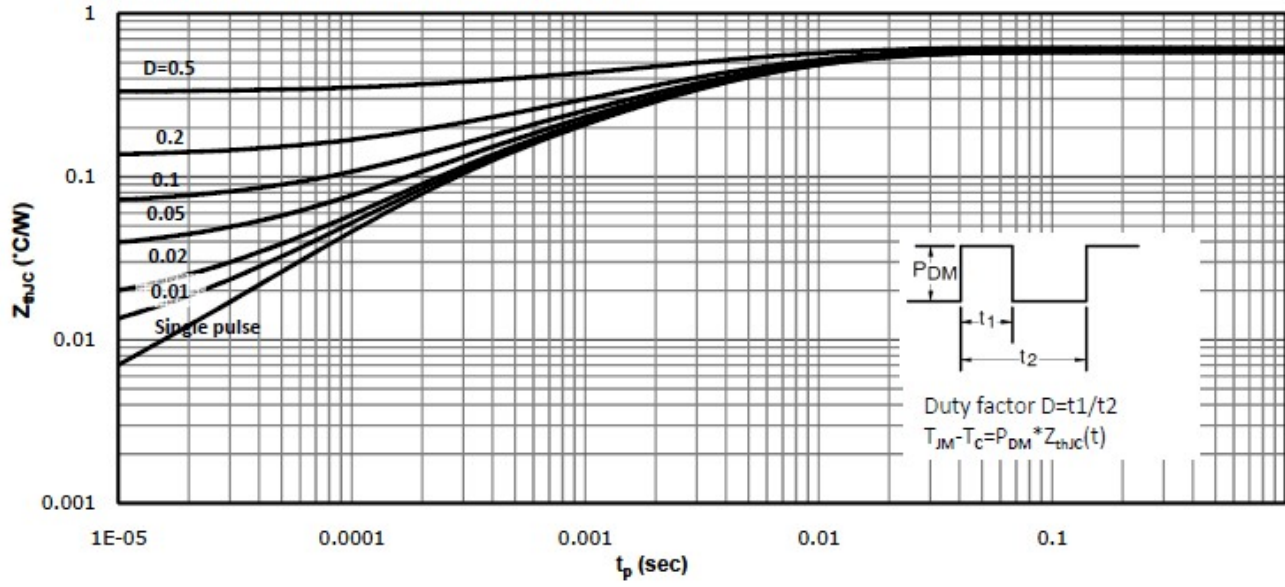


Fig 13 : Max. Transient Thermal Impedance



5. Test Circuits

Table 8 Diode characteristics

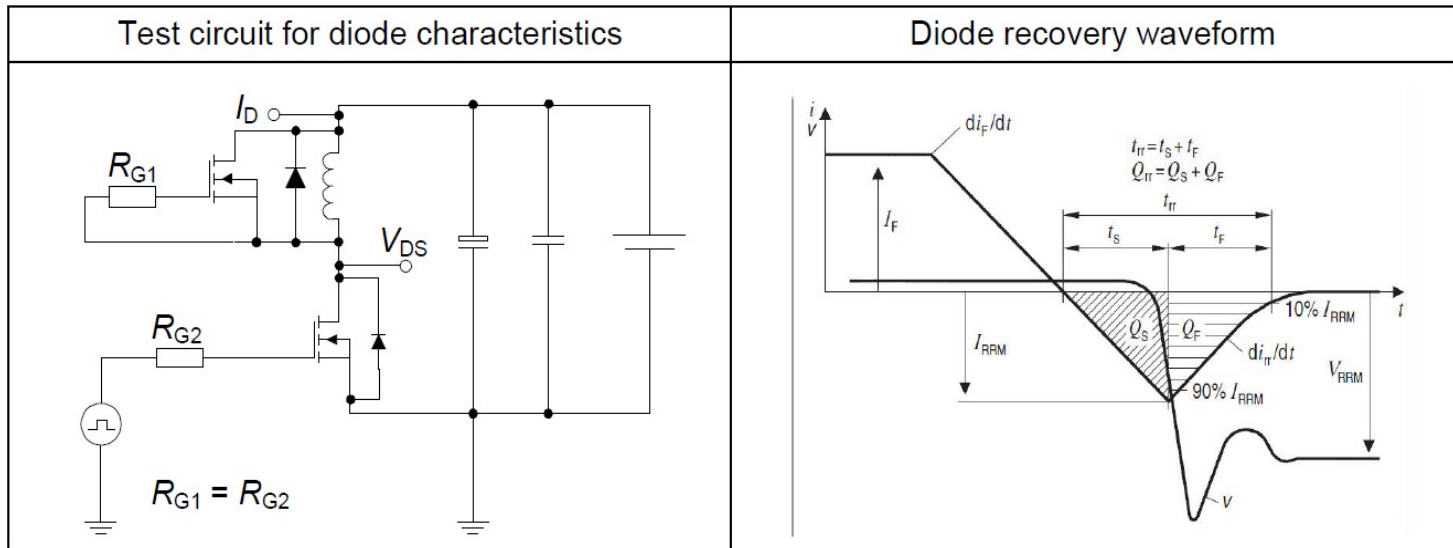


Table 9 Switching times

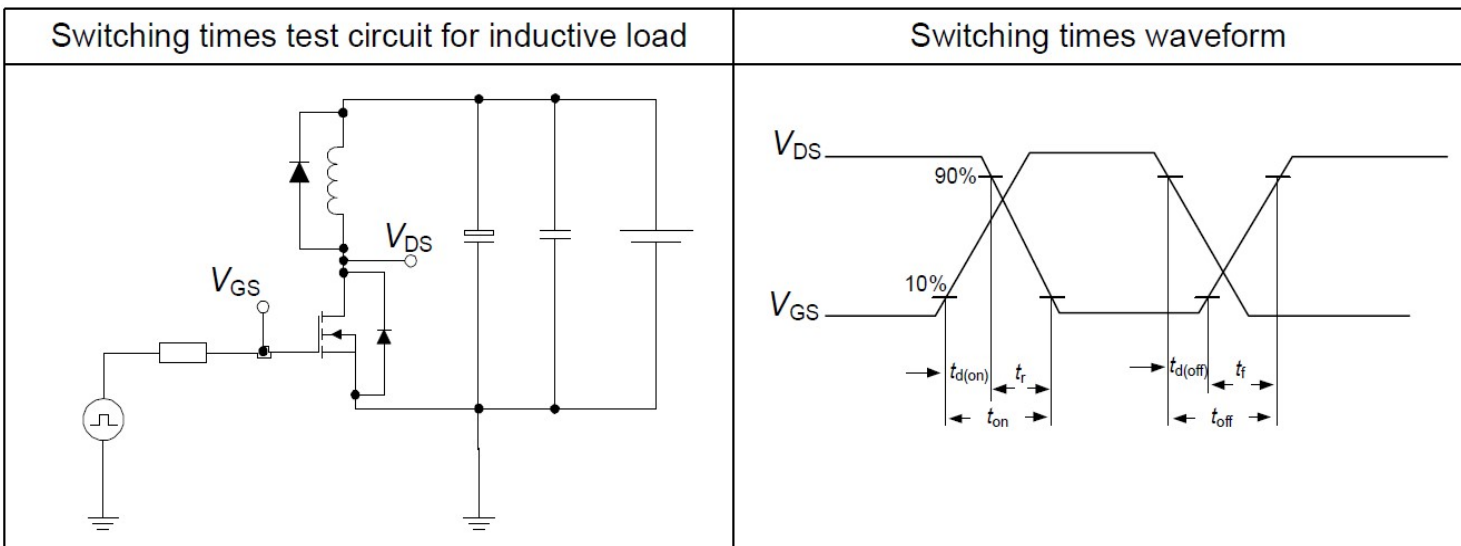
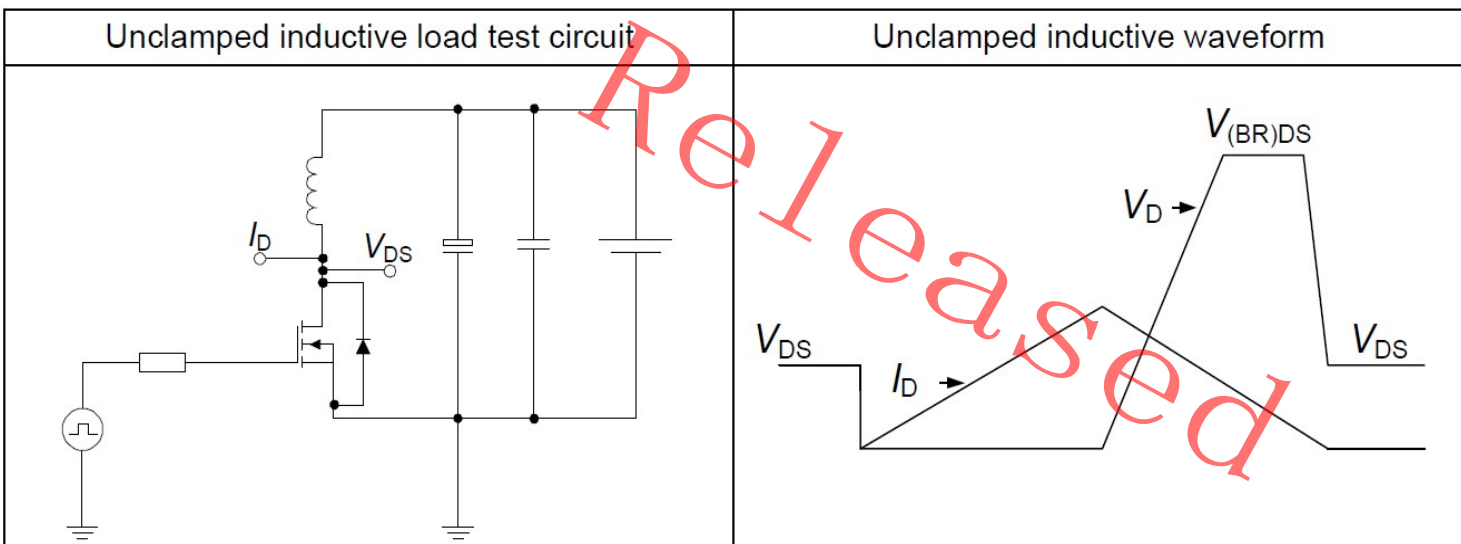
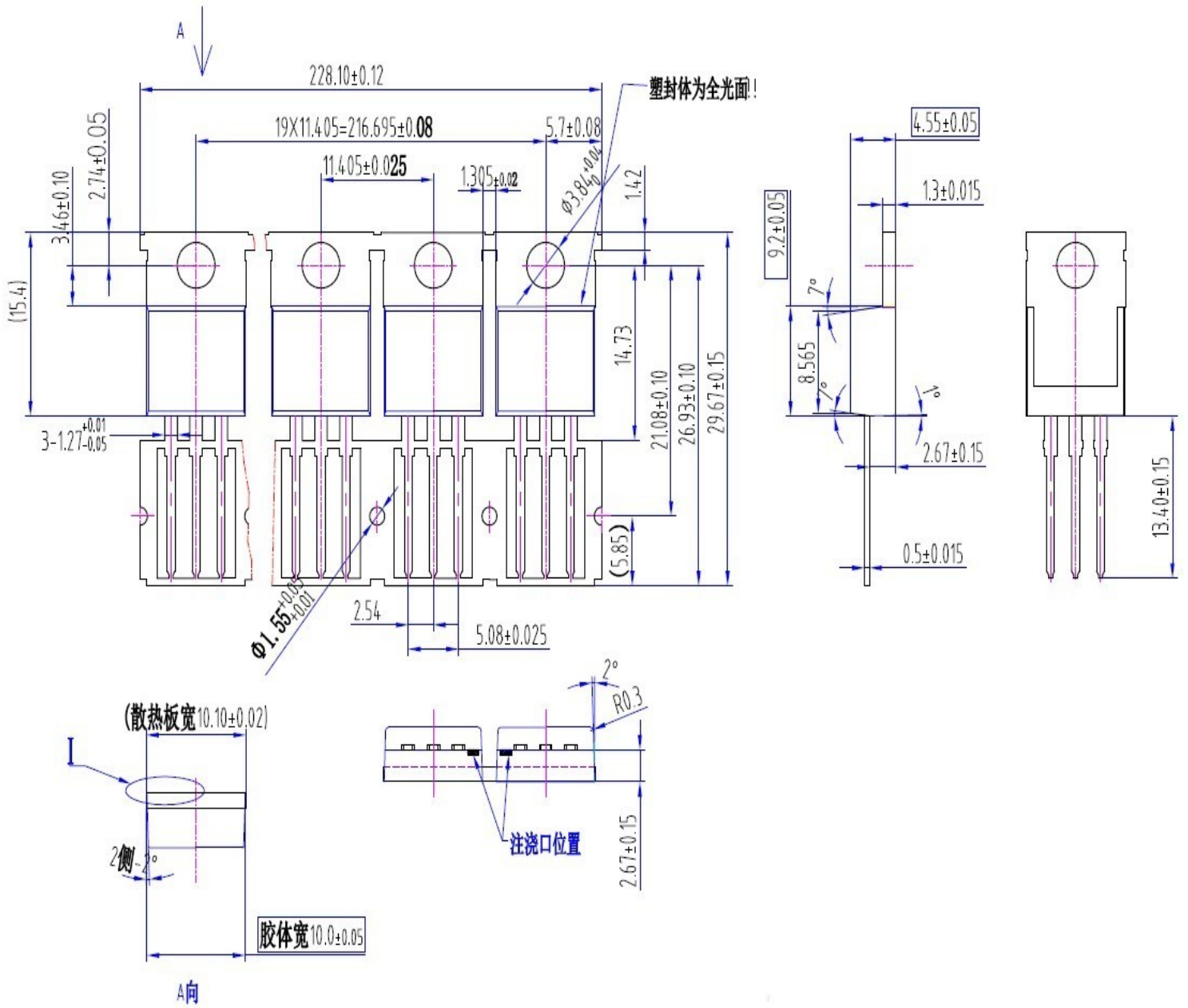


Table 10 Unclamped inductive load

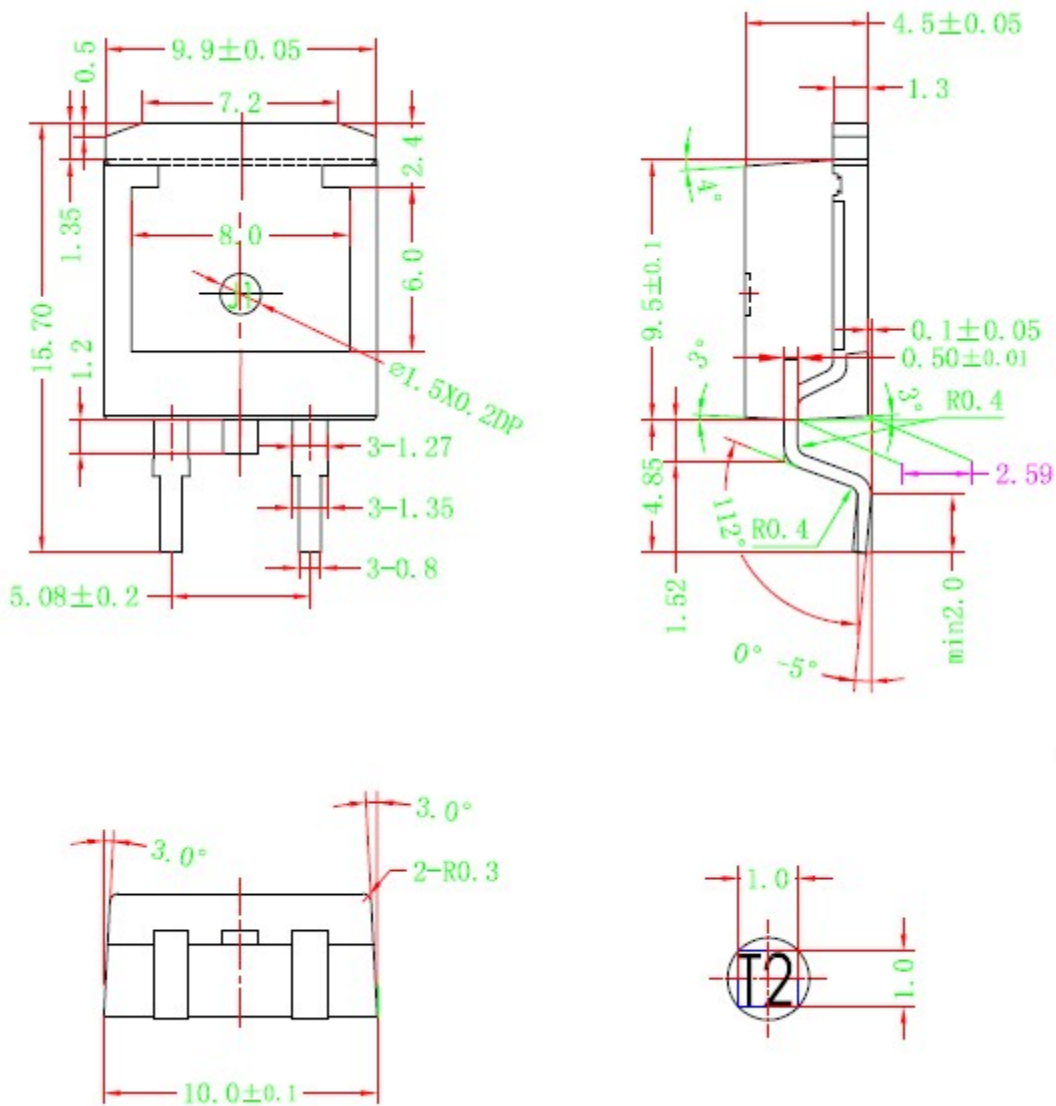


6 Package Outlines

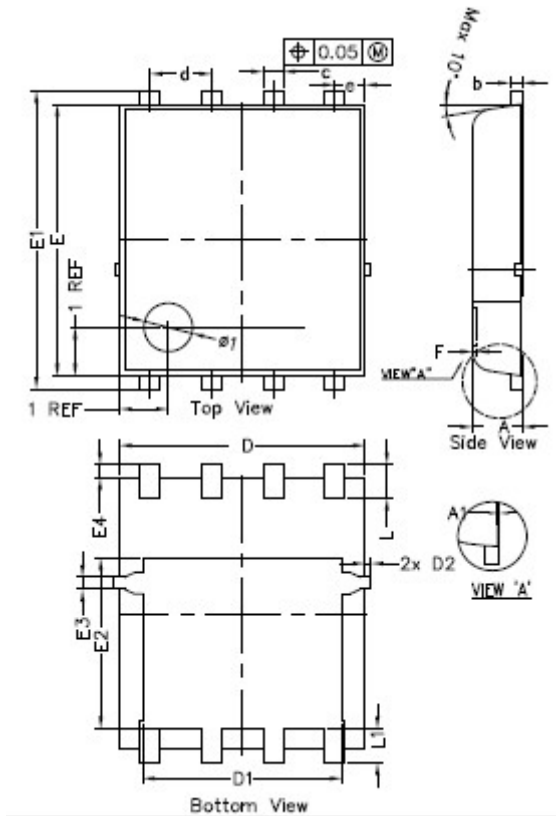


Outline PG-T0220

Outline PG-T0263 (JJW)



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SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	---	0.050	0.000	---	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d	1.27 BSC			0.050 BSC		
* D	4.950	5.050	5.150	0.195	0.199	0.203
D1	4.000	4.100	4.200	0.157	0.161	0.165
* D2	---	---	0.125	---	---	0.005
e	0.62 BSC			0.024 BSC		
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.425	3.525	3.625	0.135	0.139	0.143
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
* L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

NOTE:
 1. PACKAGE BODY SIZE EXCLUDE MOLD FLASH AND GATE BURR.
 MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MIL EACH SIDE.
 2. CONTROLLING DIMENSION IS MILLIMETER, INCH FOR REFERENCE ONLY.

Outline PG-DFN5X6 (JJW)

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Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2021-11-10	Preliminary version
1.1	2021-11-16	Updated Qrr
1.2	2021-11-17	Add gfs data
1.3	2021-12-28	Added Electrical characteristics diagram
1.4	2022-1-10	Added DFN5X6 package

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