

MOSFET Silicon N-Channel MOS



1. Applications

Synchronous rectification in SMPS,
Hard switching and High speed circuit
DC/DC in telecoms and industrial

2. Features

Low drain-source on-resistance:
TO220&TO263 $R_{DS(on)}$ = 2.1m Ω (typ.)
TOLL-8L $R_{DS(on)}$ = 1.8 m Ω (typ.)
High speed power switching
Enhanced body diode dv/dt capability
Enhanced avalanche ruggedness

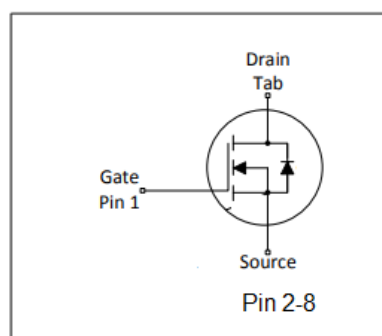
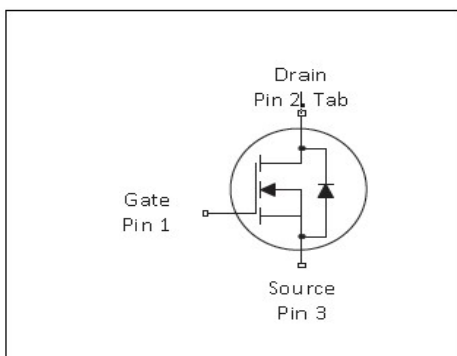
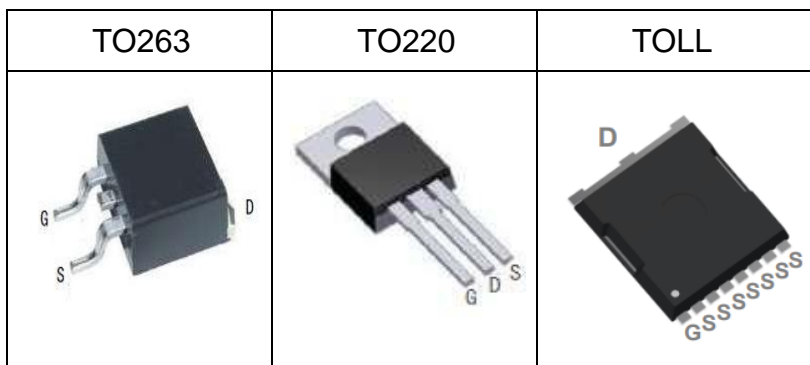


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	85	V
TO220&263 $R_{DS(on),max}$	2.6	m Ω
TOLL 8L $R_{DS(on),max}$	2.0	m Ω
$Q_{g,typ}$	152	nC
$I_{D,pulse}$	998	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
AUP026N085	TO220	AUP026N085
AUB026N085	TO263	AUB026N085
AUR020N085	TOLL	AUR020N085



1 Maximum ratings

At $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current at silicon ¹⁾	I_D		-	247	A	$T_C = 25^\circ\text{C}$
Continuous drain current at package ¹⁾	I_D		-	195	A	$T_C = 25^\circ\text{C}$
Continuous drain current at silicon ¹⁾	I_D			156	A	$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-		998	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	970	mJ	$T_C = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $V_{gs} = 10\text{V}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$
Avalanche current, single pulse	I_{AR}	-	-	62	A	$T_C = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Power dissipation	P_{tot}	-	-	275	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			300	$^\circ\text{C}$	

¹⁾Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾Pulse width t_p limited by $T_{j,max}$

³⁾Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.46	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	63	°C/W	device on PCB, minimal footprint

Table Thermal characteristics(TOLL)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.28	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	48	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	85	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{(GS)th}$	2.5		4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=85V, V_{GS}=0V, T_j=25^\circ C$
Gate-source leakage current	I_{GSS}	-	-	+/-100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance (TO220&263)	$R_{DS(on)}$	-	2.1	2.6	m Ω	$V_{GS}=10V, I_D=20A, T_j=25^\circ C$
Drain-source on-state resistance (TOLL)	$R_{DS(on)}$	-	1.8	2.0	m Ω	$V_{GS}=10V, I_D=20A, T_j=25^\circ C$
Gate resistance (Intrinsic)	R_G	-	2.1	-	Ω	$f=1MHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	11000	-	PF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$
Output capacitance	C_{oss}	-	3500	-	PF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$
Reverse transfer capacitance	C_{riss}	-	350	-	PF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$
Turn-on delay time	$t_{d(on)}$	-	33	-	ns	$V_{DD}=42V, V_{GS}=10V, I_D=80A, R_G=2.5\Omega$
Rise time	t_r	-	47	-	ns	$V_{DD}=42V, V_{GS}=10V, I_D=80A, R_G=2.5\Omega$
Turn-off delay time	$t_{d(off)}$	-	89	-	ns	$V_{DD}=42V, V_{GS}=10V, I_D=80A, R_G=2.5\Omega$
Fall time	t_f	-	46	-	ns	$V_{DD}=42V, V_{GS}=10V, I_D=80A, R_G=2.5\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	46	-	nC	$V_{DD}=42V, I_D=80A, V_{GS}=10V$
Gate to drain charge	Q_{gd}	-	46	-	nC	$V_{DD}=42V, I_D=80A, V_{GS}=10V$
Gate charge total	Q_g	-	152	-	nC	$V_{DD}=42V, I_D=80A, V_{GS}=10V$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous Source Current at silicon	I_{SD}	-	-	229	A	Maximum Ratings
Diode forward voltage	V_{SD}	-	0.8	1.2	V	$V_{GS}=0V, I_s=1A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	103	-	ns	$V_{GS}=0V, I_F=80A, di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	118	-	nC	$V_{GS}=0V, I_F=80A, di_F/dt=100A/\mu s$

4 Electrical characteristics diagram

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

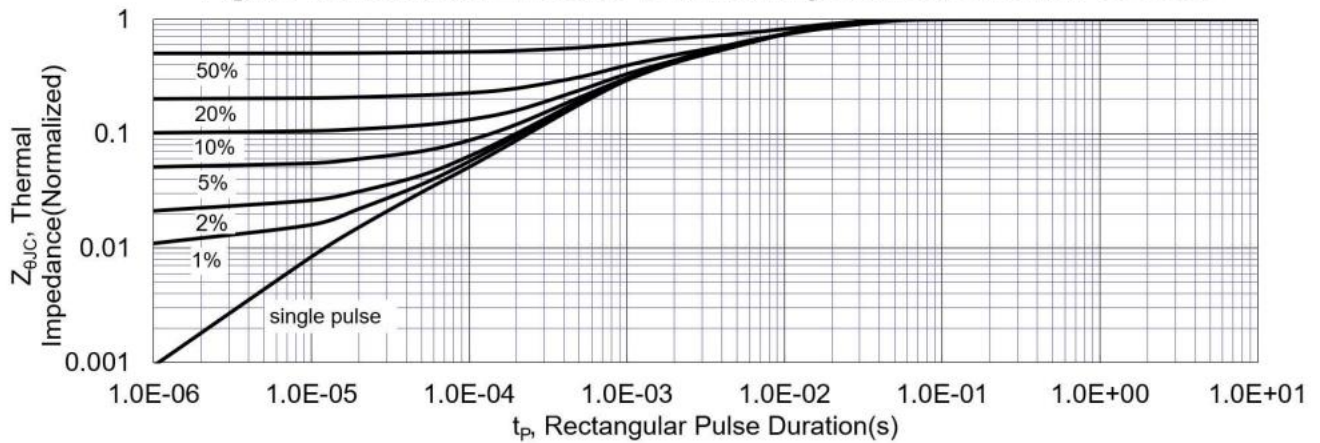


Figure 2. Maximum Power Dissipation vs. Case Temperature

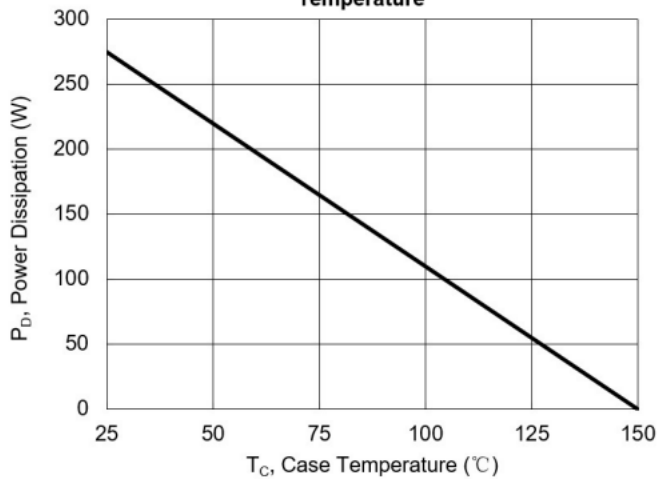


Figure 3. Maximum Continuous Drain Current vs Case Temperature

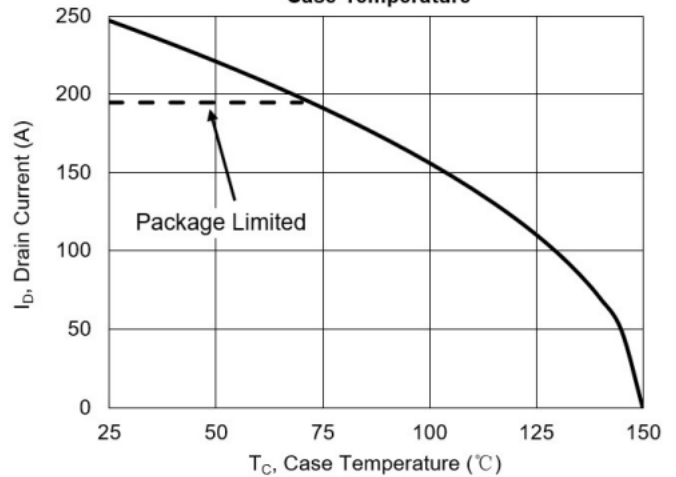


Figure 4. Typical Output Characteristics

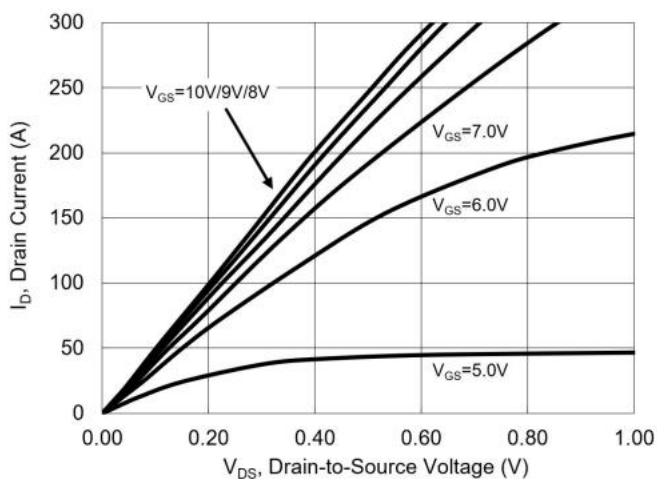


Figure 5. Unclamped Inductive Switching Capability

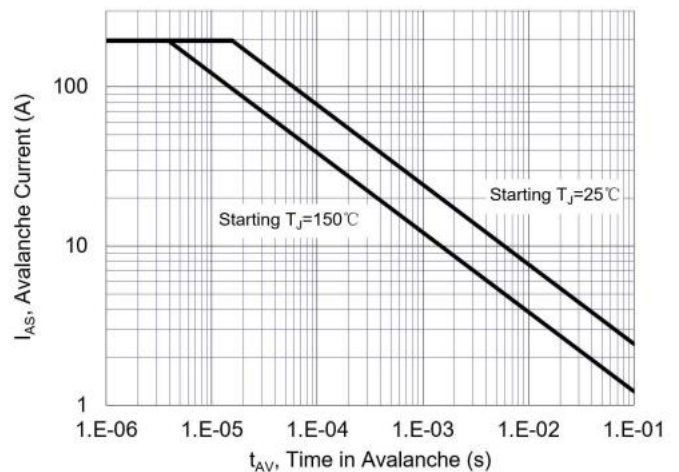


Figure 6. Maximum Peak Current Capability

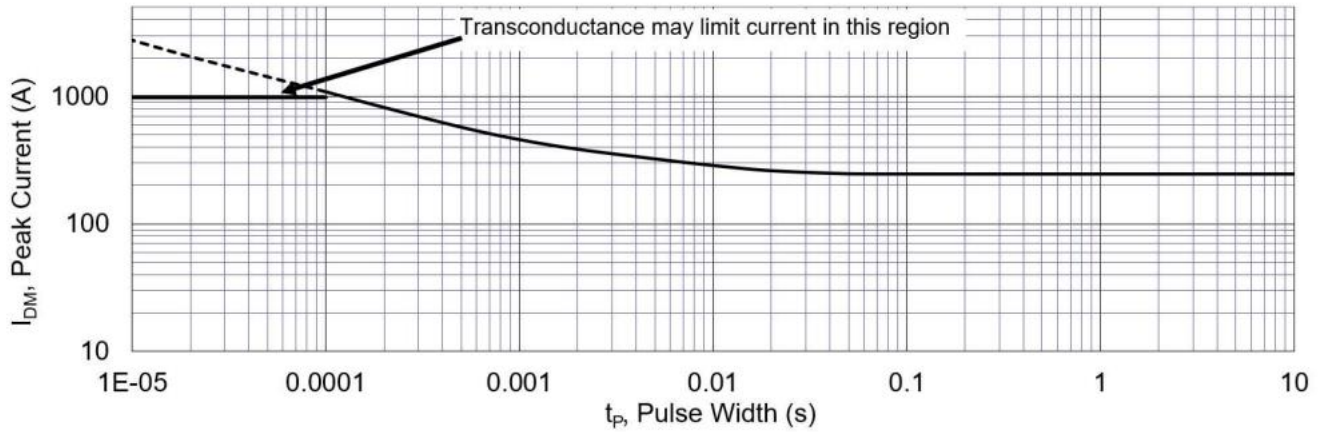


Figure 7. Maximum Forward Safe Operation Area

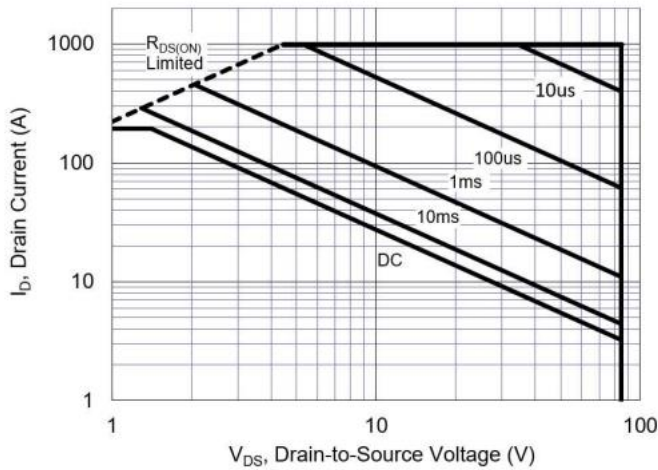


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

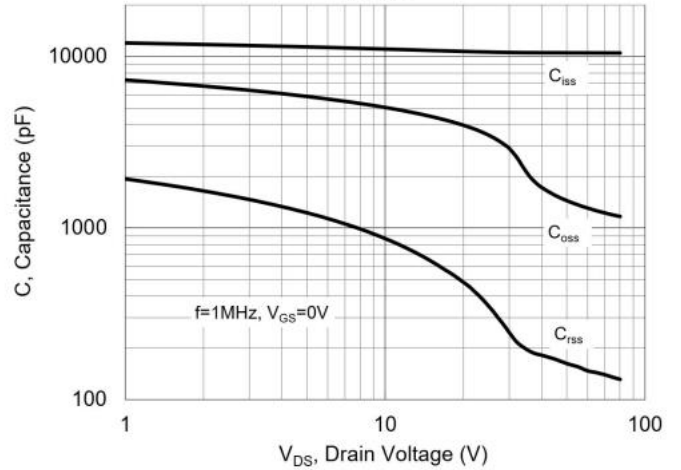
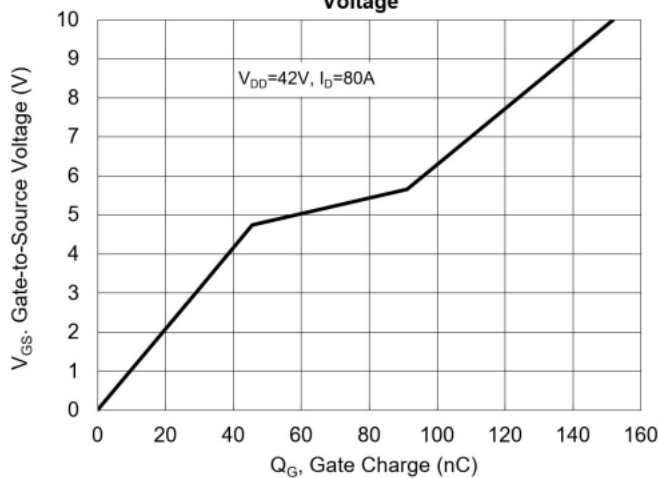


Figure 9. Typical Gate Charge vs. Gate-to-Source Voltage



5. Package Outlines

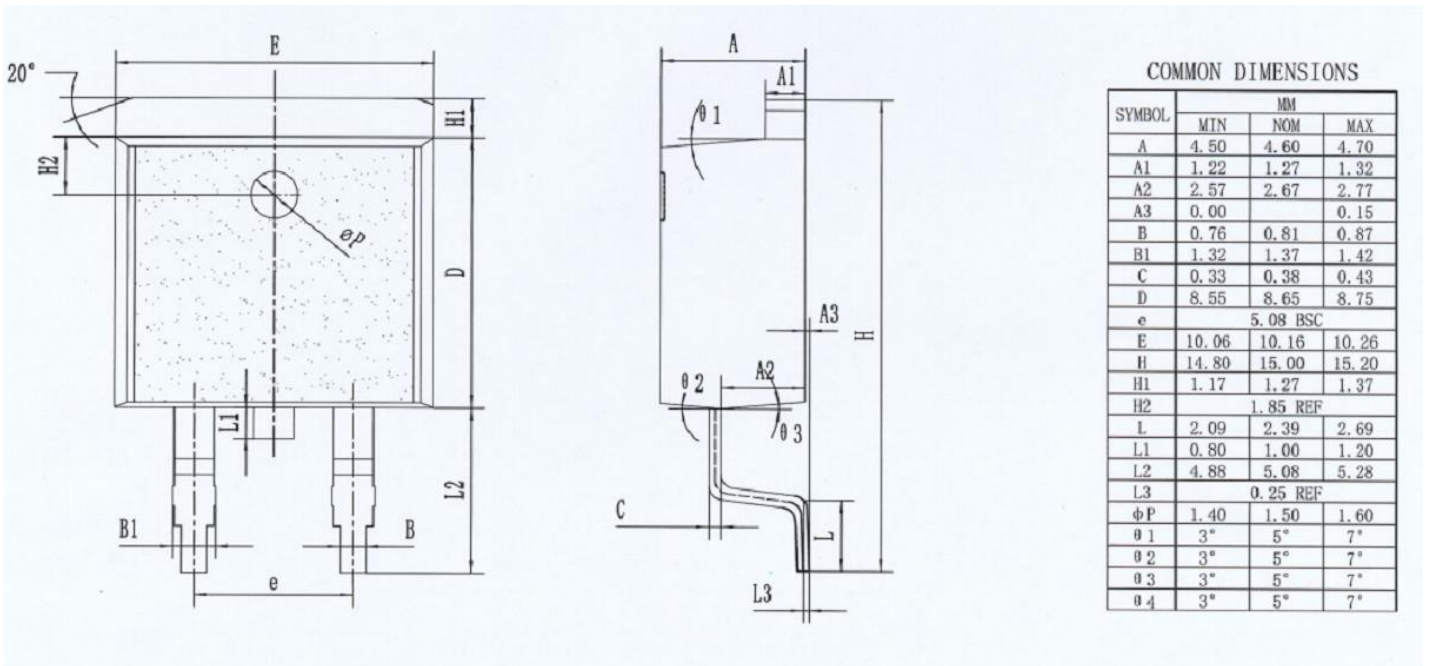
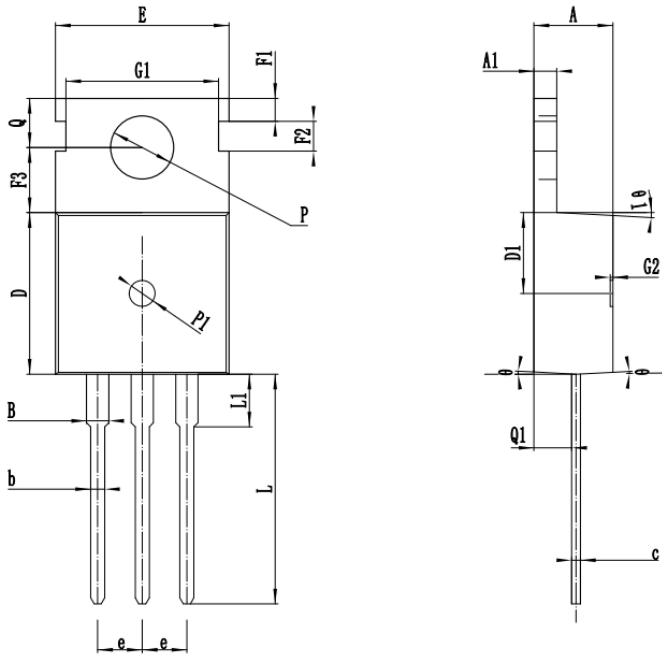
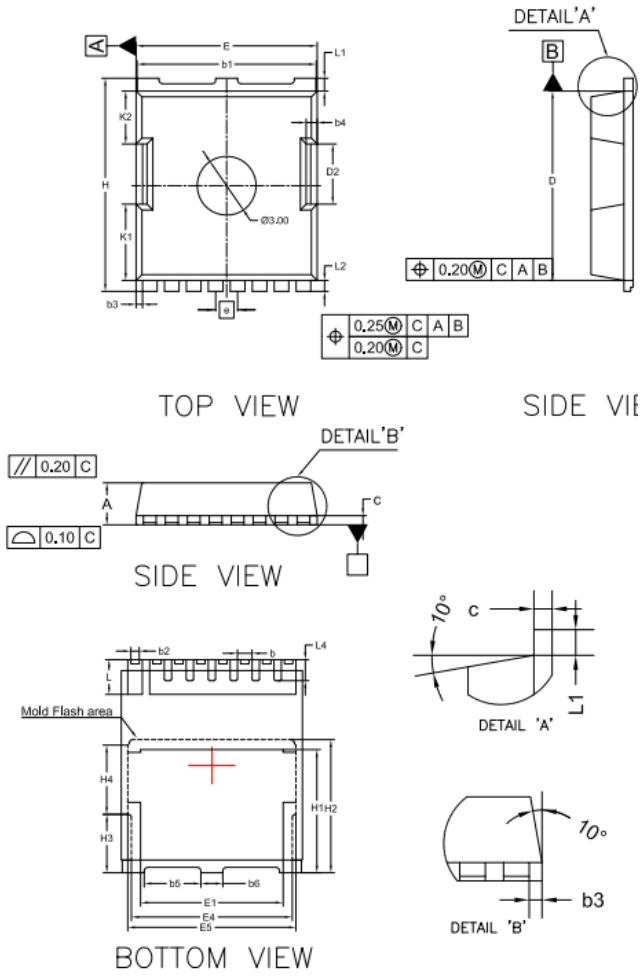


Figure1: Outline PG-T0263(LM)



符号 symbol	MIN	NOM	MAX
*A	4.400	4.500	4.600
*A1	1.290	1.300	1.380
*B	1.220	1.270	1.370
*b	0.760	0.800	0.900
*c	0.450	0.500	0.600
*D	9.100	9.200	9.300
*D1	4.500	4.600	4.700
*E	9.780	9.880	10.050
*E1	9.920	10.020	10.120
e	2.480	2.540	2.600
F1	1.220	1.300	1.380
F2	1.600	1.700	1.800
*F3	3.600	3.700	3.800
G1	8.600	8.700	8.800
G2	0.100	0.150	0.200
*L	12.980	13.080	13.230
L1	2.900	3.000	3.100
*ΦP	3.540	3.650	3.670
ΦP1	1.400	1.500	1.600
Q	2.700	2.800	2.900
*Q1	2.300	2.400	2.500
θ	1°	3°	5°
*θ1	1°	3°	5°

Figure2: Outline PG-TO220(LM)



SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
* A	2.200	2.300	2.400
c	0.492	0.500	0.508
* D	10.280	10.380	10.480
* E	9.800	9.900	10.000
e	1.20 BSC		
* H	11.580	11.680	11.780
H1	6.650	6.750	6.850
H2	7.300		
H3	3.200		
H4	3.800		
K1	4.180		
K2	2.900		
* D2	3.300		
b	0.700	0.800	0.900
b1	9.700	9.800	9.900
b2	0.420	0.460	0.500
b3	0.350		
b4	0.600		
b5	3.100		
b6	1.200		
L	1.700	1.900	2.100
L1	0.700		
L2	0.600		
L4	1.050	1.150	1.250
L5	0.500	0.600	0.700
E1	7.800		
E4	8.800		
E5	9.200		

Figure3: Outline PG-TOLL(JJW)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2022-08-02	Preliminary version
1.1	2022-09-13	Updated Vth limit
1.2	2023-04-12	Updated TO220&263 POD to LM and added TOLL package
1.3	2023-05-05	Updated TO220 POD to LM liangmian

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