1MHz, High Efficiency, Step-Up Converter with Internal FET Switch

Features

- **Wide 2.5V to 6V Input Voltage Range**
- **Built-in 0.6W N-Channel MOSFET**
- **Built-in Soft-Start**
- **High Efficiency up to 90%**
- **<1mA Quiescent Current During Shutdown**
- **Current-Mode Operation**
  - **Stable with Ceramic Output Capacitors**
  - **Fast Transient Response**
- **Current-Limit Protection**
- **Over-Temperature Protection with Hysteresis**
- **Available in a Tiny 5-Pin SOT-23 and TSOT-23 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

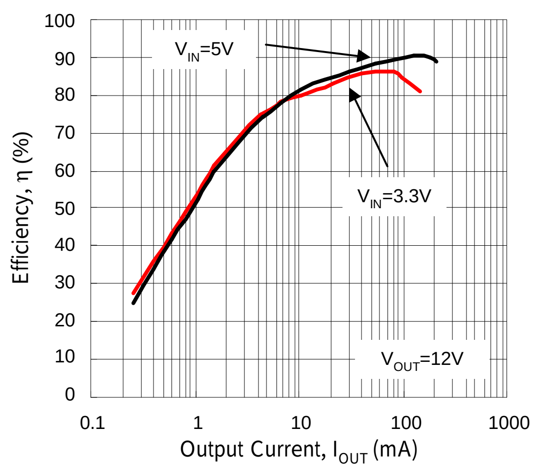
Applications

- **Cell Phone and Smart Phone**
- **PDA, PMP, MP3**
- **Digital Camera**
- **Boost Regulators**

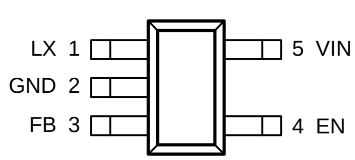
General Description

The APW7137 is a fixed switching frequency (1MHz typical), current-mode, step-up regulator with an integrated N-channel MOSFET. The device allows the usage of small inductors and output capacitors for portable devices. The current-mode control scheme provides fast transient response and good output voltage accuracy.

The APW7137 includes under-voltage lockout, current-limit, and over-temperature shutdown preventing damage in the event of an output overload.

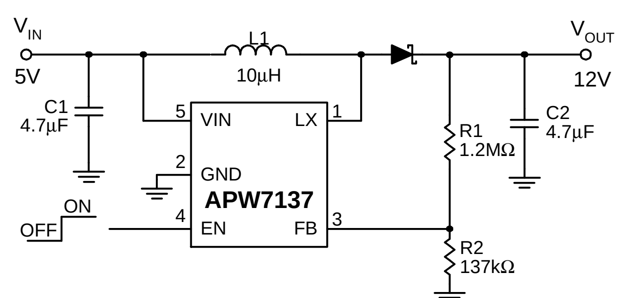


Pin Configuration



SOT-23-5 / TSOT-23-5
(Top View)

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW7137 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code B : SOT-23-5 BT : TSOT-23-5 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7137 B : W37X	X - Date Code
APW7137 BT : 37WX	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin to GND	-0.3 to 7	V
V_{LX}	LX Pin to GND	-0.3 to 40	V
V_{EN}	EN Pin to GND	-0.3 to V_{IN}	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance (Note 2) SOT-23-5 TSOT-23-5	 260 220	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.5 ~ 6	V
V_{LX}	LX to GND Voltage	-0.3 ~ 36	V
V_{OUT}	Converter Output Voltage	V_{IN} ~ 35	V
C_{IN}	Input Capacitor	2.2 ~	μF
C_{OUT}	Output Capacitor	2.2 ~	μF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Please refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over. V_{IN}=3.6V, I_{OUT}=0mA, T_A=-40°C to 85°C, unless otherwise noted. Typical values are at T_A=25°C.

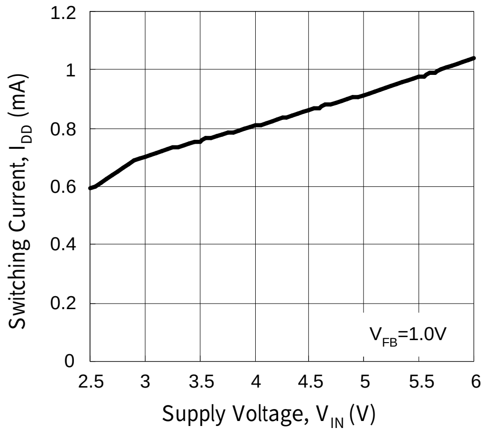
Symbol	Parameter	Test Conditions	APW7137			Unit
			Min.	Typ.	Max.	
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range	T_A = -40 ~ 85°C, T_J = -40 ~ 125°C	2.5	-	6	V
I_{DD}	Input DC Bias Current	V_{FB} = 1.0V, switching	-	1	2	mA
I_{SD}		EN = GND	-	0.1	1	μA
UNDER-VOLTAGE LOCKOUT						
	UVLO Threshold Voltage	V_{IN} Rising	2.0	2.2	2.4	V
	UVLO Hysteresis Voltage		50	100	150	mV
REFERENCE AND OUTPUT VOLTAGES						
V_{REF}	Regulated Feedback Voltage	T_A = 25°C	1.212	1.23	1.248	V
		T_A = -40 ~ 85°C	1.205	-	1.255	
I_{FB}	FB Input Current		-50	-	50	nA
INTERNAL POWER SWITCH						
F_{SW}	Switching Frequency	V_{FB}=1.1V	0.8	1.0	1.2	MHz
R_{ON}	Power Switch On Resistance		-	0.6	-	Ω
I_{LIM}	Power Switch Current Limit		1	1.3	1.6	A
	LX Leakage Current	V_{EN}=0V, V_{LX}=0V or 5V, V_{IN} = 5V	-1	-	1	μA
D_{MAX}	LX Maximum Duty Cycle		92	95	98	%
SOFT-START AND SHUTDOWN						
T_{SS}	Soft-Start Duration (Note 4)		-	2	3	ms
V_{TEN}	EN Voltage Threshold	V_{EN} Rising	0.4	0.7	1	V
	EN Voltage Hysteresis		-	0.1	-	V
I_{LEN}	EN Leakage Current	V_{EN}=5V, V_{IN} = 5V	-1	±0.5	1	μA
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over-Temperature Protection (Note 4)	T_J Rising	-	150	-	°C
	Over-Temperature Protection Hysteresis (Note 4)		-	40	-	°C

Note 4: Guaranteed by design, not production tested.

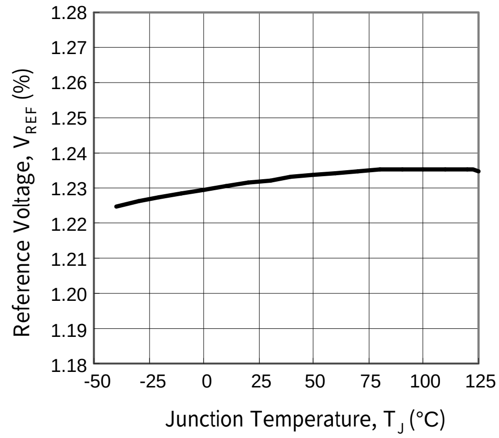
Typical Operating Characteristics

(Refer to the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, unless otherwise specified)

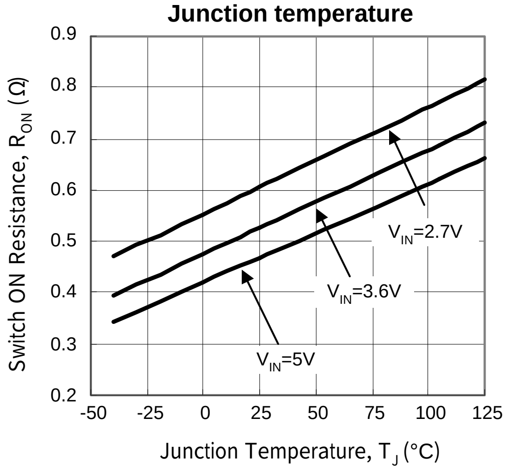
Switching Current vs. Supply Voltage



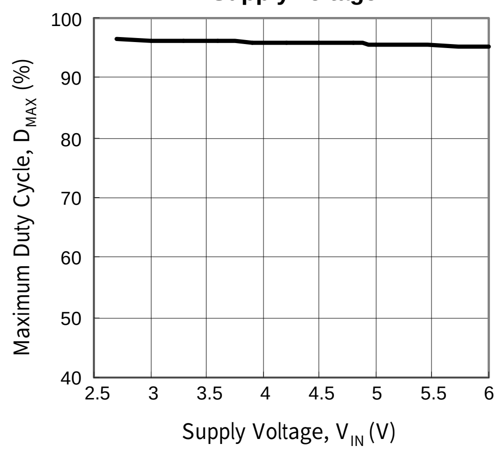
Reference Voltage vs. Junction Temperature



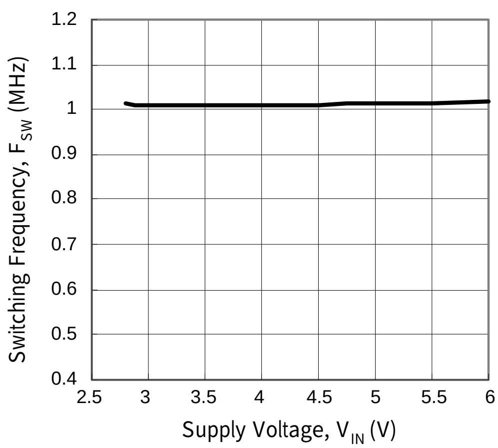
Switch ON Resistance vs. Junction temperature



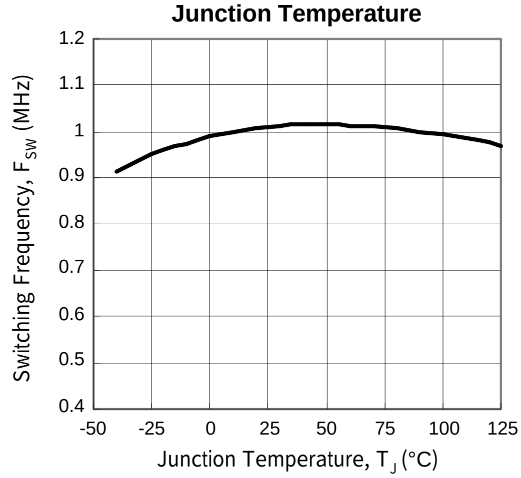
Maximum Duty Cycle vs. Supply Voltage



Switching Frequency vs. Supply Voltage



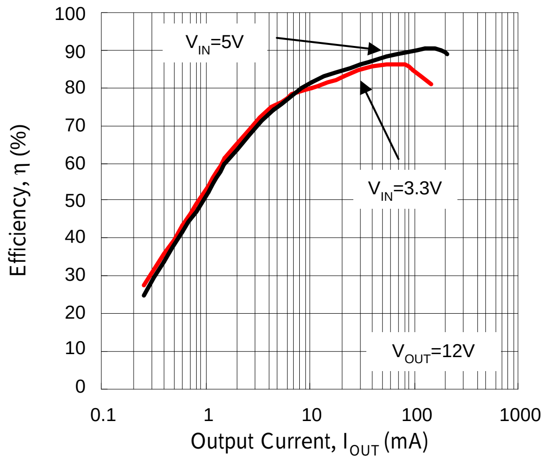
Switching Frequency vs. Junction Temperature



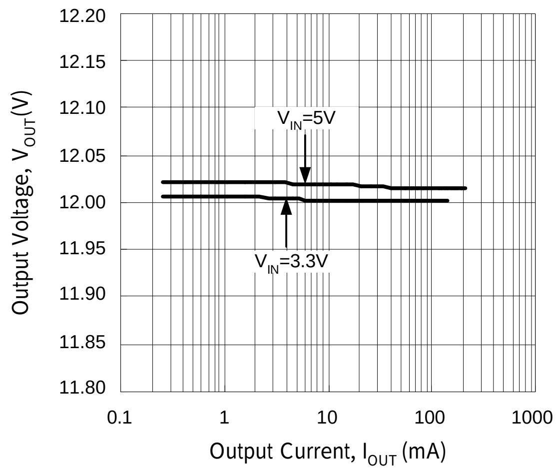
Typical Operating Characteristics (Cont.)

(Refer to the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, unless otherwise specified)

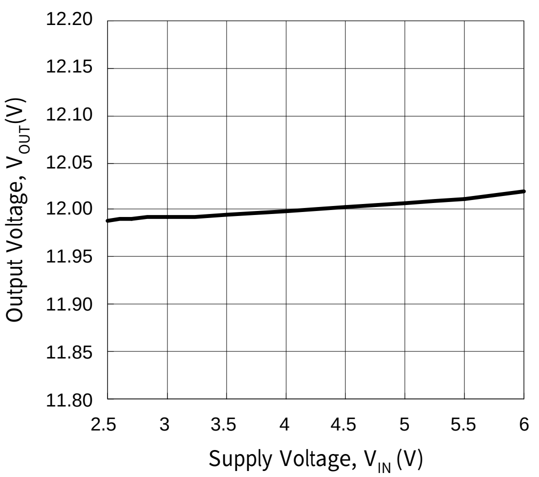
Efficiency vs. Output Current



Output Voltage vs. Output Current



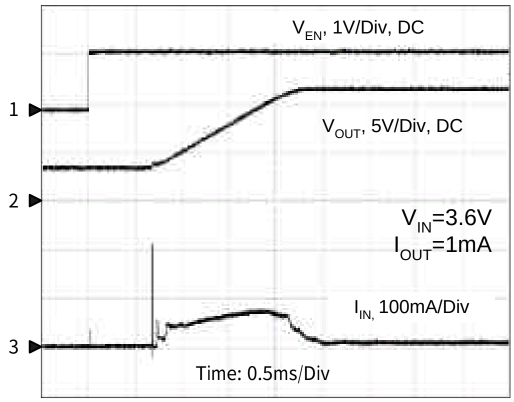
Output Voltage vs. Supply Voltage



Operating Waveforms

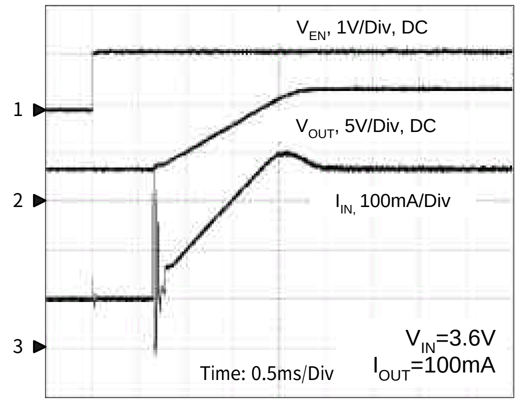
(Refer to the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, unless otherwise specified)

Start-up



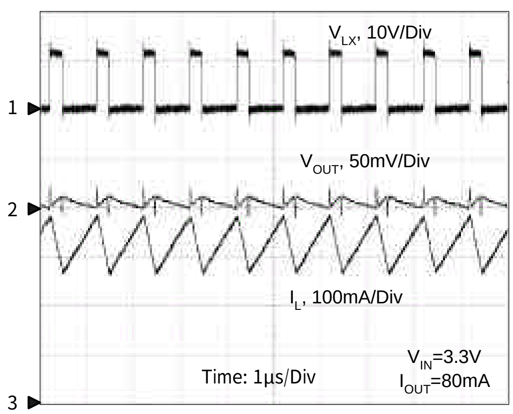
CH1: V_{EN}, 1V/Div, DC
CH2: V_{OUT}, 5V/Div, DC
CH3: I_{IN}, 100mA/Div, DC
Time: 0.5ms/Div

Start-up



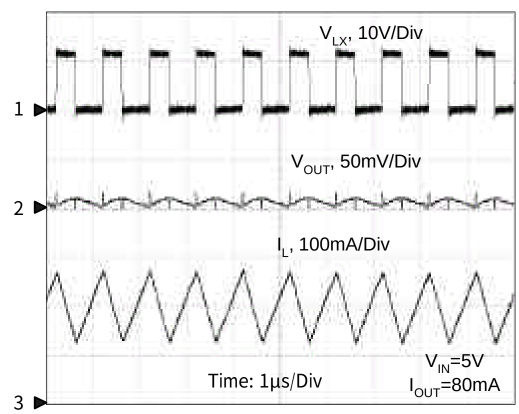
CH1: V_{EN}, 1V/Div, DC
CH2: V_{OUT}, 5V/Div, DC
CH3: I_{IN}, 100mA/Div, DC
Time: 0.5ms/Div

Normal Operation



CH1: V_{LX}, 10V/Div, DC
CH2: V_{OUT}, 50mV/Div, AC
CH3: I_L, 100mA/Div, DC
Time: 1µs/Div

Normal Operation

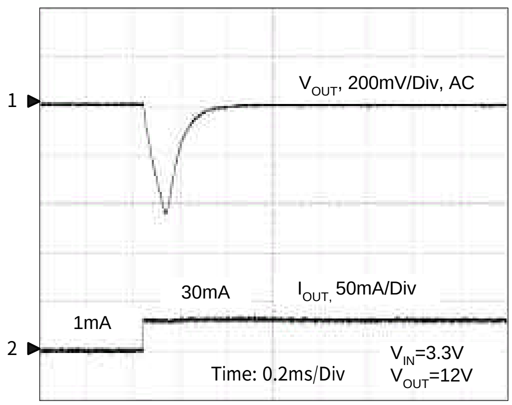


CH1: V_{LX}, 10V/Div, DC
CH2: V_{OUT}, 50mV/Div, AC
CH3: I_L, 100mA/Div, DC
Time: 1µs/Div

Operating Waveforms (Cont.)

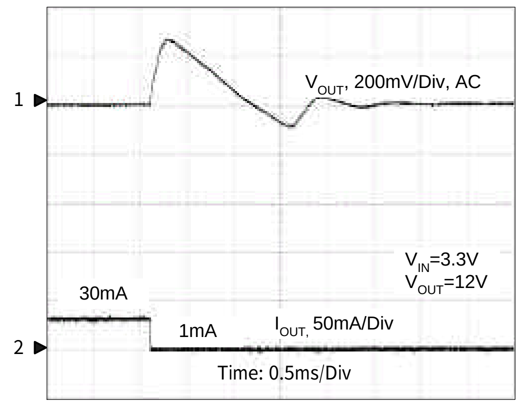
(Refer to the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, unless otherwise specified)

Load Transient Response



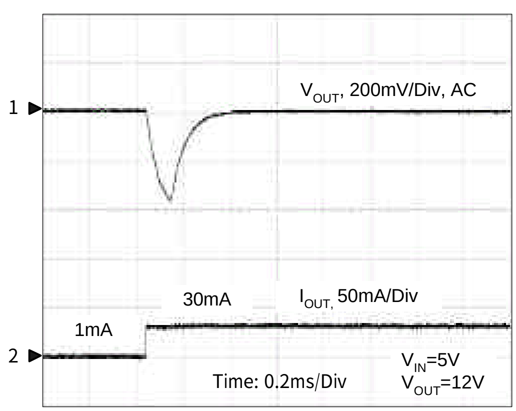
CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.2ms/Div

Load Transient Response



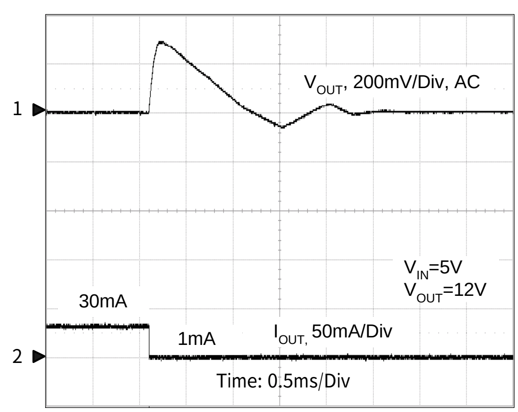
CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.5ms/Div

Load Transient Response



CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.2ms/Div

Load Transient Response

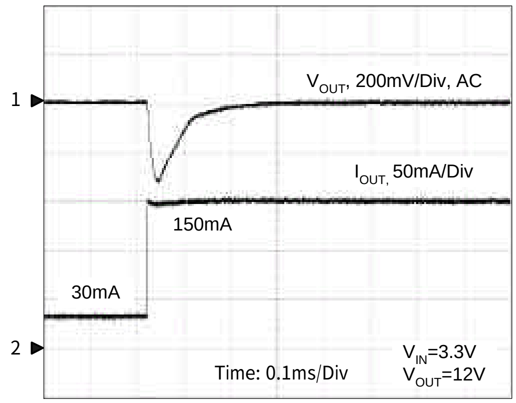


CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.5ms/Div

Operating Waveforms (Cont.)

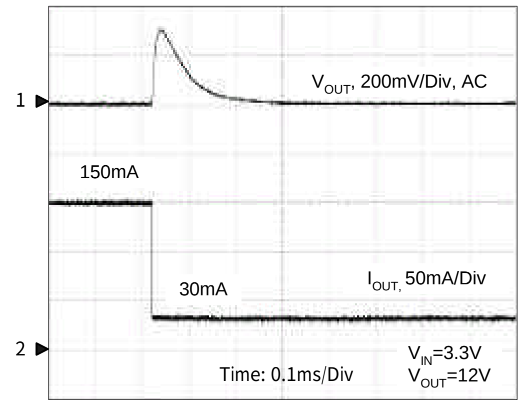
(Refer to the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, unless otherwise specified)

Load Transient Response



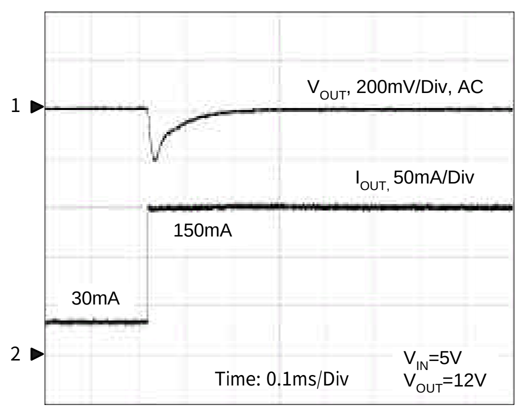
CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.1ms/Div

Load Transient Response



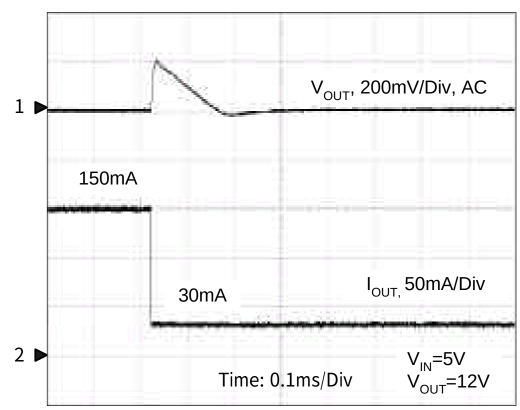
CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.1ms/Div

Load Transient Response



CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.1ms/Div

Load Transient Response

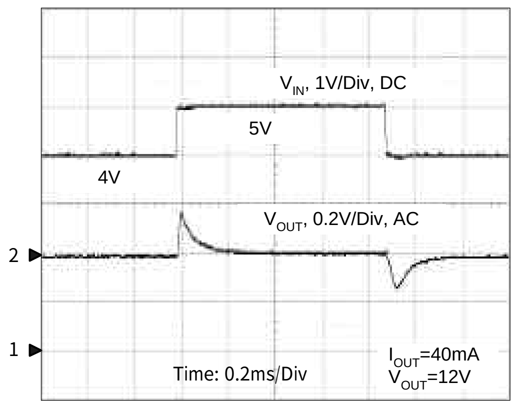


CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 50mA/Div, DC
Time: 0.1ms/Div

Operating Waveforms (Cont.)

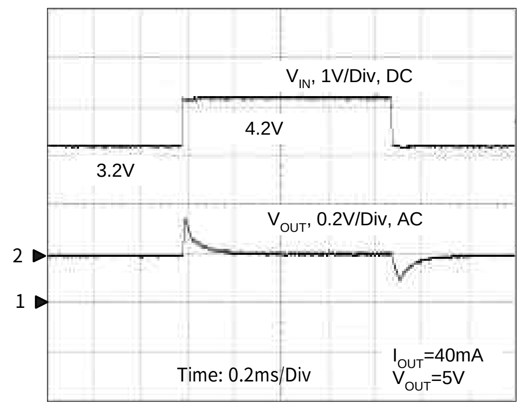
(Refer to the section "Typical Application Circuits", V_{IN}=3.6V, T_A=25°C, unless otherwise specified)

Line Transient Response



CH1: V_{IN}, 1V/Div, DC
CH2: V_{OUT}, 0.2/Div, AC
Time: 0.2ms/Div

Line Transient Response

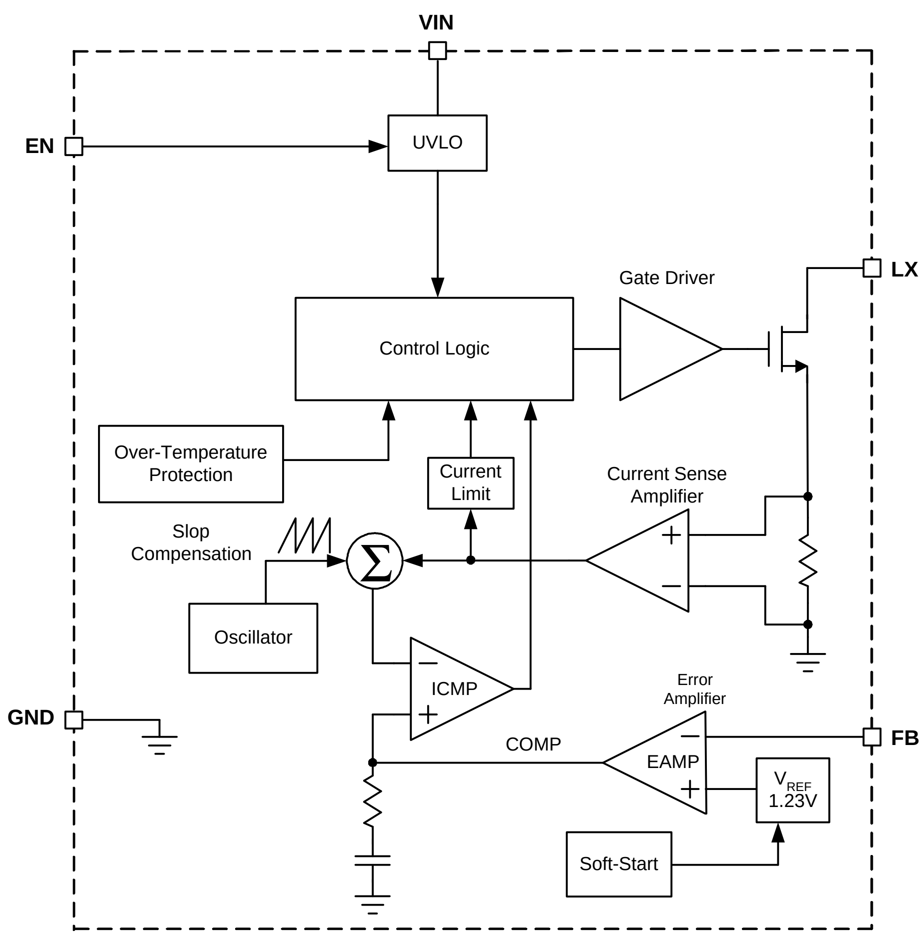


CH1: V_{IN}, 1V/Div, DC
CH2: V_{OUT}, 0.2/Div, AC
Time: 0.2ms/Div

Pin Description

PIN.		FUNCTION
NO	NAME	
1	LX	Switch pin. Connect this pin to inductor/diode here.
2	GND	Power and signal ground pin.
3	FB	Feedback Input. The device senses feedback voltage via FB and regulate the voltage at 1.23V. Connecting FB with a resistor-divider from the output that sets the output voltage in the range from V_{IN} to 30V.
4	EN	Enable Control Input. Forcing this pin above 1.0V enables the device. Forcing this pin below 0.4V to shut it down. In shutdown, all functions are disabled to decrease the supply current below 1µA. Do not left this pin floating.
5	VIN	Main Supply Pin. Must be closely decoupled to GND with a 2.2µF or greater ceramic capacitor.

Block Diagram



Typical Application Circuits

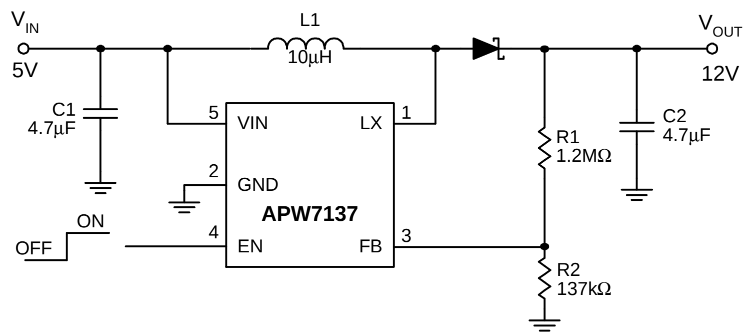


Figure 1. Typical 5V to 12V Supply

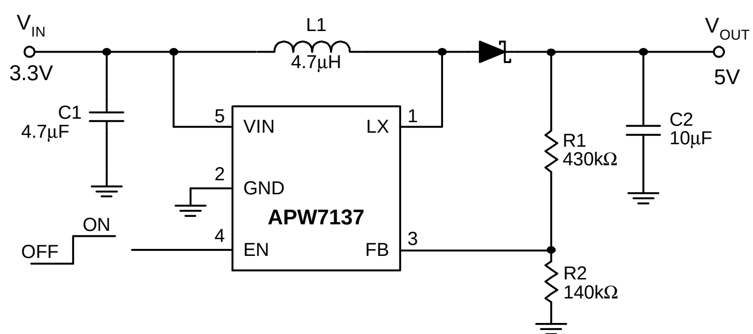


Figure 2. Standard 3.3V to 5V Supply

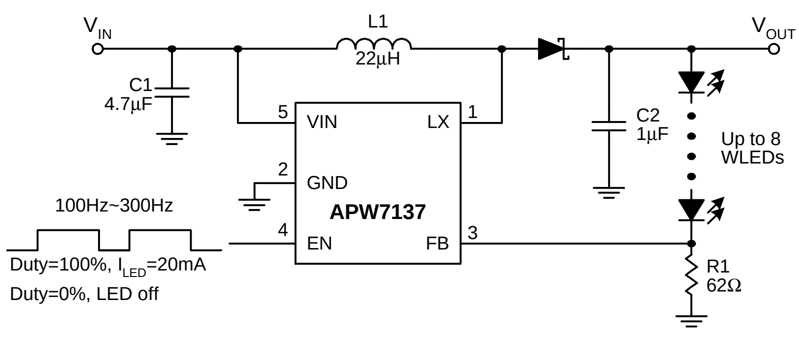


Figure 3. Brightness control using a PWM signal apply to EN

Typical Application Circuits (Cont.)

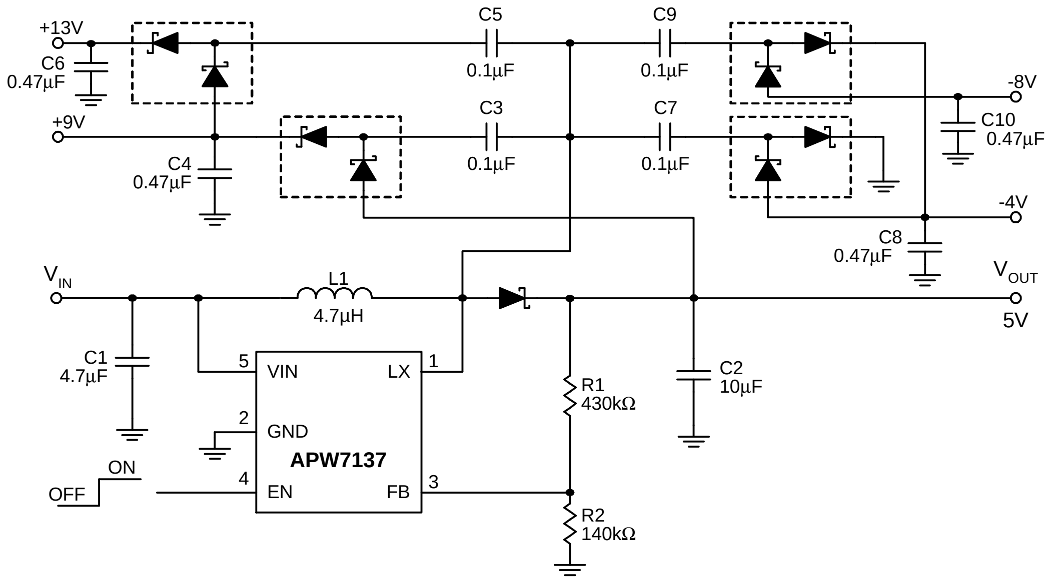


Figure 4. Multiple Output for TFT-LCD Power Supply

Function Description

Main Control Loop

The APW7137 is a constant frequency and current-mode switching regulator. In normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch, and then turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP node which is the output of the error amplifier (EAMP). An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slightly to decrease in V_{FB} associated with the 1.23V reference, which in turn, it causes the COMP voltage to increase until the average inductor current matches the new load current.

VIN Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

Soft-Start

The APW7137 has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage (1.23V typical) until the ramp voltage reaches the reference voltage.

Current-Limit Protection

The APW7137 monitors the inductor current, flows through the N-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the APW7137 from damaging during overload or short-circuit conditions.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7137. When the junction temperature exceeds 150°C, a thermal sensor turns off the power MOSFET allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulates the output voltage again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions increasing the lifetime of the device.

Enable/Shutdown

Driving EN to the ground places the APW7137 in shutdown mode. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down, and the quiescent supply current reduces to 1μA maximum.

Application Information

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the ripple of the input current drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller when an input capacitor with larger capacitance is used. For reliable operation, it is recommended to select the capacitor with maximum voltage rating at least 1.2 times of the maximum input voltage. The capacitors should be placed close to the VIN and the GND.

Inductor Selection

Selecting an inductor with low dc resistance reduces conduction losses and achieves high efficiency. The efficiency is moderated whilst using small chip inductor which operates with higher inductor core losses. Therefore, it is necessary to take further consideration while choosing an adequate inductor. Mainly, the inductor value determines the inductor ripple current: larger inductor value results in smaller inductor ripple current and lower conduction losses of the converter. However, larger inductor value generates slower load transient response. A reasonable design rule is to set the ripple current, ΔI_L, to be 30% to 50% of the maximum average inductor current, $I_{L(AVG)}$. The inductor value can be obtained as below,

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{F_{SW} \cdot I_{OUT(MAX)}} \times \frac{\eta}{\left(\frac{\Delta I_L}{I_{L(AVG)}}\right)}$$

where

V_{IN} = input voltage

V_{OUT} = output voltage

F_{SW} = switching frequency in MHz

I_{OUT} = maximum output current in amp.

η = Efficiency

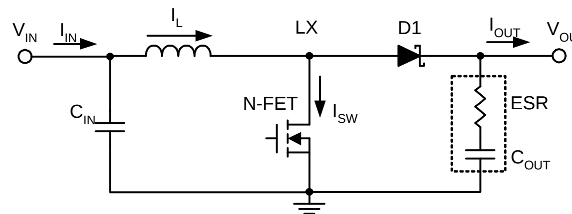
$\Delta I_L / I_{L(AVG)}$ = inductor ripple current/average current (0.3 to 0.5 typical)

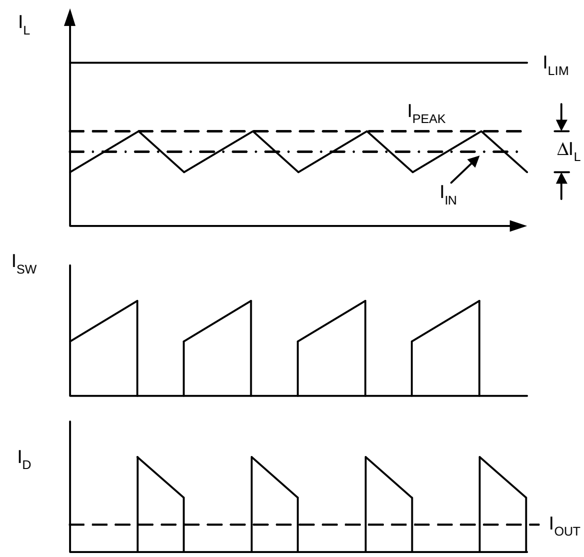
To avoid the saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)} \cdot V_{OUT}}{V_{IN} \cdot \eta}$$

The peak inductor current is calculated as the following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} \cdot \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot L \cdot F_{SW}}$$





Output Capacitor Selection

The current-mode control scheme of the APW7137 allows the usage of tiny ceramic capacitors. The higher capacitor value provides good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{COUT} \approx \frac{I_{OUT}}{C_{OUT}} \cdot \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \cdot F_{SW}}\right)$$

$$\Delta V_{ESR} \approx I_{PEAK} \cdot R_{ESR}$$

where I_{PEAK} is the peak inductor current.

Application Information (Cont.)

Output Capacitor Selection (Cont.)

For ceramic capacitor application, the output voltage ripple is dominated by the ΔV_{COUT}. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

Output Voltage Setting

The output voltage is set by a resistive divider. The external resistive divider is connected to the output which allows remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of the maximum value of R1 is 2MΩ and R2 is 200kΩ for keeping the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) = 1.23\left(1 + \frac{R1}{R2}\right)$$

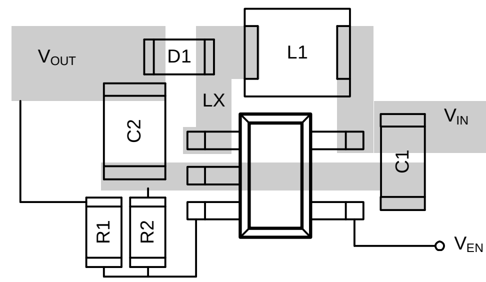
Diode Selection

To achieve the high efficiency, a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter.

Layout Consideration

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

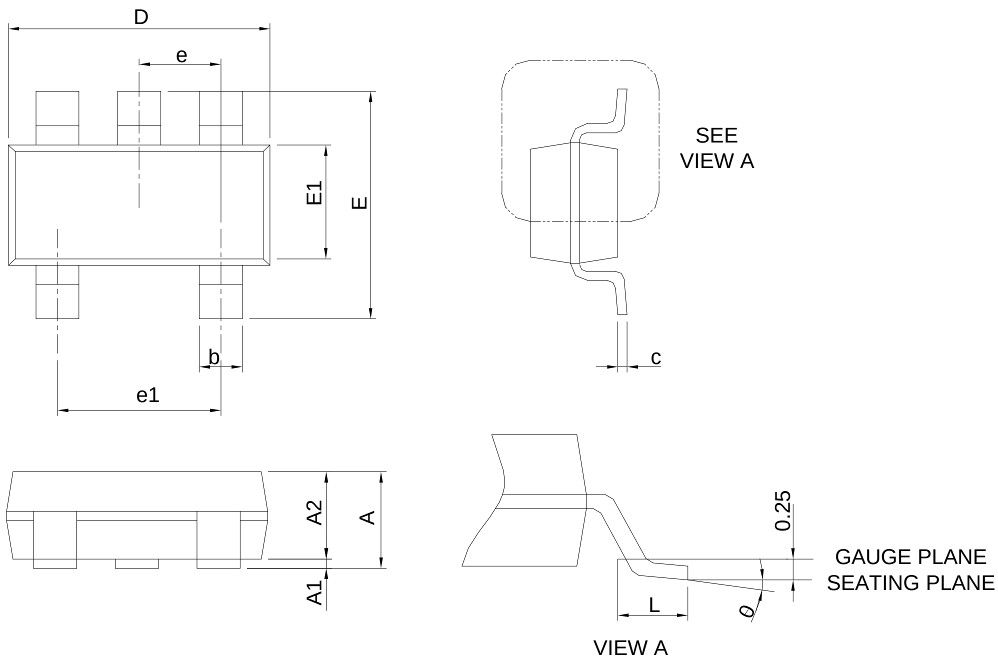
1. The input capacitor should be placed close to the VIN and the GND without any via holes for good input voltage filtering.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.



Optimized APW7137 Layout

Package Information

SOT-23-5

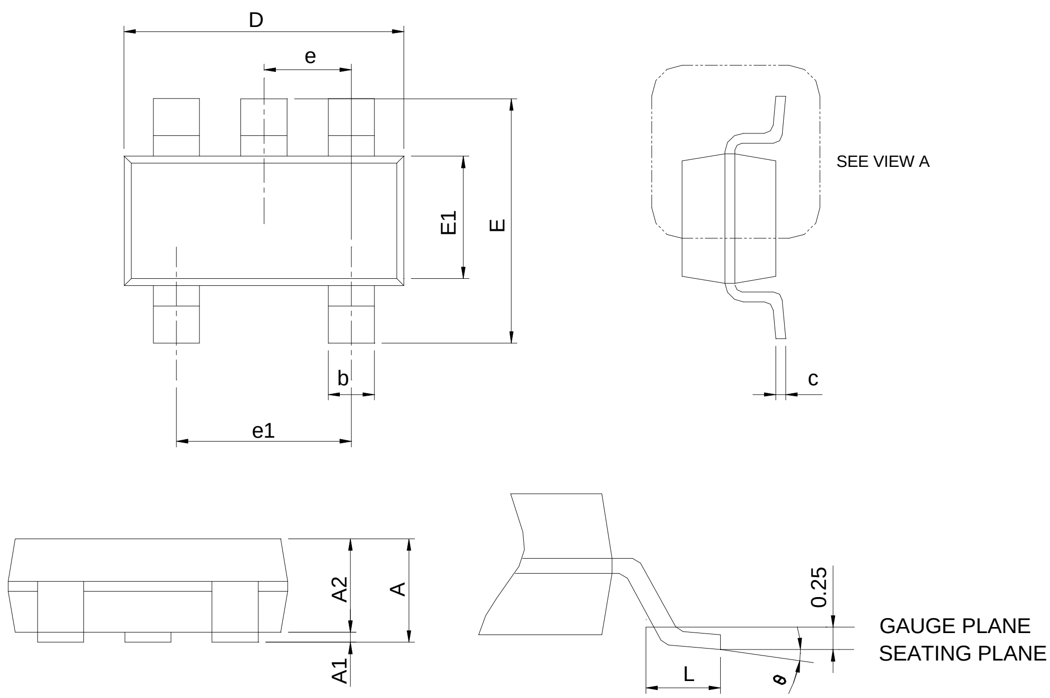


SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

TSOT-23-5

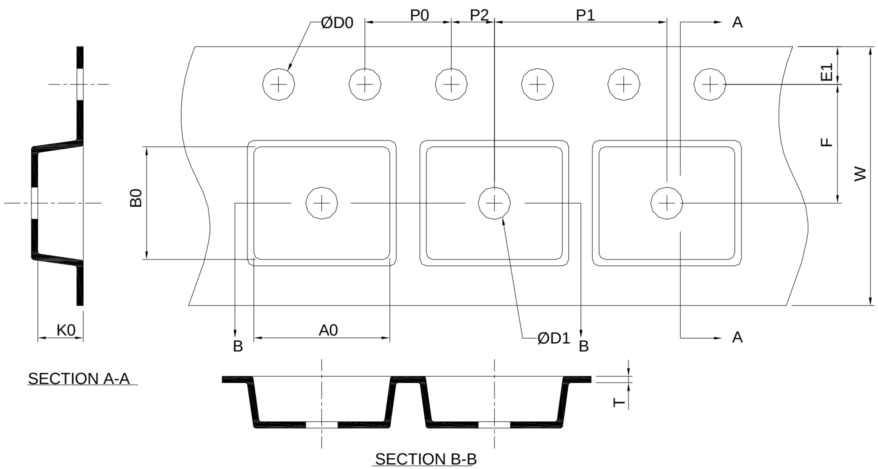


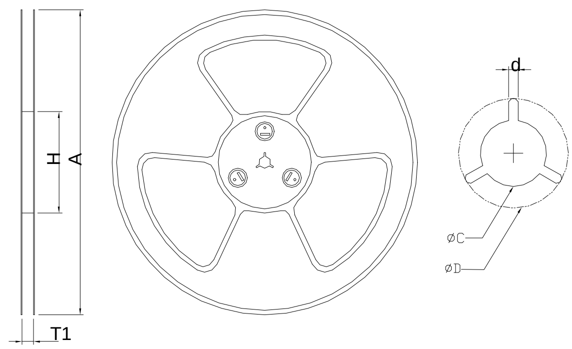
VIEW A

SYMBOL	TSOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
TSOT-23-5	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

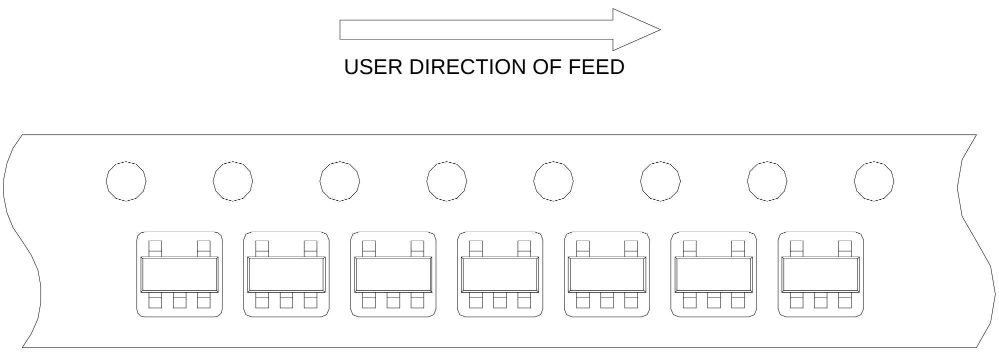
(mm)

Devices Per Unit

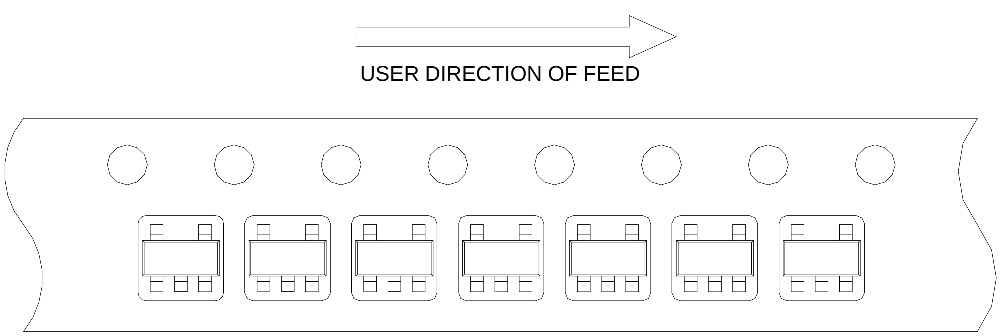
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
TSOT-23-5	Tape & Reel	3000

Taping Direction Information

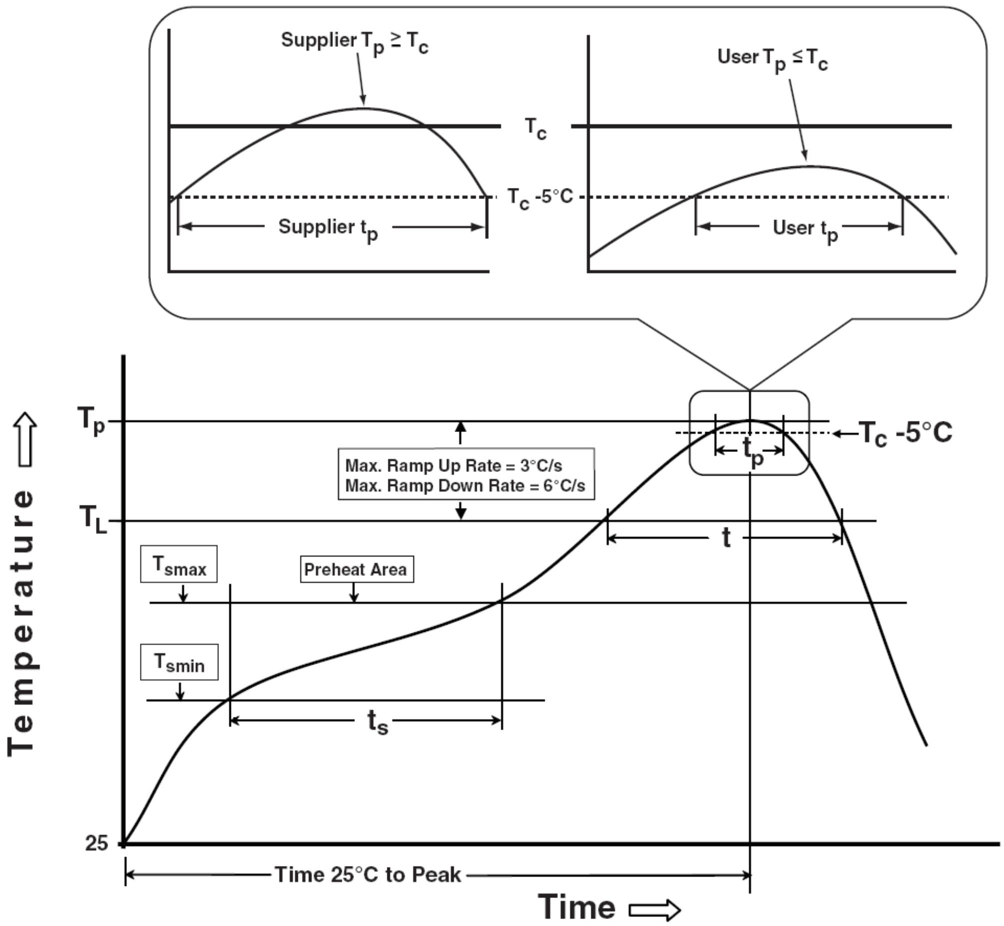
SOT-23-5



TSOT-23-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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