2A 28V 380kHz Asynchronous Buck Converter

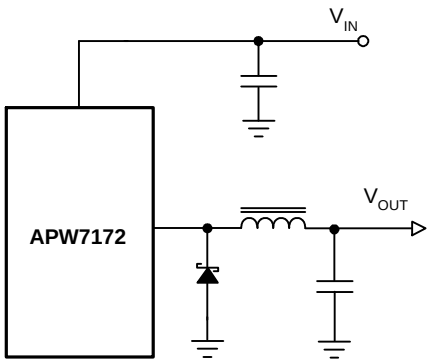
Features

- **Wide Input Voltage from 4.5V to 28V**
- **2A Continuous Output Current**
- **Adjustable Output Voltage from 0.92V to 19V**
- **0.18Ω Integrated High Side Power MOSFET**
- **Fixed 380kHz Switching Frequency**
- **Stable with Low ESR Output Capacitors**
- **Built-In Diode for Bootstrap Function**
- **Power-On-Reset Detection**
- **Programmable Soft-Start**
- **Over-Temperature Protection**
- **Current-Limit Protection with Frequency Foldback**
- **Enable/Shutdown Function**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD Monitor /TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Notebook Computer**

Simplified Application Circuit

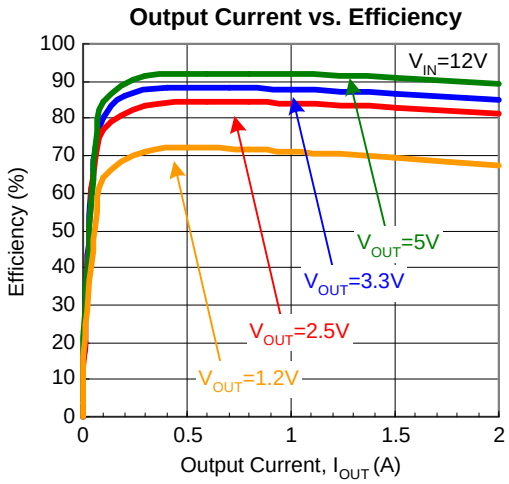


General Description

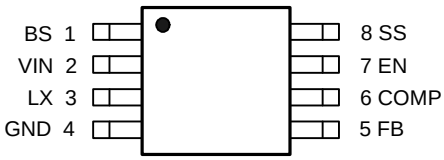
The APW7172 is a 2A, 380kHz asynchronous buck converter with an integrated 0.18Ω N-channel power MOSFET. The APW7172, designed with a current mode control scheme, can convert wide input voltage of 4.5V to 28V to the adjustable output voltage from 0.92V to 19V to provide excellent output voltage regulation.

The APW7172 is equipped with power-on-reset, soft-start, over-temperature protection, and current-limit into a single package. In shutdown mode, the supply current is only 25μA (typical).

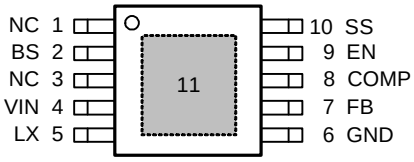
The device, which is available in SOP-8 and MSOP-10P packages, provides a very compact system solution with minimal external components and PCB area.



Pin Configuration



SOP-8 Top View



MSOP-10P Top View

11 =Exposed Pad
(connected to GND plane for better heat dissipation)

Ordering and Marking Information

APW7172 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-8 XA : MSOP-10P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7172 K : APW7172 XXXXX	XXXXX - Date Code
APW7172 XA : W7172 XXX XX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Supply Voltage (VIN to GND)	-0.3 ~ 30	V
V_{LX}	LX to GND Voltage	-1 ~ V_{IN}+0.3	V
	FB, COMP, SS, EN to GND Voltage (<V_{IN}+0.3V)	-0.3 ~ 6	V
V_{BS}	BS to GND Voltage	V_{LX} -0.3~ V_{LX}+6	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air (Note 2) SOP-8 MSOP-10P	 110 120	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance in Free Air SOP-8 MSOP-10P	 30 30	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of MSOP-10P is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.5 ~ 28	V
V_{OUT}	Converter Output Voltage	0.92 ~ 19	V
I_{OUT}	Converter Output Current	0 ~ 2	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits, these specifications apply over V_{IN}=12V and T_A= 25°C, unless otherwise specified.

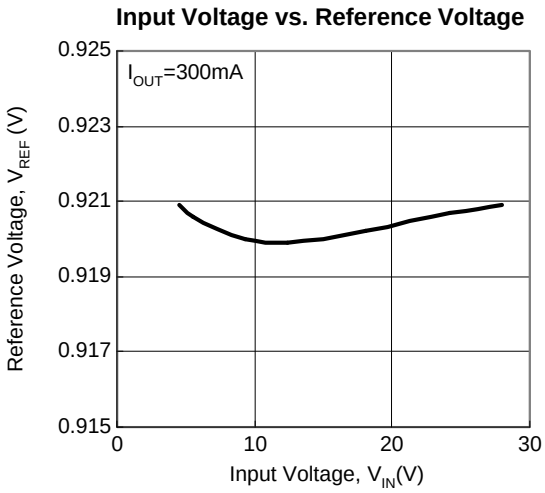
Symbol	Parameter	Test Conditions	APW7172			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB} = 1V, V_{EN} = 3V, LX = NC	-	1.3	1.6	mA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN} = 0V	-	25	-	μA
POWER-ON-RESET (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	3.9	4.2	4.5	V
	VIN POR Hysteresis		-	0.5	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Regulated on FB pin	0.897	0.92	0.943	V
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency		320	380	440	kHz
	Foldback Frequency	V_{OUT} = 0V	-	80	-	kHz
	Maximum Converter's Duty	V_{FB} = 0.92V	-	90	-	%
T_{ON_MIN}	Minimum Pulse Width of V_{LX}		-	130	-	ns
POWER MOSFET						
	High Side Switch Resistance		-	0.18	-	Ω
	High Side Switch Leakage Current	V_{EN} = 0V, V_{LX} = 0V	-	0.1	10	μA
	Low Side Switch Resistance		-	10	-	Ω
CURRENT MODE PWM CONVERTER						
G_{EA}	Error Amplifier Transconductance		500	800	1100	μA /V
A_{VEA}	Error Amplifier Voltage Gain		-	400	-	V/V

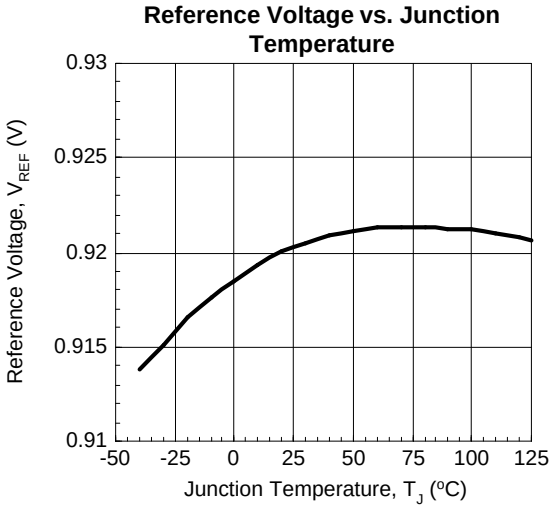
Electrical Characteristics (Cont.)

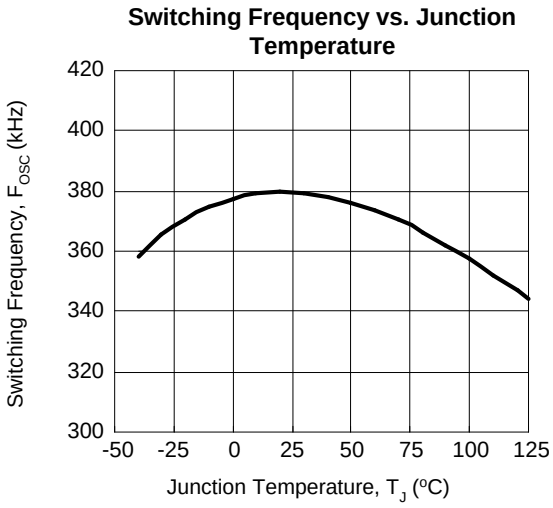
Refer to the typical application circuits, these specifications apply over V_{IN}=12V and T_A= 25°C, unless otherwise specified.

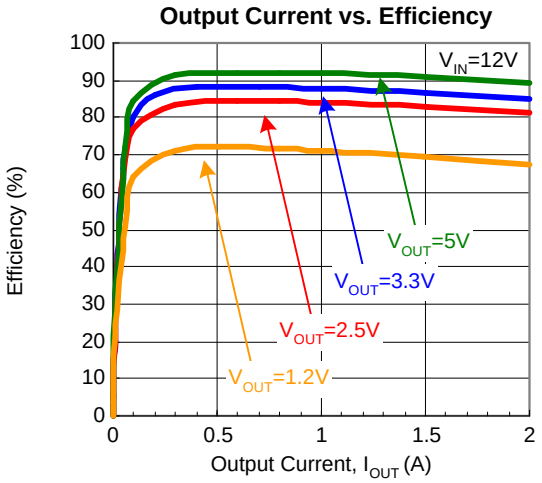
Symbol	Parameter	Test Conditions	APW7172			Unit
			Min.	Typ.	Max.	
CURRENT MODE PWM CONVERTER (CONT.)						
G_{CS}	Switch Current to COMP Voltage Transresistance		-	1.95	-	A/V
PROTECTIONS						
I_{LIM}	High Side Switch Current-Limit	Peak Current	-	3.2	-	A
T_{OTP}	Over-Temperature Trip Point		-	160	-	°C
	Over-Temperature Hysteresis		-	40	-	°C
SOFT-START, ENABLE, AND INPUT CURRENTS						
I_{SS}	Soft-Start Current		-	10	-	µA
	EN Enable Threshold Voltage		0.7	1.1	1.5	V
	EN Under-Voltage Lockout (UVLO) Threshold	V_{EN} rising	2.5	2.6	2.7	V
	EN UVLO Hysteresis		-	200	-	mV
I_{FB}	FB Pin Input Current		-100	-	+100	nA
I_{EN}	EN Pin Pull High Current		-	1	2.5	µA

Typical Operation Characteristic



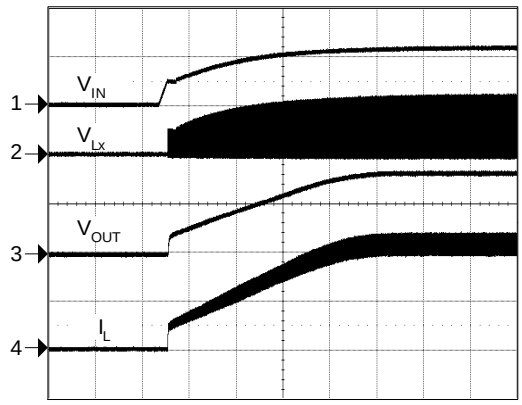






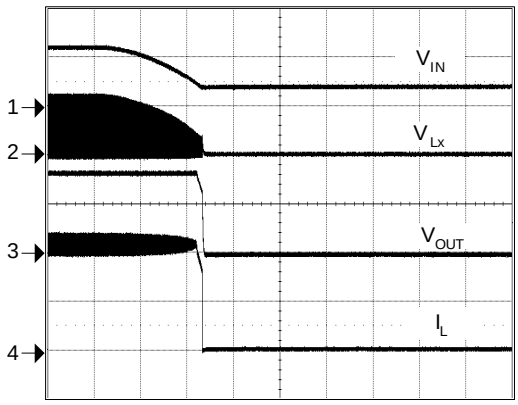
Operation Waveforms

Power On



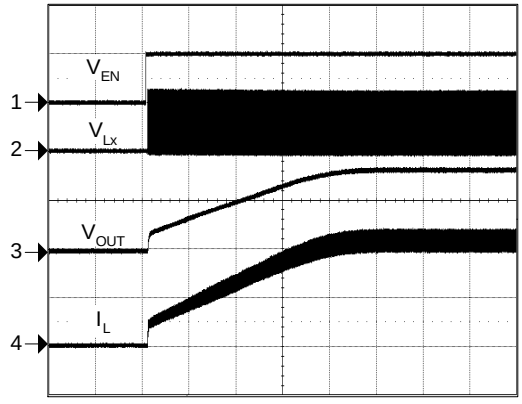
CH1 : V_{IN} , 10V/div
CH2 : V_{LX} , 10V/div
CH3 : V_{OUT} , 2V/div
CH4 : I_L , 1A/div
Time : 2ms/div

Power Off



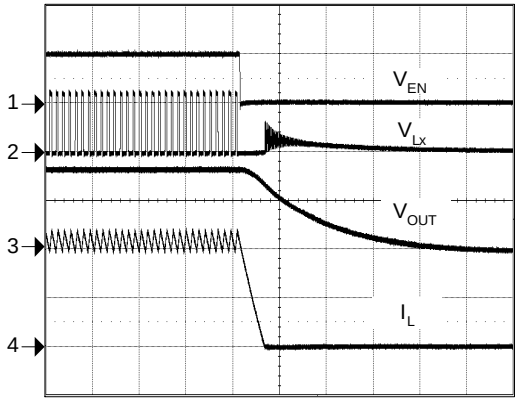
CH1 : V_{IN} , 10V/div
CH2 : V_{LX} , 10V/div
CH3 : V_{OUT} , 2V/div
CH4 : I_L , 1A/div
Time : 2ms/div

Power On with EN Pin



CH1 : V_{EN} , 5V/div
CH2 : V_{LX} , 10V/div
CH3 : V_{OUT} , 2V/div
CH4 : I_L , 1A/div
Time : 2ms/div

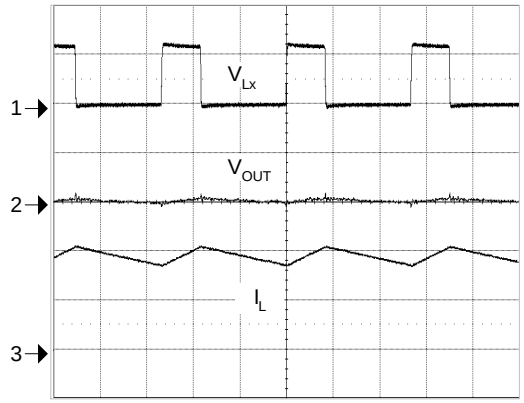
Power Off with EN Pin



CH1 : V_{EN} , 5V/div
CH2 : V_{LX} , 10V/div
CH3 : V_{OUT} , 2V/div
CH4 : I_L , 1A/div
Time : 20µs/div

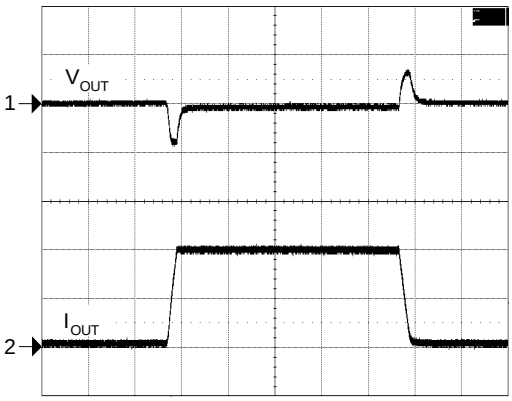
Operation Waveforms (Cont.)

Switching Waveform



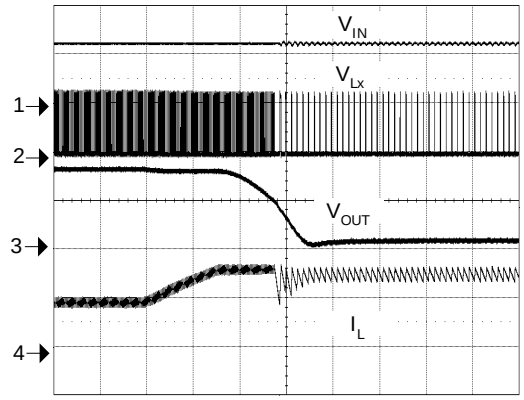
CH1 : V_{LX} , 10V/div
CH2 : V_{OUT} , 20mV/div, DC Offset=3.3V
CH3 : I_L , 1A/div
Time : 1µs/div

Load Transient Response



CH1 : V_{OUT} , 50mV/div, DC Offset=3.3V
CH2 : I_{OUT} , 1A/div
Time : 1ms/div

Short Circuit

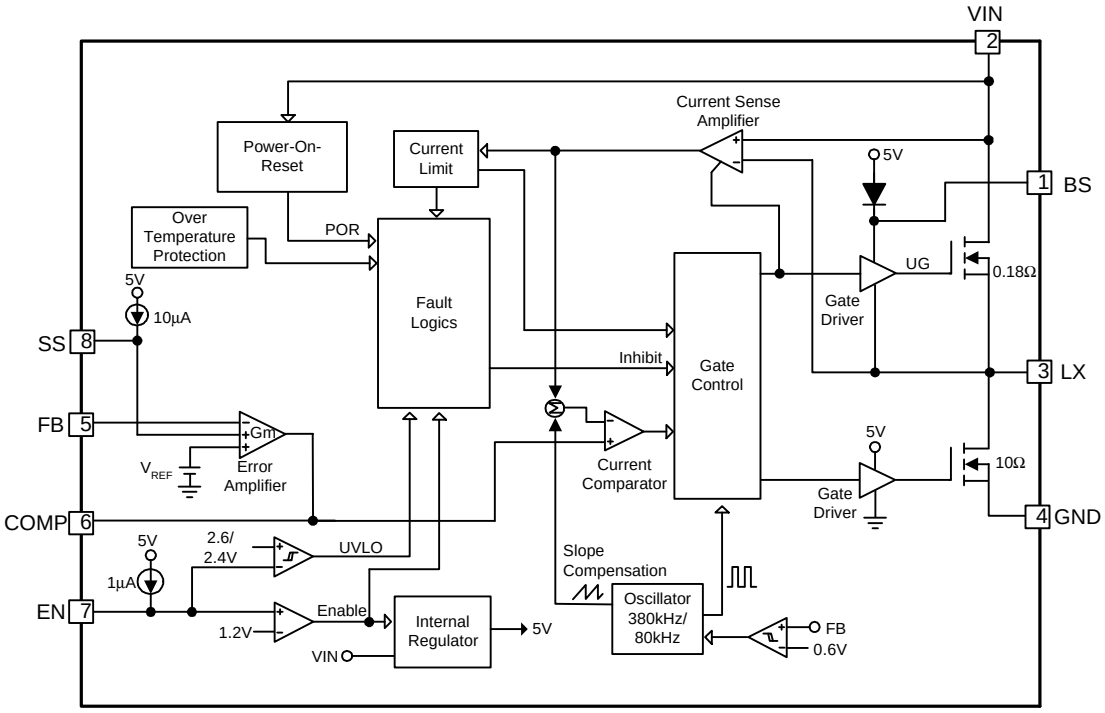


CH1 : V_{IN} , 10V/div
CH2 : V_{LX} , 10V/div
CH3 : V_{OUT} , 2V/div
CH4 : I_L , 2A/div
Time : 100µs/div

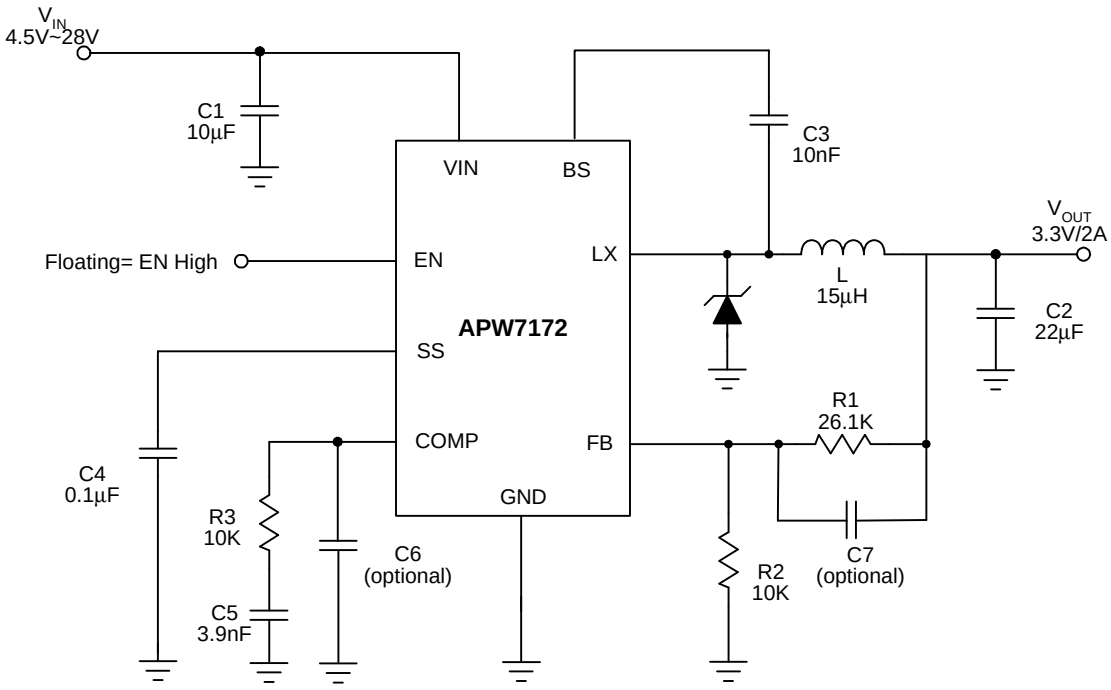
Pin Description

PIN		NAME	FUNCTION
NO.			
SOP-8	MSOP-10P		
1	2	BS	High-Side Gate Driver Supply Voltage Input. BS supplies the voltage to drive the high-side N-channel MOSFET. At least 10nF capacitor should be connected from LX to BS to supply the high-side switch.
2	4	VIN	Power Input. VIN supplies the power (4.5V to 28V) to the control circuitry, gate drivers and step-down converter switch. Connecting a ceramic bypass capacitor and a suitably large capacitor between VIN and GND eliminates switching noise and voltage ripple on the input to the IC.
3	5	LX	Power Switching Output. LX is the Source of the N-Channel power MOSFET to supply power to the output LC filter.
4	6	GND	Power and Signal Ground.
5	7	FB	Output feedback Input. The APW7172 senses the feedback voltage via FB and regulates the voltage at 0.92V. Connecting FB with a resistor-divider from the converter's output sets the output voltage from 0.92V to 19V.
6	8	COMP	Output of the error amplifier. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required for noise decoupling.
7	9	EN	Enable/shutdown function Input. EN is a digital input that turns the regulator on or off. Drive EN higher than 2.9V to turn on the regulator, lower than 0.9V to turn it off. For automatic startup, leave EN unconnected.
8	10	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.
-	1, 3	NC	No Connect
-	11	Exposed Pad	Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.

Block Diagram



Typical Application Circuit



Recommended Feedback Compensation Value

VOUT(V)	L1(µH)	C4(µF)	R1(kΩ)	R2(kΩ)	R3(kΩ)	C5(nF)
1.2	10	22 Ceremic	3	10	5.1	2.2
1.8	10	22 Ceremic	9.53	10	6.2	3.3
2.5	10	22 Ceremic	17.4	10	8.2	2.7
3.3	15	22 Ceremic	26.1	10	10	3.9
5	15	22 Ceremic	44.2	10	13	1.5
12	15	22 Ceremic	120	10	22	1.5

Function Description

Main Control Loop

The APW7172 is a constant frequency current mode switching regulator. During normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and would be turned off when an internal current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier (EAMP). An external resistive divider connected between VOUT and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.92V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

Soft-Start

The APW7172 provides the programmed soft-start function to limit the inrush current. The soft-start time can be programmed by the external capacitor between SS and GND. Typical charge current is 10μA, and the soft-start time is 10ms with 0.1μF capacitor.

Boostrap Capacitor

The APW7172 employs a N-channel power MOSFET which is drived by a high-side gate driver. The gate driver, with a supply voltage inputted between BS and LX pin, needs a bootstrap capacitor to provide large current pulse for turning on the power MOSFET. Thereby, the boostrap capacitor must be connected between BS and LX pin as close as possible. When the LX voltage is pulled low, the capacitor is charged by the current flowing through the internal bootstrap diode and is suppllied by an internal linear regulator. The bootstrap capacitor must in the range of 10nF to 0.1μF for sufficient gate voltage.

Application Information

Setting Output Voltage

The regulated output voltage is determined by:

$$V_{OUT} = 0.92 \times (1 + \frac{R1}{R2}) \quad (V)$$

To prevent stray pickup, please locate resistors R1 and R2 close to APW7172.

Input Capacitor Selection

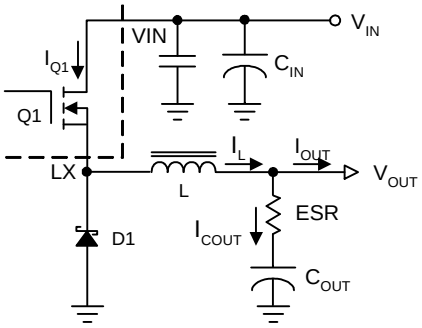
Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time the N-channel power MOSFET (Q1) turns on. Place the small ceramic capacitors physically close to the VIN and between the VIN and GND.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current (I_{RMS}) of the bulk input capacitor is calculated as the following equation:

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1-D)} \quad (A)$$

where D is the duty cycle of the power MOSFET.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.



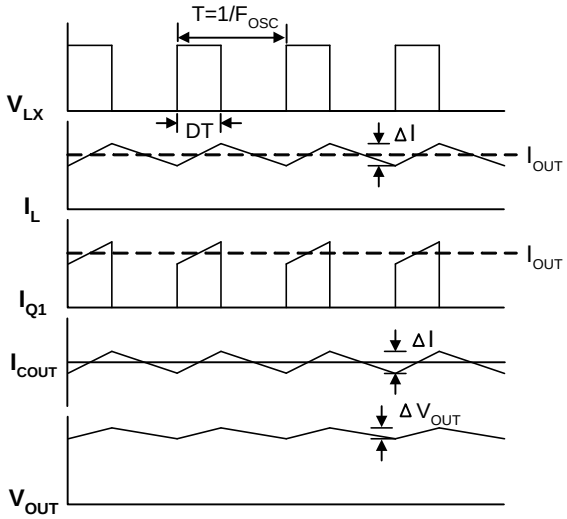


Figure 1. Converter Waveforms

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are the function of the switching frequency and the ripple current (ΔI). The output ripple is the sum of the voltages, having phase shift, across the ESR and the ideal output capacitor. The peak-to-peak voltage of the ESR is calculated as the following equations:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{..... (1)}$$

$$\Delta I = \frac{V_{OUT} \cdot (1-D)}{F_{OSC} \cdot L} \quad \text{..... (2)}$$

$$V_{ESR} = \Delta I \cdot ESR \quad \text{..... (3)}$$

The peak-to-peak voltage of the ideal output capacitor is calculated as the following equation:

$$\Delta V_{COUT} = \frac{\Delta I}{8 \cdot F_{OSC} \cdot C_{OUT}} (V) \quad \text{..... (4)}$$

For the applications using bulk capacitors, the ΔV_{COUT} is much smaller than the V_{ESR} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is shown as below:

$$\Delta V_{OUT} = \Delta I \cdot ESR \quad (V) \quad \text{..... (5)}$$

For the applications using ceramic capacitors, the V_{ESR} is much smaller than the ΔV_{COUT} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is close to ΔV_{COUT}.

Application Information (Cont.)

Output Capacitor Selection (Cont.)

The load transient requirements are the function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Table 1. Capacitor Selection Guide

Vender	Model	Capacitance (μF)	TC	Voltage Rating(V)	Size
Murata	GRM31CR61E106K	10	X5R	25	1206
Murata	GRM31CR61C226K	22	X5R	16	1206

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses. The equation (2) shows that the inductance value has a direct effect on ripple current.

Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I \le 0.4 \times I_{OUT(MAX)}$. Please be noticed that the maximum ripple current occurs at the maximum input voltage. The minimum inductance of the inductor is calculated by using the following equation:

$$\frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{380000 \cdot L \cdot V_{IN}} \le 1.2$$

$$L \ge \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{456000 \cdot V_{IN}} \quad (H) \quad \text{..... (6)}$$

where $V_{IN} = V_{IN(MAX)}$

Table 2. Inductor Selection Guide

Vender	Model	Inductance (μH)	DCR(mΩ)	Current Rating(A)
CYNTEC	PCMB063T-100MS	10	62	4
Gausstek	PL94P051M-15U	15	50	3
Gausstek	PL94P051M-10U	10	38	3.8

Output Diode Selection

The Schottky diode carries load current during the off-time. The average diode current is therefore dependent on the N-channel power MOSFET duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \frac{V_{IN} - V_{OUT}}{V_{IN} - V_D} \cdot I_{OUT}$$

The APW7172 is equipped with whole protections to reduce the power dissipation during short-circuit condition. Therefore, the maximum power dissipation of the diode is calculated from the maximum output current as below:

$$P_{DIODE(MAX)} = V_D \cdot I_{D(MAX)}$$

where $I_{OUT} = I_{OUT(MAX)}$

Remember to keep lead length short and observe proper grounding to avoid ringing and increased dissipation.

Table 3. Diode Selection Guide

Vender	Model	Voltage Rating(V)	Current Rating(A)
ZOWIE	BSCD24H	40	2
ZOWIE	CSCD24H	40	2
ZOWIE	SCD24H	40	2
PANJIT	SK24	40	2

Application Information (Cont.)

Thermal Consideration

The APW7172 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

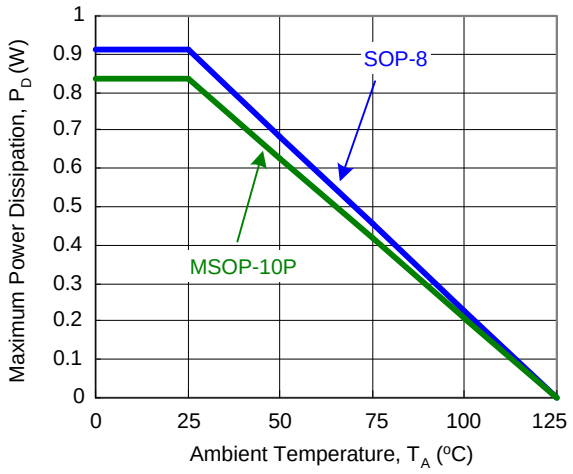
$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. For SOP-8 package, the T_A=25°C and maximum T_J=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)} = (160-25)/110$$
$$= 1.22(W)$$

For normal operation, do not exceed the maximum junction temperature rating of T_J = 125°C. The calculated power dissipation should less than:

$$P_D = (125-25)/110$$
$$= 0.90(W)$$



Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedance should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separating and finally combined using the ground plane construction or single point grounding. Figure 3 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Begin the layout by placing the power components first. Orient the power circuitry to achieve a clean power flow path. If possible, make all the connections on one side of the PCB with wide, copper filled areas.
2. In Figure 3, the loops with same color bold lines conduct high slew rate current. These interconnecting impedances should be minimized by using wide and short printed circuit traces.
3. Keep the sensitive small signal nodes (FB, COMP) away from switching nodes (LX or others) on the PCB and it should be placed near the IC as close as possible. Therefore, place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.
4. Place the decoupling ceramic capacitor C1 near the VIN as close as possible. Use a wide power ground plane to connect the C1, C2, and Schottky diode to provide a low impedance path between the components for large and high slew rate current.

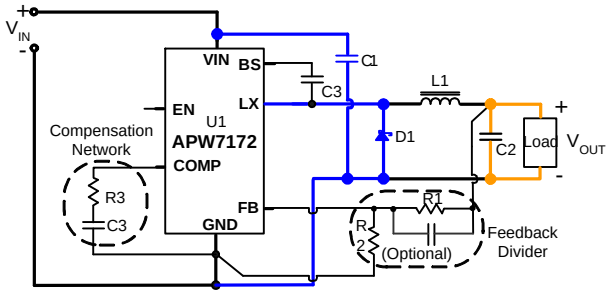


Figure 3. Current Path Diagram

Application Information (Cont.)

Layout Consideration (Cont.)

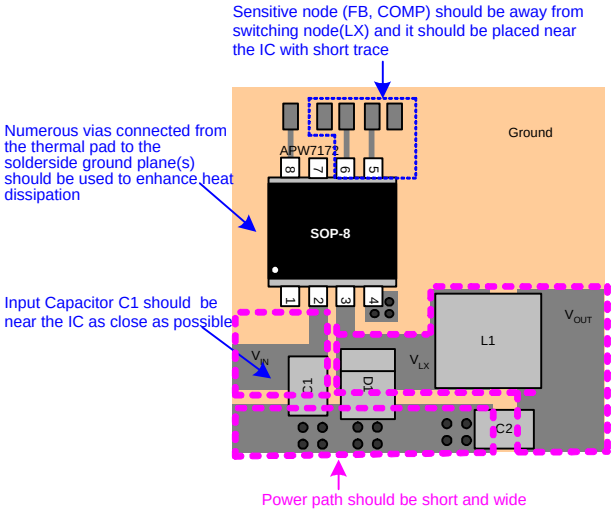
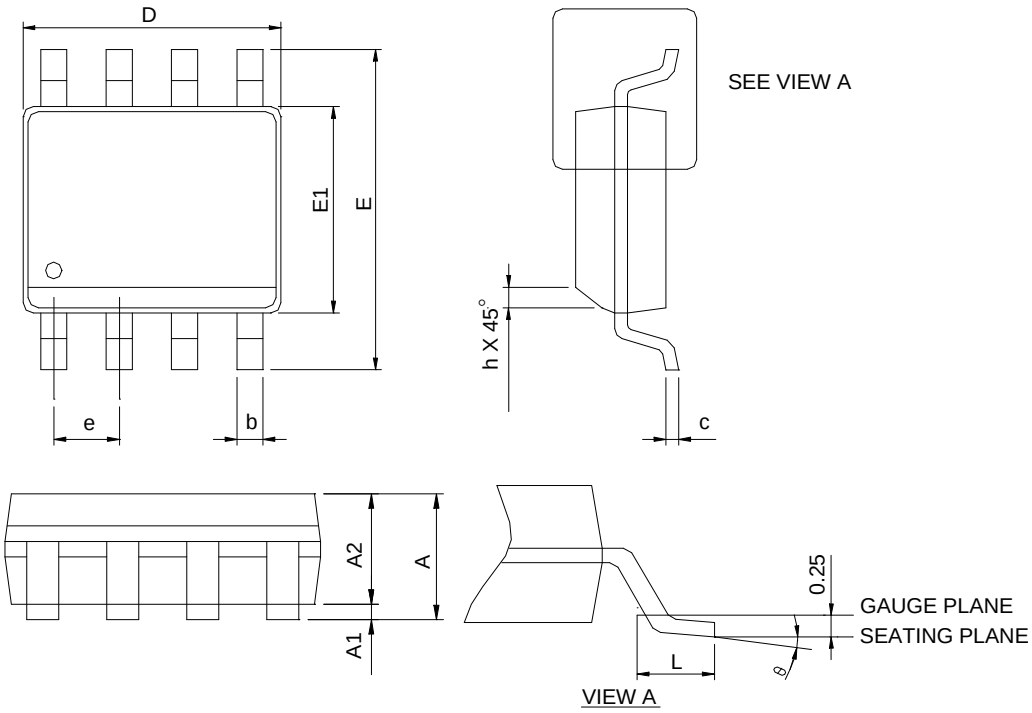


Figure 4. Recommended Layout Diagram

Package Information

SOP-8

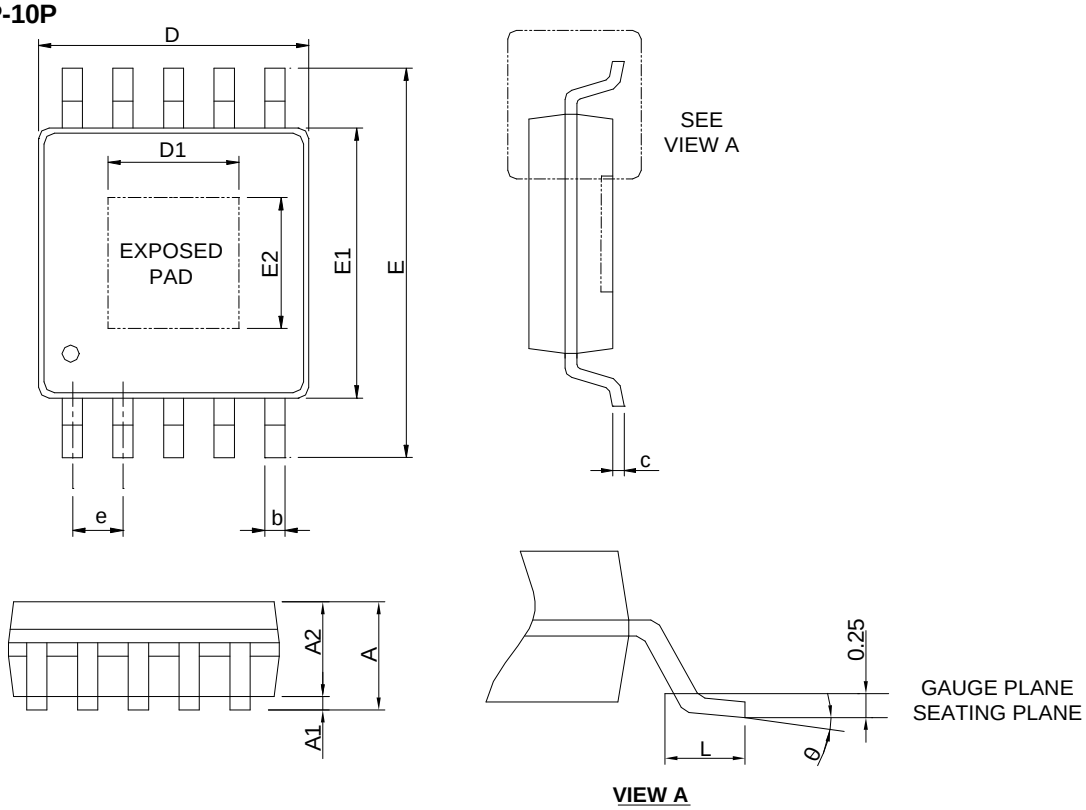


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

MSOP-10P

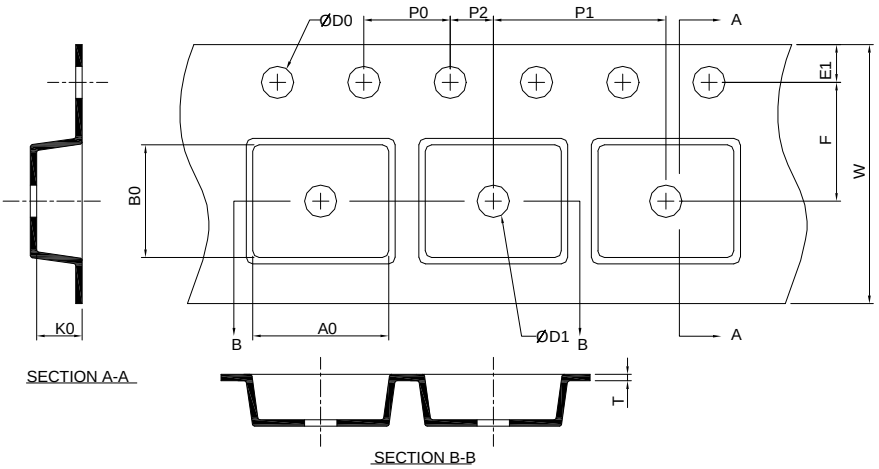


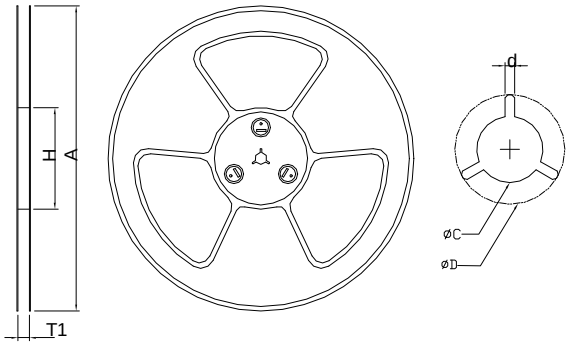
VIEW A

SYMBOL	MSOP-10P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.17	0.33	0.007	0.013
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
D1	1.50	2.50	0.059	0.098
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
E2	1.50	2.50	0.059	0.098
e	0.50 BSC		0.020 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 BA-T.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not flash or protrusions.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 6 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
MSOP-10P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	3.30±0.20	1.40±0.20

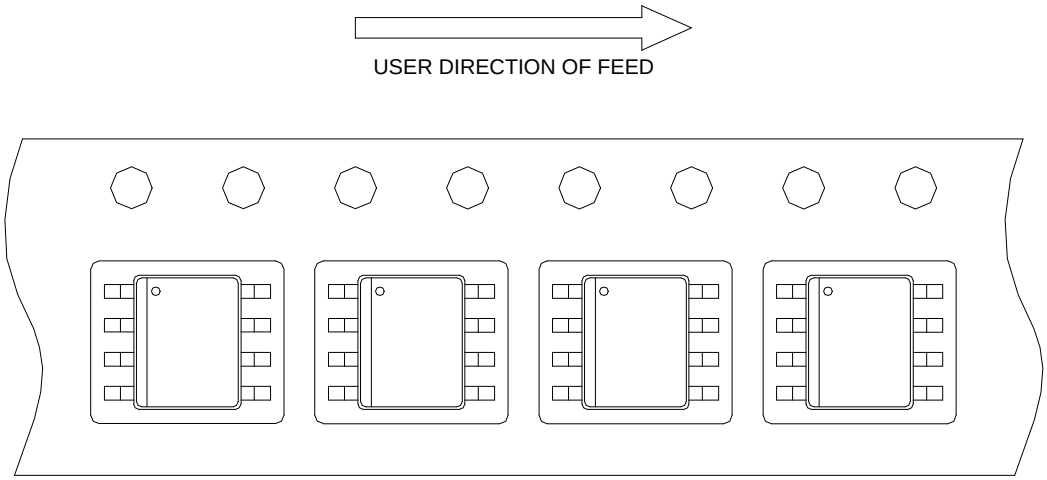
(mm)

Devices Per Unit

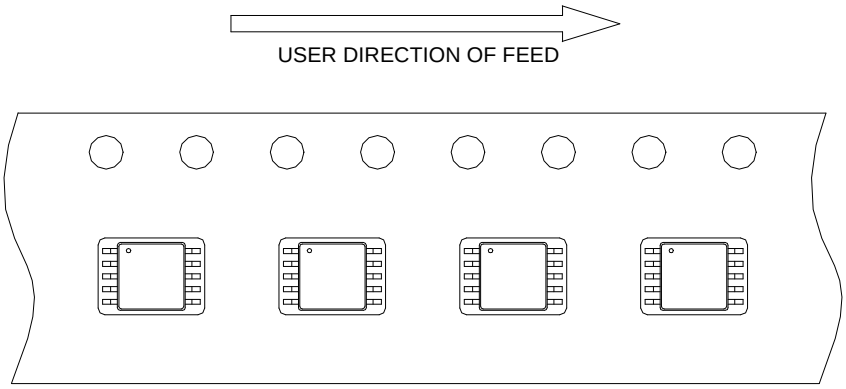
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
MSOP-10P	Tape & Reel	3000

Taping Direction Information

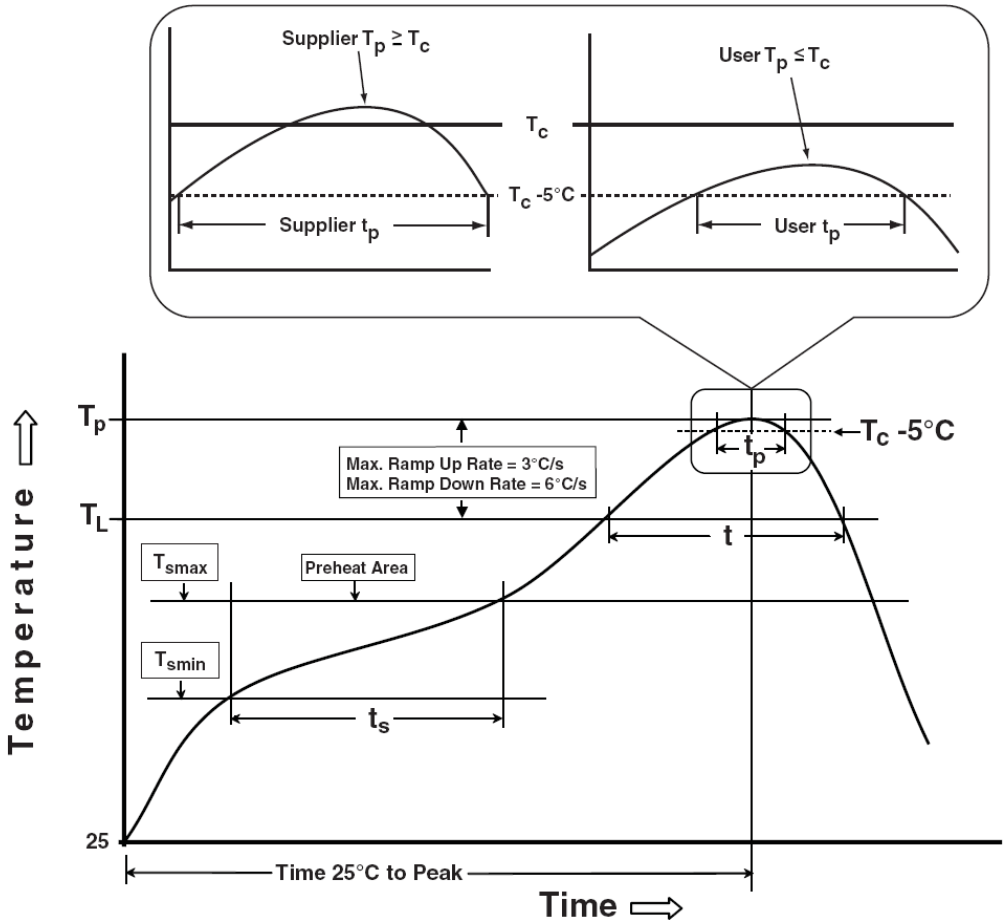
SOP-8



MSOP-10P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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