3MHz Synchronous Switch-Mode Battery Charger with Full USB Compliance and USB-OTG Boost Regulator

Features

- Charge Faster Than Linear Charger
- 3MHz with Wide Duty Cycle Synchronous Switch-Mode Charger with 1.5A Integrated N-MOSFETs
- 4V-6V Input Operating Range
- 20V Absolute Maximum Input Voltage
- Safety
  - -Reverse leakage protection to prevent battery drainage
  - -Thermal regulation and protection
  - -Input/output over-voltage protection
  - -Cycle-by-cycle current limit
- Accuracy
  - -±1% charge voltage regulation (0 to 85°C)
  - -±5% charge current regulation
  - -±5% input current regulation (100mA and 500mA)
- Built-In Input Current Sensing and Limiting
- Automatic Charging
- Programmable Through High-Speed I²C Interface (3.4Mb/s)
  - -Input Current Limit
  - -Fast-Charge and Termination Current
  - -Charge Regulation Voltage
  - -VIN DPM Threshold
  - -Termination Enable/Disable
  - -OTG Enable/Disable
  - -Reset All Parameter Control
  - -Safety Timer with Reset Control
- 5V, 500mA Boost Mode for USB OTG for 2.5V to 4.5V Battery Input
- Available in 1.73mmx2.0mm WLCSP-20 Package

General Description

The APW7261 combine switch-mode battery charger and a boost regulator with fixed 3MHz switching frequency, which drives two integrated N-channel power MOSFETs. In battery charging, the high-efficiency step-down DC/DC converter is capable of delivering 1.5A output current over a wide input voltage range from 4V to 6V for APW7261, the step-down DC/DC converter is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery. The Charging parameters and operating modes can be programmed through an I²C interface. The APW7261 has high accuracy regulation of input current, charge current and charge voltage. It equipped with charge termination, and charge status monitoring for battery detection.

The APW7261 charge the battery in three phases: conditioning, constant current and constant voltage. The APW7261 features Dynamic Power Management (DPM) mode to accomplish input power limiting. The input current is limited to the value set by the I²C host. This feature reduces battery charge current when the input power limit is reached to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. The charge termination is based on battery voltage, a programmed minimum current level and charge current termination bit set by the I²C host.

If the battery voltage falls below an internal threshold, the APW7261 automatically restarts the charge cycle, and when the input voltage falls below the battery voltage, it will enter a low-quiescent current sleep mode. The APW7261 supports the thermal regulation and over temperature protection to maintain the junction temperature of 120°C by reducing charge current.

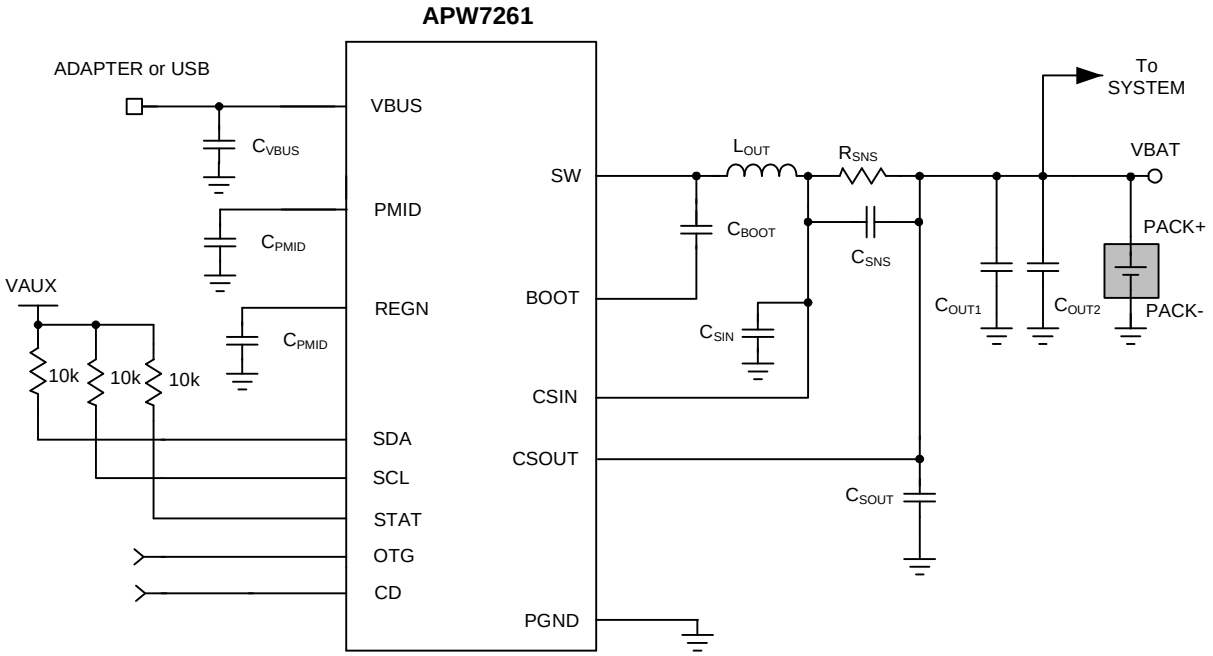
The APW7261 can operate as a boost regulator. To support USB OTG device, APW7261 can provide VBUS (5.05V) by boosting the battery voltage.

The APW7261 is available in1.73mmx2.0mm WLCSP-20 package.

Applications

- **Cell Phones, Smart Phones and PDAs**
- **Tablet PC**
- **Portable Media Players, Handheld Device**

Simplified Application Circuit



Ordering and Marking Information

APW7261 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

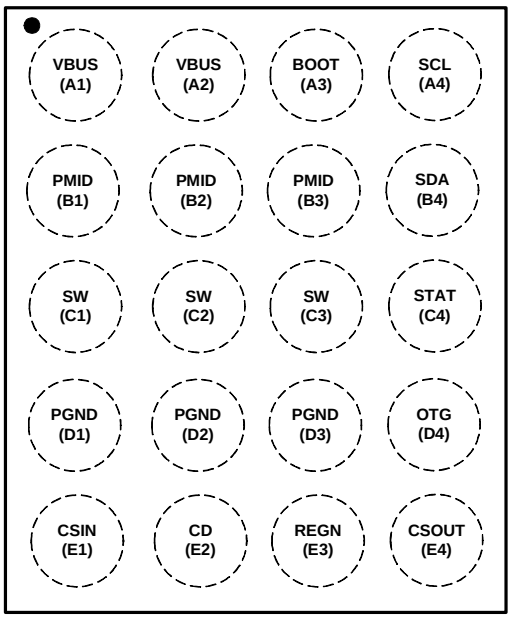
Package Code
HA : WLCSP1.73x2.0-20
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW7261HA: 7261 • X X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration

APW7261 Top View



1.73X2.0mm 20-pin WLCSP-20

Absolute Maximum Ratings (Note 1,2)

Symbol	Parameter	Rating	Unit
$V_{I/O}$	VBUS, PMID and STAT to PGND Voltage	-0.3 to 20	V
	BOOT and SW to PGND Voltage	-0.3 to 20	V
	SCL, SDA, OTG, REGN, CSIN, CSOUT and CD to PGND Voltage	-0.3 to 7	V
V_{BOOT}	BOOT Supply Voltage (BOOT to SW)	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics (Note 3)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	85	°C/W
θ_{JC}	Junction-to-Case Resistance in free air	25	°C/W

Note 3: θ_{JA} is measured with the component mounted on a high effective the thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{BUS}	Supply Voltage (VBUS to GND)	4 to 6	V
V_{OUT}	Converter Output Voltage	3.5 to 4.44	V
I_{OUT}	Output Current (R_{SNS}=68mΩ)	0.55~1.55	A
T_A	Ambient Temperature	-40 to 85	°C
T_J	Junction Temperature	-40 to 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{BUS}=5V, CD=0, HZ_MODE=0, OPA_MODE=0 and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7261			Unit
			Min	Typ	Max	
INPUT CURRENT						
I_{VBUS}	VBUS supply current control	V_{BUS} > $V_{BUS(min)}$, PWM switching	-	10	-	mA
		V_{BUS} > $V_{BUS(min)}$, PWM no switching	-	-	5	mA
		0°C < T_J < 85°C, CD=1 or HZ_MODE=1	-	140	260	µA
I_{LKG}	Leakage current from battery to VBUS pin	0°C < T_J < 85°C, V_{CSOUT}=4.2V, High Impedance Mode, V_{BUS}=0V	-	0.2	5	µA
	Battery discharge current in High Impedance Mode, (CSIN, CSOUT, SW pins)	0°C < T_J < 85°C, V_{CSOUT}=4.2V, High Impedance Mode, SCL, SDA, OTG=0V or 1.8V	-	23	50	µA
VOLTAGE REGULATION						
V_{OREG}	Output Regulation voltage programmable range	Operating in voltage regulation	3.5	-	4.44	V
	Voltage regulation accuracy	T_A = 25°C	-0.5	-	0.5	%
		T_A = -40 ~ 85°C	-1	-	1	
CURRENT REGULATION (FAST CHARGE)						
$I_{O(CHARGE)}$	Output charge current programmable range	V_{LOWV}≦V_{CSOUT}<V_{OREG}, V_{BUS}>V_{SLP}, R_{SNS}=68mΩ, LOW_CHG=0	550	-	1500	mA
	Low charge current	V_{LOWV}≦V_{CSOUT}<V_{OREG}, V_{BUS}>V_{SLP}, R_{SNS}=68mΩ, LOW_CHG=1	-	325	350	mA
	Charge Current Accuracy Across R_{SNS}	20mV < V_{IREG} < 40mV	-8	-	2	%
		40mV < V_{IREG}	-6	-	0	%
	Regulation accuracy of the voltage across R_{SNS} (for charge current regulation) V_{IREG} = $I_{O(CHARGE)}$ x R_{SNS}	37.4mV≦V_{IREG}<44.2mV	-3.5	-	3.5	%
		44.2mV≦V_{IREG}	-3	-	3	
LOW BATTERY DETECTION						
V_{LOWV}	Low battery voltage threshold		-	-	3.7	V

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{BUS}=5V, CD=0, HZ_MODE=0, OPA_MODE=0 and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APW7261			Unit
				Min	Typ	Max	
CD and OTG PIN LOGIC LEVEL							
V_{IL}	Input low threshold level			-	-	0.4	V
V_{IH}	Input high threshold level			1.5	-	-	V
I_{bias}	Input bias current	Voltage on control pin is 5V		-	-	1	µA
CHARGE TERMINATION DETECTION							
I_{TERM}	Termination charge current programmable range	V_{CSOUT}>V_{OREG}-V_{REGH}, V_{BUS}>V_{SLP}, R_{SNS}=68mΩ		50	-	400	mA
	Deglitch time for charge termination	Both rising and falling, 2mV overdrive, t_{RISE}, t_{FALL}=100ns		-	30	-	ms
	Regulation accuracy for termination current across RSNS V_{IREG_TERM}=I_{OTERM} x R_{SNS}	3.4mV≦ V_{IREG_TERM}≦6.8mV		-25	-	25	%
		6.8mV≦ V_{IREG_TERM}≦17mV		-25	-	25	
		17mV≦ V_{IREG_TERM}≦27.2mV		-5	-	5	
INPUT BASED DYNAMIC POWER MANAGEMENT							
V_{IN_DPM}	Input voltage DPM threshold programmable range			4.2	-	4.76	V
	VIN DPM threshold accuracy			-3	-	3	%
INPUT CURRENT LIMIT							
I_{IN_LIMIT}	Input current limiting threshold	I_{IN}=100mA	T_A=25°C	88	93	98	mA
		I_{IN}=500mA	T_A=25°C	450	475	500	
VREF BIAS REGULATOR							
V_{REGN}	Input bias regulator voltage	V_{BUS}>$V_{IN(min)}$ or V_{CSOUT}>$V_{BUS(min)}$, I_{REGN}=1mA, C_{REGN}=1µF		-	-	6.5	V
	V_{REGN} output short current limit			-	30	-	mA
BATTERY RECHARGE THRESHOLD							
V_{RCH}	Recharge threshold voltage	Below V_{OREG}		-	120	-	mV
	Deglitch time	V_{CSOUT} decreasing below threshold, t_{FALL}=100ns, 10mV overdrive		-	130	-	ms
STAT OUTPUT							
$V_{OL(STAT)}$	Low-level output saturation voltage, STAT pin	I_O=10mA, sink current		-	-	0.55	V
	High-level leakage current for STAT	Voltage on STAT pin is 5V		-	-	1	µA
I^2C BUS LOGIC LEVELS AND TIMING CHARACTERISTIC							
V_{OL}	Output low threshold level	I_O=10mA, sink current		-	-	0.4	V
V_{IL}	Input low threshold level	V_{PULL_UP}=1.8V, SDA and SCL		-		0.4	V
V_{IH}	Input high threshold level	V_{PULL_UP}=1.8V, SDA and SCL		1.2	-	-	V
I_{BIAS}	Input bias current	V_{PULL_UP}=1.8V, SDA and SCL		-	-	1	µA
f_{SCL}	SCL clock frequency	V_{PULL_UP}=1.8V, SDA and SCL		-	-	3.4	MHz

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{BUS}=5V, CD=0, HZ_MODE=0, OPA_MODE=0 and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7261			Unit
			Min	Typ	Max	
BATTERY DETECTION (In Termination)						
I_{DETECT}	Battery detection current before charge done (sink current)	Begins after termination detected, $V_{CSOUT} \leqq V_{OREG}$	-	-0.8	-	mA
t_{DETECT}	Battery detection time		-	262	-	ms
SLEEP COMPARATOR						
V_{SLP}	SLEEP mode entry threshold, V_{BUS}-V_{CSOUT}	2.3V $\leqq V_{CSOUT} \leqq V_{OREG}$, V_{BUS} falling	0	40	100	mV
V_{SLP_EXIT}	Sleep mode exit hysteresis	2.3V $\leqq V_{CSOUT} \leqq V_{OREG}$	140	200	260	mV
	Deglitch time for V_{BUS} rising above V_{SLP}+V_{SLP_EXIT}	Rising voltage, 2mV overdrive, t_{RISE}=100ns	-	30	-	ms
UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO	IC active threshold voltage	V_{BUS} rising, Exit UVLO	3.6	3.8	4	V
UVLO_HYS	IC active hysteresis	V_{BUS} falling below UVLO, Enter UVLO	-	150	-	mV
PWM						
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT}=500mA, Measured from VBUS to PMID	-	90	135	mΩ
	Internal top N-Channel Switching MOSFET on-resistance	Measured from PMID to SW, V_{BOOT}-V_{SW}=4V	-	130	225	
	Internal bottom N-Channel MOSFET on-resistance	Measured from SW to PGND	-	120	180	
f_{OSC}	Oscillator frequency		2.7	3	3.3	MHz
CHARGE MODE PROTECTION						
$V_{OVP\_IN\_USB}$	Input VBUS OVP threshold voltage	V_{BUS} threshold to turn off converter during charge $V_{OVP\_IN\_USB}$	6.3	6.5	6.7	V
	$V_{OVP\_IN\_USB}$ hysteresis	VBUS falling from above $V_{OVP\_IN\_USB}$	-	170	-	mV
V_{OVP}	Output OVP threshold voltage	V_{CSOUT} threshold over V_{OREG} to turn off charger during charge	110	117	121	%
	V_{OVP} hysteresis	Lower limit for V_{CSOUT} falling from above V_{OVP}	-	11	-	%
I_{ILIMIT}	Cycle-by-cycle current limit for charge	Charge mode operation	3	4	5	A
V_{SHORT}	Trickle to fast charge threshold	V_{CSOUT} rising	1.9	2.1	2.3	V
	V_{SHORT} hysteresis	V_{CSOUT} falling below V_{SHORT}	-	100	-	mV

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{BUS}=5V, CD=0, HZ_MODE=0, OPA_MODE=0 and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7261			Unit
			Min	Typ	Max	
CHARGE MODE PROTECTION						
I_{SHORT}	Trickle charge charging current	$V_{CSOUT} \leqq V_{SHORT}$	25	35	45	mA
BOOST MODE OPERATION FOR VBUS (OPA_MODE=1, HZ_MODE=0)						
V_{BUS_B}	Boost output voltage (to VBUS pin)	2.5V<V_{CSOUT}<4.5V	4.9	5.05	5.2	V
	Boost output voltage accuracy	Including line and load regulation	-3	-	3	%
I_{BO}	Maximum output current for boost	V_{BUS_B}=5.05V, 2.5V<V_{CSOUT}<4.5V	500	-	-	mA
I_{BLIMIT}	Cycle by cycle current	V_{BUS_B}=5.05V, 2.5V<V_{CSOUT}<4.5V	-	1.59	-	A
V_{BUSOVP}	Overvoltage protection threshold fo boost (VBUS pin)	Threshold over VBUS to turn off converter during boost	5.8	6	6.2	V
	V_{BUSOVP} hysteresis	V_{BUS} falling from above V_{BUSOVP}	-	162	-	mV
V_{BATMAX}	Maximum battery voltage for boost (CSOUT pin)	V_{CSOUT} rising edge during boost	4.75	4.9	5.05	V
	V_{BATMAX} hysteresis	V_{CSOUT} falling from above V_{BATMAX}	-	200	-	mV
V_{BATMIN}	Minimum battery voltage for boost (CSOUT pin)	During boosting	-	2.5	-	V
		Before boost starts	-	2.9	3.2	V
	Boost output resistance at high-impedance mode (From VBUS to PGND)	CD=1 or HZ_MODE=1	220	-	-	kΩ
PROTECTION						
$T_{SHUTDOWN}$	Thermal trip		-	150	-	°C
	Thermal hysteresis		-	25	-	
T_{CF}	Thermal regulation threshold	Charge current begins to reduce	-	120	-	
t_{40M}	40 minute timer	40 minute mode	35	40	45	Min

I²C Serial Control Port Operation

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	APW7261			Unit
			Min.	Typ.	Max.	
f_{SCL}	Frequency, SCL	No Wait States	-	-	400	kHz
$t_{W(H)}$	Pulse Duration, SCL High		0.6	-	-	µs
$t_{W(L)}$	Pulse Duration, SCL Low		1.3	-	-	
t_r	Rise Time, SCL and SDA		-	-	300	ns
t_f	Fall Time, SCL and SDA		-	-	300	ns
t_{setup1}	Setup Time, SCL to SDA		100	-	-	ns
t_{hold1}	Hold Time, SCL to SDA		0	-	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition		1.3	-	-	µs
t_{setup2}	Setup Time, SCL to Start Condition		0.6	-	-	
t_{hold2}	Hold Time, Start condition to SCL		0.6	-	-	
t_{setup3}	Setup Time, SCL to Stop Condition		0.6	-	-	
C_L	Load Capacitance for Each Bus Line		-	-	400	pF

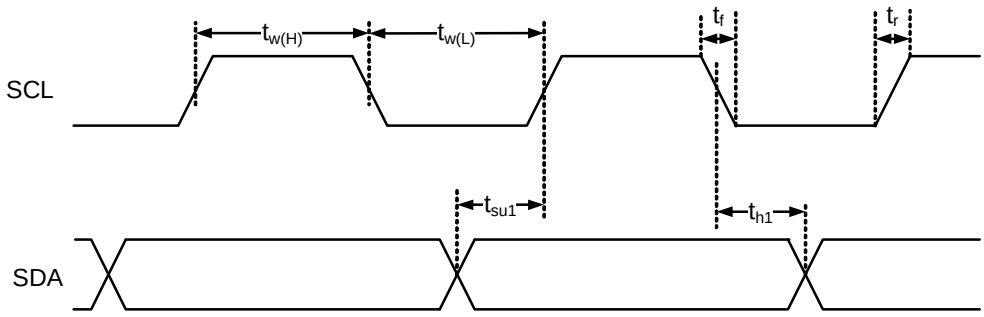


Figure1. SCL and SDA Timing

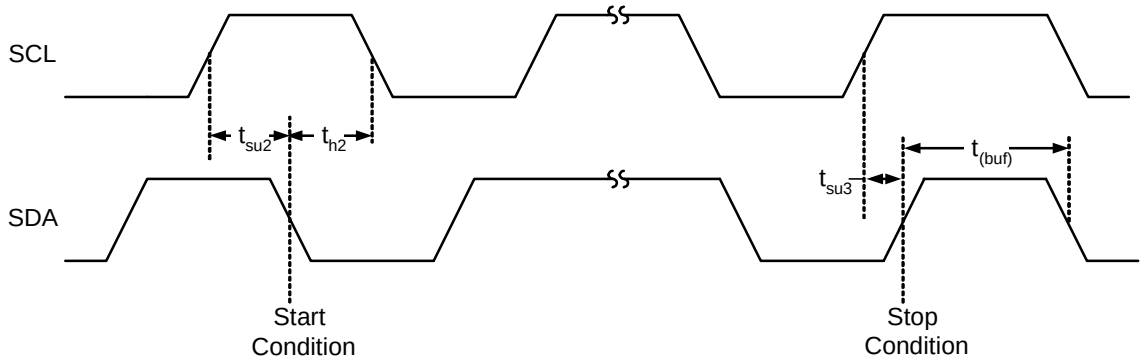


Figure 2. Start and Stop Conditions Timing

Reset Timing

Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to “Recommended Use Model” section on usage of all terminals.

Symbol	Parameter	Test Conditions	APW7261			Unit
			Min.	Typ.	Max.	
$t_{p(RST)}$	Pulse Duration, RESET Active.	No Load	100	-	-	µs
$t_{d(I2C\_Ready)}$	Time to Enable I^2C		-	-	13.5	ms

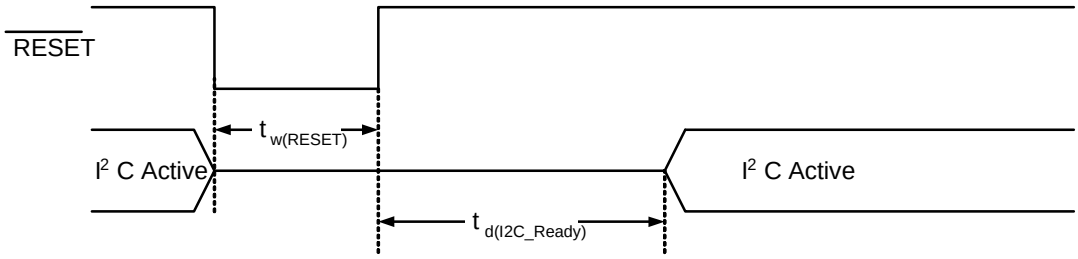


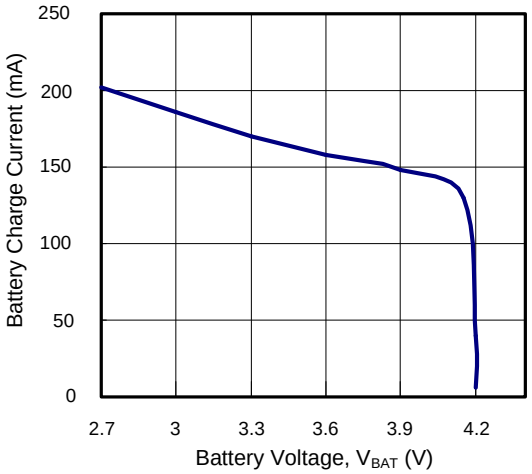
Figure 3. Reset Timing

Pin Description

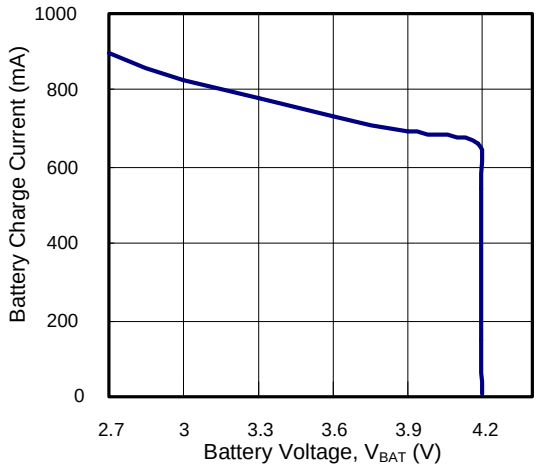
PIN	NAME	Description
A1, A2	VBUS	Charge Input Voltage.
A3	BOOT	Supply Input for the Internal high-side gate driver and an internal level-shift circuit. Connect to an external ceramic capacitor and internal diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
A4	SCL	I^2C Interface Clock. This pin should not be left floating.
B1, B2, B3	PMID	Converter Input Voltage. Connect at least 4.7µF ceramic capacitor from PVCC to PGND and place it as close as possible to IC.
B4	SDA	I^2C Interface Data. This pin should not be left floating.
C1, C2, C3	SW	Junction point of the Internal high-side MOSFET Source, output filter inductor and internal the low-side MOSFET Drain. Connect the 0.01µF bootstrap capacitor from SW to BOOT.
C4	STAT	STAT is an open drain output used to indicate the status of the various charger operations. Low when charge in progress. STAT can be used to drive a LED or communicate with a host processor.
D1, D2, D3	PGND	Power ground. Ground connection for high current power converter node. This pin is used as sink for internal low-side gate drivers.
D4	OTG	Boost Mode Enable Control Pin. When OTG actives, the device operates in boost mode.
E1	CSIN	Positive Input of current sensing Amplifier for charge terminal. A 0.1µF ceramic capacitor is placed from CSIN to CSOUT to provide differential-mode filtering. An optional 0.1µF ceramic capacitor is placed from CSIN pin to PGND for common-mode filtering.
E2	CD	Charge Disable. CD=Low, charge is enabled, CD=High, charge is disabled.
E3	REGN	Supply Voltage. This pin provides bias supply, low-side gate drivers and the bootstrap circuit for high-side drivers. Ensure that this pin is bypassed by a 1µF ceramic capacitor next to the pin.
E4	CSOUT	Battery Output and Negative Input of current sensing Amplifier for charge terminal. A 0.1µF ceramic capacitor is placed from CSOUT to CSIN to provide differential-mode filtering. An optional 0.1µF ceramic capacitor is placed from CSOUT pin to PGND for common-mode filtering.

Typical Operating Characteristics

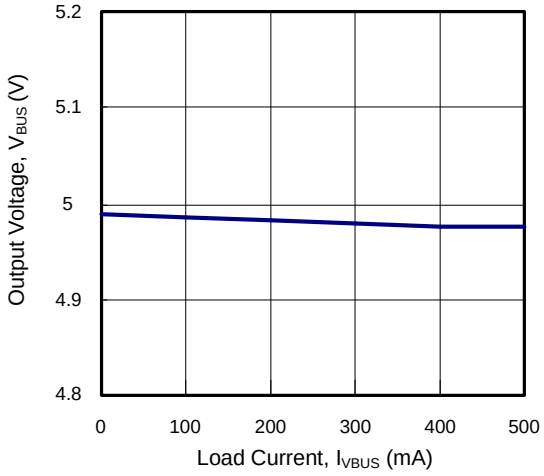
Battery Charge Current vs. V_{BAT}, V_{OREG}=4.2V, I_{IN_LIMIT}=100mA



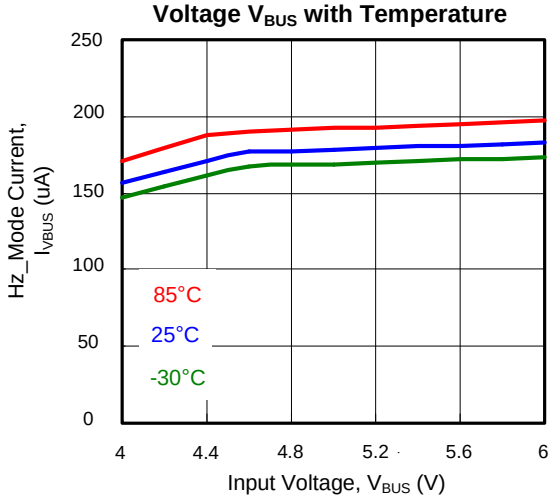
Battery Charge Current vs. V_{BAT}, V_{OREG}=4.2V, I_{IN_LIMIT}=500mA



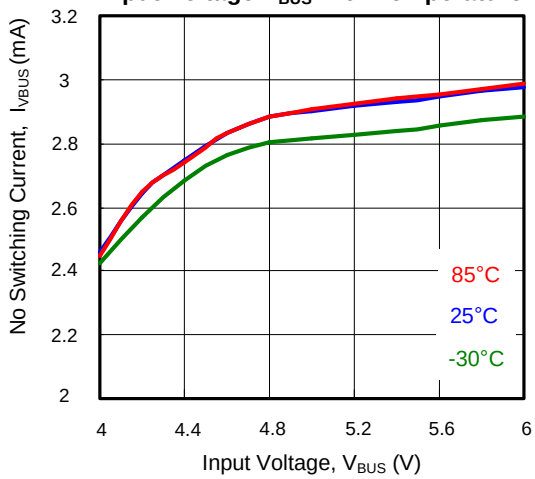
OTG, Load Regulation, V_{BUS} vs. I_{VBUS}



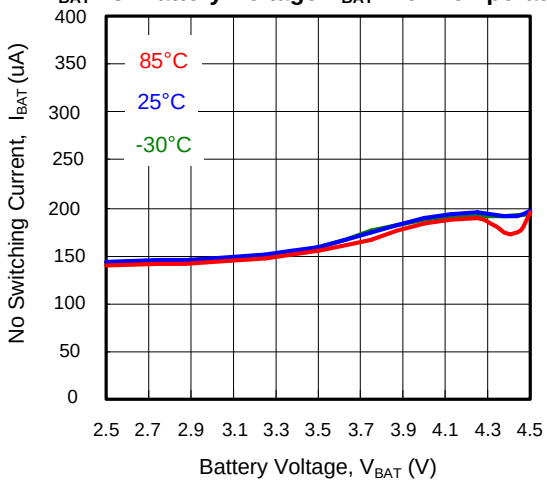
HZ_Mode Current I_{VBUS} vs. Input Voltage V_{BUS} with Temperature



No Switching Quiescent I_{VBUS} vs. Input Voltage V_{BUS} with Temperature

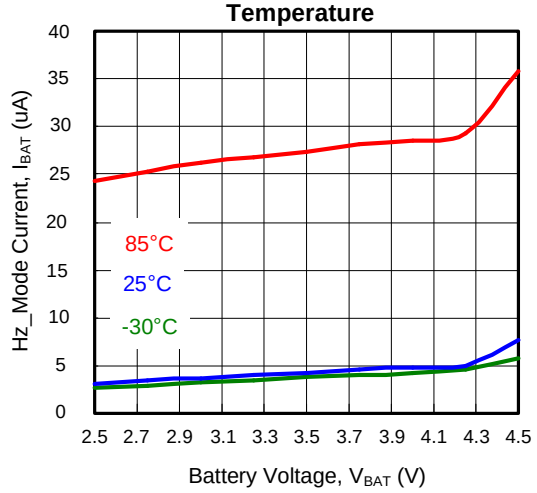


Boost Mode, No Switching Quiescent Current I_{BAT} vs. Battery Voltage V_{BAT} with Temperature



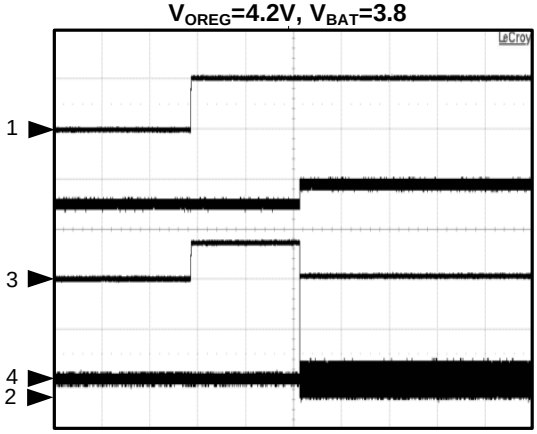
Typical Operating Characteristics

Boost Mode, Quiescent Current I_{BAT} vs. Battery Voltage V_{BAT} in HZ_Mode with Temperature



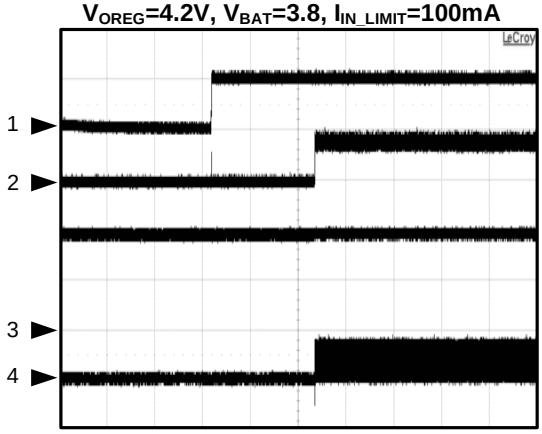
Operating Waveforms

Charge Mode start-up V_{BUS}, V_{OREG}=4.2V, V_{BAT}=3.8



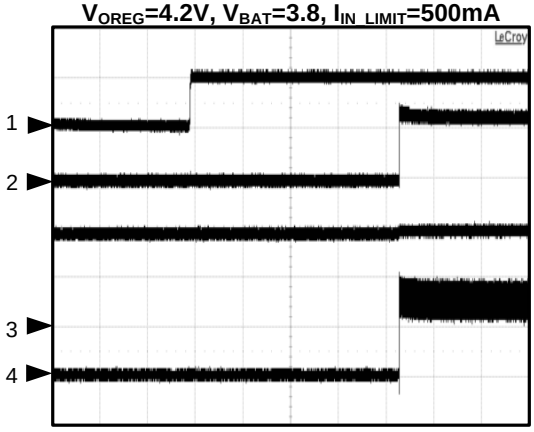
CH1: V_{BUS} (5V/div)
CH2: V_{BAT} (1V/div)
CH3: V_{STAT} (5V/div)
CH4: I_{BAT} (500mA/div)
Time: 1s/div

Charge Mode start-up V_{BUS}, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=100mA



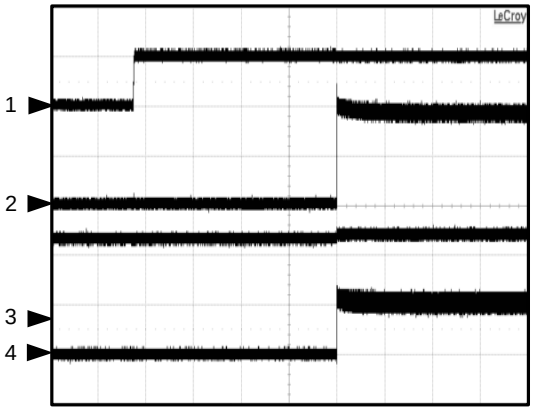
CH1: V_{BUS} (5V/div)
CH2: I_{VBUS} (200mA/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (500mA/div)
Time: 1s/div

Charge Mode start-up V_{BUS}, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=500mA



CH1: V_{BUS} (5V/div)
CH2: I_{VBUS} (500mA/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (500mA/div)
Time: 500ms/div

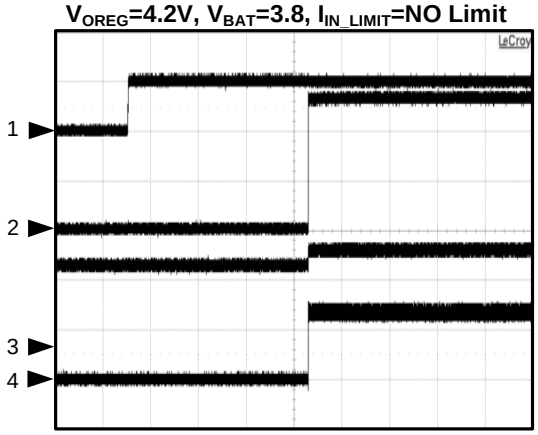
Charge Mode start-up V_{BUS}, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=800mA



CH1: V_{BUS} (5V/div)
CH2: I_{VBUS} (500mA/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 500ms/div

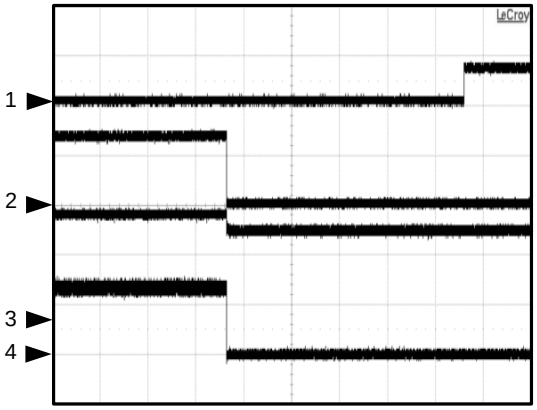
Operating Waveforms

Charge Mode start-up V_{BUS}, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit



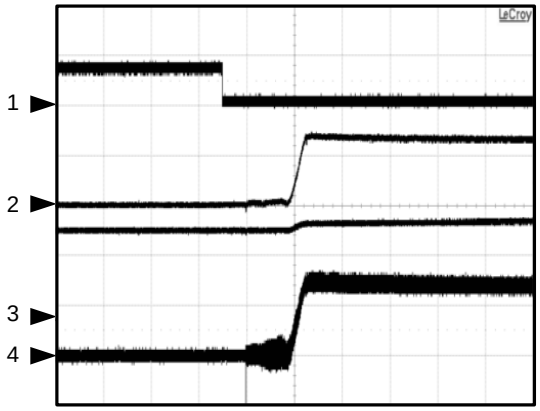
CH1: V_{BUS} (5V/div)
CH2: I_{VBUS} (500mA/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 500ms/div

Charge Shutdown with HZ_MODE Bit Set, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit



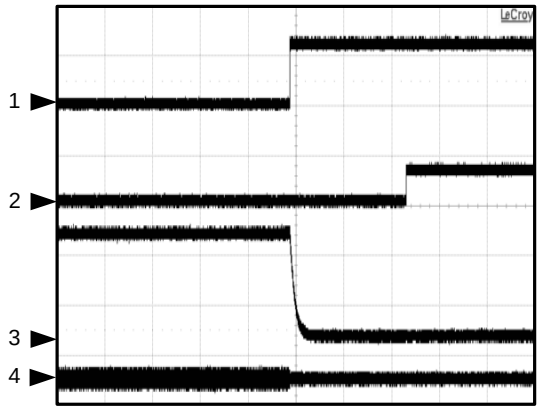
CH1: V_{STAT} (5V/div)
CH2: I_{VBUS} (1A/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 100ms/div

Charge Start-up with HZ _MODE Bit Reset, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit



CH1: V_{STAT} (5V/div)
CH2: I_{VBUS} (1A/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 200µs/div

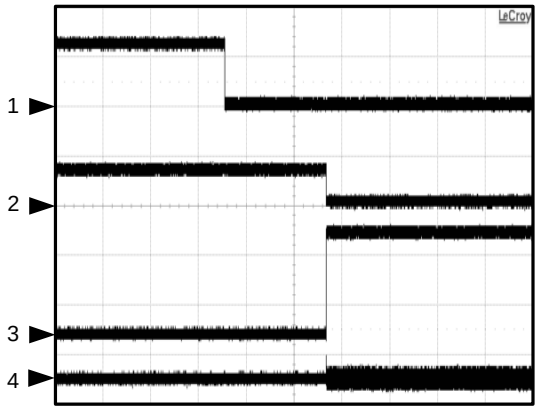
Charge Shutdown with CD Pin Pulled High, V_{OREG}=4.2V, V_{BAT}=Float, I_{IN_LIMIT}=NO Limit



CH1: V_{CD} (2V/div)
CH2: V_{STAT} (5V/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 100ms/div

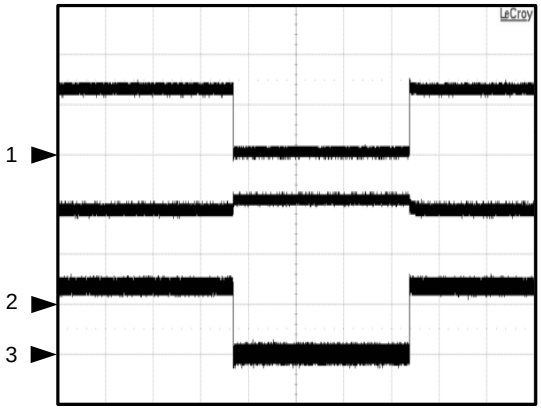
Operating Waveforms

Charge Start-up with CD Pin Pulled Low, V_{OREG}=4.2V, V_{BAT}=Float, I_{IN_LIMIT}=NO Limit



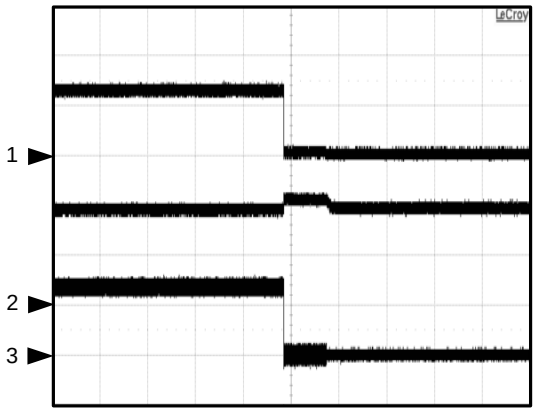
CH1: V_{CD} (2V/div)
CH2: V_{STAT} (5V/div)
CH3: V_{BAT} (2V/div)
CH4: IL (1A/div)
Time: 1s/div

Battery Remove/Insertion during Charging, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit, TE=0



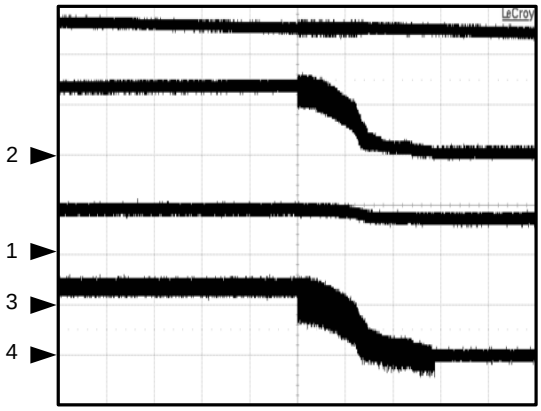
CH1: I_{VBUS} (1A/div)
CH2: V_{BAT} (2V/div)
CH3: I_L (1A/div)
Time: 50ms/div

Battery Remove during Charging, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit, TE=1



CH1: I_{VBUS} (1A/div)
CH2: V_{BAT} (2V/div)
CH3: I_L (1A/div)
Time: 500ms/div

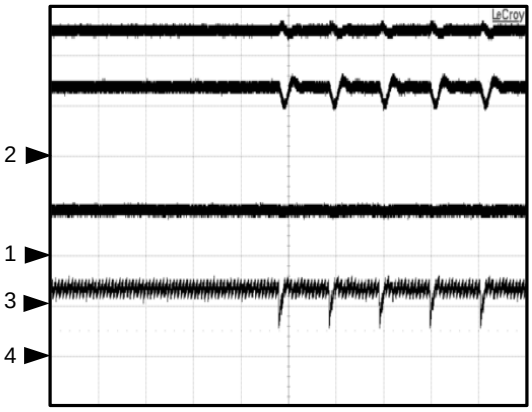
DPM, V_{SP}=4.533V, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit, TE=1



CH1: V_{BUS} (1V/div)
CH2: I_{VBUS} (1A/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 5ms/div

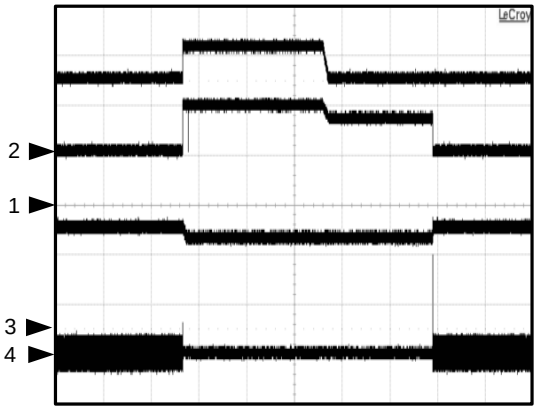
Operating Waveforms

DPM, V_{SP}=4.533V, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit, TE=1 (Cont.)



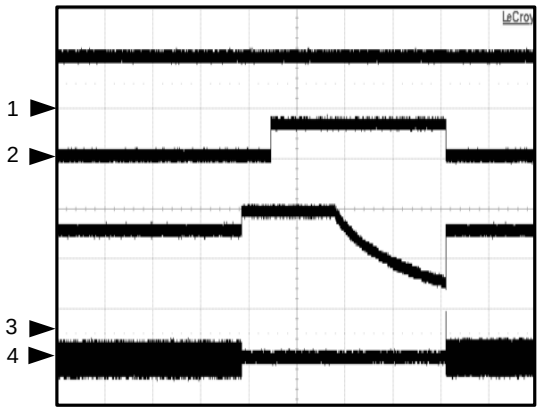
CH1: V_{BUS} (1V/div)
CH2: I_{VBUS} (1A/div)
CH3: V_{BAT} (2V/div)
CH4: I_L (1A/div)
Time: 20µs/div

Charge Mode, V_{BUS} OVP/Released OVP, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit



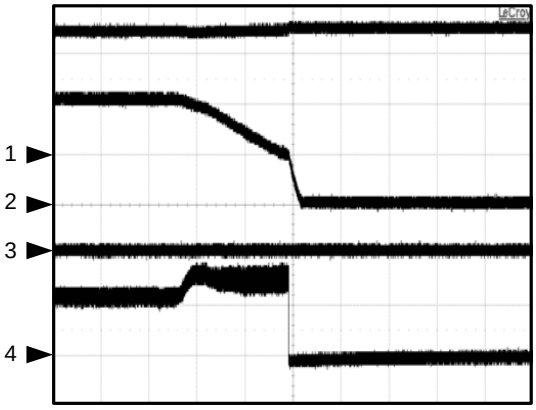
CH1: V_{BUS} (2V/div)
CH2: V_{STAT} (5V/div)
CH3: V_{BAT} (2V/div)
CH4: IL (500mA/div)
Time: 1s/div

Charge Mode, Battery OVP/Released OVP, V_{OREG}=4.2V, I_{IN_LIMIT}=NO Limit



CH1: V_{BUS} (5V/div)
CH2: V_{STAT} (5V/div)
CH3: V_{BAT} (2V/div)
CH4: IL (500mA/div)
Time: 1s/div

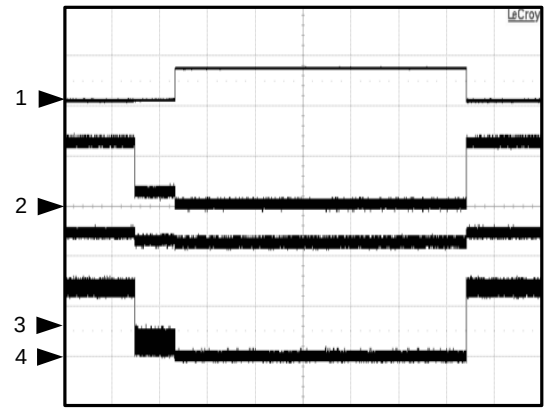
Battery Overload, V_{OREG}=4.2V, V_{BAT}=Float, I_{IN_LIMIT}=NO Limit



CH1: V_{BUS} (2V/div)
CH2: V_{BAT} (2V/div)
CH3: V_{STAT} (5V/div)
CH4: I_L (1A/div)
Time: 200µs/div

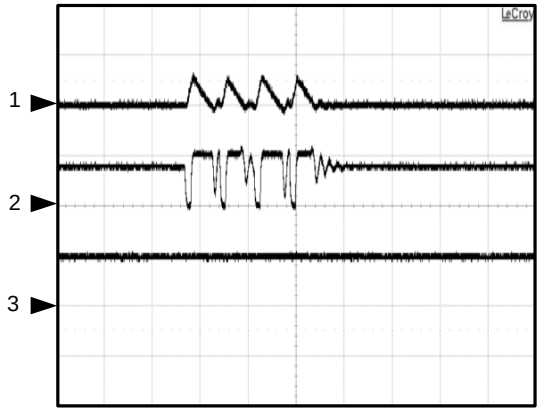
Operating Waveforms

OTP, V_{OREG}=4.2V, V_{BAT}=3.8, I_{IN_LIMIT}=NO Limit, TE=1



CH1: V_{STAT} (5V/div)
CH2: I_{VBUS} (1A/div)
CH3: V_{BAT} (2V/div)
CH4: I_{BAT} (1A/div)
Time: 500ms/div

Boost Mode, V_{BAT}=3.8V, I_{VBUS}= No Load, In PFM Operation

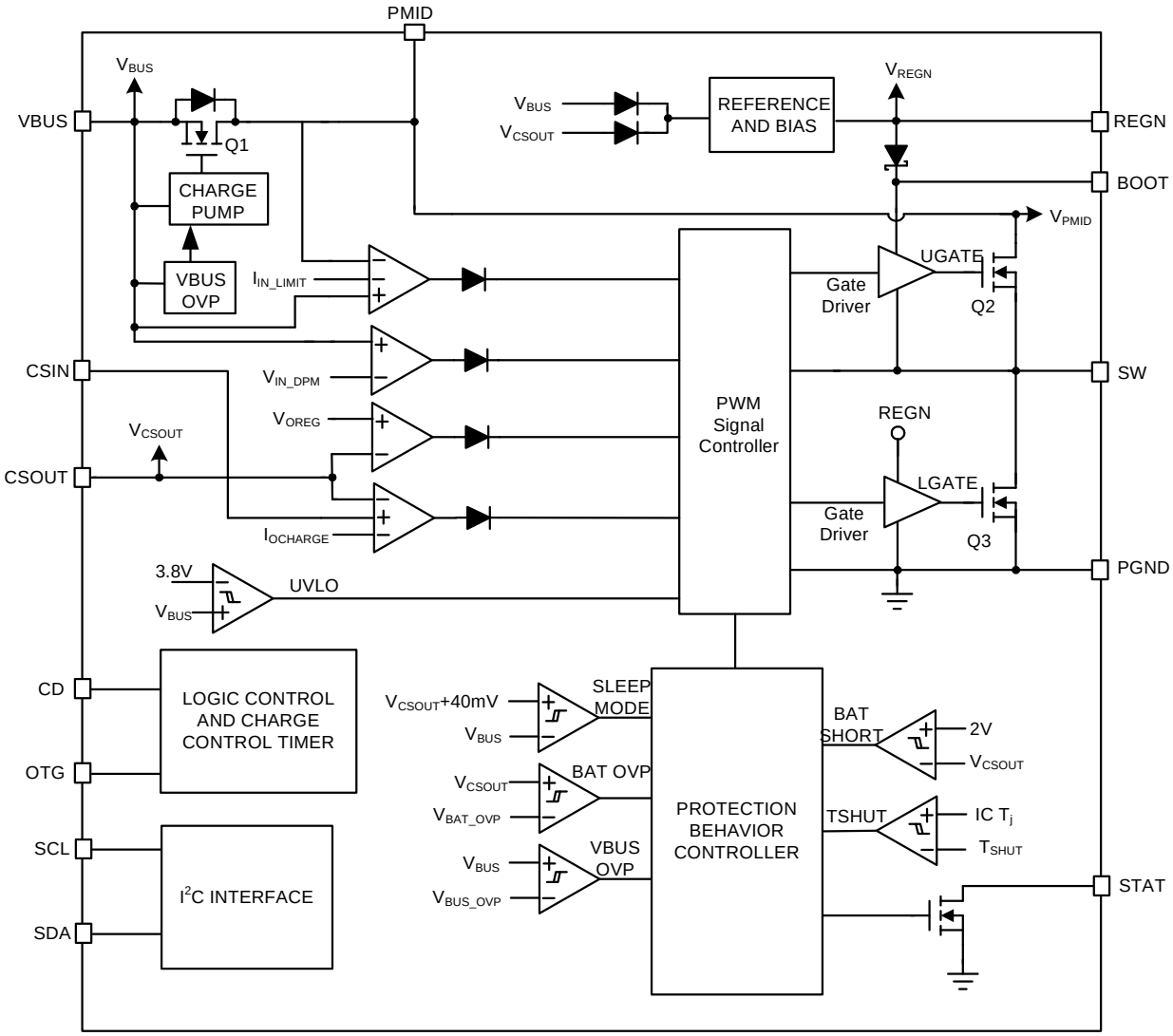


CH1: I_L (500mA/div)
CH2: V_{SW} (5V/div)
CH3: V_{BUS} (5V/div)
Time: 500ns/div

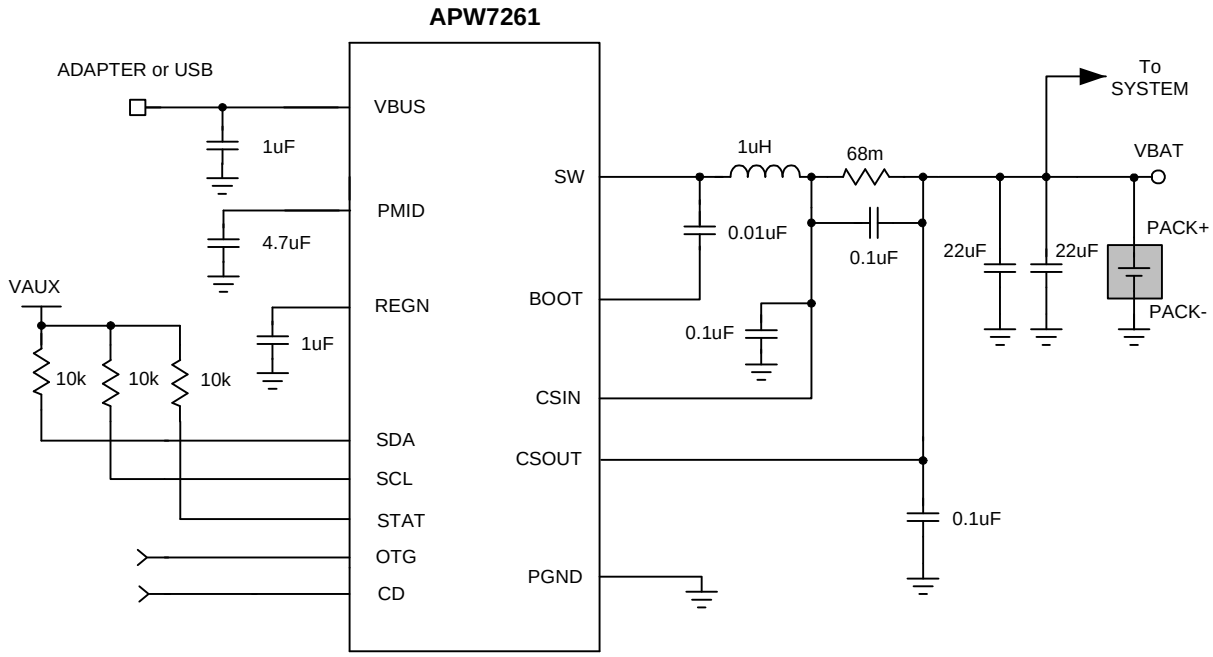
Boost Mode, V_{BAT}=3.8V, I_{VBUS}= 500mA, In CCM Operation

CH1: I_L (500mA/div)
CH2: V_{SW} (5V/div)
CH3: V_{BUS} (5V/div)
CH4: I_{VBUS} (500mA/div)
Time: 200ns/div

Block Diagram



Typical Application Circuit



Typical Application Circuit

Charger VBUS POR

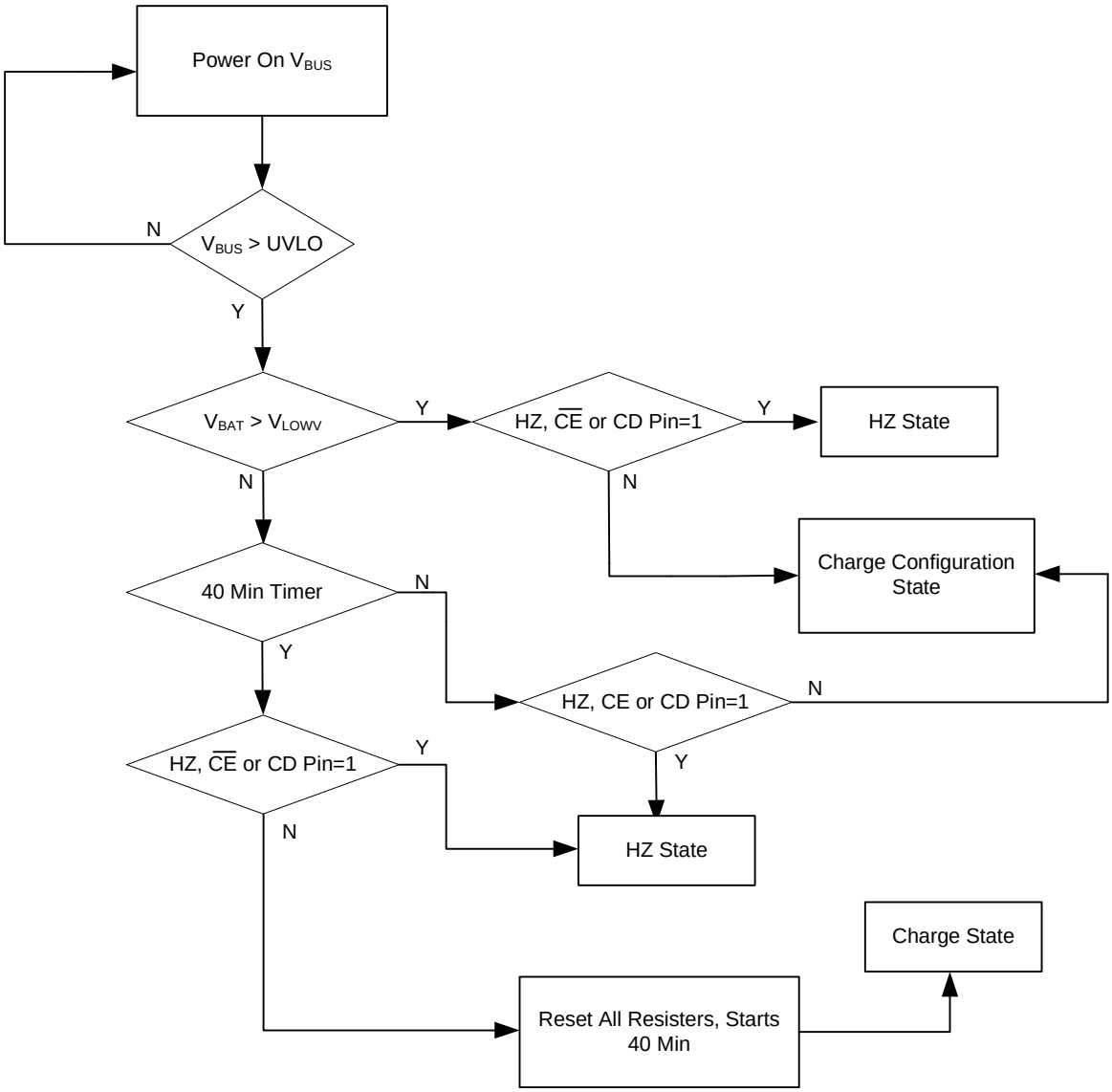


Figure 4. Charger VBUS POR Flow Chart

Typical Application Circuit

HZ State

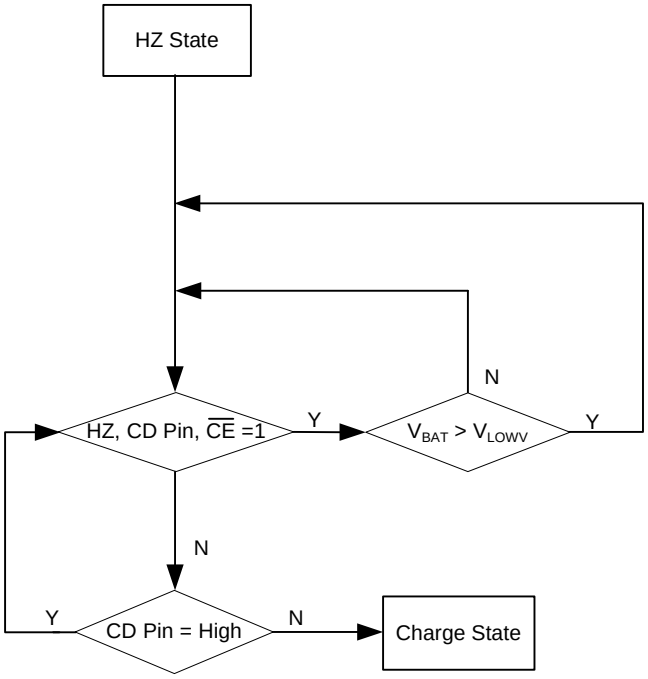


Figure 5. HZ State Flow Chart

Charge Configuration State

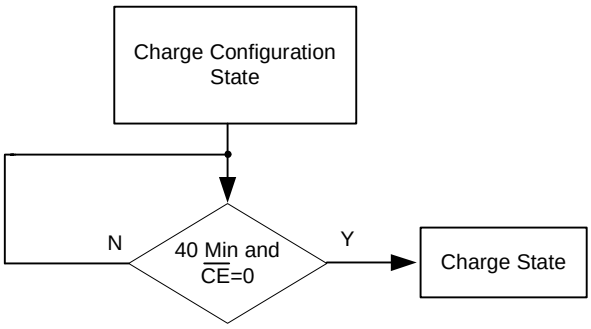


Figure 6. Charge Configuration Flow Chart

Typical Application Circuit

Charge State

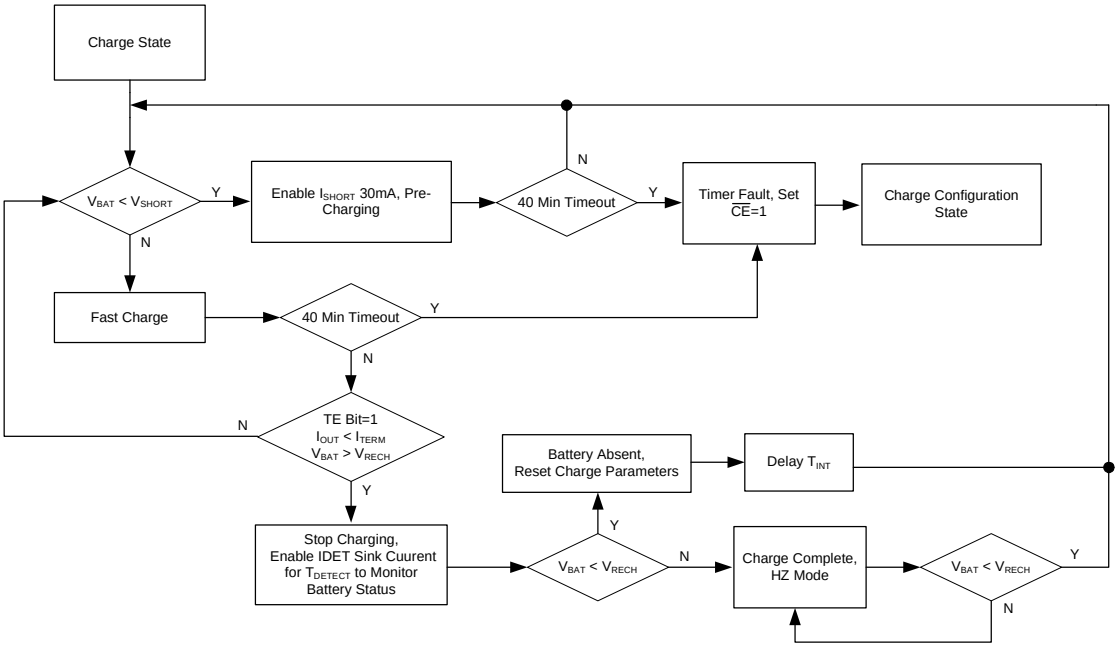


Figure 7. Operational Flow Chart in Charge Mode

In Charge State=>Charge Start

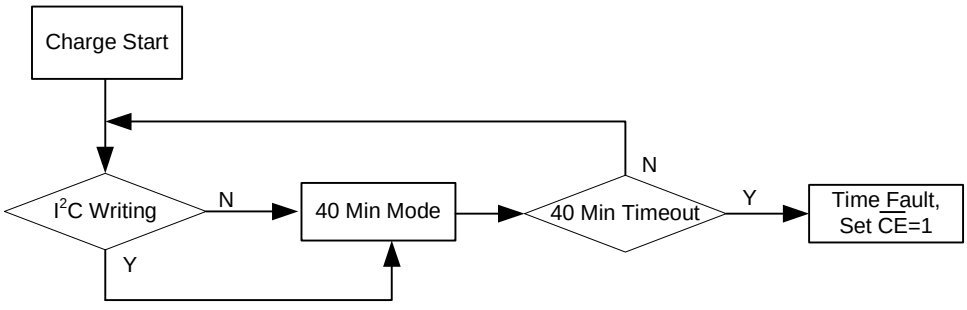


Figure 8. Charger Timer Flow Chart

Function Description

The APW7261 is a switch-mode battery charger with fixed 3MHz switching frequency, which drives two integrated N-channel power MOSFETs. The step-down DC/DC converter is ideally suited for portable electronic devices. In addition, the APW7261 can supply 5V to USB On-The-Go (OTG) peripherals through I²C programmable.

The APW7261 has three operation states in substance:

1.Charge State - charges a single-cell Li-ion or Li-polymer battery with an integrated synchronous rectification buck regulator.

2.Boost State - supply 5V power to USB-OTG with an integrated synchronous rectification boost regulator using battery terminal as input.

3.High-Impedance State - Both the charging and boost circuits are off. This state consumes low quiescent current from VBUS or the battery.

CHARGEMODE

Battery Current Regulation

Limits the maximum charging current. Using the resistor R_{SNS} connected between CSIN and CSOUT as the battery sensing.

Input Current Regulation

The total input current is a function of the system supply current and the battery charging current. When the summation of system power and charge power exceeds the maximum VBUS input power, the device will reduce input current by using Dynamic Power Management (DPM). Using the internal MOSFET $R_{DS(on)}$ from VBUS to PMID terminal as the input current sensing.

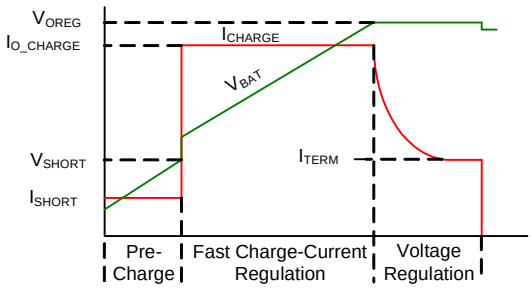
Charge Voltage Regulation

The regulator is restricted from exceeding this voltage. When the voltage which is across R_{SNS} drops below the termination current threshold (I_{TERM}), programmed by TE bit (REG1[3]) the battery charging is completed.

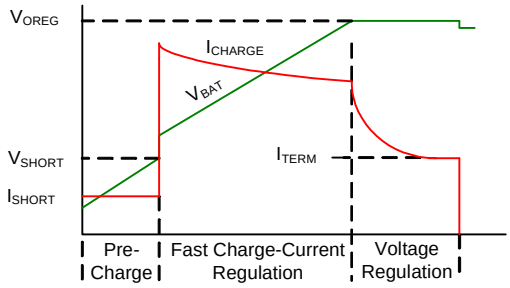
Battery Charging Process

While battery voltage is below the V_{SHORT} threshold, the IC applies a constant short-circuit current I_{SHORT}, to the battery. The charge current ramps up to fast charge current, $I_{O(CHARGE)}$, or a charge current is limited by the input current of I_{IN_LIMIT} when the battery voltage is above V_{SHORT} and below V_{OREG}.

The input current limit, I_{IN_LIMIT}, fast charge current, $I_{O(CHARGE)}$, and the battery regulation voltage, V_{OREG}, can be set by the host. Once the battery voltage reaches V_{OREG}, the charge current is decreased as shown in Figure 9.



(a) Charging Process, Not Limited by I_{IN_LIMIT}



(b) Charge Curve, I_{IN_LIMIT} Limits I_{CHARGE}

Figure 9. Typical Charge Process

The APW7261 monitors the battery-pack voltage between the CSOUT and PGND pins as voltage regulation feedback. The regulation voltage is adjustable from 3.5V to 4.44V and is programmed through I²C interface.

The IC monitors the charging current during the whole voltage regulation phase. The termination current level is programmable by I²C interface. The host can set the charge termination bit (REG1[3]) of charge control register to 0 to disable the charge current termination behavior. When below condition is occurred, a new charge cycle is initiated.

- The battery voltage falls below the V_{OREG} - V_{RECH} threshold when TE bit is set to 0.

Function Description

Safety Timer

At the beginning of charging process, the IC starts a 40-minute timer that can be only disabled by VBUS POR Toggle. When the 40-minute timer times out, the IC turns off the charging operation, set CE bit to 1 (REG1[2]) and indicates a timer fault (110) on the FAULT bit (REG[2:0]). Toggle POR or write CE bit to 0 can restart charging process. Fault condition is cleared by POR and fault status bits can only be updated after the STAT bit are read by the host.

In default operation condition, 32-second timer is disabled and it can be programmable through 32sec timer bit (REG6[7]). If 32-second timer is enabled, it can be reset by any write-action performed by host through I²C interface. Writing "1" to reset the TMR_RST bit (REG0[7]) will reset the 32-second timer and TMR_RST is automatically set to "0" after the 32-second timer is reset. The charge is terminated and charge parameters are reset to default values when the 32-second timer expires. Then the 40-minute timer starts and the charge resumes.

Special Charger

The APW7261 has additional functionality to limit Input current in case a current-limited "special charger" is supplying VBUS. If V_{BUS} voltage is equal to the programmable V_{SP} (REG5[4]), the PWM controller starts to decrease the operation frequency and limits the charge current to keep V_{BUS}=V_{SP}.

Safety Settings

The APW7261 provides a SAFETY register (REG6)

To avoid the value of the I_{O_CHARGE} exceeding from the value of the ISAFE (REG4[6:4]).

The ISAFE register establishes value that limit the maximum value of I_{O_CHARGE} used by the control logic. If the host attempts to write a value higher than ISAFE to I_{O_CHARGE}, the ISAFE value as the I_{O_CHARGE} register value.

Input Current Limit

The APW7261 integrated the input current sensing circuit and control loop. When operating in boost mode, the input current limit is default 500mA. In charge mode, the input current limit is set by the programmed control bits in register 01H.

Thermal Regulation

To prevent overheating of the chip during the charging process, the IC monitors the junction temperature, T_J, of the die. Once T_J reaches the thermal regulation threshold, T_{CF}, the IC begins to taper down the charge current. When the junction temperature increases approximately 10°C above T_{CF}, the charge current is reduced to zero. In any state, The IC suspends charging if T_J exceeds T_{SHTDWN}. In thermal shutdown mode, PWM is turned off and all timers are frozen. When T_J falls below T_{SHTDWN} by approximately 10°C, the APW7261 resumes charging process.

Sleep Mode

If the V_{BUS} voltage falls below the sleep mode entry threshold, V_{CSOUT}+V_{SLP}, the IC enters to the sleep mode. This feature prevents draining the battery during the absence of VBUS. During sleep mode, the internal reverse blocking switch and PWM controller are turned off.

VBUS Low Voltage Detection (UVLO)

During charging process, the APW7261 continuously monitors V_{BUS} voltage. If V_{BUS} falls below UVLO threshold, the IC stops to charge and sets STAT bits to "11", the FAULT bits to "011" off.

If VBUS rises above UVLO rising threshold, the charging process is repeated.

VBUS Over-Voltage Protection

The IC provides a built-in input over voltage protection (OVP) to protect the device and other components against damage if the VBUS voltage goes too high. When the VBUS OVP condition is detected, the IC turns off the PWM converter, sets the STAT bit to "11" and FAULT bits to "001". Once VBUS drops below the VBUS OVP exit threshold, the fault is cleared and charge process resumes.

Battery Over-Voltage Protection

The IC provides a built-in over voltage protection to protect the device and other components against damage if the battery voltage goes too high, as when the battery is suddenly removed. When the battery OVP condition is detected, the IC turns off the PWM converter, sets the STAT bit to "11" and FAULT bits to "100".

Once V_{BAT} drops to the battery OVP threshold, the fault is cleared and charge process resumes.

Function Description

Battery Short Circuit Protection

If the battery voltage V_{BAT} is below the short circuit threshold V_{SHORT}, a constant current source I_{SHORT} supplies V_{BAT} until $V_{BAT} > V_{SHORT}$.

Cycle-by-Cycle Charge Mode Current Limit

The APW7261 monitors internal high-side MOSFET for current sensing. If the peak current exceeds the high-side MOSFET limit threshold, it will turn off the high-side MOSFET until the next cycle. When the current is below the over-current threshold, the high-side driver automatically resumes.

BOOST MODE

BOOST mode can be enabled if OTG pin and OPA_MODE bits as indicated in below table.

OTG_EN	OTG PIN	OTG_PL	OPA_MODE	BOOST
1	HIGH	1	X	ENABLE
1	LOW	0	X	ENABLE
X	X	X	1	ENABLE
1	HIGH	0	0	DISABLE
1	LOW	1	0	DISABLE
0	X	X	0	DISABLE

The APW7261 operates in boost mode and delivers power to VBUS from the battery. In normal boost mode, the APW7261 converts the battery voltage (2.5V to 4.5V) to VBUS (5V) and delivers a current I_{BO} 500mA at lowest to support other USB OTG devices connected to the USB connector.

PWM Controller in BOOST Mode

In boost mode, the APW7261 provides an integrated, fixed 3-MHz frequency voltage-mode controller to regulate output voltage VBUS as the same as charge mode operation.

In boost mode, cycle-by-cycle current limit is sensed through the R_{SNS} from CSIN to CSOUT. The peak current limit threshold is equal to ($0.12V/R_{SNS}$). For Example, if R_{SNS}=68mΩ, the peak current limit is about 1.76A. When current limit event is triggered, IC will turn off Q3 driver. If current limit event is released, it will re-back normal operation.

PFM Mode at Light Load

In boost mode, under light load conditions, the IC operates in PFM mode (power saving) to reduce the power loss and improve the converter efficiency.

In PFM Mode, the on-time pulse width is constant and regulates off-time by zero crossing sensing.

VBUS Over-Voltage Protection

The IC provides a built-in over voltage protection to protect the device and other components against damage if the V_{BUS} voltage goes too high. When the VBUS OVP condition is detected, the IC turns off the PWM converter, sets the STAT bit to “11”, FAULT bits to “001” and resets OPA_MODE bit to 0. And then, APW7261 will return to charge mode.

Battery Over-Voltage Protection

In Boost mode, the IC provides a built-in input over voltage protection to protect the device and other components against damage if the VBAT voltage goes too high. When the VBAT OVP condition is detected, the IC turns off the PWM converter, sets the STAT bit to “11” and resets OPA_MODE bit to 0. And then, APW7261 will return to charge mode.

Layout Consideration

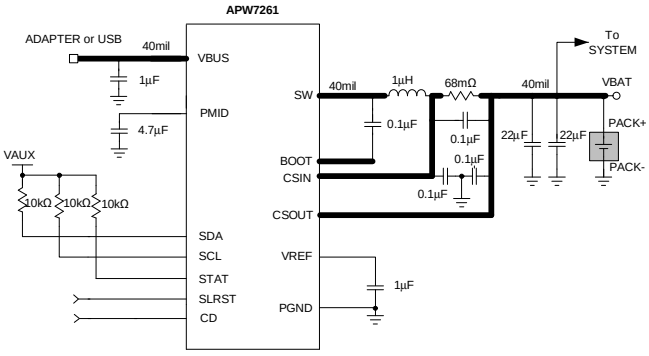
In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding if the above seperated pinout ground condirtions are satisfied.

Function Description (Cont.)

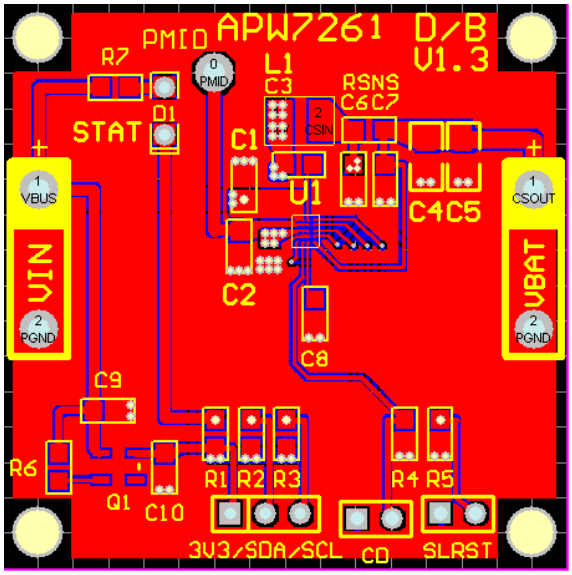
Layout Consideration (Cont.)

Below are Layout consideration checklist, recommended layout Schematic diagram and demoboard layout for your reference:

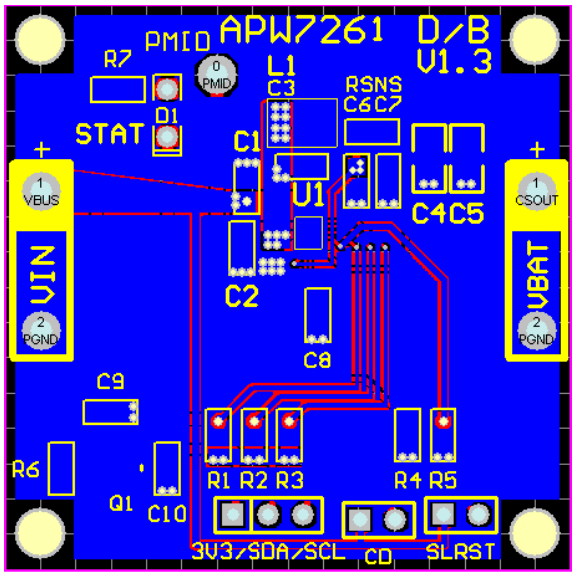
- Keep the switching nodes (BOOT and SW) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The large layout plane between the drain of the MOSFETs (VIN and SW nodes) can get better heat sinking.
- The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path).
- The high-current charge paths into VBUS, PMID and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- Place all decoupling capacitors close to their respective IC pins and close to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors.



Top Layer



Bottom Layer



I²C Introduction

I²C SERIAL CONTROL INTERFACE

The APW7261 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz), fast mode (400-kHz) and the high-speed mode (up to 3.4Mbps in wire mode) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum), the fast I²C bus operation (400 kHz maximum) and the high-speed mode (up to 3.4Mbps in wire mode). The DAP performs all I2C operations without I²C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 10. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The APW7261 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

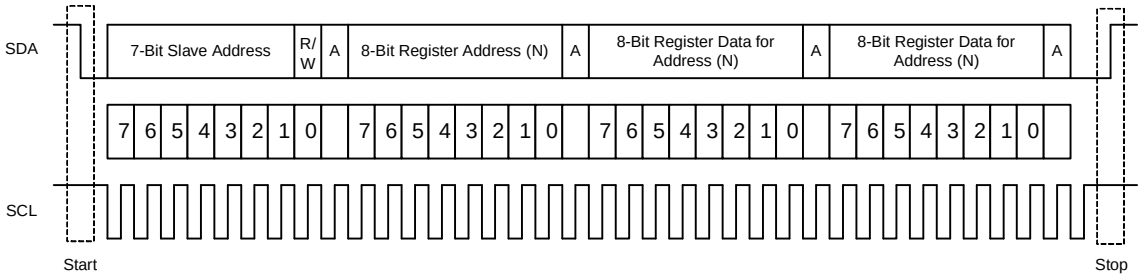


Figure 10. Typical I²C sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 10. Pin A_SEL defines the I²C device address. The device 7-bit address is defined as “1101010” (6AH) for APW7261.

I²C Introduction

Single-Byte Transfer

The serial control interface supports single-byte read/write operations for sub-addresses 0x00 to 0xFF.

Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7261 also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7261. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 11, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I²C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7261 internal memory address being accessed. After receiving the address byte, the APW7261 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7261 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

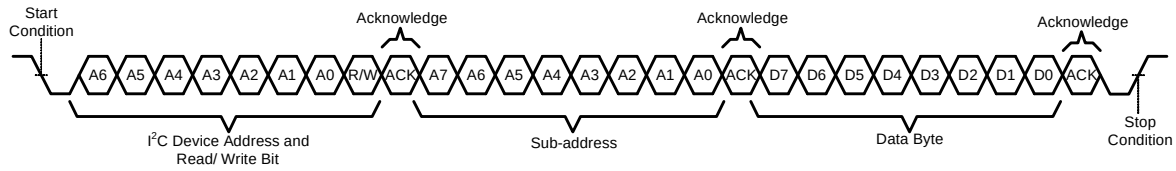


Figure 11. Single-Byte Write Transfer

Single-Byte Read

As shown in Figure 12, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the APW7261 address and the read/write bit, APW7261 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7261 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the APW7261 again responds with an acknowledge bit. Next, the APW7261 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

I²C Introduction

Single-Byte Read (Cont.)

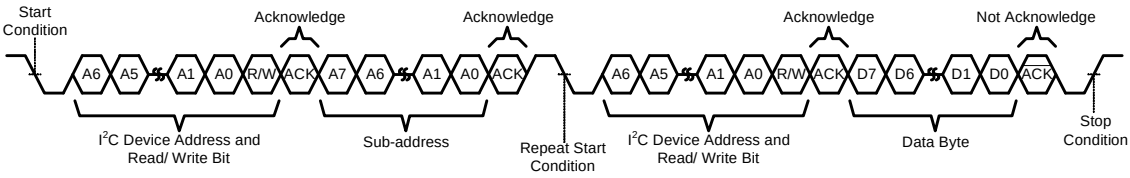


Figure 12. Single-Byte Read Transfer

Register Description

The APW7261 has seven user-accessible registers. It is as defined as below table.

Register Address	Name	Read/Write/Read Only State	Default Value
00	Control/Status	Read/Write	X1XX 0XXX
01	Control/Input Current Limit	Read/Write	0111 0000
02	Control/Battery Voltage	Read/Write	0000 1010
03	Vender/Part/Revision	Read Only	010X XXXX
04	Termination/Fast Charge Current	Read/Write	0000 0001
05	Enable/Special Charger Voltage	Read/Write/Read Only	001X X100
06	Safety Limit	Read/Write	1100 0000

The below tables define the operation of each register bit. Default values are in **bold** text.

Table1. Register Address: 00

Bit	Name	Data	Read/Write	Description
7	TMR_RST/OTG		Write	Default Condition, write "0" or "1" has no effect ; If call out 32sec timer, Writing a 1 resets the t_{32s} timer
			Read	OTG pin status. "0"=> OTG=Low; "1"=> OTG=High
6	EN_STAT	0	Read/Write	Disable STAT pin function
		1	**Read/Write**	**Enable STAT pin function**
[5:4]	STAT	00	Read	Ready
		01	Read	Charge in process
		10	Read	Charge done
		11	Read	Fault
3	BOOST	**0**	**Read**	**Not in boost mode**
		1	Read	In boost mode
[2:0]	FAULT	000	Read	Charge mode : Normal Boost mode : Normal
		001	Read	Charge mode : VBUS OVP Boost mode : VBUS OVP
		010	Read	Charge mode : Sleep mode Boost mode : Over load
		011	Read	Charge mode : VBUS < UVLO Boost mode : VBAT < $UVLO_{BST}$

Register Description

Bit	Name	Data	Read/Write	Description
[2:0]	FAULT	100	Read	Charge mode : Battery OVP Boost mode : N/A
		101	Read	Charge mode : Thermal Shutdown Boost mode : Thermal Shutdown
		110	Read	Charge mode : Timer fault Boost mode : Timer fault
		111	Read	Charge mode : No battery Boost mode : N/A

Table2. Register Address: 01

Bit	Name	Data	Read/Write	Description
[7:6]	I_{IN_LIMIT}	00	Read/Write	100mA
		01	**Read/Write**	**500mA**
		10	Read/Write	800mA
		11	Read/Write	No Current Limit
[5:4]	V_{LOWV}	00	Read/Write	3.4V
		01	Read/Write	3.5V
		10	Read/Write	3.6V
		11	**Read/Write**	**3.7V**
3	TE	**0**	**Read/Write**	**Disable charge current termination**
		1	Read/Write	Enable charge current termination
2	CE	**0**	**Read/Write**	**Charge enabled**
		1	Read/Write	Charge disabled
1	HZ_MODE	**0**	**Read/Write**	**Not High-Impedance Mode**
		1	Read/Write	High-Impedance Mode
0	OPA_MODE	**0**	**Read/Write**	**Charge Mode**
		1	Read/Write	Boost Mode

Register Description

Table3. Register Address: 02

Bit	Name	Data	Read/Write	Description
[7:2]	OREG	000000	Read/Write	3.5V
		000001	Read/Write	3.52V
		000010	**Read/Write**	**3.54V**
		000011	Read/Write	3.56V
		000100	Read/Write	3.58V
		000101	Read/Write	3.6V
		000110	Read/Write	3.62V
		000111	Read/Write	3.64V
		001000	Read/Write	3.66V
		001001	Read/Write	3.68V
		001010	Read/Write	3.7V
		001011	Read/Write	3.72V
		001100	Read/Write	3.74V
		001101	Read/Write	3.76V
		001110	Read/Write	3.78V
		001111	Read/Write	3.8V
		010000	Read/Write	3.82V
		010001	Read/Write	3.84V
		010010	Read/Write	3.86V
		010011	Read/Write	3.88V
		010100	Read/Write	3.9V
		010101	Read/Write	3.92V
		010110	Read/Write	3.94V
		010111	Read/Write	3.96V
		011000	Read/Write	3.98V
		011001	Read/Write	4V
		011010	Read/Write	4.02V
		011011	Read/Write	4.04V
		011100	Read/Write	4.06V
		011101	Read/Write	4.08V
		011110	Read/Write	4.1V
		011111	Read/Write	4.12V
		100000	Read/Write	4.14V
		100001	Read/Write	4.16V
		100010	Read/Write	4.18V
		100011	Read/Write	4.2V
		100100	Read/Write	4.22V

Register Description

Table3. Register Address: 02

Bit	Name	Data	Read/Write	Description
[7:2]	OREG	100100	Read/Write	4.22V
		100101	Read/Write	4.24V
		100110	Read/Write	4.26V
		100111	Read/Write	4.28V
		101000	Read/Write	4.3V
		101001	Read/Write	4.32V
		101010	Read/Write	4.34V
		101011	Read/Write	4.36V
		101100	Read/Write	4.38V
		101101	Read/Write	4.4V
		101110	Read/Write	4.42V
		101111	Read/Write	4.44V
		110000	Read/Write	4.44V
		110001	Read/Write	4.44V
		110010	Read/Write	4.44V
		110011	Read/Write	4.44V
		110100	Read/Write	4.44V
		110101	Read/Write	4.44V
		110110	Read/Write	4.44V
		110111	Read/Write	4.44V
		111000	Read/Write	4.44V
		111001	Read/Write	4.44V
		111010	Read/Write	4.44V
		111011	Read/Write	4.44V
		111100	Read/Write	4.44V
		111101	Read/Write	4.44V
		111110	Read/Write	4.44V
1	OTG_PL	0	Read/Write	OTG pin active Low
		1	**Read/Write**	**OTG pin active High**
0	OTG_EN	**0**	**Read/Write**	**OTG pin is disabled**
		1	Read/Write	OTG pin is enabled

Register Description

Table4. Register Address: 03

Bit	Name	Data	Read/Write	Description
[7:5]	Vender code	010	Read Only	
[4:3]	PN	XX	Read Only	For I^2C Address
[2:0]	REV	XXX	Read Only	IC Revision

Table5. Register Address: 04

Bit	Name	Data	Read/Write	Description
7	Reserved	0	Read Only	Unused
[6:4]	IOCHARGE	**000**	**Read/Write**	**R_{SNS}: 56mW=>668mA; R_{SNS}: 68mW=>550mA ; R_{SNS}: 100mW=>374mA**
		001	Read/Write	R_{SNS}: 56mΩ=>789mA; R_{SNS}: 68mΩ=>650mA ; R_{SNS}: 100mΩ=>442mA
		010	Read/Write	R_{SNS}: 56mΩ=>911mA; R_{SNS}: 68mΩ=>750mA ; R_{SNS}: 100mΩ=>510mA
		011	Read/Write	R_{SNS}: 56mΩ=>1032mA; R_{SNS}: 68mΩ=>850mA ; R_{SNS}: 100mΩ=>578mA
		100	Read/Write	R_{SNS}:56mΩ=>1275mA; R_{SNS}: 68mΩ=>1050mA ; R_{SNS}: 100mΩ=>714mA
		101	Read/Write	R_{SNS}: 56mΩ=>1396mA; R_{SNS}: 68mΩ=>1150mA ; R_{SNS}: 100mΩ=>782mA
		110	Read/Write	R_{SNS}: 56mΩ=>1639mA; R_{SNS}: 68mΩ=>1350mA ; R_{SNS}: 100mΩ=>918mA
		111	Read/Write	R_{SNS}:56mΩ=>1882mA; R_{SNS}: 68mΩ=>1550mA ; R_{SNS}: 100mΩ=>1054mA
3	Reserved	**0**	**Read Only**	**Unused**
[2:0]	ITERM	000	Read/Write	R_{SNS}: 56mΩ=>59mA; R_{SNS}: 68mΩ=>49mA; R_{SNS}: 100mΩ=>33mA
		001	**Read/Write**	**R_{SNS}: 56mW=>118mA; R_{SNS}: 68mW=>97mA; R_{SNS}: 100mW=>66mA**
		010	Read/Write	R_{SNS}: 56mΩ=>177mA; R_{SNS}: 68mΩ=>146mA; R_{SNS}: 100mΩ=>99mA
		011	Read/Write	R_{SNS}: 56mΩ=>236mA; R_{SNS}: 68mΩ=>194mA; R_{SNS}: 100mΩ=>132mA
		100	Read/Write	R_{SNS}: 56mΩ=>295mA; R_{SNS}: 68mΩ=>243mA; R_{SNS}: 100mΩ=>165mA
		101	Read/Write	R_{SNS}: 56mΩ=>353mA; R_{SNS}: 68mΩ=>291mA; R_{SNS}: 100mΩ=>198mA
		110	Read/Write	R_{SNS}: 56mΩ=>412mA; R_{SNS}: 68mΩ=>340mA; R_{SNS}: 100mΩ=>231mA
		111	Read/Write	R_{SNS}: 56mΩ=>471mA; R_{SNS}: 68mΩ=>388mA; R_{SNS}: 100mΩ=>264mA

Register Description

Table6. Register Address: 05

Bit	Name	Data	Read/Write	Description
7	Reserved	**0**	**Read Only**	**Unused**
6	Reserved	**0**	**Read/Write**	**Unused**
5	IO_LEVEL	0	Read/Write	Charge current is controlled by $I_{OCHARGE}$ bits
		1	**Read/Write**	**Charge current is set to 395mA for R_{SNS}: 56mW, 325mA for R_{SNS}: 68mW, 221mA for R_{SNS}: 100mW**
4	SP	0	Read Only	Special charger is not active
		1	Read Only	Special charger is active and V_{BUS} is being regulated to V_{SP}
3	EN_LEVEL	0	Read Only	CD pin is Low
		1	Read Only	CD pin is High
[2:0]	VSP	000	Read/Write	V_{SP}=4.213V
		001	Read/Write	V_{SP}=4.29V
		010	Read/Write	V_{SP}=4.373V
		011	Read/Write	V_{SP}=4.453V
		100	**Read/Write**	**V_{SP}=4.533V**
		101	Read/Write	V_{SP}=4.613V
		110	Read/Write	V_{SP}=4.693V
		111	Read/Write	V_{SP}=4.773V

Table7. Register Address: 06

Bit	Name	Data	Read/Write	Description
7	Timer	0	Read/Write	Call out 32sec timer function
		1		**No 32sec timer function**
[6:4]	ISAFE	000	Read/Write	R_{SNS}: 56mΩ=>668mA; R_{SNS}: 68mΩ=>550mA ; R_{SNS}: 100mΩ=>374mA
		001	Read/Write	R_{SNS}: 56mΩ=>789mA; R_{SNS}: 68mΩ=>650mA ; R_{SNS}: 100mΩ=>442mA
		010	Read/Write	R_{SNS}: 56mΩ=>911mA; R_{SNS}: 68mΩ=>750mA ; R_{SNS}: 100mΩ=>510mA
		011	Read/Write	R_{SNS}: 56mΩ=>1032mA; R_{SNS}: 68mΩ=>850mA ; R_{SNS}: 100mΩ=>578mA
		100	**Read/Write**	**R_{SNS}: 56mW=>1275mA; R_{SNS}: 68mW=>1050mA ; R_{SNS}: 100mW=>714mA**
		101	Read/Write	R_{SNS}: 56mΩ=>1396mA; R_{SNS}: 68mΩ=>1150mA ; R_{SNS}: 100mΩ=>782mA
		110	Read/Write	R_{SNS}: 56mΩ=>1639mA; R_{SNS}: 68mΩ=>1350mA ; R_{SNS}: 100mΩ=>918mA
		111	Read/Write	R_{SNS}: 56mΩ=>1882mA; R_{SNS}: 68mΩ=>1550mA ; R_{SNS}: 100mΩ=>1054mA

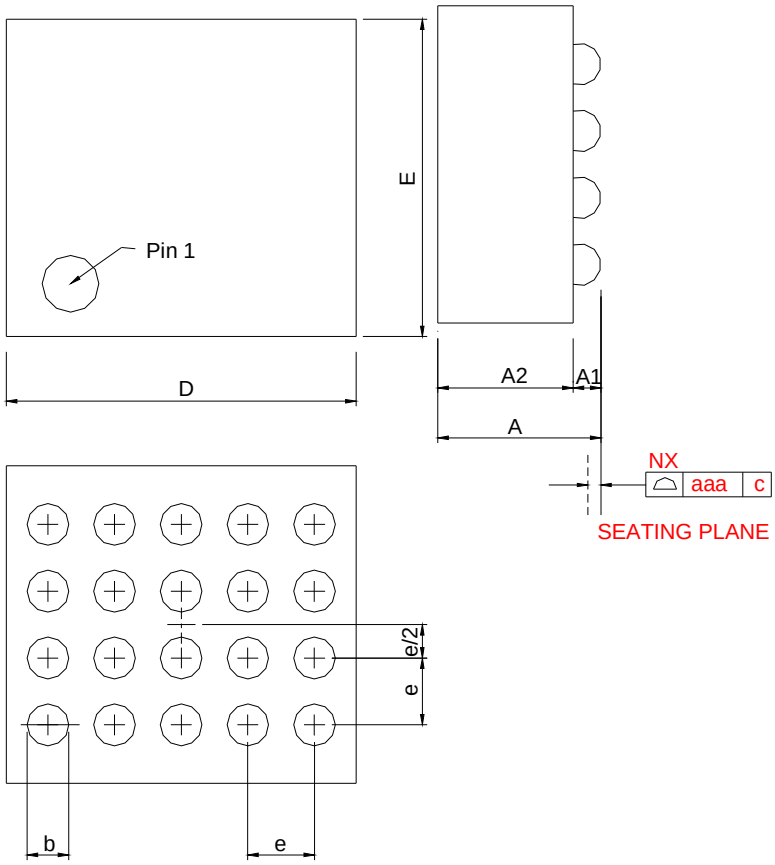
Register Description

Table6. Register Address: 06 (cont.)

[3:0]	VSAFE	**0000**	**Read/Write**	**4.2V**
		0001	Read/Write	4.22V
		0010	Read/Write	4.24V
		0011	Read/Write	4.26V
		0100	Read/Write	4.28V
		0101	Read/Write	4.3V
		0110	Read/Write	4.32V
		0111	Read/Write	4.34V
		1000	Read/Write	4.36V
		1001	Read/Write	4.38V
		1010	Read/Write	4.4V
		1011	Read/Write	4.42V
		1100	Read/Write	4.44V
		1101	Read/Write	4.44V
		1110	Read/Write	4.44V
		1111	Read/Write	4.44V

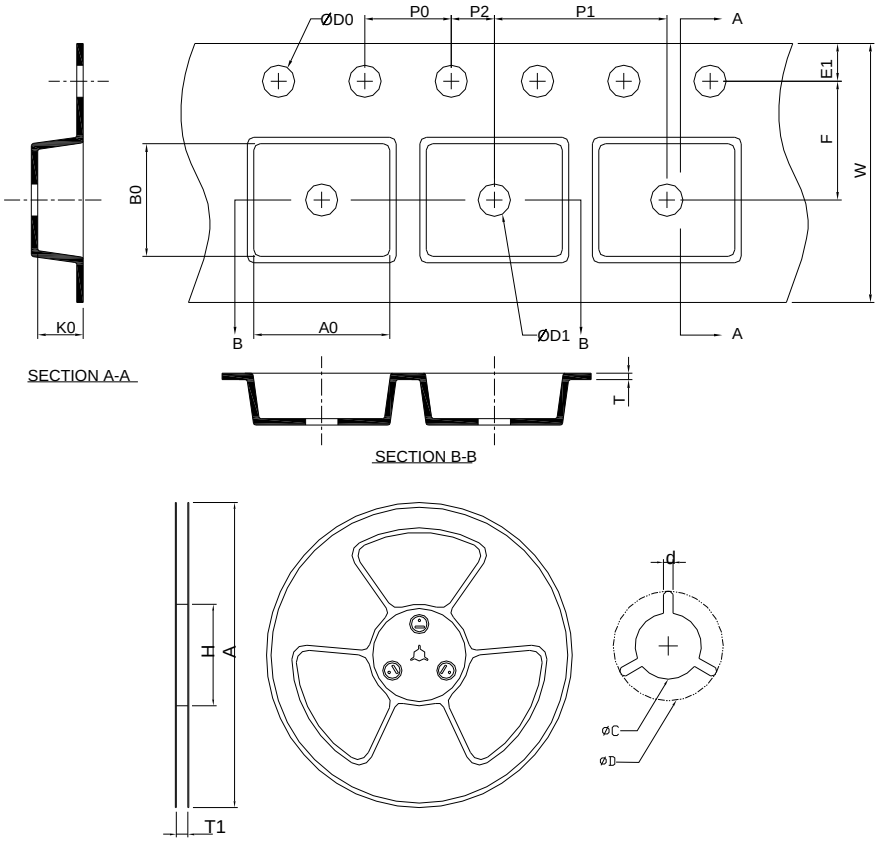
Package Information

WLCSP1.73x2.0-20



SYMBOL	WLCSP1.73*2.00-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		0.63		0.025
A1	0.15	0.19	0.006	0.007
A2	0.37	0.44	0.015	0.017
b	0.20	0.30	0.008	0.012
D	2.00	2.06	0.079	0.081
E	1.73	1.79	0.068	0.070
e	0.40 BSC		0.016 BSC	
aaa	0.05		0.002	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP(1.73X2.0)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	0.5 MIN.	0.6+0.00 -0.40	1.98±0.10	2.31±0.10	0.71±0.10

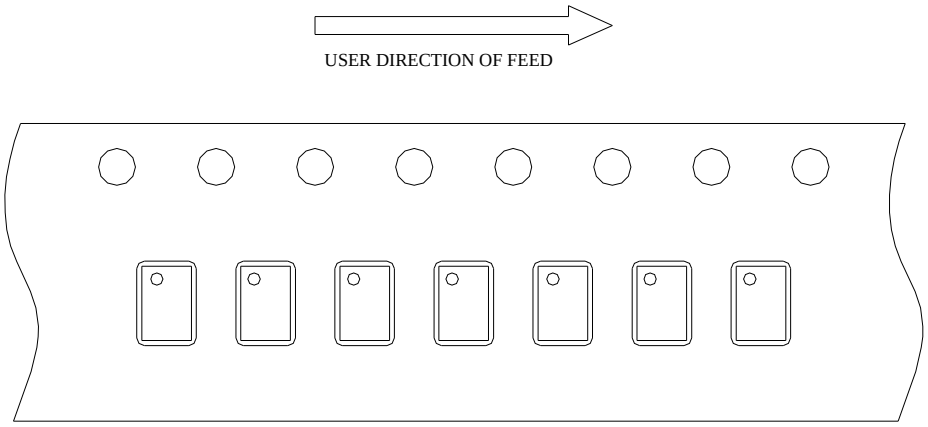
(mm)

Devices Per Unit

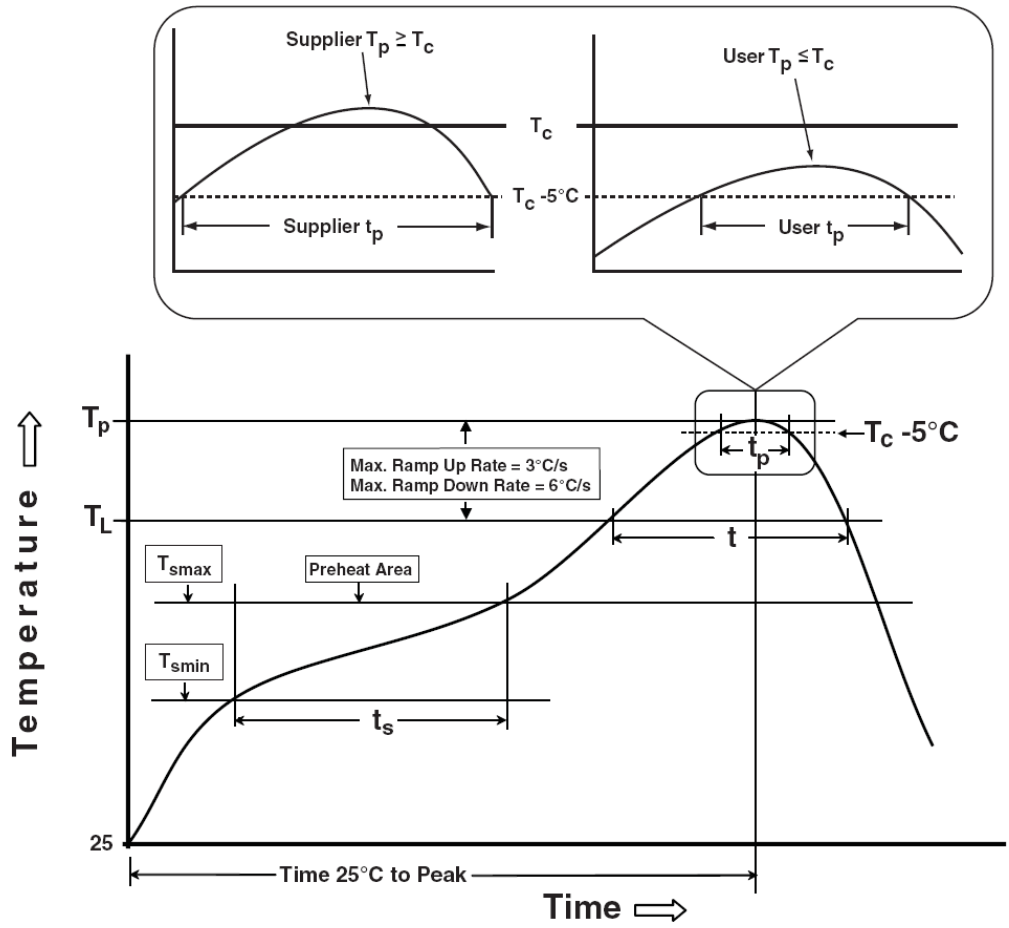
Package Type	Unit	Quantity
WLCSP1.73x2.0-20	Tape & Reel	3000

Taping Direction Information

WLCSP1.73x2.0-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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