LED Gate Driver IC

Features

- **Max. Operating Voltage 5.5V**
- **Integrated With Four 80mΩ High Side MOSFETs and a 2-4 Decoder, It Can Support 8 or 16 Channels Scanning By Multi ICs Cascade**
- **Max. 5A Current**
- **De-ghost Function**
- **Fast Turn-on & Turn-off at Bus to Output**
- **OTP Function (Over Temperature Protection)**
- **SSOP-16 and TQFN3×3-16 Packages**
- **Solution of 1st dim line and LED coupling**
- **Channel holding at turn-off**

General Description

The SPL5013C has 4 channels output for dynamic LED panel application; it is easy to supports 1/8 or 1/16 duty through multi-chips cascade. SPL5013C has fast turn off time for the de-ghost function. After the de-ghosting period, SPL5013C will hold at fixed level for the solution of 1st dim line/LED coupling, also to prevent damage LED

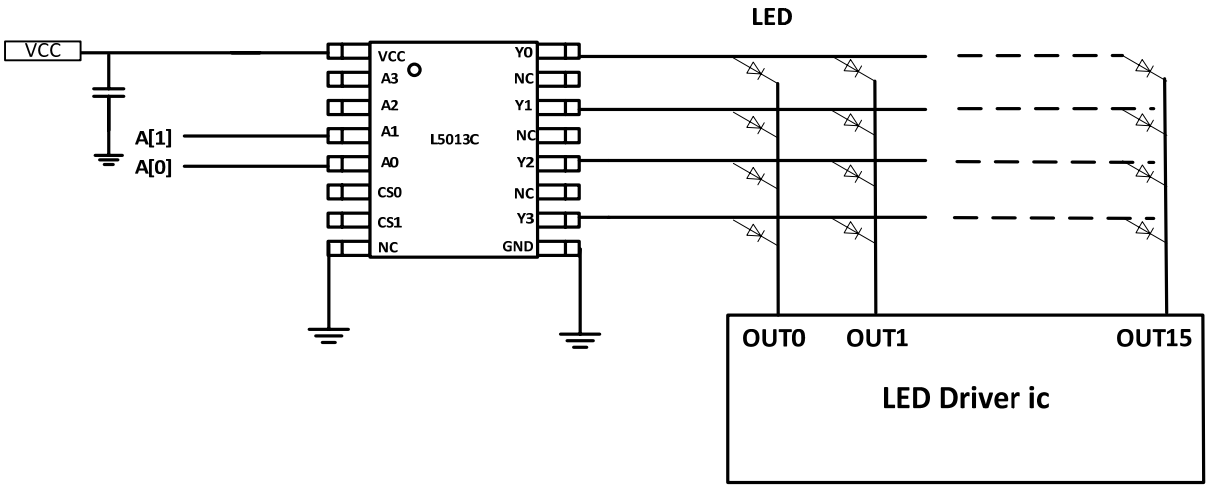
The device integrates some protection features, including OTP. The OTP function shuts down the outputs when the junction temperature rises beyond 150℃ and will automatically turn on the outputs when the temperature drops by 40℃.

The device is available in lead free SSOP-16 and TQFN3×3-16 package.

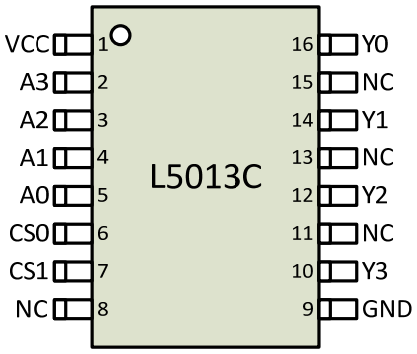
Applications

- **Outdoor LED Video Displays**
- **Indoor LED Video Displays**
- **Variable Message Signs**
- **Gaming Features**

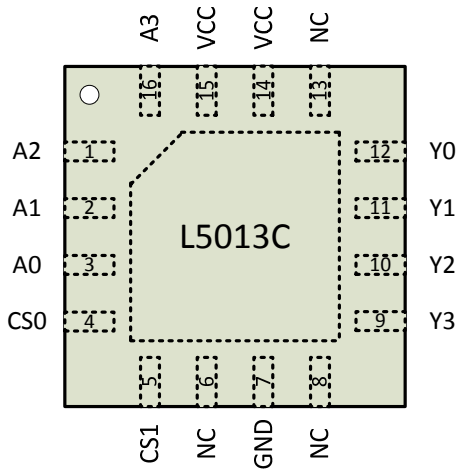
Simplified Application Circuit



Pin configuration



SSOP-16

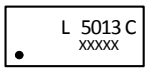


TQFN-16L

Pin Descriptions

Pin Name	Description	I/O
Vcc	Voltage supply input	Power
A0	Input ,address bus 0	Input
A1	Input ,address bus 1	Input
A2	Input ,address bus 2	Input
A3	Input ,address bus 3	Input
CS0	A2 Logic option	Input
CS1	A3 Logic option	Input
GND	Ground	GND
Y0	Output 0	Output
Y1	Output 1	Output
Y2	Output 2	Output
Y3	Output 3	Output

Ordering and Marking Information

L5013C □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code N : SSOP – 16 QB : TQFN – 16 Operating Ambient Temperature Range I : - 40 to 85 Handling Code TR Tap & Reel Assembly Material G : Halogen and Lead Free Device
L5013CN : 	XXXXX - Date Code
L5013CQB : 	XXXXX - Date Code

Note: Supec lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. Anpec lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Absolute Maximum Ratings(Note 1)

Symbol	Parameter		Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)		-0.3 ~ 6	V
V_{OUT}	Output Pin to GND Voltage		-0.3 ~ V_{CC}	V
I_{OUT}	Output Current		6	A
P_D	Maximum Power Dissipation	SSOP-16	0.8	W
		TQFN3×3-16	2	
T_J	Maximum Junction Temperature		-40~150	℃
T_{STG}	Storage Temperature		-65 ~ 150	℃
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	℃
V_{ESD}	Minimum ESD Rating(Human Body Mode)		2	KV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2) SSOP-16 TQFN3×3-16	 155 50	℃/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of xxxxx is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	4.5～5.5	V
T_A	Ambient Temperature	-40 ~ 85	℃
T_J	Junction Temperature	-40 ~ 125	℃

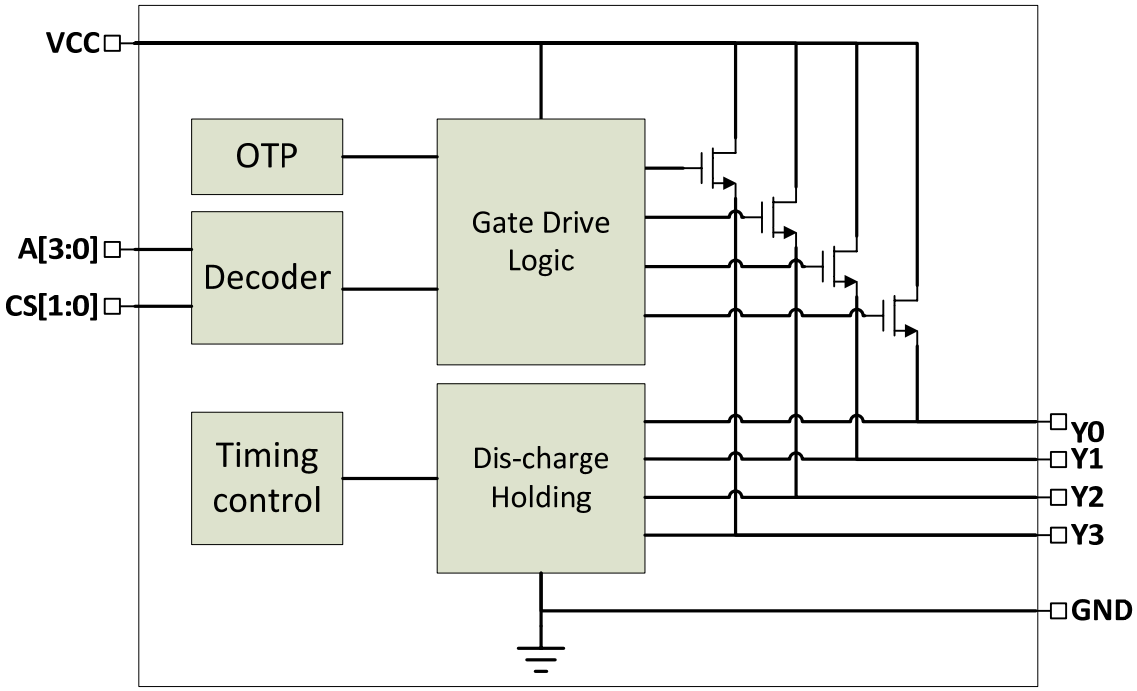
Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=5V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

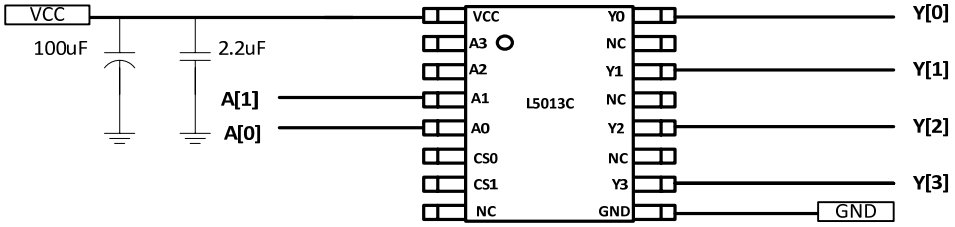
Symbol	Parameter	Test Conditions	SPL5013C			Unit
			Min	Typ	Max	
SUPPLY VOLTAGE AND CURRENT						
V_{CC}	Supply Voltage		3	5.0	5.5	V
IQ	Quiescent Current	Vcc =5V		700	950	uA
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	Vcc=5V, I_{OUT} =1A		80		mΩ
LOGIC INPUTS(A0 A1 A2 A3 CS0 CS1)						
V_L	Input Low Voltage				0.2*Vcc	V
V_H	Input High Voltage		0.8*Vcc			V
T_M	A[3:2]Timing Mismatch to A[1:0]			5		nS
DELAY TIME						
$T_{D(ON)}$	Logic Input to Output Turn On Delay Time			30	35	ns
$T_{D(OFF)}$	Logic Input to Output Turn Off Delay Time			30	35	ns
OUTPUT RISE / FALL TIME						
T_{R_OUT}	Output Rise Time	Vcc=5V, C_{OUT}=0,I_{OUT}=0		30	35	ns
		Vcc=5V, C_{OUT}=0,I_{OUT}=1A		60	70	
		Vcc=5V, C_{OUT}=0.01uF,I_{OUT}=1A		100	120	
T_{F_OUT}	Output Fall Time	Vcc=5V, C_{OUT}=0,I_{OUT}=0			0.1	us
		Vcc=5V, C_{OUT}=0.01uF,I_{OUT}=1A			1	
OVERT-TEMPERATURE PROTECTION						
OTP	Over-Temperature Threshold	T_J rising		150		℃
	Over-Temperature Hysteresis			40		℃

Block Diagram



Typical Application Circuit

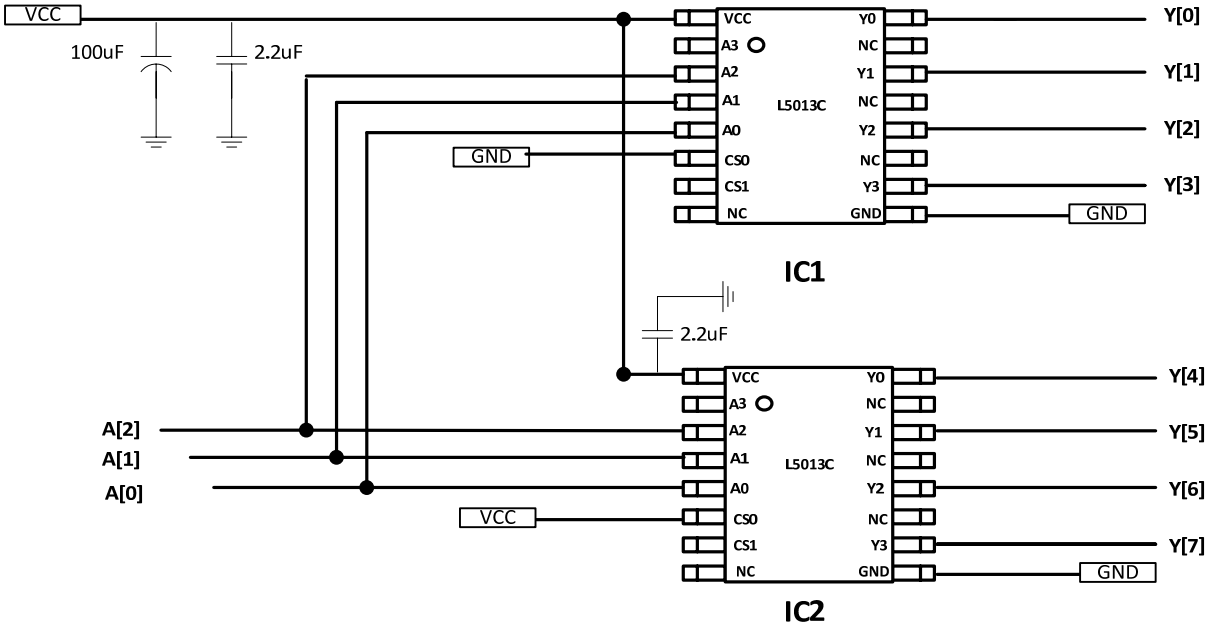
Duty=1/4 application



True table

Input		Output			
A[0]	A[1]	Y[0]	Y[1]	Y[2]	Y[3]
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

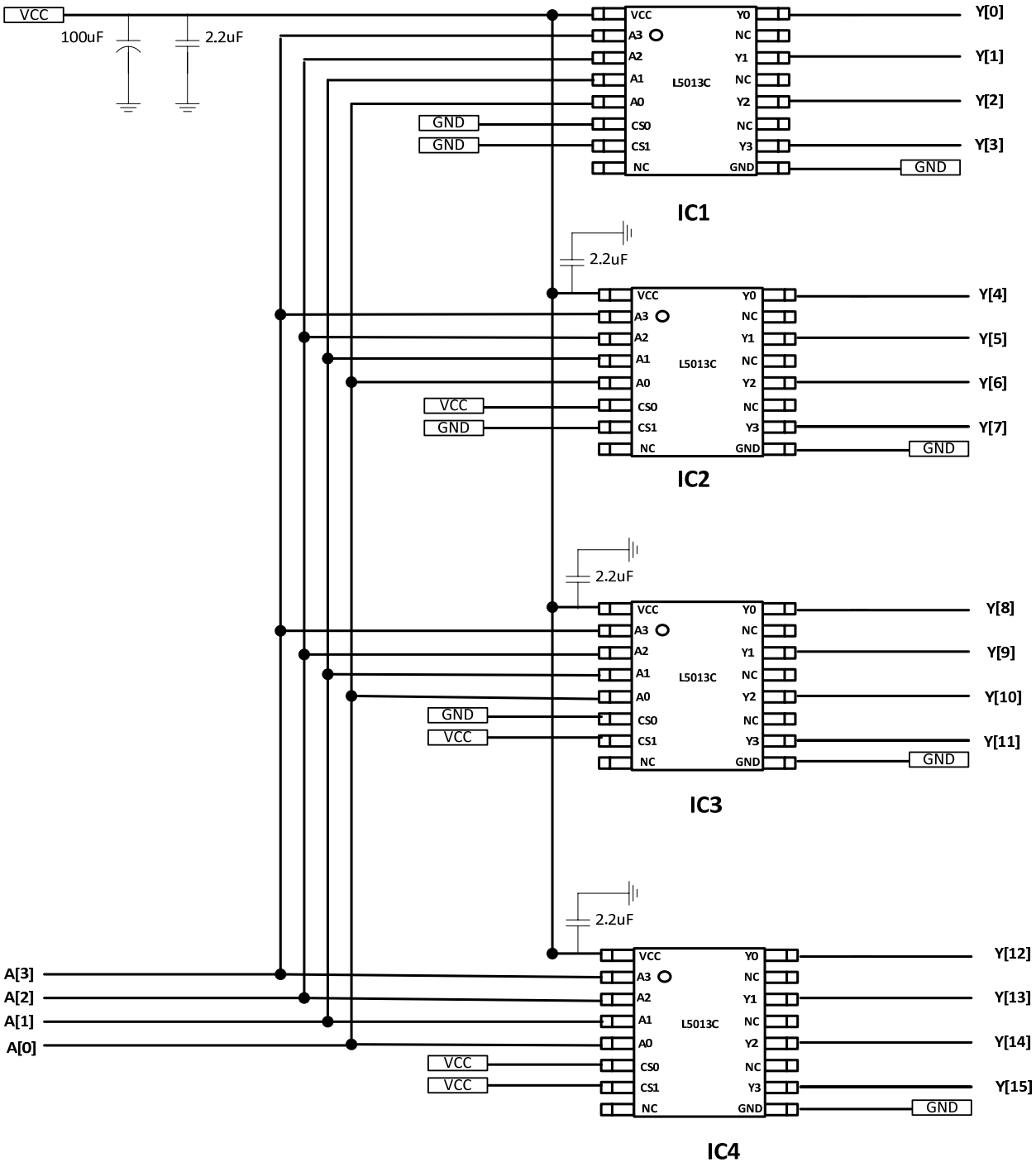
Duty=1/8 application



True table

Input			Output							
A[0]	A[1]	A[2]	Y[0]	Y[1]	Y[2]	Y[3]	Y[4]	Y[5]	Y[6]	Y[7]
0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Duty=1/16 application



True table

Input				Output							
A[0]	A[1]	A[2]	A[3]	Y[0]	Y[1]	Y[2]	Y[3]	Y[4]	Y[5]	Y[6]	Y[7]
0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0
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1	1	1	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0
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1	1	0	1	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0

Input				Output							
A[0]	A[1]	A[2]	A[3]	Y[8]	Y[9]	Y[10]	Y[11]	Y[12]	Y[13]	Y[14]	Y[15]
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
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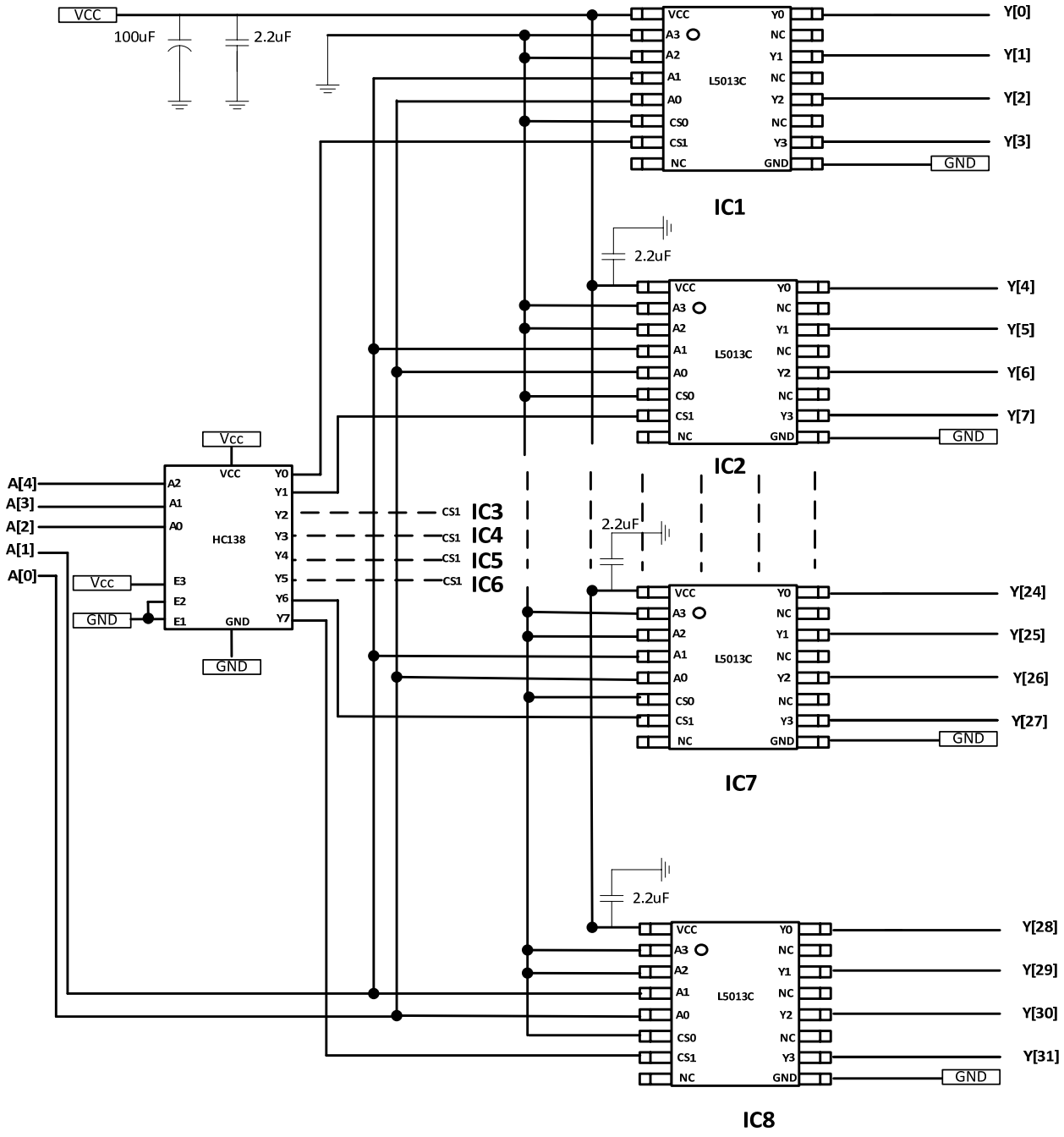
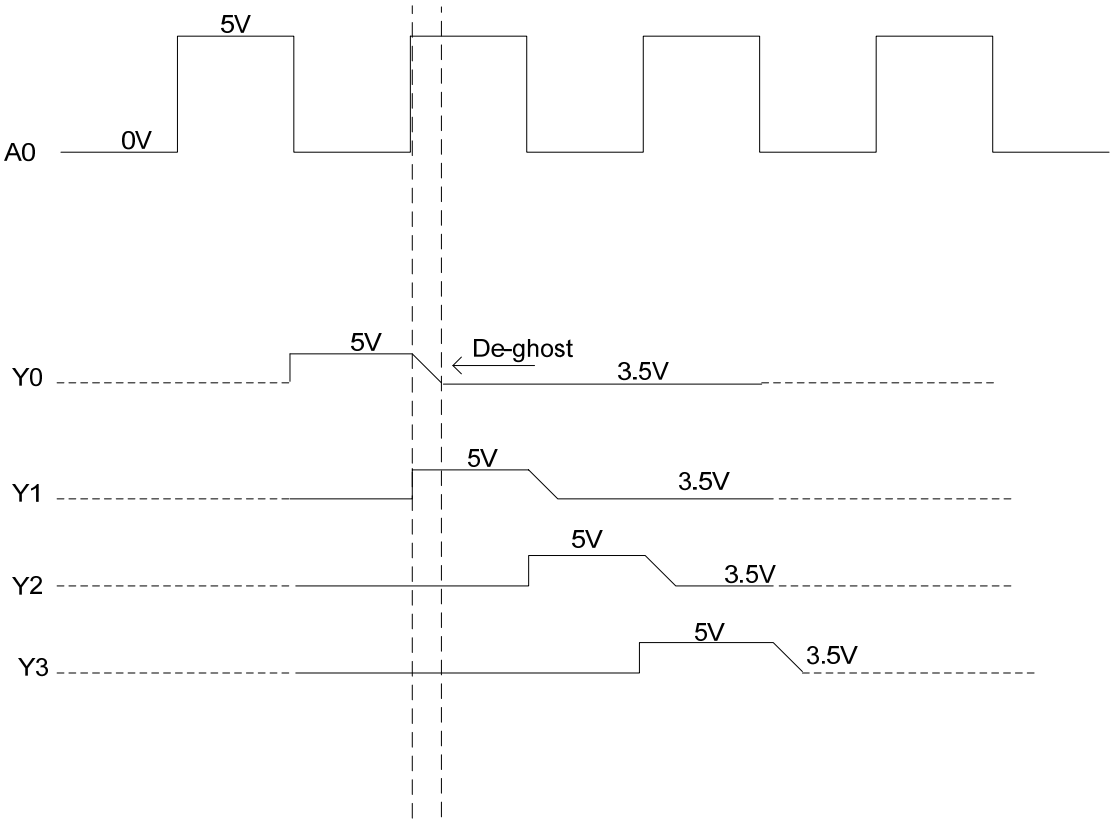
0	1	1	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Duty=1/32 application



Application Information

De-ghost Function Descriptions



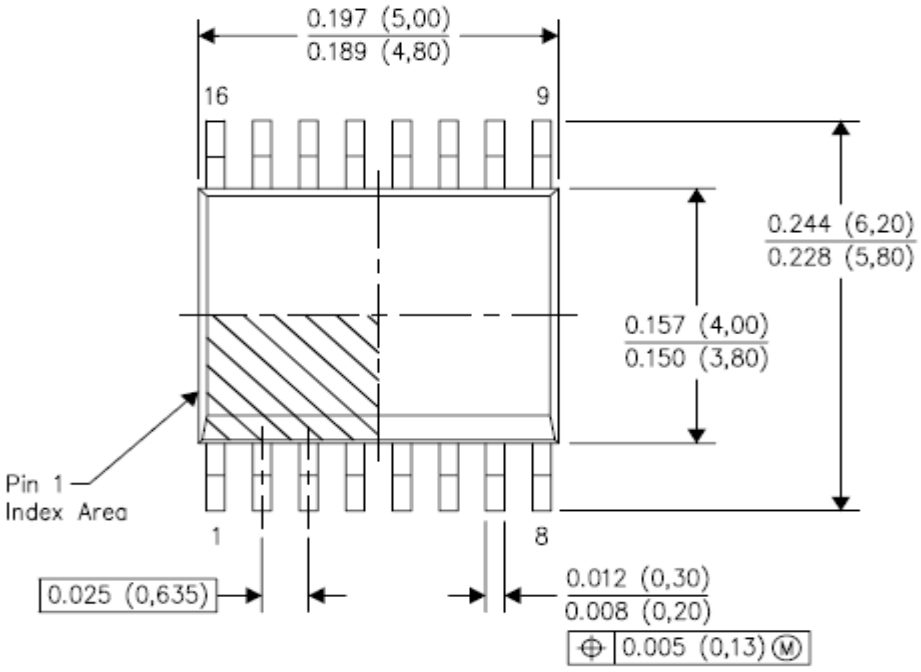
When the output turn off ,it will be De-ghost, the De-ghost level is 70%Vcc

Layout Guidelines

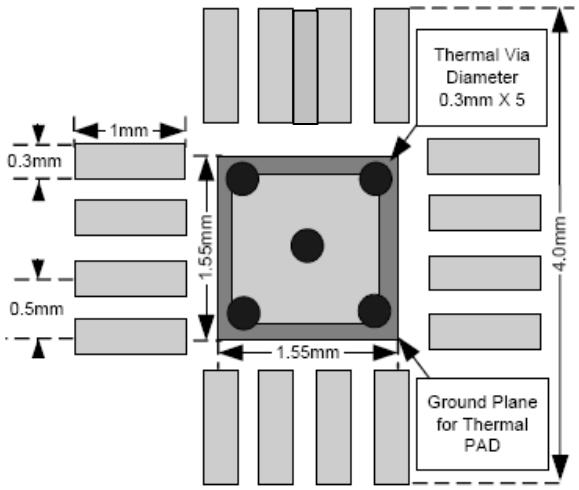
- All components should be placed close to the SPL5013C.For example; the input capacitor should be close to SPL5013C's Vcc pins to decouple the power rail noise.
- The output traces should be short, wide (>60mil),symmetric.
- The power trace width should be greater than 60mil.

.

PCB Drawings



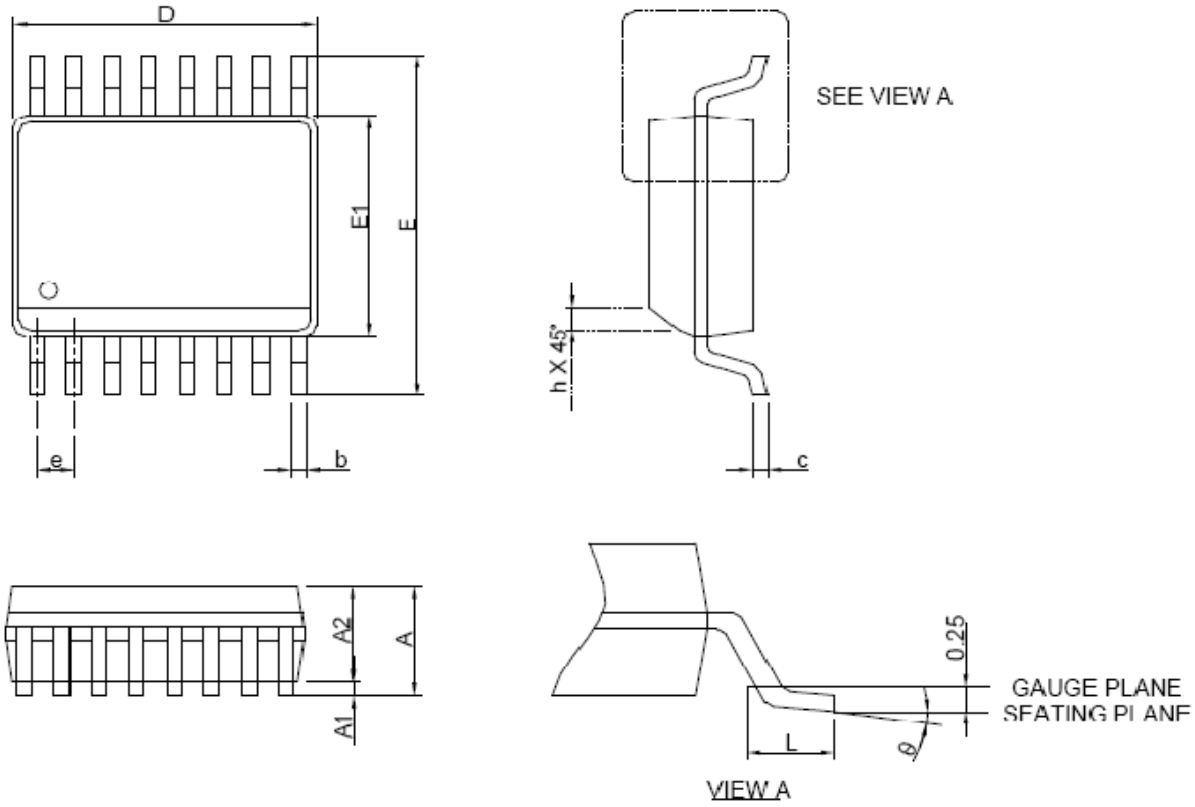
Vcc short on PCB



TQFN3x3-16 Layout Recommendation

Package Information

SSOP-16

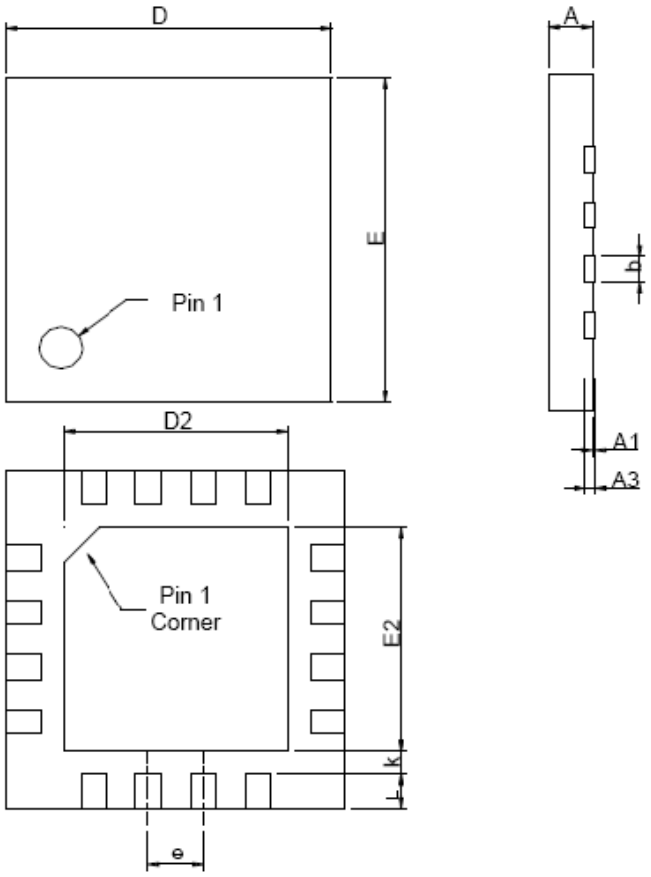


SYMBOL	SSOP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.24		0.049	
b	0.20	0.30	0.008	0.012
c	0.15	0.25	0.006	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	0.635 BSC		0.025 BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC MO-137 AB.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

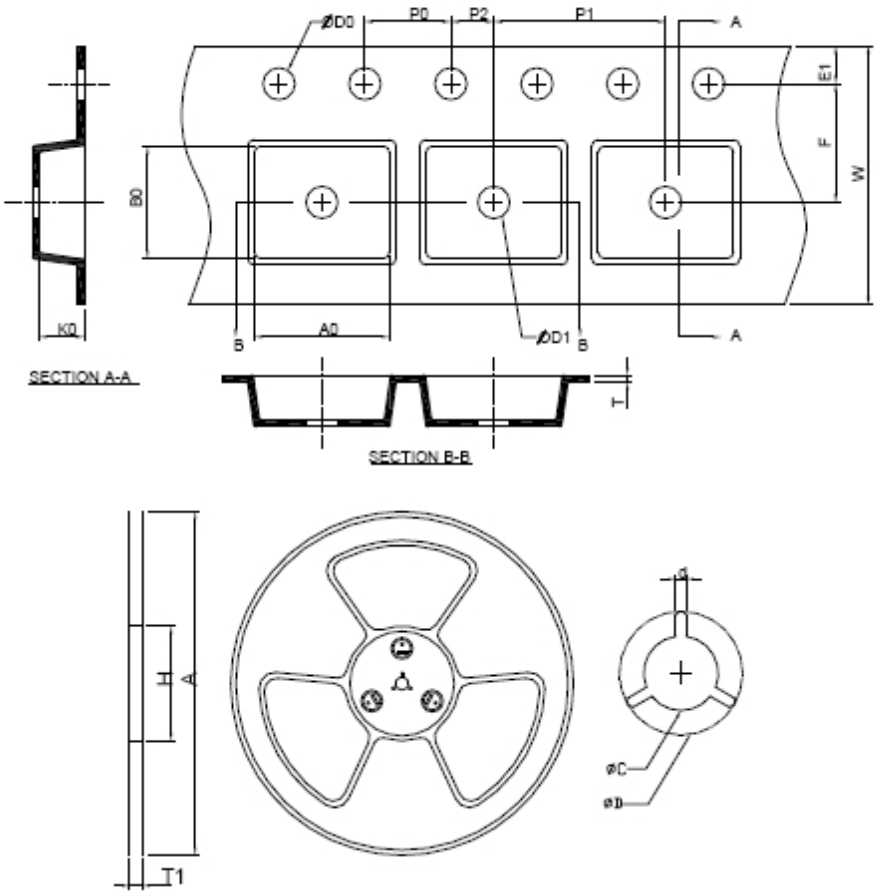
Package Information

TQFN3×3-16



SYMBOL	TQFN3x3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SSOP-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

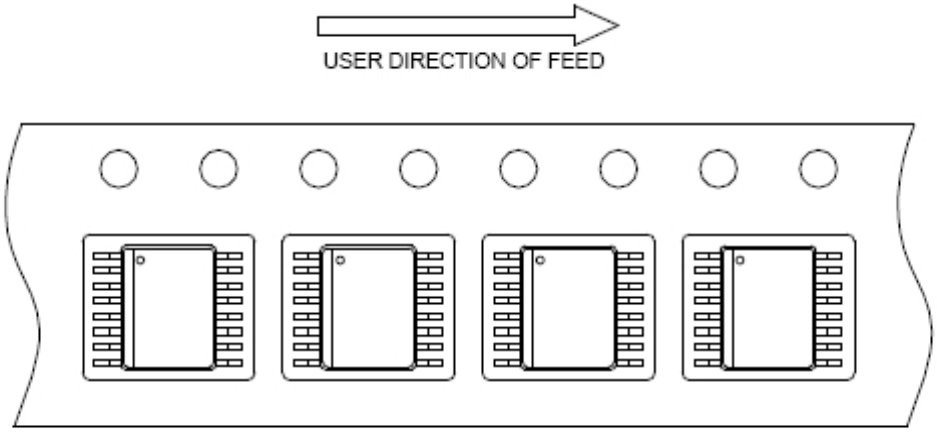
(mm)

Devices Per Unit

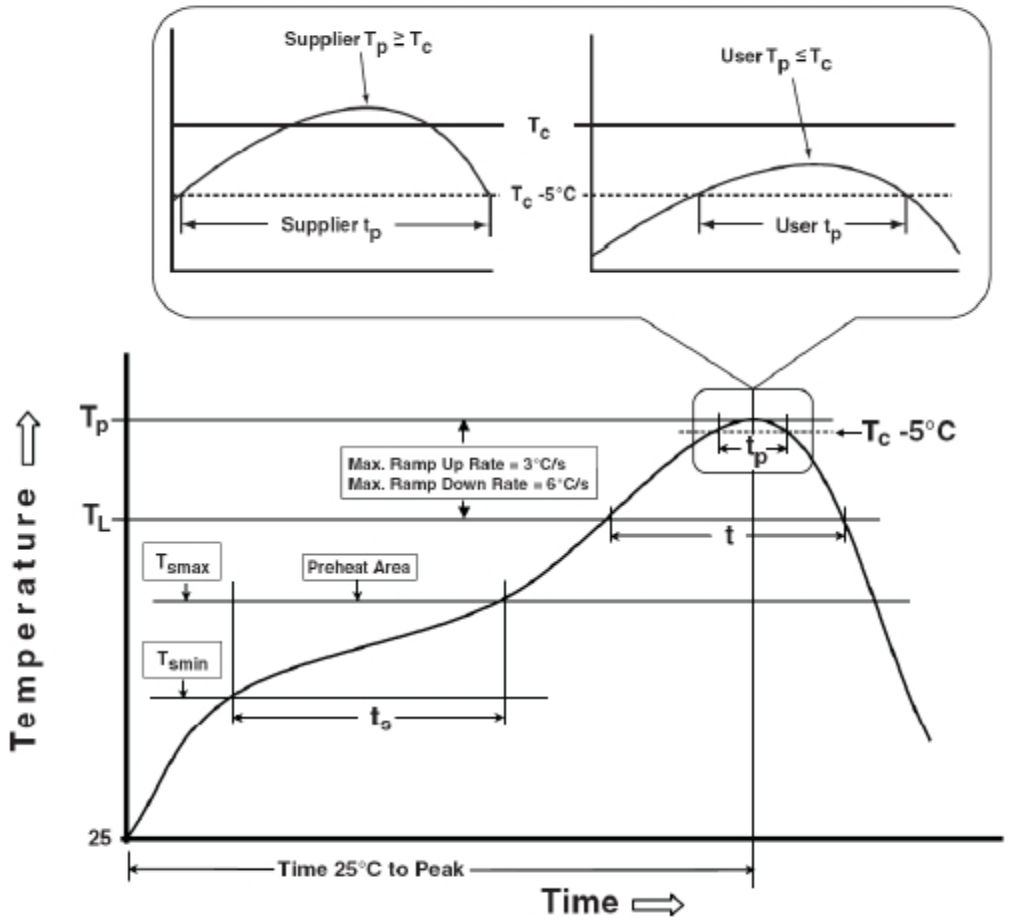
Package Type	Unit	Quantity
SSOP- 16	Tape & Reel	2500

Taping Direction Information

SSOP-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Customer Service

Supec (Suzhou) Co., Ltd

Head Office:

Room C502,1355 Jinjihu Avenue,
Suzhou Industrial Park, P.R. China

Tel: 0512-62522212
Fax: 0512-62522126

Shenzhen Office :

B-701 Hi-Tech Venture Park,Tian'an Cyber Park,
Futian District, Shenzhen,P.R.China

Tel : 0755-82049356
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