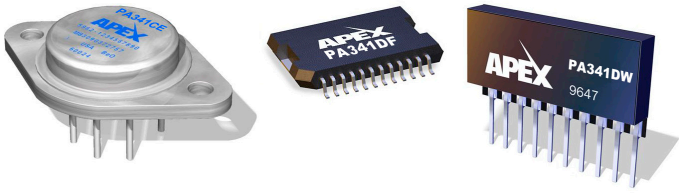
PA341

High Voltage Power Operational Amplifier

RoHS COMPLIANT

FEATURES



- RoHS Compliant
- Monolithic MOS Technology
- Low Cost
- High Voltage Operation 350V
- Low Quiescent Current Typ. 2.2mA
- No Second Breakdown
- High Output Current 120mA PEAK
- Available in Die Form CPA341

APPLICATIONS

- Piezo Electric Positioning
- Electrostatic Transducer and Deflection
- Deformable Mirror Focusing
- Biochemistry Stimulators
- Computer to Vacuum Tube Interface

DESCRIPTION

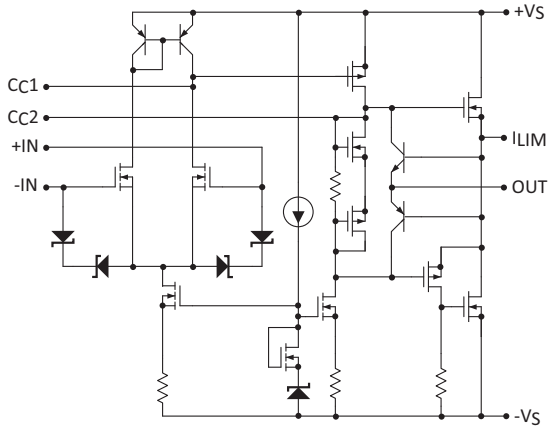
The PA341 is a high voltage monolithic MOSFET operational amplifier which achieves performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitation and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA341CE is packaged in a hermetically sealed 8-pin TO-3 package. The metal case of the PA341CE is isolated in excess of full supply voltage.

The PA341DF is packaged in a 24 pin PSOP (JEDEC MO-166) package. The metal heat slug of the PA341DF is isolated in excess of full supply voltage.

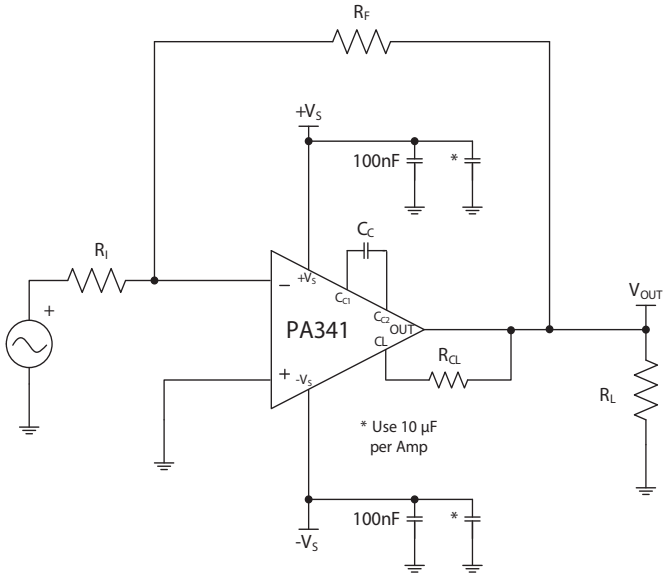
The PA341DW is packaged in Apex Microtechnology's hermetic ceramic SIP. The alumina ceramic isolates the die in excess of full supply voltage.

Figure 1: Equivalent Schematic



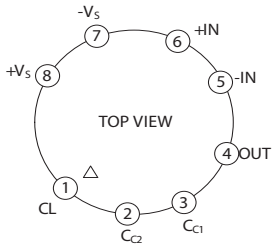
TYPICAL CONNECTION

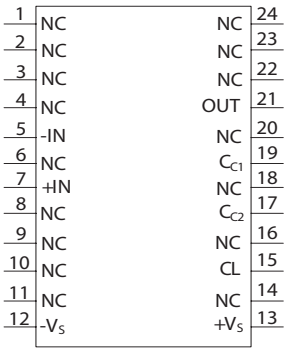
Figure 2: Typical Connection

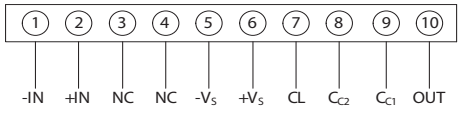


PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections







PA341CE PA341DF PA341DW

For C_C values, see graphs on page 8 & 9.

Note: C_C must be rated for full supply voltage.

Note: PA341CE Recommended mounting torque is 4-7 in•lbs (0.45 - 0.79 N•m)

CAUTION: The use of compressible, thermally conductive insulators may void warranty.

PA341CE

Pin Number	Name	Description
1	CL	Connect to the current limit resistor. Output current flows into/out of this pin through R_{CL}. The output pin and the load are connected to the other side of R_{CL}.
2, 3	CC	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
4	OUT	The output. Connect this pin to load and to the feedback resistors.
5	-IN	The inverting input.
6	+IN	The non-inverting input.
7	-Vs	The negative supply rail.
8	+Vs	The positive supply rail.

PA341DF

Pin Number	Name	Description
5	-IN	The inverting input.
7	+IN	The non-inverting input.
12	-Vs	The negative supply rail.
13	+Vs	The positive supply rail.
15	CL	Connect to the current limit resistor. Output current flows into/out of this pin through R_{CL}. The output pin and the load are connected to the other side of R_{CL}.
17, 19	CC	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
21	OUT	The output. Connect this pin to load and to the feedback resistors.
All Others	NC	No connection.

PA341DW

Pin Number	Name	Description
1	-IN	The inverting input.
2	+IN	The non-inverting input.
3, 4	NC	No connection.
5	-Vs	The negative supply rail.
6	+Vs	The positive supply rail.
7	CL	Connect to the current limit resistor. Output current flows into/out of this pin through R_{CL}. The output pin and the load are connected to the other side of R_{CL}.
8, 9	CC	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
10	OUT	The output. Connect this pin to load and to the feedback resistors.

SPECIFICATIONS

Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	PA341CE		PA341DF		PA341DW		Units
		Min	Max	Min	Max	Min	Max	
Supply Voltage, total	$+V_s$ to $-V_s$		350		*		*	V
Output Current, continuous within SOA	I_O		60		*		*	mA
Output Current, peak			120		*		*	mA
Power Dissipation, continuous @ T_c = 25°C	P_D		12		*		9	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-16	+16	*	*	*	*	V
Input Voltage, common mode	V_{cm}	$-V_S$	$+V_S$	*	*	*	*	V
Temperature, pin solder, 10s max.			350		220		220	°C
Temperature, junction [1]	T_J		150		*		*	°C
Temperature, storage		-65	+150	*	*	*	*	°C
Temperature Range, powered (case)	T_C	-40	125	*	*	*	*	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.

CAUTION The PA341 is constructed from MOSFET transistors. ESD handling procedures must be observed.
The substrate (DW package) contains beryllia (BeO). Do not crush, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA341CE, PA341DF			PA341DW			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			12	40		*	*	mV
Offset Voltage vs. temperature [1]	25° to 85°C		17	250		*	*	µV/°C
Offset Voltage vs. temperature [1]	-25° to 25°C		18	500		*	*	µV/°C
Offset Voltage vs. supply			4.5			*		µV/V
Offset Voltage vs. time			80			*		µV/kh
Bias Current, initial [2]			5/50	50/200		100	2000	pA
Bias Current vs. supply			0.2/2			15	50	pA/V
Offset Current, initial [2]			2.5/50	50/200		100	1000	pA
Input Impedance, DC			10^{11}			*		Ω
Input Capacitance			3			*		pF
Common Mode, voltage range		$+V_S$-12			*			V
Common Mode, voltage range		$-V_S$+12			*			V
Common Mode Rejection, DC	V_{CM} = ±90V DC	84	115		*	*		dB
Noise, broad band	10 kHz BW, R_S = 1 kΩ		337			*		µV RMS

1. Sample tested by wafer to 95%.
2. Specifications separated by / indicate values for the PA341CE and PA341DF respectively.

GAIN

Parameter	Test Conditions	PA341CE, PA341DF			PA341DW			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop @ 15 Hz	R_L = 5k Ω	90	103		*	*		dB
Bandwidth, gain bandwidth product	@ 1 MHz		10			*		MHz
Power Bandwidth	280V p-p		35			*		kHz

OUTPUT

Parameter	Test Conditions	PA341CE, PA341DF			PA341DW			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing	I_O = 40mA	$\pm V_S$-12	$\pm V_S$-10		*	*		V
Current, peak [1]		120			*			mA
Current, continuous		60			*			mA
Settling Time to 0.1%	10V step A_V =-10		2			*		µs
Slew Rate	C_C = 4.7pF		32			*		V/µs
Resistance, 10mA [2]	R_{CL} = 0 Ω		91			*		Ω
Resistance, 40mA [2]	R_{CL} = 0 Ω		65			*		Ω

1. Guaranteed but not tested.
2. The selected value of R_{CL} must be added to the values given for total output resistance.

POWER SUPPLY

Parameter	Test Conditions	PA341CE, PA341DF			PA341DW			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage		±10	±150	±175	*	*	*	V
Current, quiescent			2.2	2.5		*	*	mA

THERMAL

Parameter	Test Conditions	PA341CE, PA341DF			PA341DW			Units
		Min	Typ	Max	Min	Typ	Max	
PA341CE Resistance, AC junction to case	F > 60 Hz		5.4	6.5				°C/W
PA341DF Resistance, AC junction to case	F > 60 Hz		6	7				°C/W
PA341DW Resistance, AC junction to case	F > 60 Hz					7	10	°C/W
PA341CE Resistance, DC junction to case	F < 60 Hz		9	10.4				°C/W
PA341DF Resistance, DC junction to case	F < 60 Hz		9	11				°C/W
PA341DW Resistance, DC junction to case	F < 60 Hz					12	14	°C/W
PA341CE Resistance, junction to air	Full temp range		30					°C/W
PA341DF Resistance, junction to air [1]	Full temp range		25					°C/W
PA341DW Resistance, junction to air	Full temp range					30		°C/W
Temperature Range, case	Meets full range spec's	-25		+85	*		*	°C

1. Rating applies with solder connection of heatslug to a minimum 1 square inch foil area of the printed circuit board.

Note: *The specification of PA341DW is identical to the specification for PA341CE, PA341DF in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

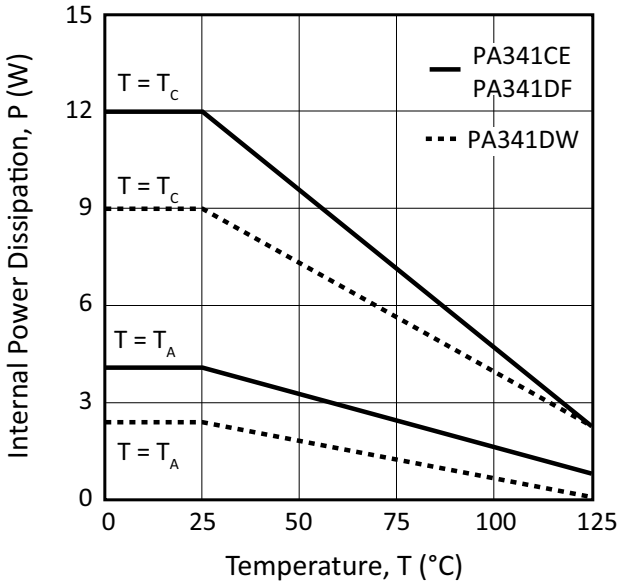


Figure 5: V_{BE} for I_{LIMIT}

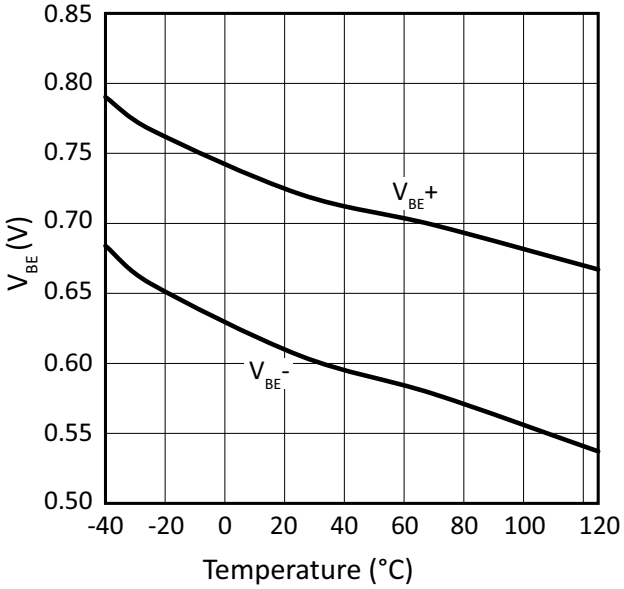


Figure 6: Small Signal Response

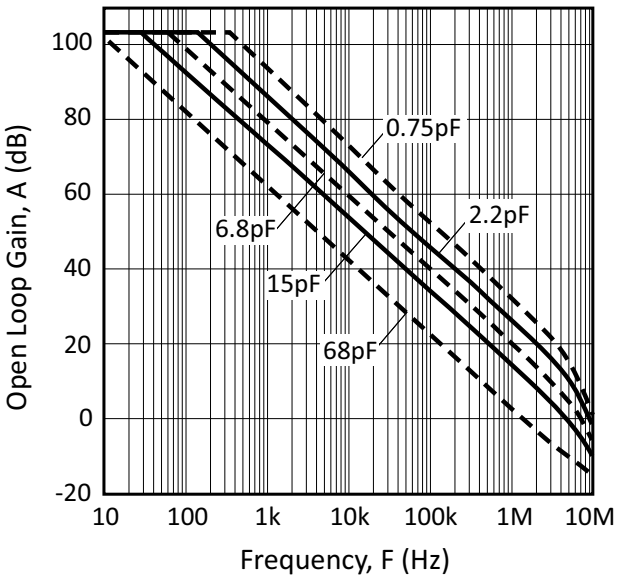


Figure 7: Phase Response

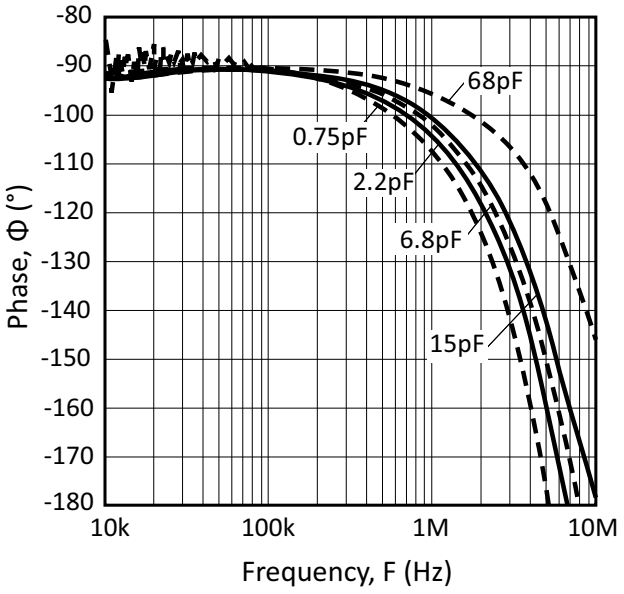


Figure 8: Gain and Compensation

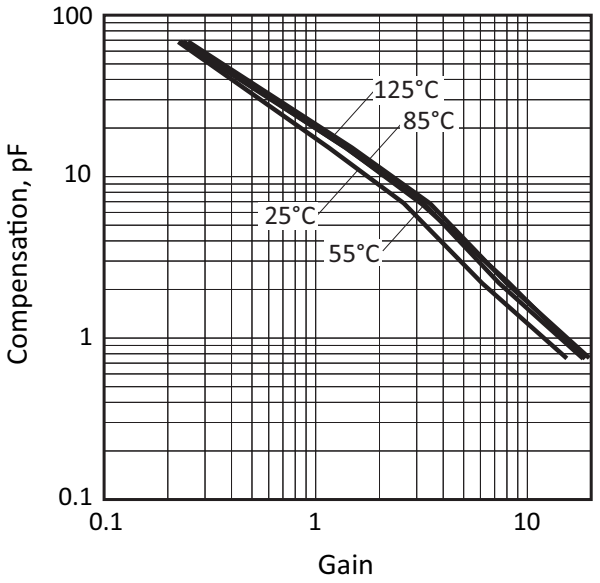


Figure 9: Power Response

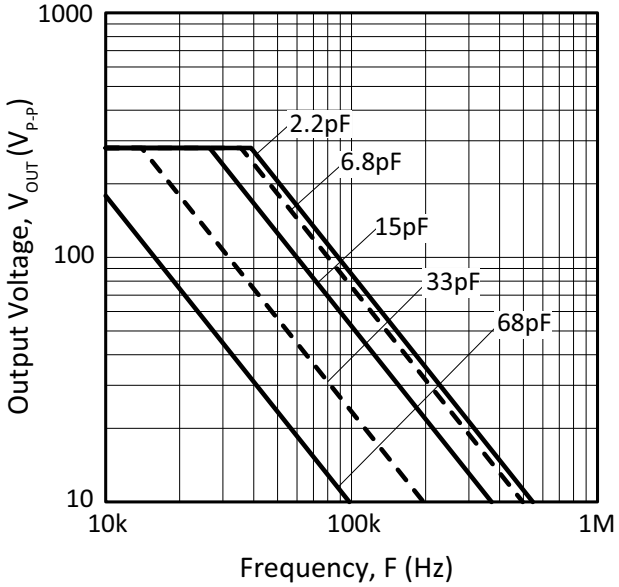


Figure 10: Harmonic Distortion

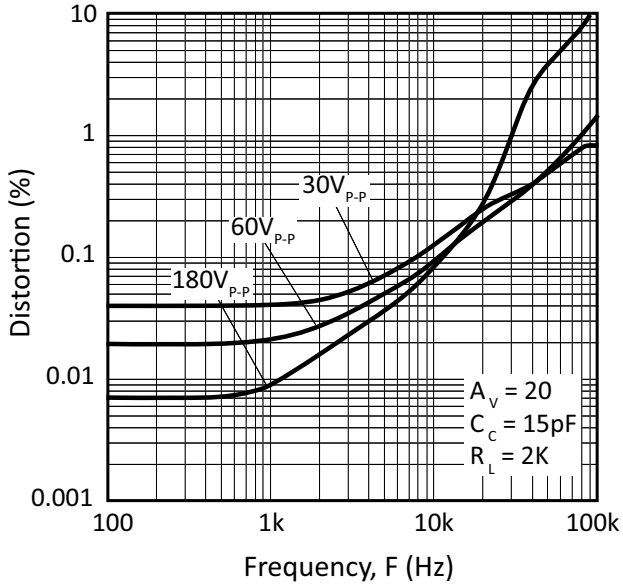


Figure 11: Slew Rate

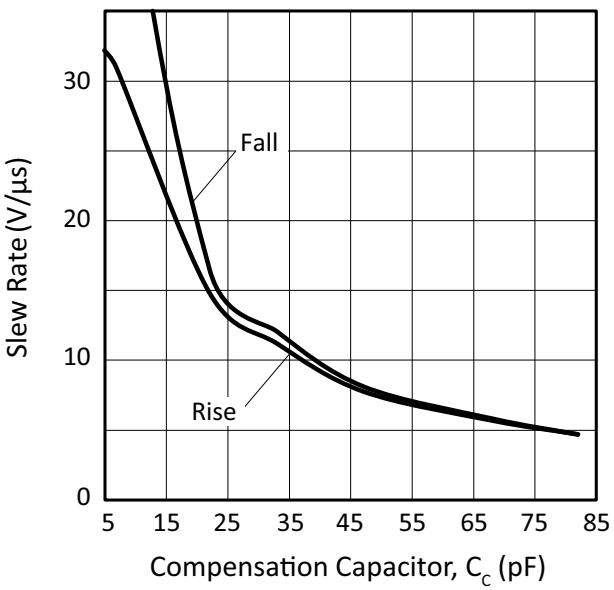


Figure 12: Quiescent Current

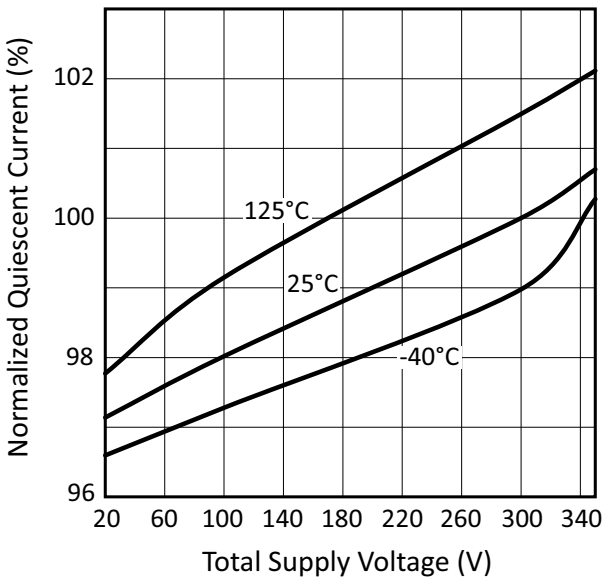


Figure 13: Common Mode Rejection

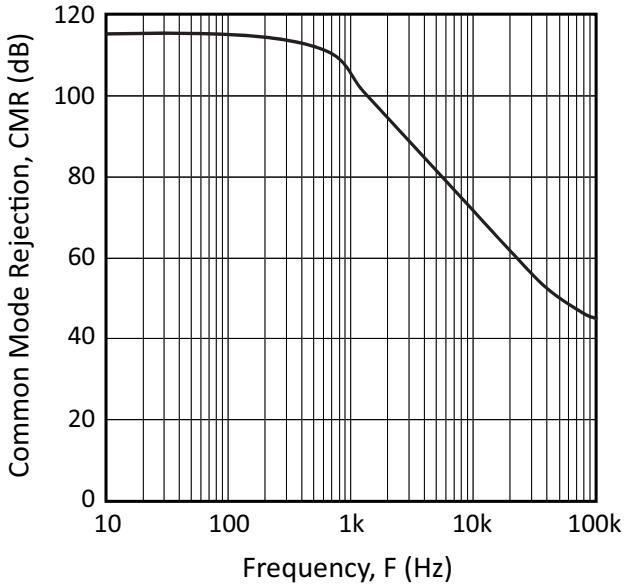


Figure 14: Power Supply Rejection

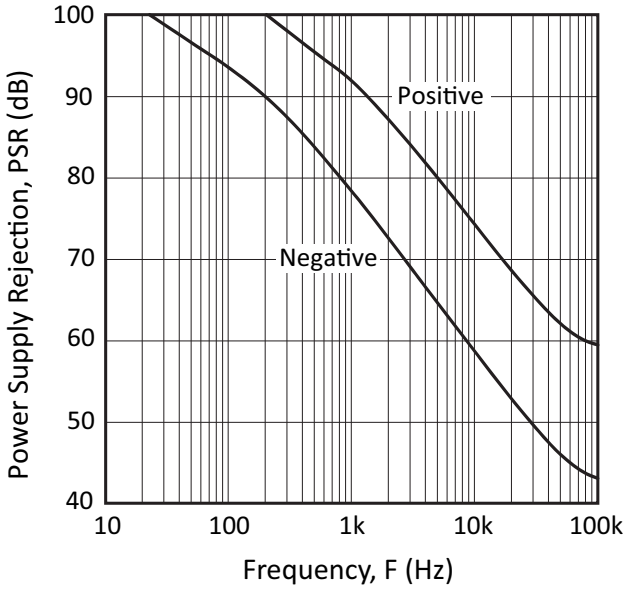
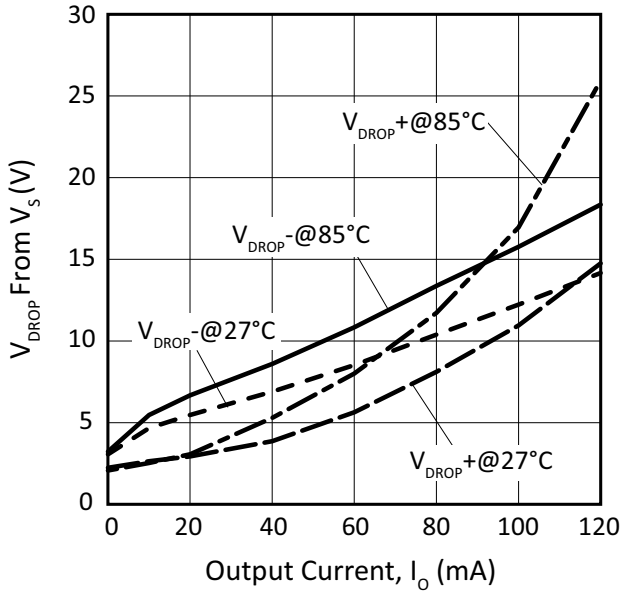


Figure 15: Output Voltage Swing



SAFE OPERATING AREA (SOA)

The MOSFET output stage of the PA341 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metalization.
3. Temperature of the output MOSFETS.

These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown for a case temperature of 25°C and correspond to thermal resistances of 5.2°C/W for the PA341CE and DF and 10.4°C/W for the PA341DW respectively. Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

Figure 16: PA341CE and DF SOA

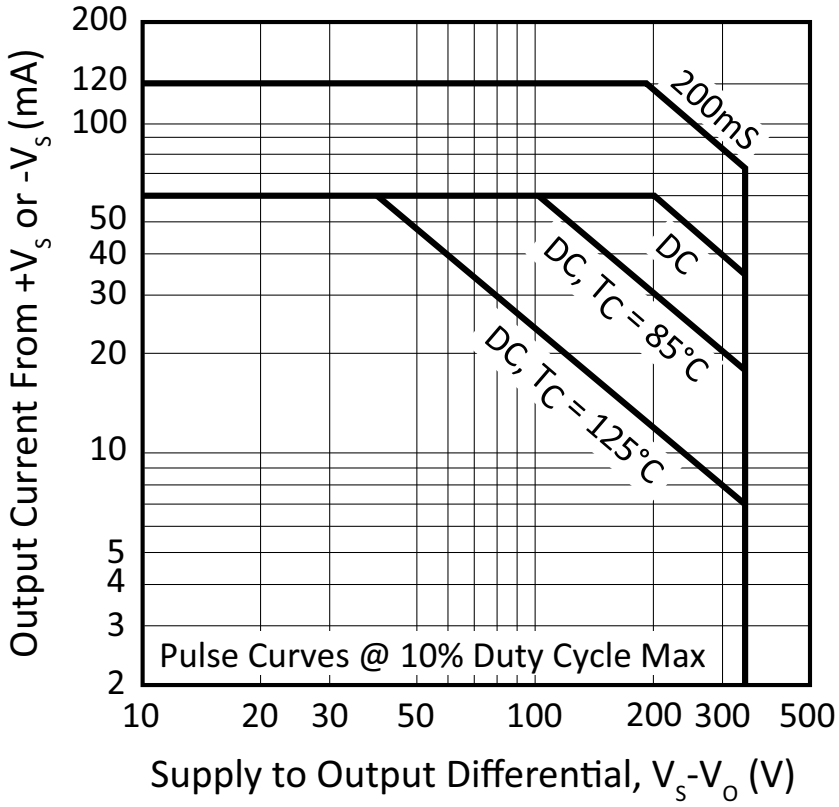
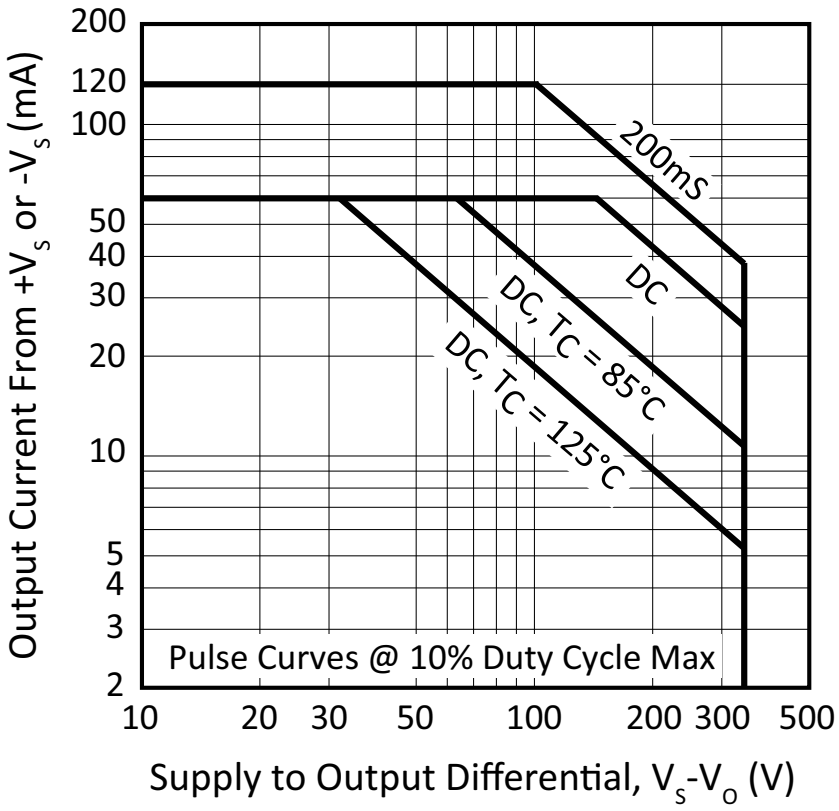


Figure 17: PA341DW SOA



GENERAL

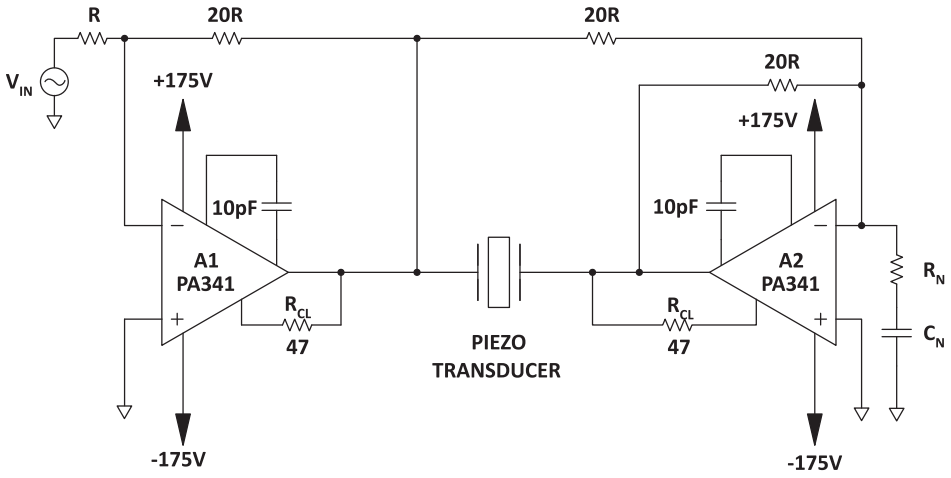
Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Ref: APPLICATION NOTE 20: “Bridge Mode Operation of Power Amplifiers”

Two PA341 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 V total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

Figure 18: Typical Application (Low Cost 660 V_{P-P} Piezo Driver)



PHASE COMPENSATION

Open loop gain and phase shift both increase with increasing temperature. The PHASE COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are based on achieving a phase margin of 50°. Calculate the highest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the finished circuit. The compensation capacitor must be rated for at least the total voltage applied to the amplifier and should be a temperature stable type such as NPO or COG.

OTHER STABILITY CONCERNS

There are two important concepts about closed loop gain when choosing compensation. They stem from the fact that while “gain” is the most commonly used term, ß (the feedback factor) is really what counts when designing for stability.

1. Gain must be calculated as a non-inverting circuit (equal input and feedback resistors can provide a signal gain of -1, but for calculating offset errors, noise, and stability, this is a gain of 2).

2. Including a feedback capacitor changes the feedback factor or gain of the circuit. Consider R_{IN}=4.7k, R_F=47k for a gain of 11. Compensation of 4.7 to 6.8pF would be reasonable. Adding 33pF parallel to the 47K rolls off the circuit at 103 kHz, and at 2 MHz has reduced gain from 11 to roughly 1.5 and the circuit is likely to oscillate.

As a general rule the DC summing junction impedance (parallel combination of the feedback resistor and all input resistors) should be limited to 5k ohms or less. The amplifier input capacitance of about 6pF, plus capacitance of connecting traces or wires and (if used) a socket will cause undesirable circuit performance and even oscillation if these resistances are too high. In circuits requiring high resistances, measure or estimate the total sum point capacitance, multiply by R_{IN}/R_F, and parallel R_F with this value. Capacitors included for this purpose are usually in the single digit pF range. This technique results in equal feedback factor calculations for AC and DC cases. It does not produce a roll off, but merely keeps ß constant over a wide frequency range. Paragraph 6 of Application Note 19 details suitable stability tests for the finished circuit.

CURRENT LIMIT

For proper operation, the current limiting resistor, R_{CL}, must be connected as shown in Figure 2, “Typical Connections”. The current limit can be predicted as follows:

$$I_{LIMIT}(A) = \frac{V_{BE}}{R_{CL}(\Omega)}$$

The “V_{BE} for I_{LIMIT}” performance graph is used to find V_{BE}. On this graph, the V_{BE}+ and V_{BE}– curves show the voltages across the current limiting resistor at which current limiting is turned on. The V_{BE}+ curve shows these turn-on voltages when the amplifier is sourcing current, and the V_{BE}– curve shows these voltages when the amplifier is sinking current.

The current limit can be thought of as a ceiling or limit for safe operation. For continuous operation it is any value between the desired load current and 60 mA (as long as the curves on the SOA graph are not exceeded, please refer to Safe Operating Area). As an example, suppose the desired load current for the application is 20 mA. In this case we may set a current limit of 30 mA. Starting with the smaller V_{BE}^- of 0.6 we have:

$$R_{CL} = \frac{0.6V}{1.03} = 20\Omega$$

For the larger V_{BE}^+ this R_{CL} resistor will allow for a maximum current of:

$$I_{LIMIT}(A) = \frac{0.7V}{20} = 35mA$$

This value is still acceptable because it is less than 60 mA. For the case of continuous load currents, check that the current limit does not exceed 60 mA.

The V_{BE} values used above are approximate and can vary with process. To allow for this possibility the user can reduce the V_{BE} = 0.6 value by 20%. This results in a R_{CL} value of 16 Ω. Using this same R_{CL} value and allowing for a 20% increase in the other V_{BE}, the current limit maximum is 52 mA.

The absolute minimum value of the current limiting resistor is bounded by the largest current and the largest V_{BE} in the application. The largest V_{BE} is determined by the coldest temperature in the application. In general the largest V_{BE} is V_{BE}+ = 0.78V, which occurs at T = − 40°C. The largest allowed current occurs in pulsed applications where, from the SOA graph, we can see current pulses of 120 mA. This gives us an absolute minimum R_{CL} value of 0.78V/0.12 (A) = 6.5 Ω.

HEATSINKING

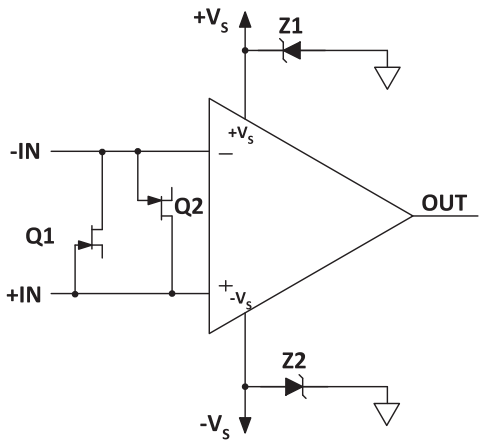
The PA341DF package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area, on the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA341DF. Solder connection to an area of 1 to 2 square inches is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.

OVERVOLTAGE PROTECTION

Although the PA341 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 19. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.
In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 19.

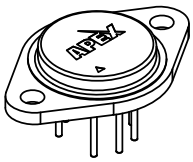
Figure 19: Overvoltage Protection

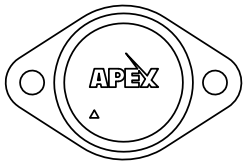


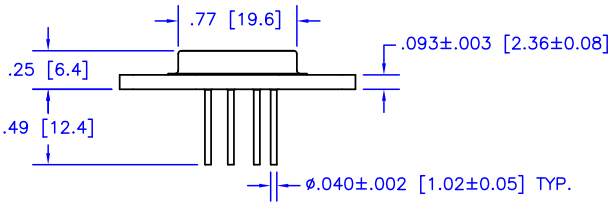
PACKAGE OPTIONS

Part Number	Apex Package Style	Description
PA341CE	CE	8-pin TO-3
PA341DF	DF	24-pin MO-166
PA341DW	DW	10-pin SIP

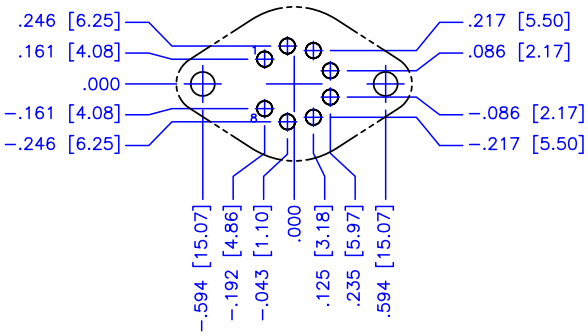
PACKAGE STYLE CE

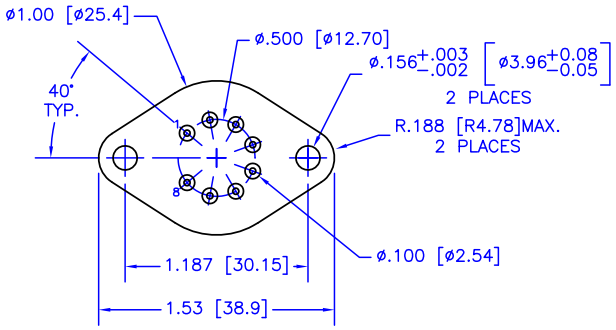






Ordinate dimensions for CAD layout

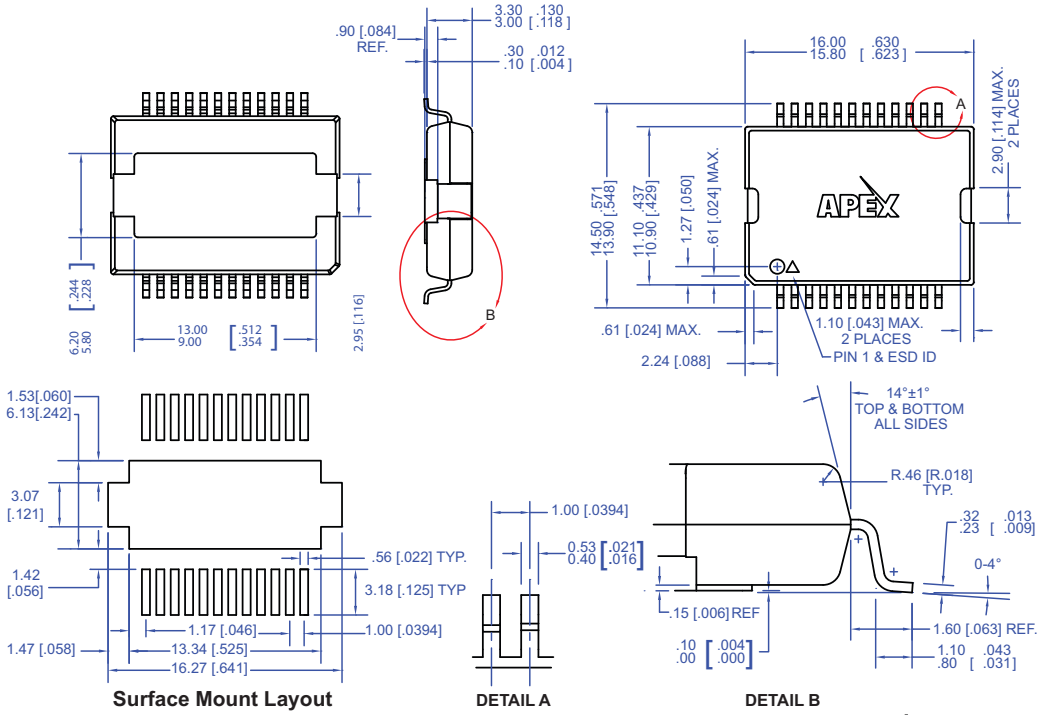




NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel–plated Alloy 52.
6. Header material: Nickel–plated cold–rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

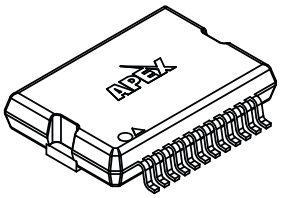
PACKAGE STYLE DF



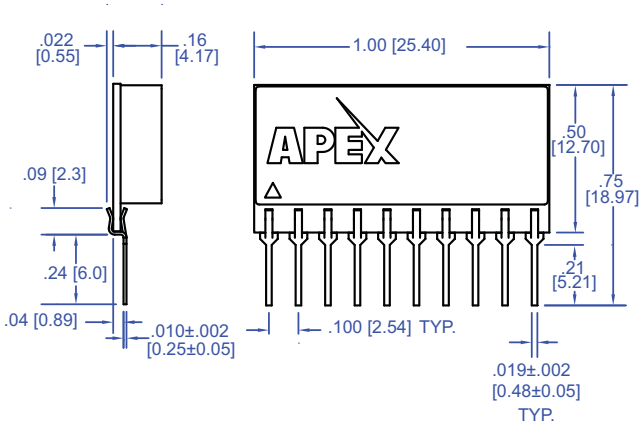
Surface Mount Layout **DETAIL A** **DETAIL B**

NOTES:

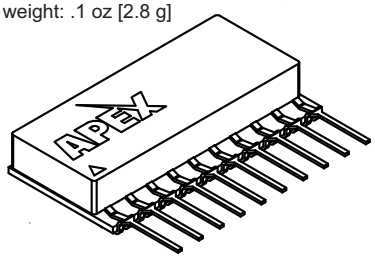
1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Dimple on lid & ESD triangle denote pin 1.
4. Pins & Heat Slug: CDA 194 copper with bismuth solder finish
5. Mold compound: MP-8000AN epoxy
6. Package weight: .086 oz. [2.44 g]
7. Suggested surface mount layout for reference only.



PACKAGE STYLE DW



NOTES:
1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin
   tin (150 - 300µ") over nickel (50 µ" max.) underplate.
4. Package Material: Alumina with hermetic glass seal.
5. Package weight: .1 oz [2.8 g]



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