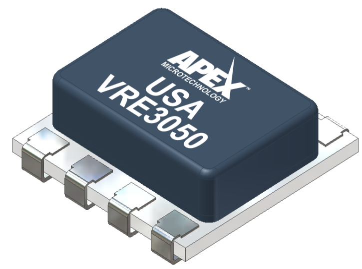
APEX MICROTECHNOLOGY
PRECISION • POWER • ANALOG

VRE3050

RoHS COMPLIANT

Precision Voltage Reference

FEATURES



- +5 V Output, ± 0.5 mV (0.01%)
- Temperature Drift: 0.6 ppm/°C
- Low Noise: 3 μV_{P-P} (0.1 Hz - 10 Hz)
- Low Thermal Hysteresis: 1 ppm Typical
- ±15mA Output Source and Sink Current
- Excellent Line Regulation: 5 ppm/V Typical
- Optional Noise Reduction and Voltage Trim
- Industry Standard Pinout: 8-pin Surface Mount Package

APPLICATIONS

The VRE3050 is recommended for use as a reference for 14, 16, or 18 bit data converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution data converters. The VRE3050 offers superior performance over monolithic references.

DESCRIPTION

The VRE3050 is a low cost, high precision 5 V reference that operates from +10 V. The device features a buried zener for low noise and excellent long term stability. Packaged in an 8-pin SMT, the device is ideal for high resolution data conversion systems.

The device provides ultrastable +5 V output with ±0.5 mV (0.01%) initial accuracy and a temperature coefficient of 0.6 ppm/°C. This improvement in accuracy is made possible by a unique, patented multi-point laser compensation technique. Significant improvements have been made in other performance parameters as well, including initial accuracy, warm-up drift, line regulation, and long-term stability, making the VRE3050 series the most accurate reference available.

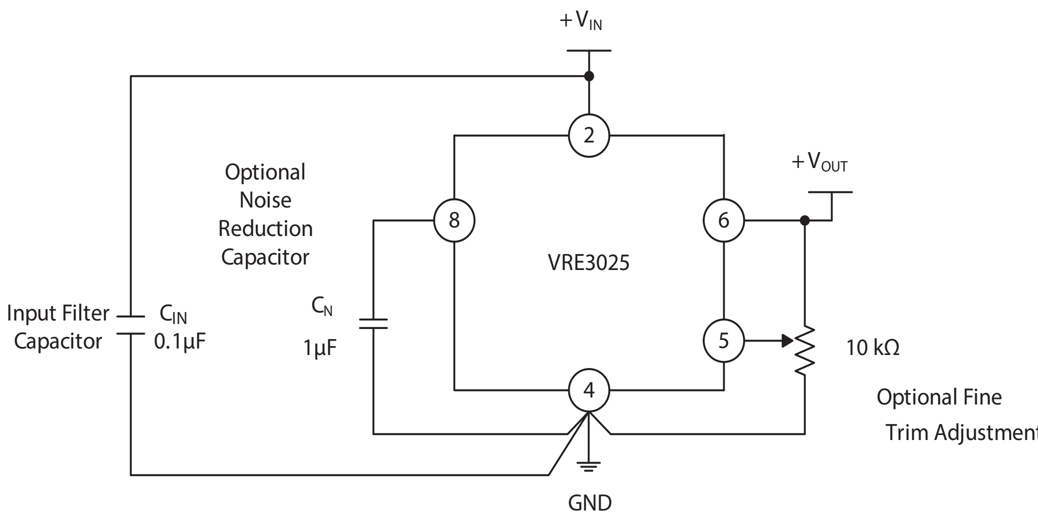
For enhanced performance, the VRE3050 has an external trim option for users who want less than 0.01% initial error. For ultra low noise applications, an external capacitor can be attached between the noise reduction pin and the ground pin. A ceramic input filter capacitor of 0.1µF is recommended to ensure output stability.

SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/°C)	Temp Range (°C)
VRE3050BS	±0.8	1.0	0°C to +70°C
VRE3050JS	±0.5	0.6	-40°C to +85°C
VRE3050LS	±1.0	2.0	-40°C to +85°C

TYPICAL CONNECTION

Figure 1: Typical Connection



PIN DESCRIPTIONS

Pin Number	Name	Description
1, 3, 7	NC	No connection.
2	V_{IN}	The supply voltage connection.
4	GND	Ground.
5	TRIM	Optional fine adjustment. Connect to a voltage divider between OUT and GND.
6	OUT	5 V output.
8	NR	Optional noise reduction. Connect a 1µF capacitor between this pin and GND.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Power Supply	V_{IN}	-0.3	+40	V
Out, Trim		-0.3	+12	V
Noise Reduction	NR	-0.3	+6	V
Operating Temp. (B)		0	+70	°C
Operating Temp. (J, L)		-40	+85	°C
Out Short Circuit to GND Duration (V_{IN}<12V)			Continuous	s
Out Short Circuit to GND Duration (V_{IN}<40V)			5	s
Out Short Circuit to IN Duration (V_{IN}<12V)			Continuous	s
Continuous Power Dissipation (T_A=+70°C)			300	mW
Storage Temperature		-65	+150	°C
Lead Temperature (soldering, 10 sec)			+250	°C

ELECTRICAL SPECIFICATIONS

V_{IN} =+15V, T = +25°C, R_L = 10 kΩ unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		+8		+36	V
Output Voltage[1]	V_{OUT}	VRE3050JS	+4.9995	+5.0000	+5.0005	V
		VRE3050BS	+4.9992	+5.0000	+5.0008	
		VRE3050LS	+4.9990	+5.0000	+5.0010	
Output Voltage Temperature Coefficient[2]	TCV_{OUT}	VRE3050JS		0.3	0.6	ppm/°C
		VRE3050BS		0.5	1.0	
		VRE3050LS		1.0	2.0	
Trim Adjustment Range	ΔV_{OUT}	Figure 1		±5.0		mV
Turn-On Setting Time	T_{ON}	To 0.01% of final value		2.0		µs
Output Noise Voltage	e_n	0.1 Hz < f< 10 Hz		3.0		µVp-p
		10 Hz < f< 1 kHz		2.5	5.0	μV_{RMS}
Temperature Hysteresis[3]				1		ppm
Long Term Stability	$\Delta V_{OUT}/t$			6		ppm/ 1000hrs.
Supply Current	I_{IN}			5	7	mA
Load Regulation [4]	$\Delta V_{OUT}/ \Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 15mA		8	12	ppm/mA
		Sinking: -15mA ≤ I_{OUT} ≤ 0mA		8	12	
Line Regulation [4]	$\Delta V_{OUT}/ \Delta V_{IN}$	10V ≤ V_{IN} ≤ 18V		5	10	ppm/V

1. The specified values are without external trim.
2. The temperature coefficient is determined by the box method. See discussion on temperature performance.
3. Hysteresis over the operating temperature range.
4. Line and load regulation are measured with pulses and do not include voltage changes due to temperature.

TYPICAL PERFORMANCE GRAPHS

Figure 2: V_{OUT} vs. Temperature (VRE3050BS)

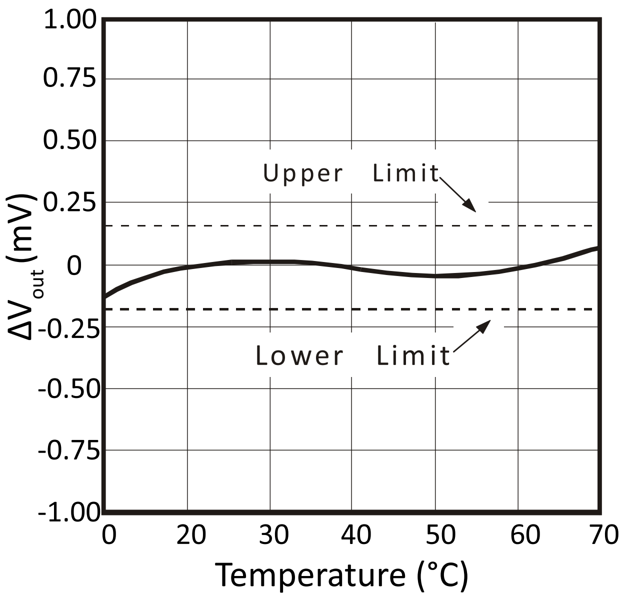


Figure 3: V_{OUT} vs. Temperature (VRE3050JS)

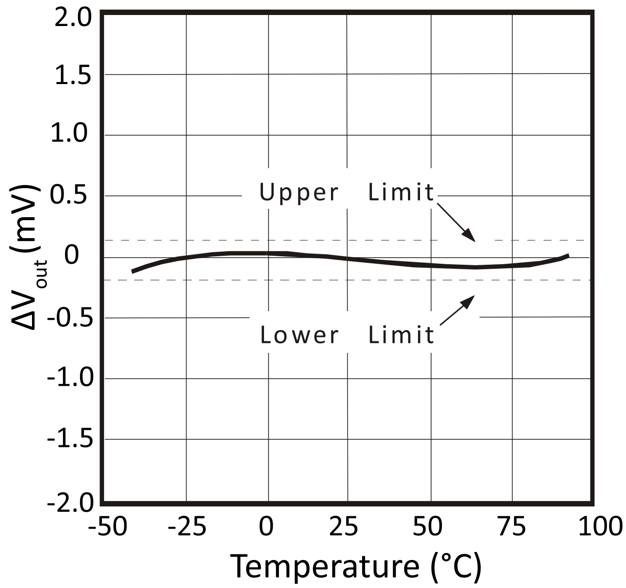


Figure 4: V_{OUT} vs. Temperature (VRE3050LS)

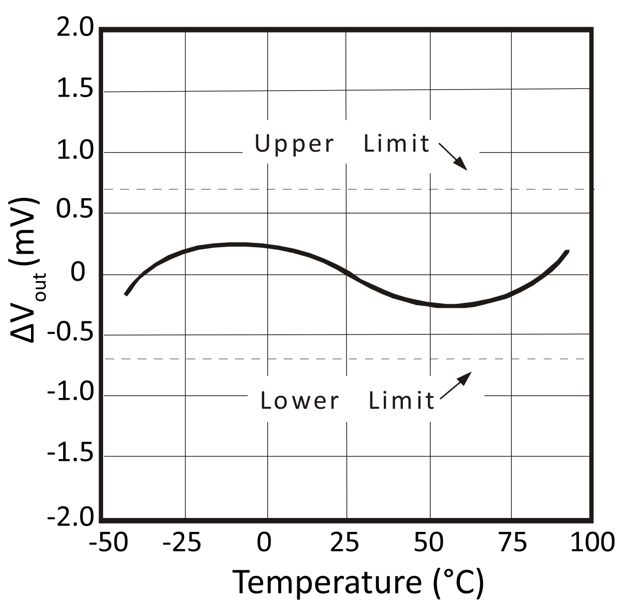


Figure 5: Supply Current vs. Supply Voltage

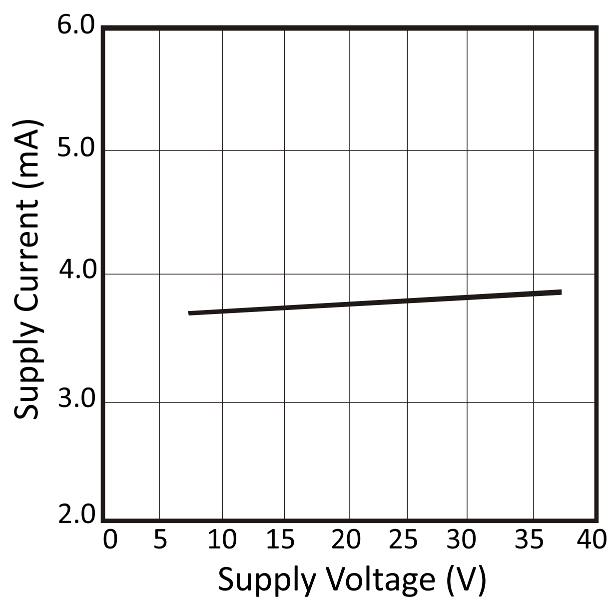


Figure 6: Quiescent Current vs. Temperature

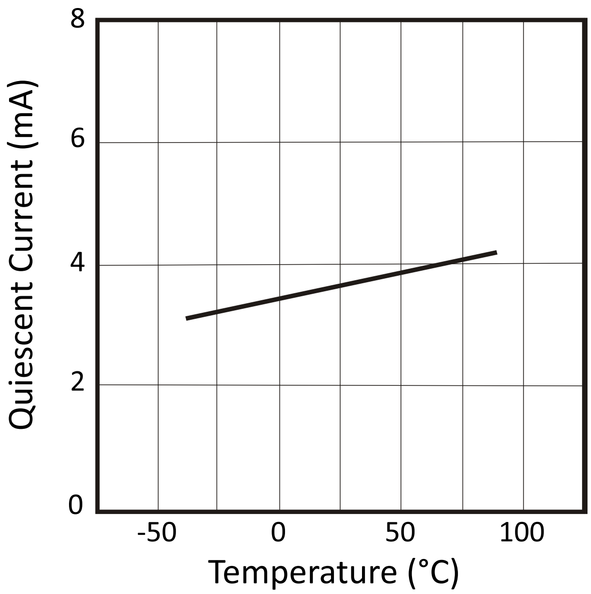


Figure 7: Output Impedance vs. Frequency

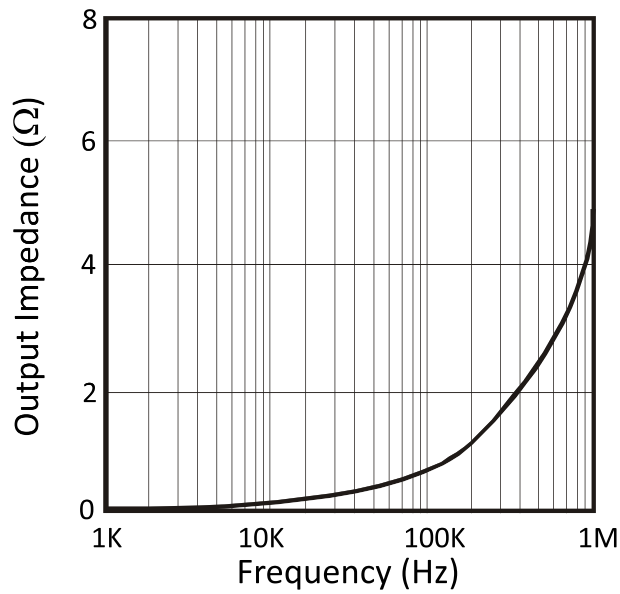


Figure 8: Junction Temp. Rise vs. Output Current

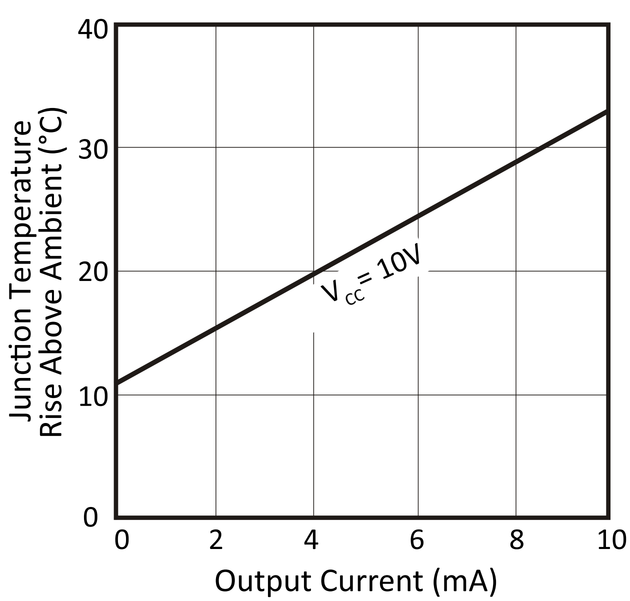


Figure 9: Ripple Rejection vs. Frequency (C_{NR} =0µF)

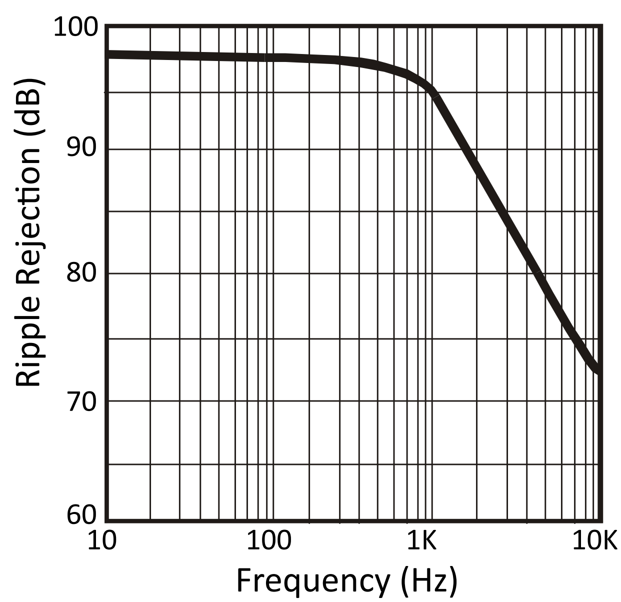


Figure 10: Turn-On & Turn-Off Transient Response

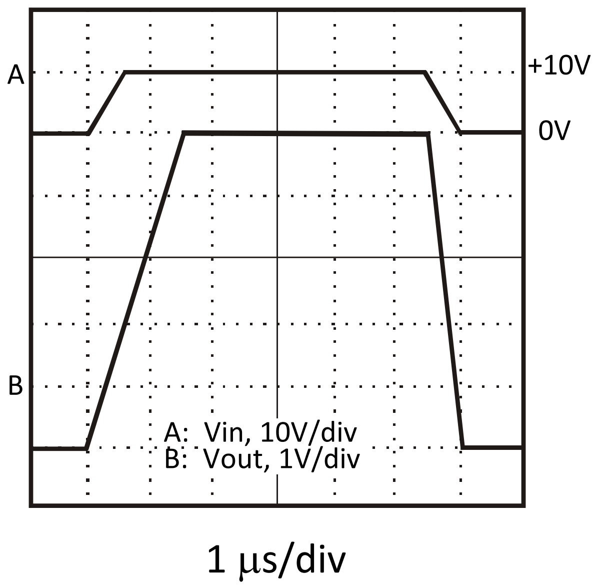


Figure 11: Output Noise-Voltage Density vs. Frequency

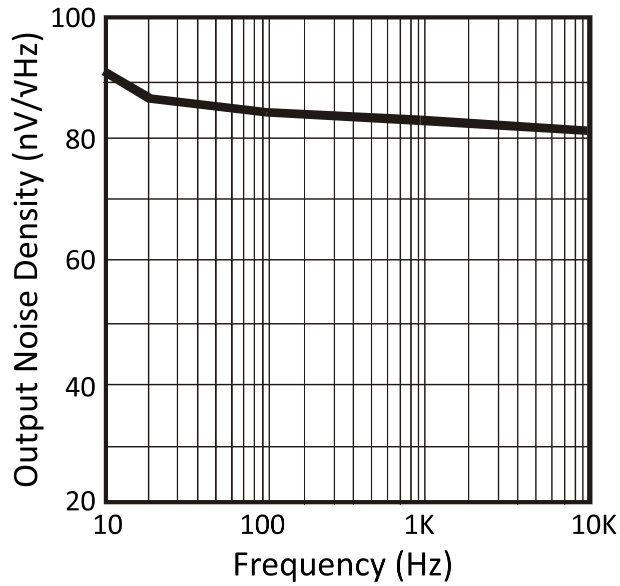


Figure 12: Change in Output Voltage vs. Output Current

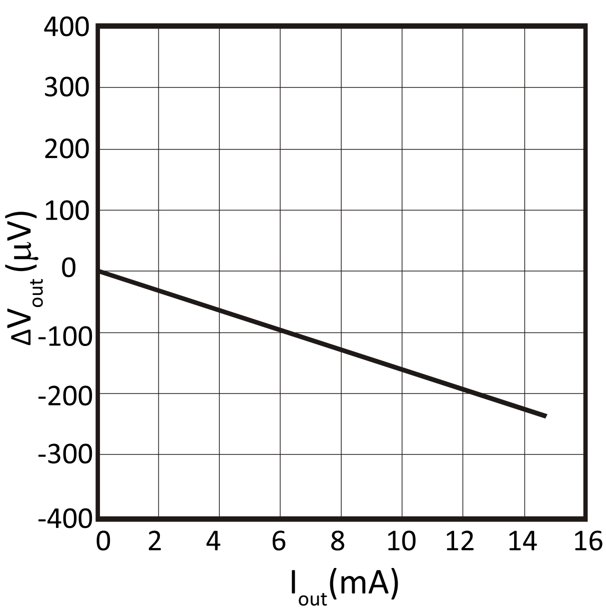


Figure 13: Change in Output Voltage vs. Input Voltage

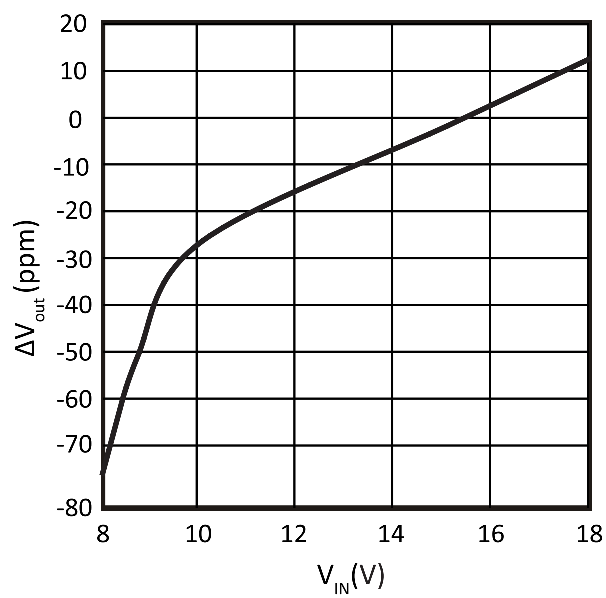
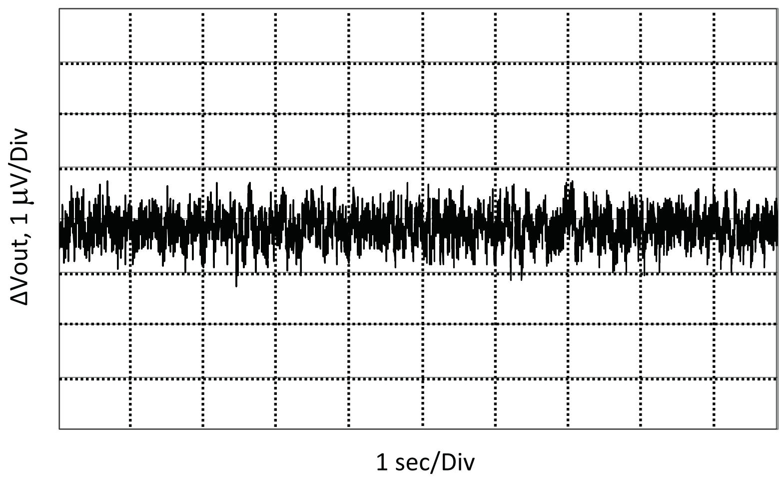
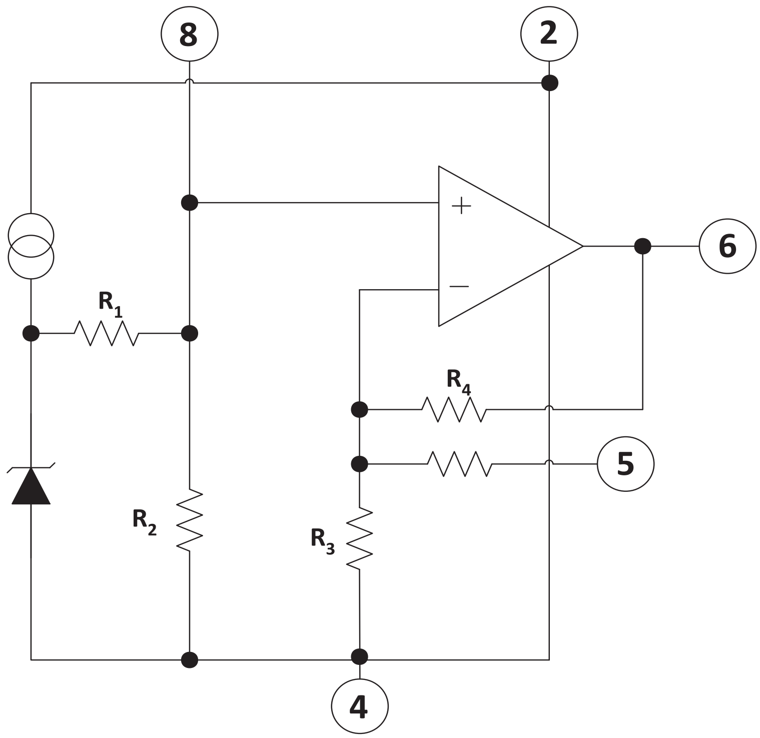


Figure 14: 0.1 Hz to 10 Hz Noise



BLOCK DIAGRAM

Figure 15: Block Diagram



THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 15. A FET current source is used to bias a 6.3 V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the non-inverting input of the operational amplifier which amplifies the voltage to produce a 5 V output. The gain is determined by the resistor networks R3 and R4: G=1 + R4/R3. The 6.3 V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the references' voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

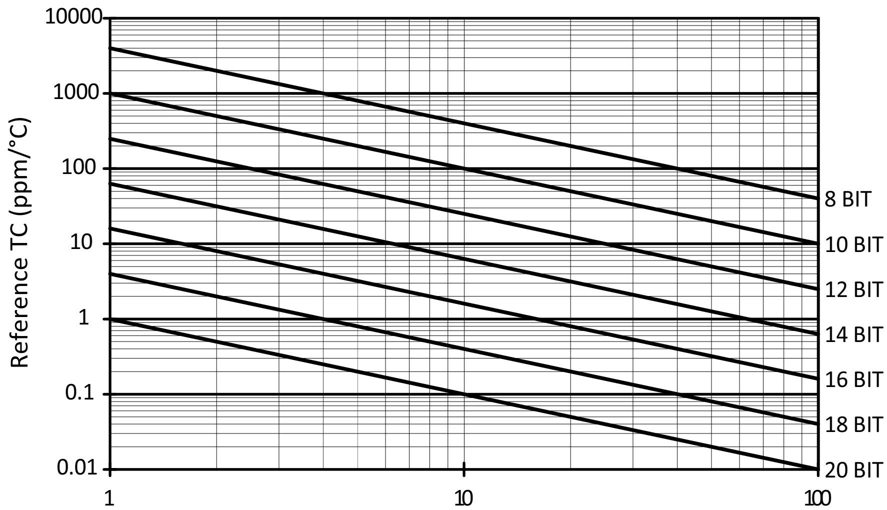
A nonlinear compensation network of thermistors and resistors that is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By adjusting the slope, a very stable voltage is produced over wide temperature ranges.

This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability. The proper connection of the VRE3050 series voltage references with the optional trim resistor for initial error and the optional capacitor for noise reduction is shown above.

BASIC CIRCUIT CONNECTION

To achieve the specified performance, pay careful attention to the layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected to a single point to minimize interconnect resistances.

Figure 16: Reference TC vs. ΔT Change from 25°C for 1 LSB Change



TEMPERATURE PERFORMANCE

The VRE3050 is designed for applications where the initial error at room temperature and drift over temperature are important to the user. For many instrument manufacturers, a voltage reference with a temperature coefficient less than 1 ppm/°C makes it possible to not perform a system temperature calibration, a slow and costly process.

Of the three TC specification methods (slope, butterfly, and box), the box method is most commonly used. A box is formed by the min/max limits for the nominal output voltage over the operating temperature range. The equation follows:

$$TC = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method guarantees limits for the temperature error but does not specify the exact shape and slope of the device under test.

A designer who needs a 14-bit accurate data acquisition system over the industrial temperature range (-40°C to +85°C), will need a voltage reference with a temperature coefficient (TC) of 1 ppm/°C if the reference is allowed to contribute an error equivalent to 1LSB. For 1/2LSB equivalent error from the reference you would need a voltage reference with a temperature coefficient of 0.5 ppm/°C. Figure 16 shows the required reference TC vs. delta T change from 25°C for resolution ranging from 8 bits to 20 bits.

THERMAL HYSTERESIS

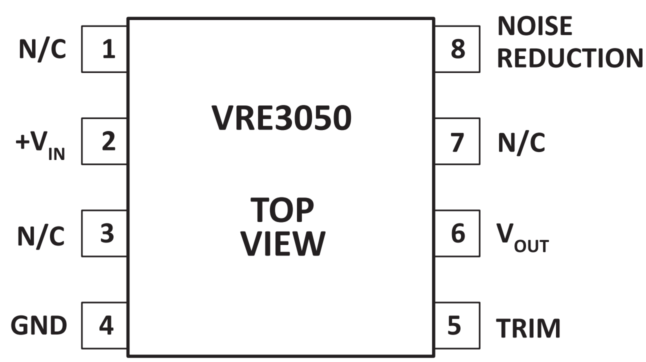
A difference in output voltage between the start of, and after return from a temperature excursion. When references experience a temperature change and return to the initial temperature, they do not always have the same initial voltage. Thermal hysteresis is difficult to correct and is a major error source in systems that experience temperature changes greater than 25°C. Reference vendors are starting to include this important specification in their datasheets.

PERFORMANCE EVALUATION

Apex Microtechnology's voltage references are highly accurate devices. Evaluation of performance and/ or meeting the specified accuracy in practice involves high-end measurement equipment, temperature chambers with inert gas to prevent condensation, shielded and battery-powered passband filters, careful board layout (star grounding at the right point), very stable noise reduction capacitors, and clean PCBs. Unthoughtful PCB layout, soldering flux residue, unstable capacitors, inaccurate DVMs, condensation, induced noise, amongst others, can adversely affect the VRE's accuracy.

PIN CONFIGURATION

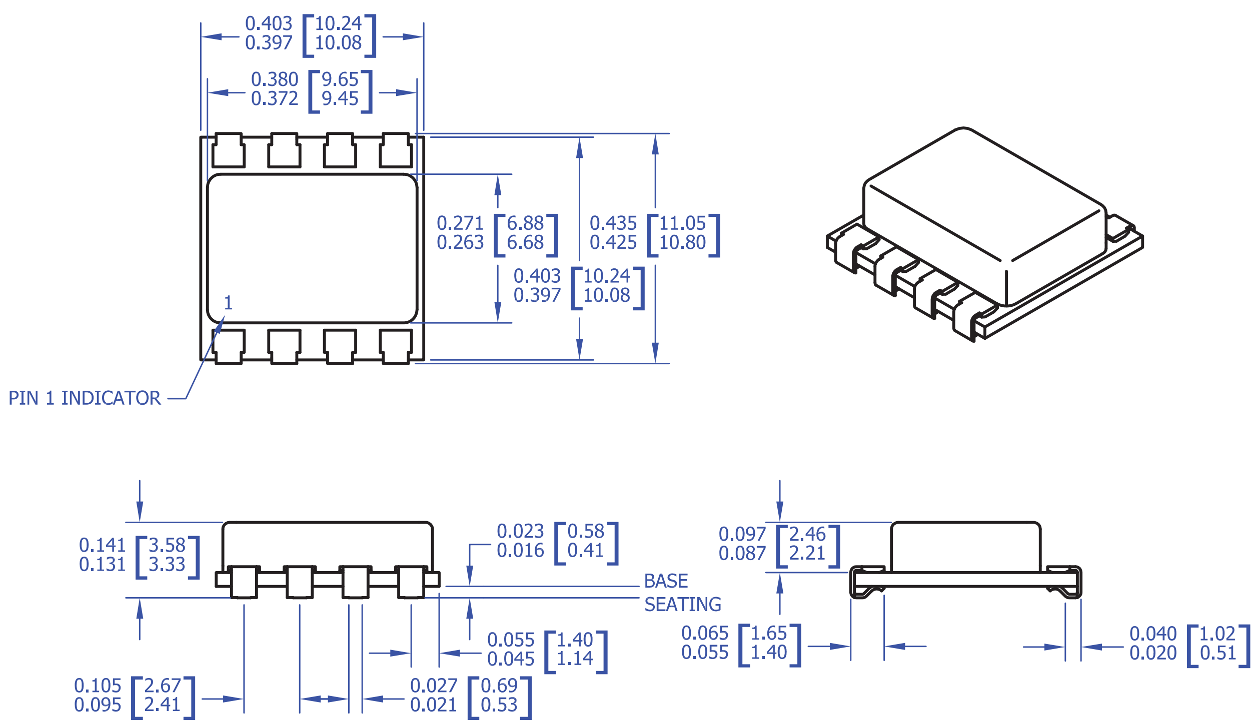
Figure 17: Pin Configuration



PACKAGE OPTIONS

Part Number	Apex Package Style	Description
VRE3050BS	GF	8-pin Surface Mount DIP
VRE3050JS	GF	8-pin Surface Mount DIP
VRE3050LS	GF	8-pin Surface Mount DIP

PACKAGE STYLE GF



NOTES:
1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Nickel Iron, Tin over Nickel plated.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.026 oz. [0.736 g].
6. Epoxy sealed, non-hermetic package

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