Octal Double-Data-Rate PSRAM

Specifications

- **Single Supply Voltage**
  - V_{DD} =1.62 to 1.98V
  - V_{DDQ} =1.62 to 1.98V
- **Interface**: Octal SPI with DDR OctaRAM mode, two byteS transfers per one clock cycle
- **Performance**: Clock rate up to 200MHz, 400MB/s read/write throughput
- **Organization**: 64Mb, 8M x 8bits with 1024 byte page size
  - Column address: AY0 to AY9
  - Row address: AX0 to AX12
- **Refresh**: Self-managed
- **Operating Temperature Range**
  - Tc = -40°C to +85°C (standard range)
  - Tc= -40°C to +105°C (extended range)
- **Maximum Standby Current**
  - 300µA @ 105°C
  - 200µA @ 85°C
  - 100µA @ 25°C

Features

- **Low Power Features**
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- **Software Reset**
- **Reset Pin Available**
- **Output Driver LVCMOS** with programmable drive strength
- **Data Mask (DM)** for write data
- **Data strobe (DQS)** enabled highspeed read operation
- **Register Configurable** write and read initial latencies
- **Write Burst Length**
  - maximum 1024 Bytes
  - minimum 2 Bytes
- **Wrap & Hybrid Burst** in 16/32/64/128 lengths.
- **Linear Burst Command** (wraps at page boundary)

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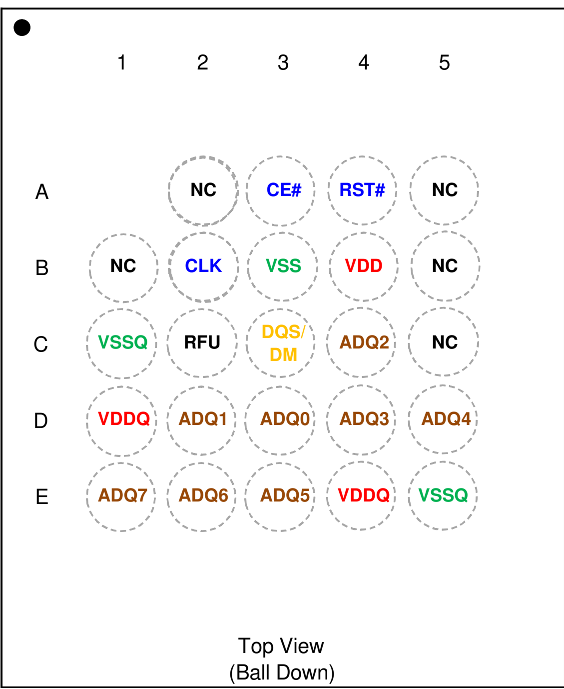
2 Package Information

The APS6408L-OCx is available in miniBGA 24L package 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm, package code "BA".

- Ball Assignment for MINIBGA 24L



(6x8x1.2mm)(P1.0)(B0.4)

Note:

1. Part Number APS6408L-OC-BA for 64Mb.

2. RFU: Reserved for future use, which is reserved for 2nd CE#.

3. NC: No internal connection.

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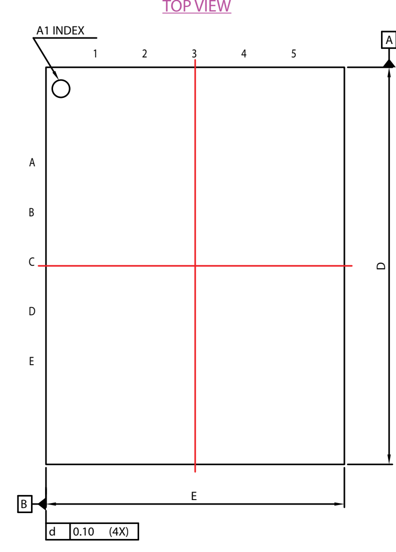
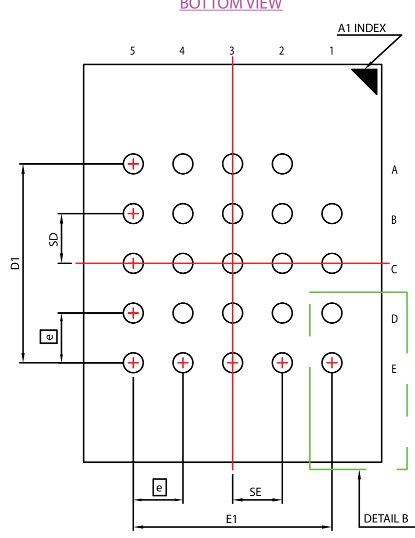
3 Package Outline Drawing

Package code "BA"

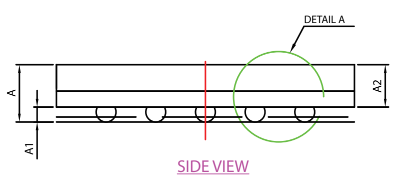


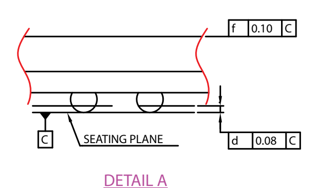


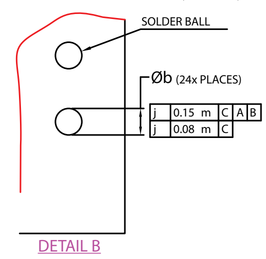
SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	0.30	0.35
A2	-	0.79	-
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
	1.00 BSC		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)







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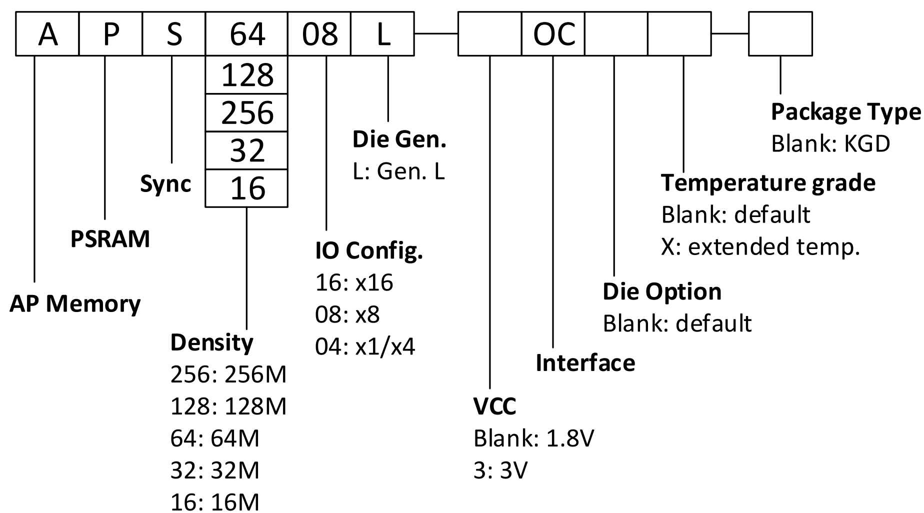
4 Ordering Information

Table 1: Ordering Information

Part Number	*Temperature Range*	*Max Frequency*	*Note*
APS6408L-OC	Tj=-40°C to +85°C	200 MHz	Bare die, SIP
APS6408L-OCX	Tj=-40°C to +105°C	200 MHz	Bare die, SIP
APS6408L-OC-BA	Tc=-40°C to +85°C	200 MHz	24b Package
APS6408L-OCX-BA	Tc=-40°C to +105°C	200 MHz	24b Package



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5 Signal Table

All signals are listed in .

Table 2: Signals Table

Symbol	Type	Description	Comments
V_{DD}	Power	Core supply 1.8V	
V_{DDQ}	Power	IO supply 1.8V	
V_{SS}	Ground	Core supply ground	
V_{SSQ}	Ground	IO supply ground	
A/DQ[7:0]	IO	Address/DQ bus [7:0]	
DQS/DM	IO	DQ strobe clock during reads, Data mask during writes. DM is active high. DM=1 means “do not write”.	
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.	
CLK	Input	Clock signal	
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.	

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6 Power-Up Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. V_{DD} and V_{DDQ} must be applied simultaneously. When they reach a stable level at or above minimum V_{DD}, the device is in Phase 1 and will require 150µs to complete its self-initialization process. The user can then choose either of two methods for Phase 2 of the initialization described in sections 6.1 & 6.2.

During Phase 1 CE# should remain HIGH (track V_{DD} within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation however Deep Sleep entry is not available until Deep Sleep Power Up (tDPDp) duration is observed.

6.1 Power-Up Initialization Method 1 (via. RESET# pin)

The RESET# pin can be used to initialize the device during Phase 2 as follows:

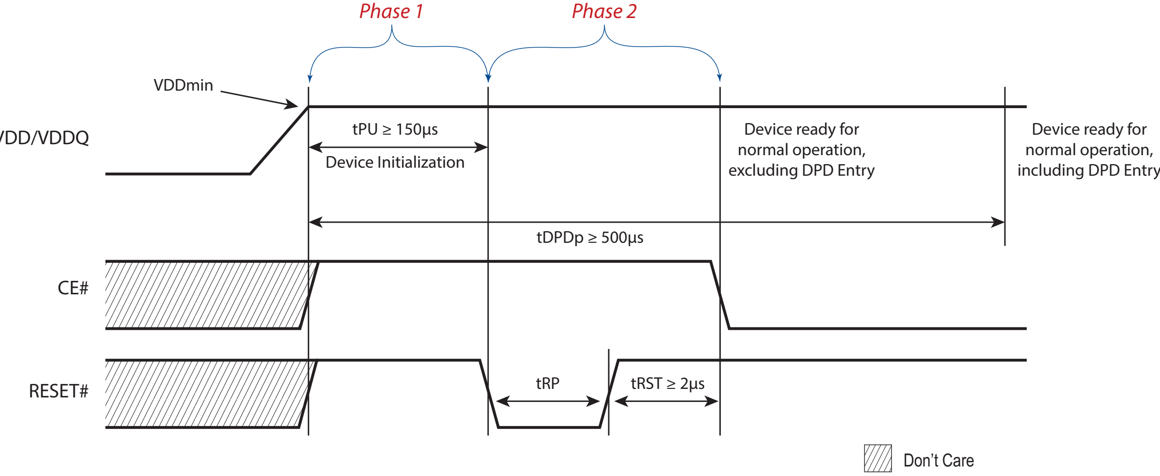

Figure 1. Power-Up Initialization Method 1 RESET#

The RESET# pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below.

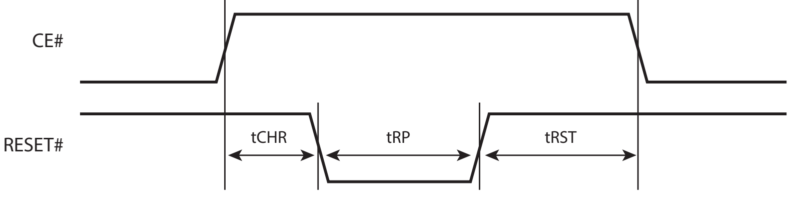

Figure 2. RESET# Timing

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6.2 *Power-Up Initialization Method 2 (via. Global Reset)*

As an alternate power-up initialization method, After the Phase 1 150µs period the Global Reset command can also be used to reset the device in Phase 2 as follows:

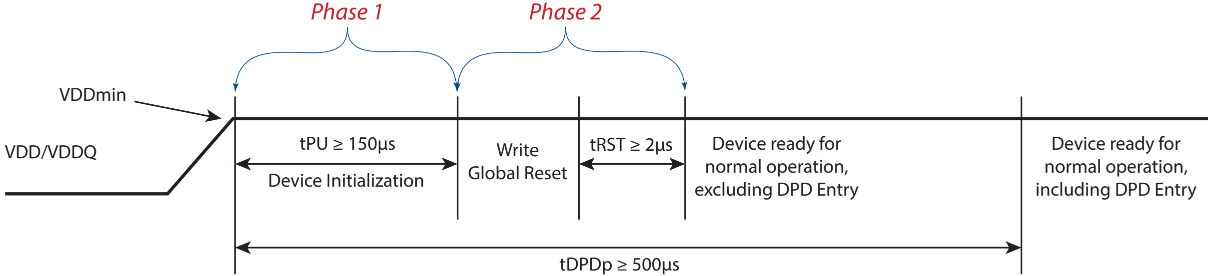

Figure 3. Power-Up Initialization Method 2 Timing with Global Reset

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is 4 clocked CE lows. The Global Reset command sequence is shown below. Note that Global Reset command can be used ONLY as Power-up initialization.

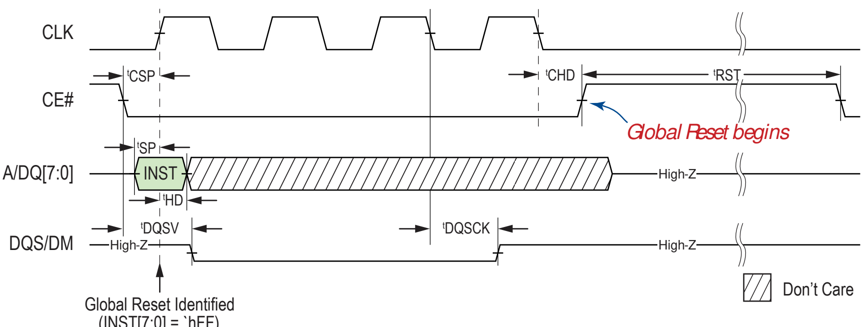

Figure 4: Global Reset

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7 Interface Description

7.1 *Address Space*

Octal DDR PSRAM device is byte-addressable. Memory accesses are required to start on even addresses (A[0]='0).

7.2 *Burst Type & Length*

Read and write operations are always in wrap mode within 16, 32, 64, 128 or 1K (see Table 8). Bursts can start on any even address. Write Burst Length has a minimum of 2 bytes (1 rising CLK and 1 falling CLK edge). Read has no minimum length. Both write and read have no restriction on maximum Burst Length as long as tCEM is met.

7.3 *Command/Address Latching*

After CE# goes LOW, instruction code is latched on 1st CLK rising edge. Row Access (RA) address is latched on the 3rd & 4th edges (2nd CLK rising edge, 2nd CLK falling edge), while Column Access (CA) address is latched on the 5th & 6th CLK edges (3rd CLK rising edge, 3rd CLK falling edge).

	1st CLK		2nd CLK		3rd CLK	
Pin	↑	↓	↑	↓	↑	↓
A/DQ[7]	INST[7]	×	rsvd.	RA[7]	CA[9]	rsvd.
A/DQ[6]	INST[6]	×	rsvd.	RA[6]	CA[8]	rsvd.
A/DQ[5]	INST[5]	×	rsvd.	RA[5]	CA[7]	rsvd.
A/DQ[4]	INST[4]	×	RA[12]	RA[4]	CA[6]	rsvd.
A/DQ[3]	INST[3]	×	RA[11]	RA[3]	CA[5]	CA[3]
A/DQ[2]	INST[2]	×	RA[10]	RA[2]	CA[4]	CA[2]
A/DQ[1]	INST[1]	×	RA[9]	RA[1]	rsvd.	CA[1]
A/DQ[0]	INST[0]	×	RA[8]	RA[0]	rsvd.	CA[0]

Remarks: × = don't care (V_{IH}/V_{IL})

During the Command/Address cycles (first three clocks) DQS/DM will be driven low by the PSRAM for all operations.

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7.4 Command Truth Table

The Octal DDR PSRAM recognizes the following commands specified on the INST (Instruction) cycle defined by the Address/DQ pins.

	1st CLK		2nd CLK		3rd CLK	
Command	↑	↓	↑	↓	↑	↓
Sync Read	80h	×	A3	A2	A1	A0
Sync Write	00h	×	A3	A2	A1	A0
Sync Read (Linear Burst)	A0h	×	A3	A2	A1	A0
Sync Write (Linear Burst)	20h	×	A3	A2	A1	A0
ID Register Read	C0h or E0h	×	00h	00h	00h	00h
Mode Register Read	C0h or E0h	×	00h	04h	00h	00h
Mode Register Write	40h or 60h	×	00h	04h	00h	00h
Global Reset	FFh	×				

Remarks:
× = don't care (V_{IH}/V_{IL})
A3 = RA[max:8], unused address bits are reserved
A2 = RA[7:0]
A1 = {CA[max:4], 2xRsvd.}, unused address bits are reserved
A0 = {4xRsvd., CA[3:0]}
MA = Mode Register Address

Notes: 1) Default Burst Type set in Mode Register is 32 Byte Wrap

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7.5 *Read Operation*

After address latching, the device initializes DQS/DM to '0 from CLK rising edge of the 3rd clock cycle (A1). See Figure 5 below.

Output data is available after LC cycles, as shown in Figure 6 & Figure 7, LC is latency configuration code as defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 8. Synchronous timing parameters are shown in Table 15 & Table 16

In case of internal refresh insertion, variable latency output data is delayed by (LCx2) latency cycles as shown in Figure 6. The 1st DQS/DM rising edge after read pre-amble will indicate the beginning of valid data.

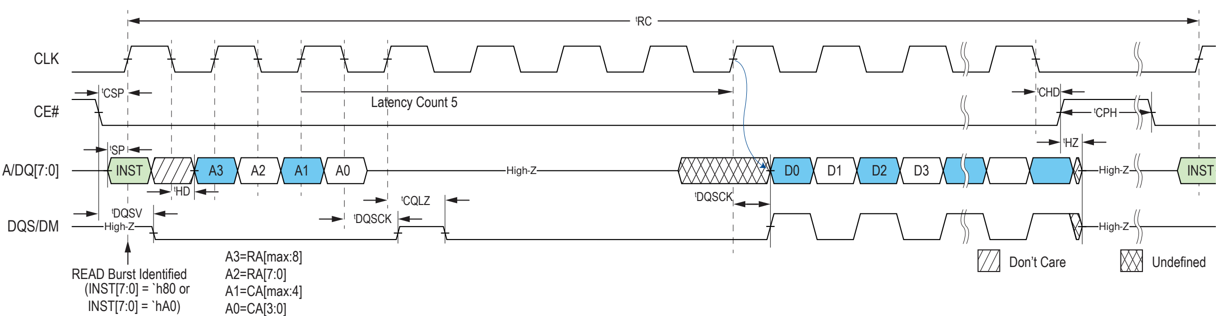

Figure 5: Synchronous Read

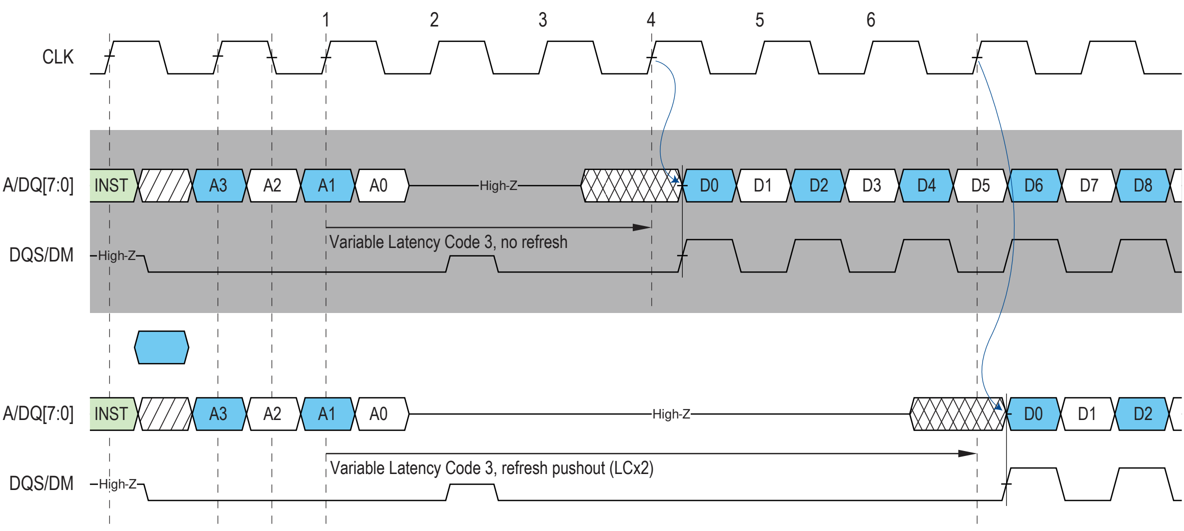

Figure 6: Variable Read Latency Refresh Pushout

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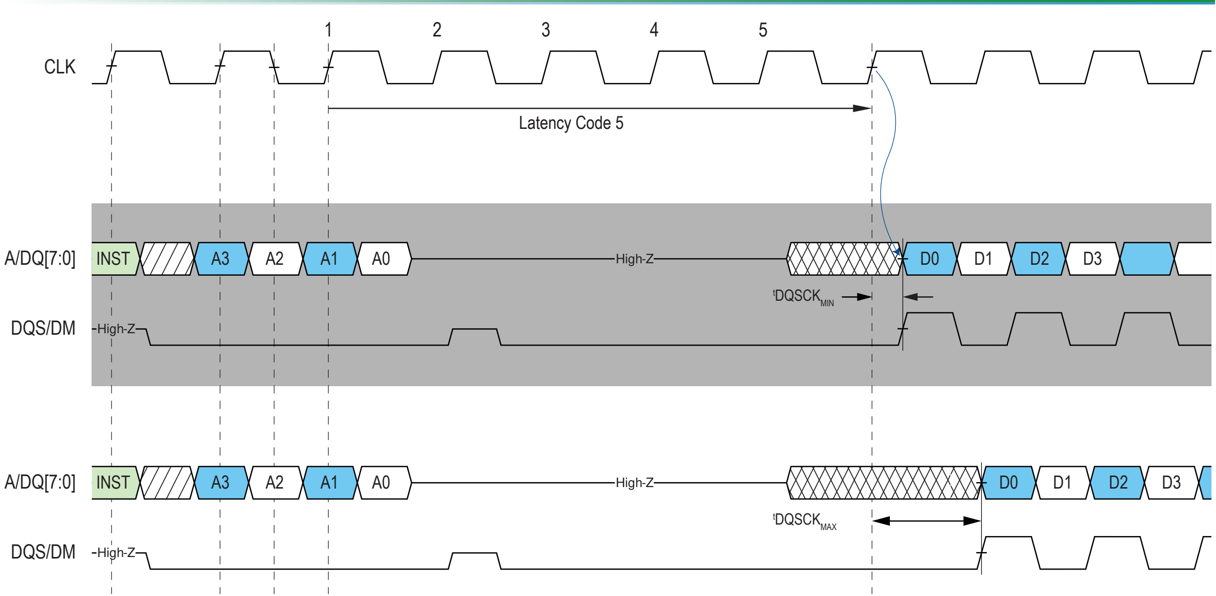

Figure 7: Read Latency & tDQSCK

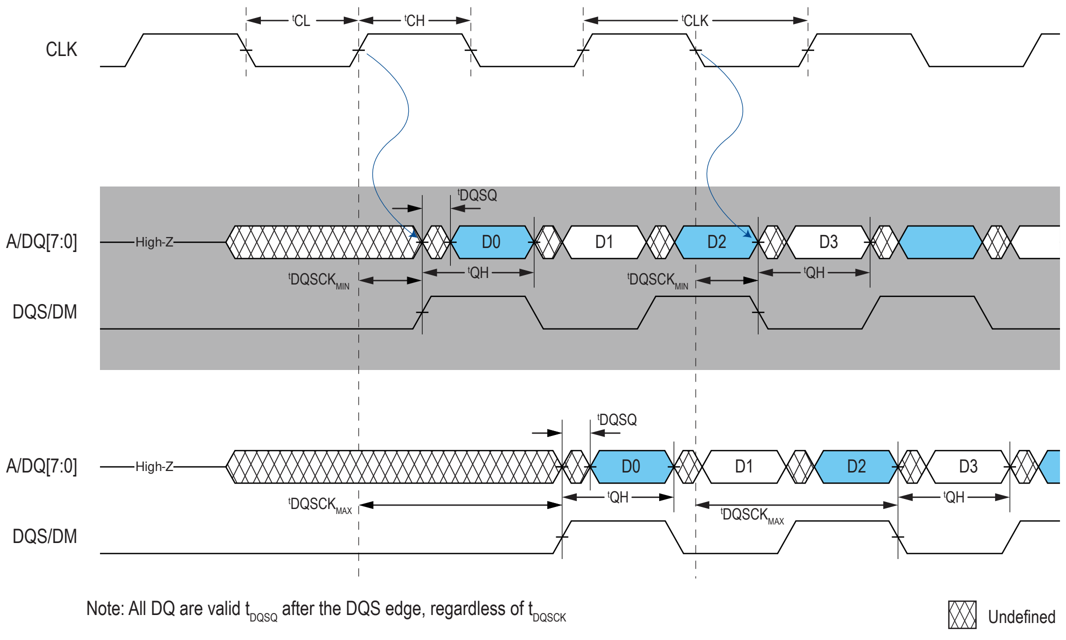

Figure 8: Read DQS/DM & DQ timing

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7.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be performed by masking the un-written byte with DQS/DM as shown in Figure 10.

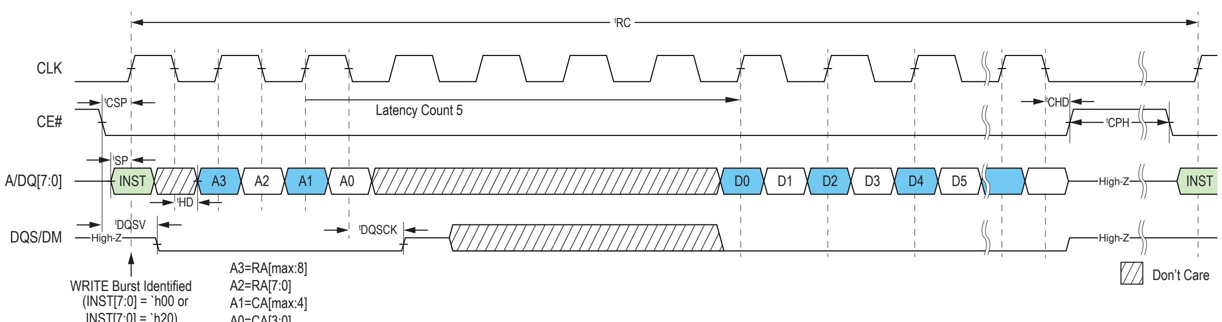

Figure 9: Synchronous Write Unmasked Example

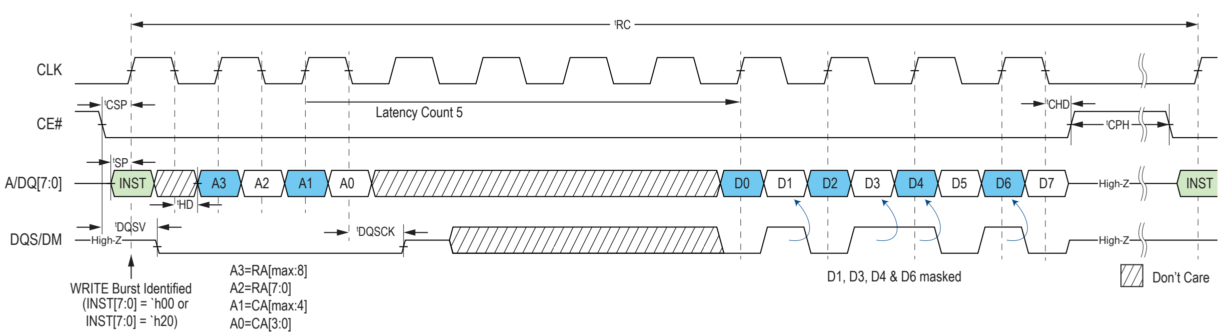

Figure 10: Synchronous Write Masking Example

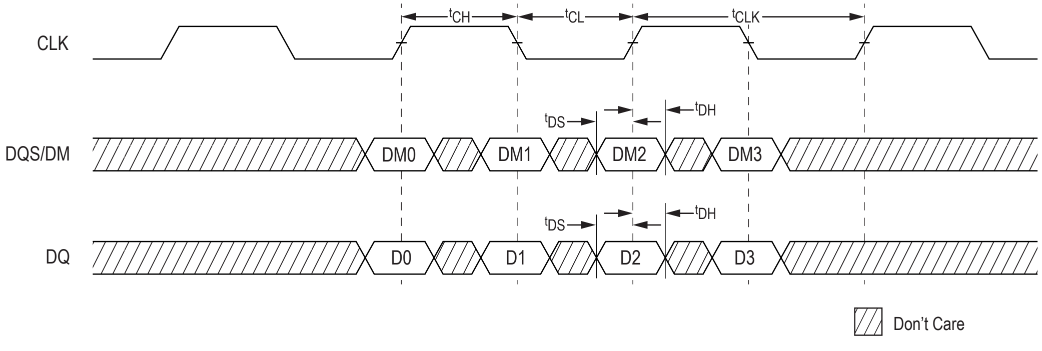

Figure 11: Write DQS/DM & DQ Timing

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7.7 Control Registers

Register Read is shown below. Register reads are always LC latency cycles. Register Address in command determines which Register is read from.

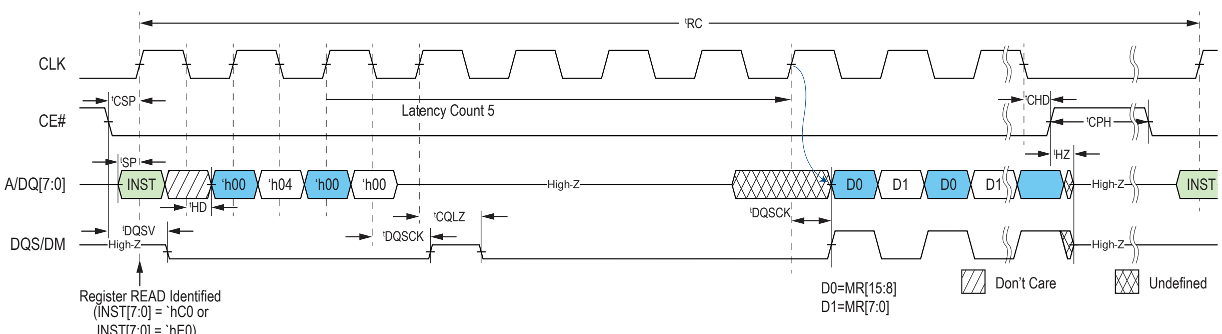

Figure 12: Mode Register Read

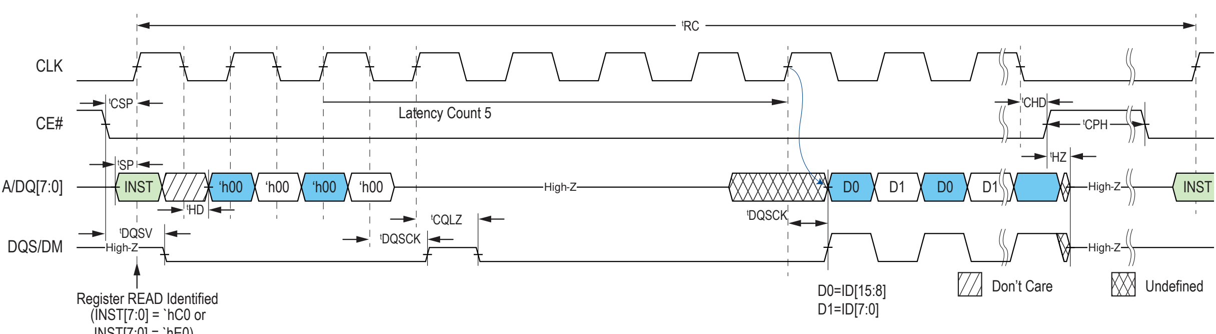

Figure 13: ID Register Read

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Register Write is shown below. Register Writes are always 0 latency cycle.

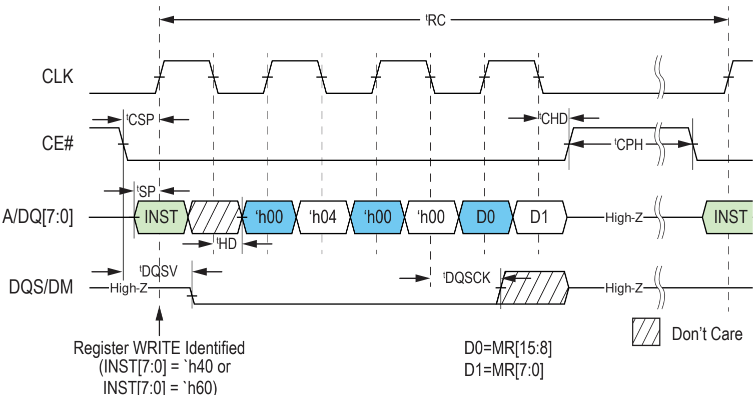

Figure 14: Register Write

ID & Mode Register mappings are shown in Table 3 & Table 4.

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Table 3: ID Register Table

Bit	Purpose	Settings
15	KBD	0 - Good Die 1 - Known Bad Die
14-13	reserved	00
12-8	Row Address MSB	01100 - 13 row address bits (64M) 01101 - 14 row address bits (128M)
7-4	Col Address MSB	1001 - 10 column address bits
3-0	Vendor	1101 - AP Memory

Table 4: Mode Register Table

Bit	Purpose	Settings
15	Deep Power Down Enable	0 - Deep Power Down Entry 1 - Normal Operation (default)
14-12	Drive Strength	see Table 7
11-8	reserved	
7-4	Latency Code	see Table 5&6
3	Latency Type	0 - Variable Latency (default) 1 - Fixed Latency
2	Burst Type	0 - Wrapped (default) 1 - Hybrid Continuous
1-0	Burst Length	00 - 128 bytes 01 - 64 bytes 10 - 32 bytes (default) 11 - 16 bytes

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Table 5: Latency Configuration Codes MR[7:4]

VL Codes (MR[3]=0)			FL Codes (MR[3]=1)	Max Input CLK Freq (MHz)	
MR[7:4]	No Refresh (LC)	Refresh (LCx2)	(LCx2)	Standard	Extended
0000	3	6	6	66	66
0001	4	8	8	104	104
0010	5	10	10	133	133
0011	6	12	12	166	166
0100	7	14	14	200	200
0101	8 (default)	16	16	200	200
others	Reserved	-	-	-	-

Table 6: Operation Latency Code Table

Type	Operation	VL (default)		FL
		No Refresh	Refresh	
Memory	Read	LC	LCx2	LCx2
	Write	LC		LC
Register	Read	LC		LC
	Write	0		0

Table 7: Drive Strength Codes MR [14:12]

Codes	Drive Strength
‘000	100Ω
‘001	66Ω
‘010	50Ω
s‘011	40Ω
‘100	33Ω
‘101	33Ω
‘110	25Ω
‘111	25Ω (default)

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Table 8: Burst Type MR[2], Burst Length MR[1:0], & Linear Burst

By default the device powers up in 32 Byte Wrap. In non-Hybrid burst (MR[2]=0), MR[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid Burst Wrap is selected (MR[2]=1), the device will burst through the initial wrapped Burst Length once, then continue to burst incrementally up to maximum column address (1K) before wrapping around within the entire column address space. Burst Length (MR[1:0]) can be set to 16,32,64 & 128 bytes.

MR[2]	*MR [1:0]*	*Burst Length*	*Example of Sequence of Bytes During Wrap*	
			Starting Address	*Byte Sequence*
'0	'00	128 Byte Wrap	4	[4,5,6,...127,0,1,2,...]
'0	'01	64 Byte Wrap	4	[4,5,6,...63,0,1,2,...]
'0	'10	32 Byte Wrap (default)	4	[4,5,6,...31,0,1,2,...]
'0	'11	16 Byte Wrap	4	[4,5,6,...15,0,1,2,...]
'1	'00	128 Byte Hybrid Wrap	2	[2,3,4,...127,0,1],128,129...1023,0,1,...
'1	'01	64 Byte Hybrid Wrap	2	[2,3,4,...63,0,1],64,65,66,...1023,0,1,...
'1	'10	32 Byte Hybrid Wrap	2	[2,3,4,...31,0,1],32,33,34,...1023,0,1,...
'1	'11	16 Byte Hybrid Wrap	2	[2,3,4,...15,0,1],16,17,18,...1023,0,1,...

The Linear Burst Command (INST[5:0]=6'b10_0000) forces the current array read or write to do 2K Byte Wrap. The burst continues linearly from the starting address and at the end of the page it wraps back to the beginning of the page. This special burst instruction can be used on both array writes and reads. A new command is needed to access a different page.

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7.8 Deep Power Down Mode

Deep Power Down Mode (DPD) is a feature which puts the device in an ultra-low power state. DPD Mode Entry is entered by using Register Write to write a 0 into MR[15]. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.

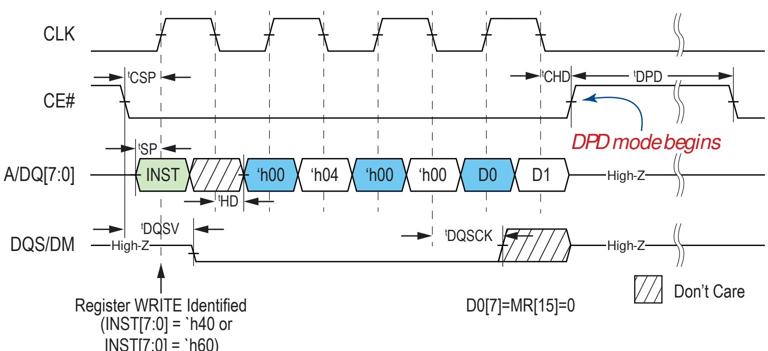

Figure 15: Deep Power Down Entry Write

Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD Exit, CE# must be held high until the first operation begins (observing minimum tXDPD).

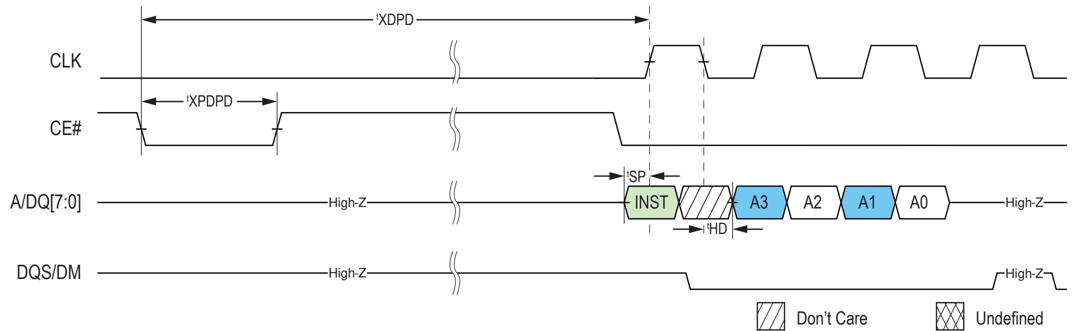

Figure 16: Deep Power Down Exit with CE# (Read Operation shown as example)

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After a RESET# DPD exit, CE# and RESET# must be held high until the first operation begins (observing minimum tRCH).

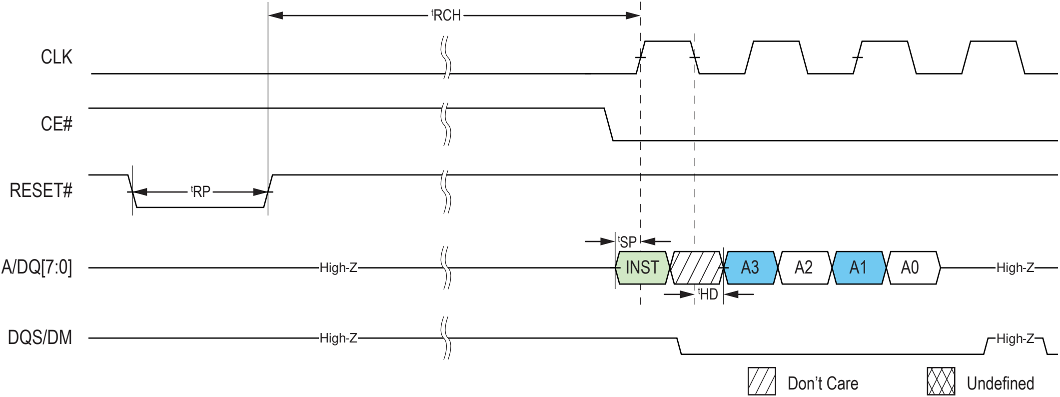

Figure 17: Deep Power Down Exit with RESET# (Read Operation shown as example)

Register values are retained in DPD Mode but memory content is not. However, if a RESET# low is used to exit DPD, register values are also reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial powerup to the first DPD entry.

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8 Electrical Specifications:

8.1 Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except V_{DD}, V_{DDQ} relative to V_{SS}	VT	-0.4 to V_{DD}/V_{DDQ}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

8.2 Pin Capacitance

Table 10: Bare Die Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note 1: spec'd at 25°C.

Table 11: Package Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note 1: spec'd at 25°C.

Table 12: Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C_L		15	pF	

Note 1: System C_L for the use of package.

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8.3 Decoupling Capacitor Requirement

It is required to have a decoupling capacitor on VDD pin for IO switchings and psram internal transient events. A low ESR 1µF ceramic cap is recommended. To minimize parasitic inductance, place the cap as close to VDD pin as possible. An optional 0.1µF can further improve high frequency transient response.

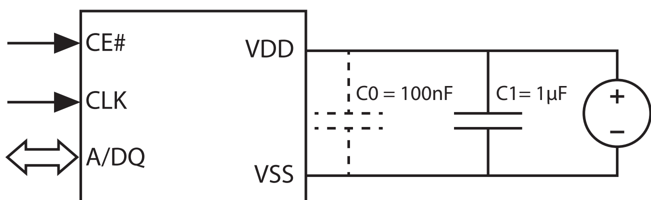

Figure 18: Decoupling Capacitor

8.4 Operating Conditions

Table 13: Operating Characteristics

Parameter	*Min*	*Max*	*Unit*	*Notes*
Operating Temperature (extended)	-40	105	°C	1
Operating Temperature (standard)	-40	85	°C	

Note 1: Extended temp range of -40 to 105°C is only characterized; Standard test condition is -32 to 105°C.

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8.5 DC Characteristics

Table 14: DC Characteristics

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{DDQ}	I/O Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DDQ}-0.4	V_{DDQ}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DDQ}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DDQ}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
ICC	Read/Write @13MHz		4	mA	2
	Read/Write @133MHz		16	mA	2
	Read/Write @166MHz		19	mA	2
	Read/Write @200MHz		22	mA	2
ISB_{EXT}	Standby current (extended temp)		300	µA	1,3
ISB_{STD}	Standby current (standard temp)		200	µA	3
$ISB_{STDroom}$	Standby current (room temp)		100	µA	3,4, 5
ISB_{STDDPD}	Standby current (Deep Power Down -40°C to +85°C)		15	µA	6

Note 1: Spec'd up to 105°C.

Note 2: Current is only characterized.

Note 3: Without CLK toggling. ISB will be higher if CLK is toggling.

Note 4: Slow Refresh.

Note 5: **Typical $ISB_{STDROOM}$ 66uA**.

Note 6: **Typical mean ISB_{STDDPD} 7uA at 25°C**

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8.6 AC Characteristics

Table 15: READ/WRITE Timing

		-7(133MHz)		-6(166MHz)		-5(200MHz)			
Symbol	***Parameter***	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***	***Unit***	***Notes***
tCLK	CLK period	7.5		6		5		ns	
tCH/tCL	Clock high/low width	0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHKL	CLK rise or fall time		1.2		1		0.8	ns	
tCPH	CE# high pulse width	15		18		20		ns	Clocking optional
tCEM	CE# low pulse width		4		4		4	µs	Standard temp
			1		1		1	µs	Extended temp
tCEM	CE# low pulse width	3		3		3		tCLK	
tCSP	CE# setup time to CLK rising edge	2		2		2		ns	
tCHD	CE# hold time from CLK falling edge	2		2		2		ns	
tSP	Setup time to active CLK edge	0.8		0.7		0.6		ns	
tHD	Hold time from active CLK edge	0.8		0.7		0.6		ns	
tDQSV	Chip enable to DQS output low	2	6	2	6	2	6	ns	
tHZ	Chip disable to DQ/DQS output high-Z		6		6		6	ns	
tRC	Write Cycle	60		60		60		ns	
tRC	Read Cycle	60		60		60		ns	
tDPD	Minimum DPD Duration	500		500		500		µs	
tDPDp	Minimum period between DPD	500		500		500		µs	
tXDPD	DPD CE# low to CLK setup time	150		150		150		µs	
tXPDPD	DPD Exit CE# low pulsewidth	60		60		60		ns	
			4		4		4	µs	
tPU	Device Initialization	150		150		150		µs	
tRP	RESET# low pulse width	1		1		1		µs	
tRST	Reset to CMD valid	2		2		2		µs	
tRCH	RESET# to CMD valid	150		150		150		µs	
tCHR	Chip-disable to RESET# low	20		20		20		ns	

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Table 16: DDR timing parameters

Symbol	Parameter	-7(133MHz) Min	-7(133MHz) Max	-6(166MHz) Min	-6(166MHz) Max	-5(200MHz) Min	-5(200MHz) Max	Unit	Notes
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	ns	
tDQSCK	DQS output access time from CLK	2	5.5	2	5.5	2	5.5	ns	
tDQSQ	DQS – DQ skew		0.6		0.5		0.4	ns	
tDS	DQ and DM input setup time	0.8		0.7		0.6		ns	
tDH	DQ and DM input hold time	0.8		0.7		0.6		ns	
tHP	Half Period	= min (tCH, tCL)						ns	
tQHS	Datahold skew factor		0.75		0.6		0.5	ns	
tQH	DQ output hold time from DQS	= tHP - tQHS						ns	

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9 Change Log

Version	Date	Description
1.7	Aug 21, 2019	Revised from -OCH
1.8	Sep 28. 2019	Update header, footer and page 1; updated ICC in Table 14

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