

### **30V N-Channel Enhancement Mode MOSFET**

#### Description

The AP100N03P/T uses advanced trench technology

to provide excellent R<sub>DS(ON)</sub>, low gate charge and

operation with gate voltages as low as 4.5V. This

device is suitable for use as a Battery protection

or in other Switching application.

### **General Features**

V<sub>DS</sub> = 30V I<sub>D</sub> =100 A

 $R_{\text{DS(ON)}} < 5.5 \text{m}\Omega \textcircled{0} V_{\text{GS}} = 10 \text{V} \quad (\text{Type: } 4.5 \text{m}\Omega)$ 

### Application

Battery protection

Load switch

Uninterruptible power supply

### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)	
AP100N03P	TO-220-3L	AP100N03P XXX YYYY	1000	
AP100N03T	TO-263-3L	AP100N03T XXX YYYY	800	
AP100N031	10-263-3L			

### Absolute Maximum Ratings (Tc=25°Cunless otherwise noted)

Or much a l	Damanakan	Maria	Units
Symbol	Parameter	Parameter Max.	
VDSS	Drain-Source Voltage	30	
VGSS	Gate-Source Voltage	Gate-Source Voltage ±20	
I₀@Tc=25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V 100		А
I <sub>D</sub> @T <sub>C</sub> =100℃	Continuous Drain Current, V <sub>GS</sub> @ 10V 46		А
IDM	Pulsed Drain Current <sup>note1</sup> 300		А
EAS	Single Pulsed Avalanche Energy note2	ulsed Avalanche Energy <sup>note2</sup> 56	
P₀@T₀=25℃	Total Power Dissipation468		W
R₀JA	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	62	°C/W
R₀JA	Thermal Resistance Junction-Ambient $^{1}$ (t <10s)	s) 25	
R0JC	Thermal Resistance, Junction to Case	2.2 °C/M	
TJ, TSTG	Operating and Storage Temperature Range	-55 to +175 °C	

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Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250µA	30	32	-	V
$\triangle BVDSS / \triangle TJ$	BVDSS Temperature Coefficient	Reference to 25°C, ID=1mA		0.028		V/°C
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250µA	1.2	1.6	2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	4.5	5.5	mΩ
RDS(on)	Static Drain-Source on-Resistance note3	V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	8.0	9.5	mΩ
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> = 0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Ciss	Input Capacitance		-	1614	-	pF
Coss	Output Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f = 1.0MHz	-	245	-	pF
Crss	Reverse Transfer Capacitance		-	215	-	pF
Qg	Total Gate Charge		-	33.7	-	nC
Qgs	Gate-Source Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	8.5	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	7.5	-	nC
td(on)	Turn-on Delay Time		-	7.5	-	ns
tr	Turn-on Rise Time	V <sub>DS</sub> =15V, I <sub>D</sub> =30A, R <sub>GEN</sub> =3Ω,	-	14.5	-	ns
td(off)	Turn-off Delay Time	$V_{GS} = 10V$	-	35.2	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	9.6	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	70	А
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	280	А
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> =30A	-	-	1.2	V

### Electrical Characteristics (TJ=25°C, unless otherwise noted)

Note :

 $1_{\mbox{\tiny V}}$  The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

 $2 \ensuremath{\,{\ensuremath{\scriptscriptstyle S}}}$  The data tested by pulsed , pulse width .The EAS data shows Max. rating .

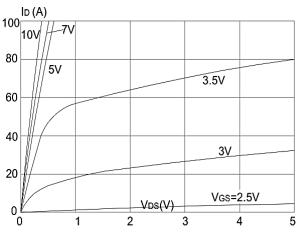
3. The test cond $\leq$  300us duty cycle  $\leq$  2%, duty cycle ition is VDD=24VGS=10V,L=0.1mH,IAS=15A

4、The power dissipation is limited by 175°C junction temperature

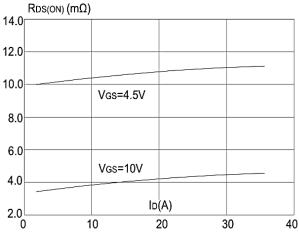
5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.



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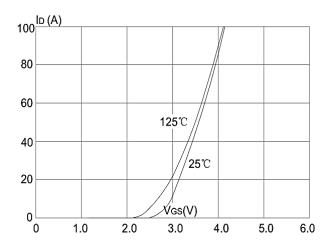
#### **Figure1: Output Characteristics**



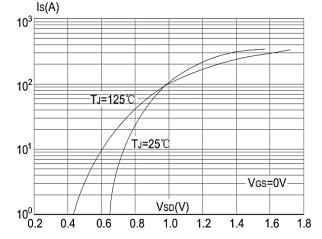
VGS(V) 10 Vps=15V ID=30A 8 6 4 2 Qg(nC) 0 8 16 24 32 40 0

Figure 3:On-resistance vs. Drain Current

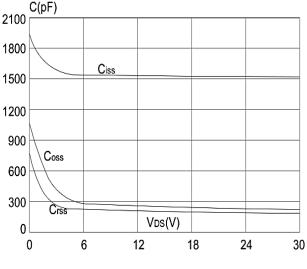
Figure 5: Gate Charge Characteristics



**Figure 2: Typical Transfer Characteristics** 







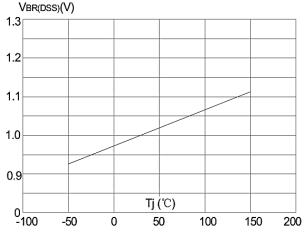
**Figure 6: Capacitance Characteristics** 

## Typical Characteristics

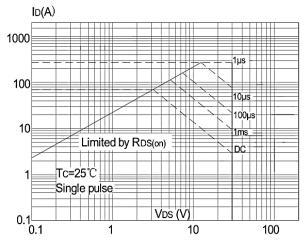
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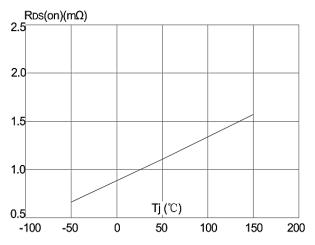
### **30V N-Channel Enhancement Mode MOSFET**



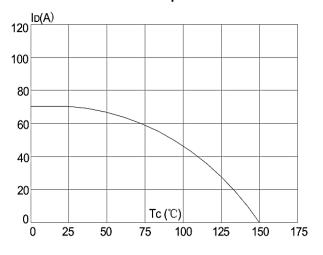
#### Figure 7: Normalized Breakdown Voltage vs. Junction Temperature







#### Figure 8: Normalized on Resistance vs Junction Temperature



#### Figure 10: Maximum Continuous Drain Current

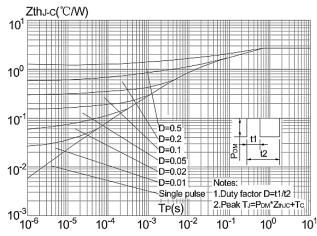
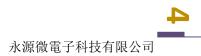
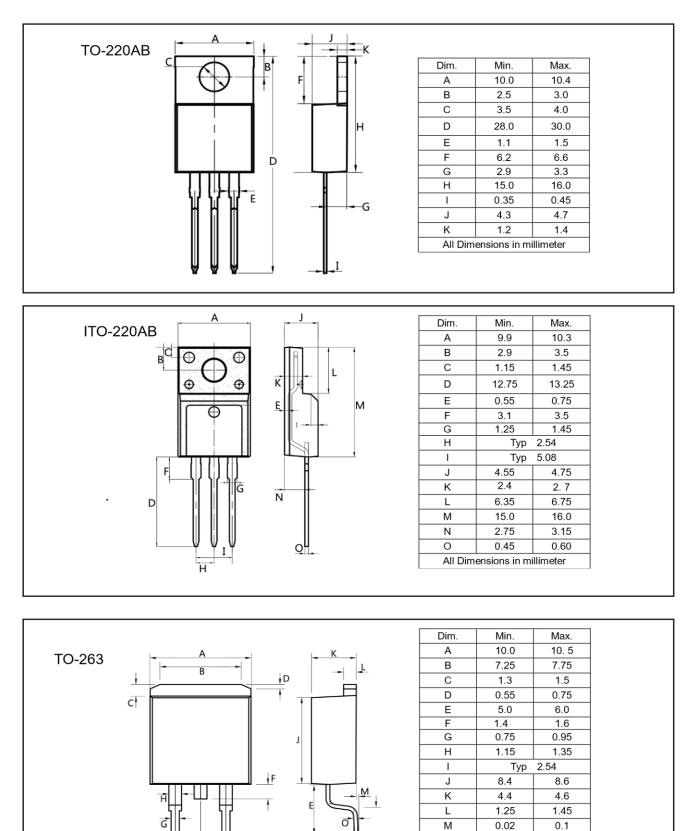


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case





### **30V N-Channel Enhancement Mode MOSFET**



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2.4

0.35

All Dimensions in millimeter

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2.8 0.45

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AP100N03P/T RVE3.9

## **30V N-Channel Enhancement Mode MOSFET**

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## **30V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change	
Rve3.8	2018/1/31	Initial release	
Rve3.9	2019/12/01	Reduce RDS(on) and QG Ciss	

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